KSZ8851-16MLLJ

Single-Port Ethernet MAC Controller with 8-Bit or 16-Bit Non-PCI Interface (Extended Temperature Support)

General Description

The KSZ8851-16MLLJ is a single-port controller chip with a non-PCI CPU interface and is available in 8-bit and 16-bit bus designs with extended temperature support (-40°C to +125°C). This datasheet describes the 48-pin LQFP KSZ8851-16MLLJ for applications requiring high-performance from single-port Ethernet Controller with 8-bit or 16-bit generic processor interface. The KSZ8851-16MLLJ offers the most cost-effective solution for adding high-throughput Ethernet connectivity to traditional embedded systems.

The KSZ8851-16MLLJ is a single-chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, an 8-bit or 16-bit generic host processor interface and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully utilizable 18KB for both TX (allocated 6KB) and RX (allocated 12KB) directions in host buffer interface.

The KSZ8851-16MLLJ is designed to be fully compliant with the appropriate IEEE 802.3 standards. An extended temperature-grade version of the KSZ8851-16MLLJ is available (see “Ordering Information section).

LinkMD®

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8851-16MLLJ is designed using a low-power CMOS process that features a single 3.3V power supply with options for 1.8V, 2.5V or 3.3V VDD I/O. The device includes an extensive feature set that offers management information base (MIB) counters and CPU control/data interfaces with single shared data bus timing.

The KSZ8851-16MLLJ includes unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8851-16MLLJ supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

Functional Diagram

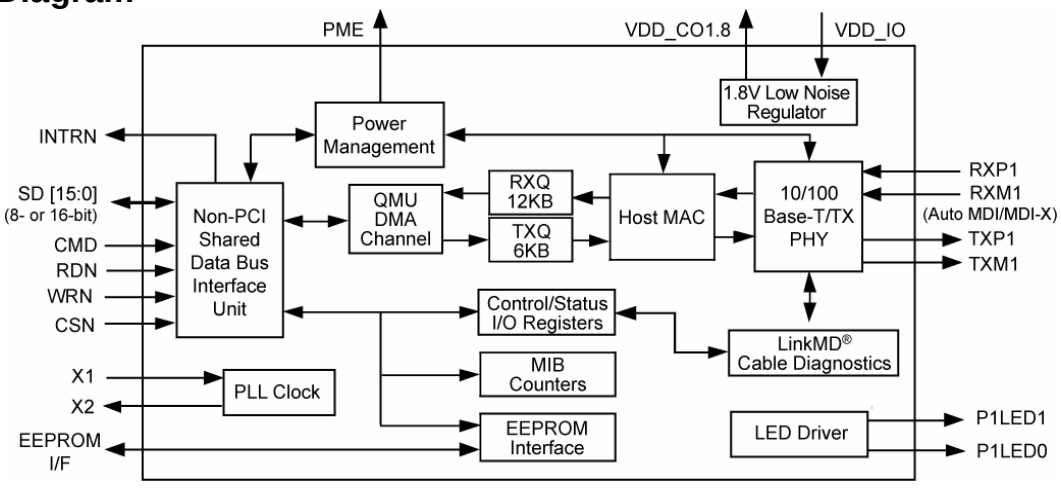

Figure 1. KSZ8851-16MLLJ Functional Diagram

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Features

- Integrated MAC and PHY Ethernet Controller fully compliant with IEEE 802.3/802.3u standards
- Designed for high performance and high throughput applications
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x full-duplex flow control and half-duplex backpressure collision flow control
- Supports DMA-slave burst data read and write transfers
- Supports IP Header (IPv4)/TCP/UDP/ICMP checksum generation and checking
- Supports IPv6 TCP/UDP/ICMP checksum generation and checking
- Automatic 32-bit CRC generation and checking
- Simple SRAM-like host interface easily connects to most common embedded MCUs.
- Supports multiple data frames for transmit and receive without address bus and byte-enable signals
- Supports both Big- and Little-Endian processors
- Larger internal memory with 12K Bytes for RX FIFO and 6K Bytes for TX FIFO. Programmable low, high and overrun watermark for flow control in RX FIFO
- Shared data bus for Data, Address and Byte Enable
- Efficient architecture design with configurable host interrupt schemes to minimize host CPU overhead and utilization
- Powerful and flexible address filtering scheme
- Optional to use external serial EEPROM configuration for MAC address
- Single 25MHz reference clock for both PHY and MAC
- HBM ESD Rating 6kV

Power Modes, Power Supplies, and Packaging

- Single 3.3V power supply with options for 1.8V, 2.5V and 3.3V VDD I/O
- Built-in integrated 3.3V or 2.5V to 1.8V low noise regulator (LDO) for core and analog blocks
- Enhanced power management feature with energy detect mode and soft power-down mode to ensure low-power dissipation during device idle periods
- Comprehensive LED indicator support for link, activity and 10/100 speed (2 LEDs) - User programmable
- Low-power CMOS design
- Extended Temperature Range: –40°C to +125°C
- Flexible package options available in 48-pin (7mm x 7mm) LQFP KSZ8851-16MLLJ or 128-pin PQFP KSZ8851-16MQLJ

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8851-16MLLJ offers:

- Flexible 8-bit and 16-bit generic host processor interfaces with same access time and single bus timing to any I/O registers and RX/TX FIFO buffers
- Supports to add two-byte before frame header in order for IP frame content with double word boundary
- Micrel LinkMD® cable diagnostic capabilities to determine cable length, diagnose faulty cables, and determine distance to fault
- Wake-on-LAN functionality
  - Incorporates Magic Packet™, wake-up frame, network link state, and detection of energy signal technology
- HP Auto MDI-X™ crossover with disable/enable option
- Ability to transmit and receive frames up to 2000 bytes

Network Features

- 10BASE-T and 100BASE-TX physical layer support
- Auto-negotiation: 10/100 Mbps full and half duplex
- Adaptive equalizer
- Baseline wander correction

Applications

- Video/Audio Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP and IPTV
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Home Base Station with Ethernet Connection
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security, Motion Control and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet
- Embedded Systems

Ordering Information

Part Number	Temperature Range	Package	Lead Finish
KSZ8851-16MLLJ	–40°C to +125°C	48-Pin LQFP	Pb-Free

Revision History

Revision	Date	Summary of Changes
1.0	01/22/2010	First-released Information.

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Pin Configuration

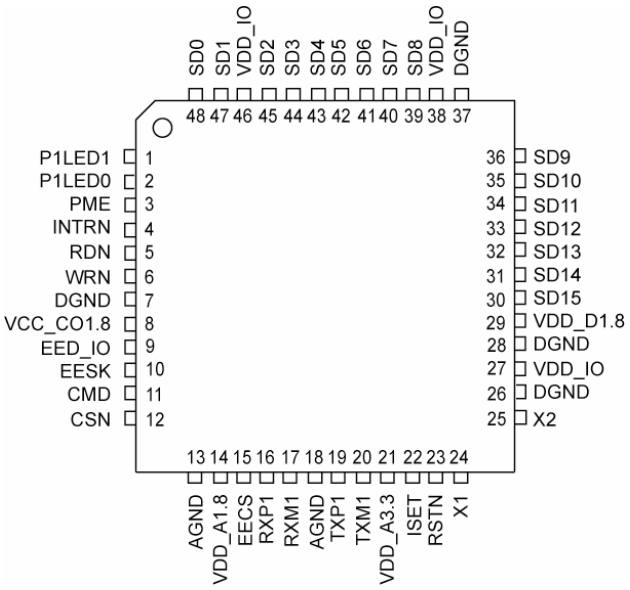


Figure 2. 48-Pin LQFP (V)

Pin Description

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>P1LED1</td><td>Ipu/O</td><td rowspan="2">Programmable LED output to indicate port activity/status.
LED is ON when output is LOW; LED is OFF when output is HIGH.
Port 1 LED indicators[1] defined as follows:
<table>
<tr><th></th><th colspan="2">Chip Global Control Register: CGCR bit [9]</th></tr>
<tr><th></th><th>0 (Default)</th><th>1</th></tr>
<tr><td>P1LED1</td><td>100BT</td><td>ACT</td></tr>
<tr><td>P1LED0</td><td>LINK/ACT</td><td>LINK</td></tr>
</table>
1. Link = LED On; Activity = LED Blink; Link/Act = LED On/Blink;
Speed = LED On (100BASE-T); LED Off (10BASE-T)
Config Mode: The P1LED1 pull-up/pull-down value is latched as 16/8-bit mode during power-up / reset. See “Strapping Options” section for details</td></tr>
<tr><td>2</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>3</td><td>PME</td><td>Opu</td><td>Power Management Event (default active low): It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851-16MLLJ. The KSZ8851-16MLLJ is requesting the system to wake up from low power mode.</td></tr>
<tr><td>4</td><td>INTRN</td><td>Opu</td><td>Interrupt: An active low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor.</td></tr>
<tr><td>5</td><td>RDN</td><td>Ipu</td><td>Read Strobe Not
Asynchronous read strobe, active low to indicate read cycle.</td></tr>
<tr><td>6</td><td>WRN</td><td>Ipu</td><td>Write Strobe Not
Asynchronous write strobe, active low to indicate write cycle.</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDD_CO1.8</td><td>P</td><td>1.8V regulator output . This 1.8V output pin provides power to pins 14 (VDD_A1.8) and 29 (VDD_D1.8) for core VDD supply.
If VDD_IO is set for 1.8V then this pin should be left floating, pins 14 (VDD_A1.8) and 29 (VDD_D1.8) will be sourced by the external 1.8V supply that is tied to pins 27, 38 and 46 (VDD_IO) with appropriate filtering.</td></tr>
<tr><td>9</td><td>EED_IO</td><td>Ipd/O</td><td>In/Out Data from/to external EEPROM.
Config Mode: The pull-up/pull-down value is latched as with/without EEPROM during power-up / reset. See “Strapping Options” section for details</td></tr>
<tr><td>10</td><td>EESK</td><td>Ipd/O</td><td>EEPROM Serial Clock
A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25MHz) or 800ns (OBCR[1:0]=00 on-chip bus speed @ 125MHz) serial output clock cycle to load configuration data from the serial EEPROM.
Config Mode: The pull-up/pull-down value is latched as big/little endian mode during power-up / reset. See “Strapping Options” section for details</td></tr>
<tr><td>11</td><td>CMD</td><td>Ipd</td><td>Command Type
This command input decides the SD[15:0] shared data bus access information.
When command input is low, the access of shared data bus is for data access in 16-bit mode shared data bus SD[15:0] or in 8-bit mode shared data bus SD[7:0].
When command input is high, the access of shared data bus is for address A[7:2] access at shared data bus SD[7:2], byte enable BE[3:0] at SD[15:12] and the SD[11:8] is “don’t care” in 16-bit mode. It is for address A[7:0] access at SD[7:0] in 8-bit mode.</td></tr>
</table>

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
12	CSN	Ipu	Chip Select Not Chip select for the shared data bus access enable, active Low.
13	AGND	Gnd	Analog ground
14	VDD_A1.8	P	1.8V analog power supply from VDD_CO1.8 (pin 8) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 27, 38 and 46 (VDD_IO) with appropriate filtering.
15	EECS	Opd	EEPROM Chip Select This signal is used to select an external EEPROM device.
16	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
17	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential).
18	AGND	Gnd	Analog ground.
19	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
20	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential).
21	VDD_A3.3	P	3.3V analog VDD input power supply with well decoupling capacitors.
22	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
23	RSTN	Ipu	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
24	X1	I	25MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50ppm for either crystal or oscillator.
25	X2	O	
26	DGND	Gnd	Digital ground
27	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power supply for IO with well decoupling capacitors.
28	DGND	Gnd	Digital ground
29	VDD_D1.8	P	1.8V digital power supply from VDD_CO1.8 (pin 8) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 27, 38 and 46 (VDD_IO) with appropriate filtering.
30	SD15	I/O (pd)	Shared Data Bus bit 15. Data D15 access when CMD=0. Byte Enable 3 at double-word boundary access (BE3, 4th byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
31	SD14	I/O (pd)	Shared Data Bus bit 14. Data D14 access when CMD=0. Byte Enable 2 at double-word boundary access (BE2, 3rd byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
32	SD13	I/O (pd)	Shared Data Bus bit 13. Data D13 access when CMD=0. Byte Enable 1 at double-word boundary access (BE1, 2nd byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
33	SD12	I/O (pd)	Shared Data Bus bit 12. Data D12 access when CMD=0. Byte Enable 0 at double-word boundary access (BE0, 1st byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
34	SD11	I/O (pd)	Shared Data Bus bit 11. Data D11 access when CMD=0. Don’t care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
35	SD10	I/O (pd)	Shared Data Bus bit 10. Data D10 access when CMD=0. Don’t care when CMD=1. This pin must be tied to GND in 8-bit bus mode.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
36	SD9	I/O (pd)	Shared Data Bus bit 9. Data D9 access when CMD=0. Don't care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
37	DGND	Gnd	Digital ground
38	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power supply for IO with well decoupling capacitors.
39	SD8	I/O (pd)	Shared Data Bus bit 8. Data D8 access when CMD=0. Don't care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
40	SD7	I/O (pd)	Shared Data Bus bit 7. Data D7 access when CMD=0. Address A7 access when CMD=1.
41	SD6	I/O (pd)	Shared Data Bus bit 6. Data D6 access when CMD=0. Address A6 access when CMD=1.
42	SD5	I/O (pd)	Shared Data Bus bit 5. Data D5 access when CMD=0. Address A5 access when CMD=1.
43	SD4	I/O (pd)	Shared Data Bus bit 4. Data D4 access when CMD=0. Address A4 access when CMD=1.
44	SD3	I/O (pd)	Shared Data Bus bit 3. Data D3 access when CMD=0. Address A3 access when CMD=1.
45	SD2	I/O (pd)	Shared Data Bus bit 2. Data D2 access when CMD=0. Address A2 access when CMD=1.
46	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power supply for IO with well decoupling capacitors.
47	SD1	I/O (pd)	Shared Data Bus bit 1. Data D1 access when CMD=0. In 8-bit mode, this is address A1 access when CMD=1. In 16-bit mode, this is "Don't care" when CMD=1.
48	SD0	I/O (pd)	Shared Data Bus bit 0. Data D0 access when CMD=0. In 8-bit mode, this is address A0 access when CMD=1. In 16-bit mode, this is "Don't care" when CMD=1.

Legend:

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output.
Ipd = Input with internal pull-down (58K ±30%).

Ipu = Input with internal pull-up (58K ±30%).

Opd = Output with internal pull-down (58K ±30%).

Opu = Output with internal pull-up (58K ±30%).

Ipu/O = Input with internal pull-up (58K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (58K ±30%) during power-up/reset; output pin otherwise.
I/O (pd) = Input/Output with internal pull-down (58K ±30%).

Strapping Options

Pin Number	Pin Name	Type	Pin Function
1	P1LED1	Ipu/O	8 or 16-bit bus mode select during power-up / reset: NC or Pull-up (default) = 16-bit bus Pull-down = 8-bit bus This pin value is also latched into register CCR, bit 6/7.
9	EED_IO	Ipd/O	EEPROM select during power-up / reset: Pull-up = EEPROM present NC or Pull-down (default) = EEPROM not present This pin value is latched into register CCR, bit 9.
10	EESK	Ipd/O	Endian mode select during power-up / reset: Pull-up = Big Endian NC or Pull-down (default) = Little Endian This pin value is latched into register CCR, bit 10. When this pin is no connect or tied to GND, the bit 11 (Endian mode selection) in RXFDPR register can be used to program either Little (bit11=0 default) Endian mode or Big (bit11=1) Endian mode.

Notes:
Ipu/O = Input with internal pull-up (58K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (58K ±30%) during power-up/reset; output pin otherwise.
Pin strap-ins are latched during power-up or reset.

Functional Description

The KSZ8851-16MLLJ is a single-chip Fast Ethernet MAC/PHY controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Bus Interface Unit (BIU) that controls the KSZ8851-16MLLJ via an 8-bit or 16-bit host bus interface.

The KSZ8851-16MLLJ is fully compliant to IEEE802.3u standards.

Functional Overview

Power Management

The KSZ8851-16MLLJ supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are four operation modes under the power management function which is controlled by two bits in PMECR (0xD4) register as shown below:

PMECR[1:0] = 00 Normal Operation Mode

PMECR[1:0] = 01 Energy Detect Mode

PMECR[1:0] = 10 Soft Power Down Mode

PMECR[1:0] = 11 Power Saving Mode

Table 1 indicates all internal function blocks status under four different power management operation modes.

KSZ8851-16MLLJ Function Blocks	Power Management Operation Modes			
	Normal Mode	Power Saving Mode	Energy Detect Mode	Soft Power Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
Tx/Rx PHY	Enabled	Rx unused block disabled	Energy detect at Rx	Disabled
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

Table 1. Internal Function Blocks Status

Normal Operation Mode

This is the default setting bit[1:0]=00 in PMECR register after the chip power-up or hardware reset (pin 67). When KSZ8851-16MLLJ is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in PMECR register to transit the current normal operation mode to any one of the other three power management operation modes.

Energy Detect Mode

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8851-16MLLJ is not connected to an active link partner. For example, if cable is not present or it is connected to a powered down partner, the KSZ8851-16MLLJ can automatically enter to the low power state in energy detect mode. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851-16MLLJ can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8851-16MLLJ reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0]=01 in PMECR register. When the KSZ8851-16MLLJ is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in GSWUTR register, KSZ8851-16MLLJ will go into a low power state. When KSZ8851-16MLLJ is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable and is continuously presented for a time longer than pre-configured value at bit[15:8] Wake-Up time in GSWUTR register, the KSZ8851-16MLLJ will enter either the normal power state if the auto-wakeup enable bit[7] is set in PMECR register or the normal operation mode if both auto-wakeup enable bit[7] and wakeup to normal operation mode bit[6] are set in PMECR register.

The KSZ8851-16MLLJ will also assert PME output pin if the corresponding enable bit[8] is set in PMECR (0xD4) register or generate interrupt to signal an energy detect event occurred if the corresponding enable bit[2] is set in IER (0x90) register. Once the power management unit detects the PME output asserted or interrupt active, it will power up the host CPU and issue a wakeup command which is a read cycle to read the Globe Reset Register (GRR at 0x26) to wake up the KSZ8851-16MLLJ from the low power state to the normal power state in case the auto-wakeup enable bit[7] is disabled. When KSZ8851-16MLLJ is at normal power state, it is able to transmit or receive packet from the cable.

Soft Power Down Mode

The soft power down mode is entered by setting bit[1:0]=10 in PMECR register. When KSZ8851-16MLLJ is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change, and the host interface is only used to wake-up this device from current soft power down mode to normal operation mode.

In order to go back the normal operation mode from this soft power down mode, the only way to leave this mode is through a host wake-up command which the CPU issues to read the Globe Reset Register (GRR at 0x26).

Power Saving Mode

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0]=11 in PMECR register and bit [10]=1 in P1SCLMD register. When KSZ8851M is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851M can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can program the bit[1:0] in PMECR register and set bit[10]=0 in P1SCLMD register to transit the current power saving mode to any one of the other three power management operation modes.

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic. The KSZ8851-16MLLJ controller can be programmed to notify the host of the wake-up frame detection with the assertion of the interrupt signal (INTRN) or assertion of the power management event signal (PME).

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

1. Detection of energy signal over a pre-configured value (bit 2 in ISR register)

2. Detection of a linkup in the network link state (bit 3 in ISR register)

3. Receipt of a Magic Packet (bit 4 in ISR register)

4. Receipt of a network wake-up frame (bit 5 in ISR register)

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

Detection of Energy

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

Detection of Linkup

Link status wake events are useful to indicate a linkup in the network’s connectivity status.

Wake-Up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a 'wake up' frame. The KSZ8851-16MLLJ supports up to four users defined wake-up frames as below:

1. Wake-up frame 0 is defined in wakeup frame registers (0x30 – 0x3B) and is enabled by bit 0 in wakeup frame control register (0x2A).

2. Wake-up frame 1 is defined in wakeup frame registers (0x40 – 0x4B) and is enabled by bit 1 in wakeup frame control register (0x2A).

3. Wake-up frame 2 is defined in wakeup frame registers (0x50 – 0x5B) and is enabled by bit 2 in wakeup frame control register (0x2A).

4. Wake-up frame 3 is defined in wakeup frame registers (0x60 – 0x6B) and is enabled by bit 3 in wakeup frame control register (0x2A).

Magic Packet™

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8851-16MLLJ. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8851-16MLLJ has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8851-16MLLJ controller detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PME pin) to wake up the system.

Physical Layer Transceiver (PHY)

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 3.01KΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer can generate either 125MHz, 62.5MHz, 41.66MHz, or 25MHz clocks by setting the on-chip bus control register (0x20) for KSZ8851-16MLLJ system timing. These internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-Scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.4V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8851-16MLLJ decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8851-16MLLJ supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8851-16MLLJ device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers. The IEEE 802.3u standard MDI and MDI-X definitions are as below:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 2. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

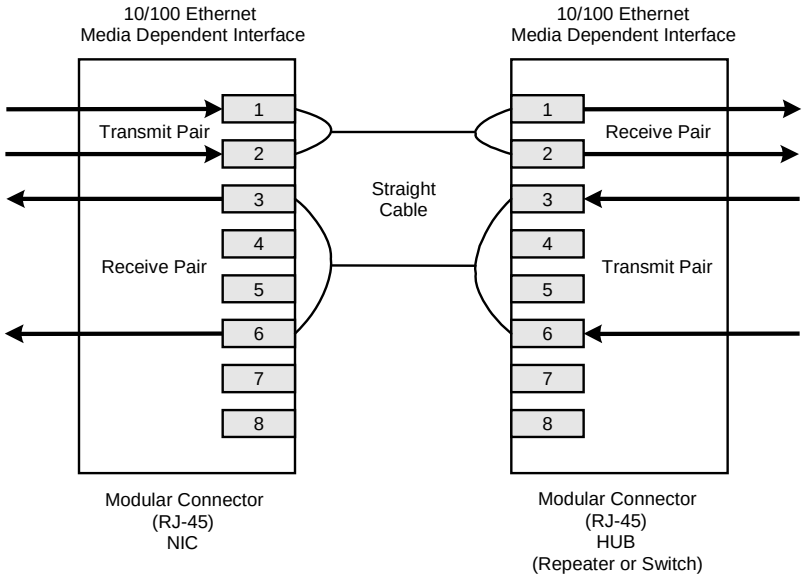


Figure 3. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two chips or hubs (two MDI-X devices).

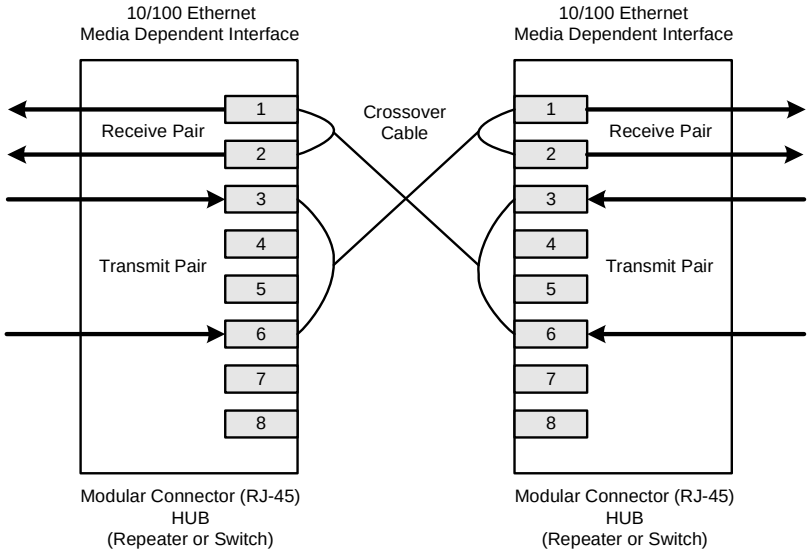


Figure 4. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8851-16MLLJ conforms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10Base-T or 100Base-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8851-16MLLJ is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram (Figure 5).

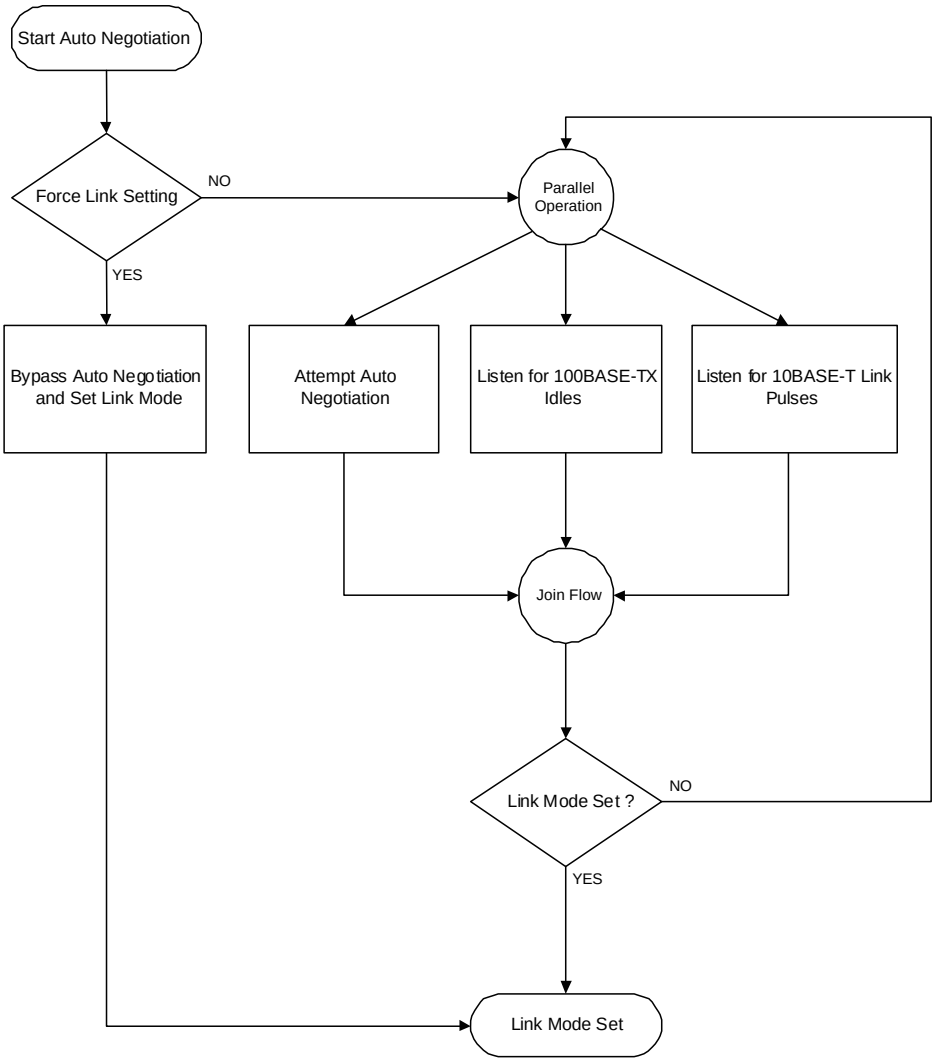


Figure 5. Auto Negotiation and Parallel Operation

LinkMD® Cable Diagnostics

The KSZ8851-16MLLJ LinkMD® uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1SCLMD[8:0].

Note: cable diagnostics are only valid for copper connections – fiber-optic operation is not supported.

Access

LinkMD® is initiated by accessing register P1SCLMD, the PHY special control/status & LinkMD® register (0xF4).

Usage

LinkMD® can be run at any time by ensuring that Auto-MDIX has been disabled. To disable Auto-MDIX, write a '1' to P1CR[10] to enable manual control over the pair used to transmit the LinkMD® pulse. The self-clearing cable diagnostic test enable bit, P1SCLMD [12], is set to '1' to start the test on this pair.

When bit P1SCLMD[12] returns to '0', the test is complete. The test result is returned in bits P1SCLMD[14:13] and the distance is returned in bits P1SCLMD[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD® failed

If P1SCLMD[14:13]=11, this indicates an invalid test, and occurs when the KSZ8851-16MLLJ is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8851-16MLLJ to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

P1SCLMD[8:0] x 0.4m for port 1 cable distance

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Media Access Control (MAC) Operation

The KSZ8851-16MLLJ strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

Back-Off Algorithm

The KSZ8851-16MLLJ implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Flow Control

The KSZ8851-16MLLJ supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8851-16MLLJ receives a pause control frame, the KSZ8851-16MLLJ will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8851-16MLLJ are transmitted.

On the transmit side, the KSZ8851-16MLLJ has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources.

There are three programmable low watermark register FCLWR (0xB0), high watermark register FCHWR (0xB2) and overrun watermark register FCOWR (0xB4) for flow control in RXQ FIFO. The KSZ8851-16MLLJ will send PAUSE frame when the RXQ buffer hit the high watermark level (default 3.072KByte available) and stop PAUSE frame when the RXQ buffer hit the low watermark level (default 5.12KByte available). The KSZ8851-16MLLJ will drop packet when the RXQ buffer hit the overrun watermark level (default 256-Byte available).

The KSZ8851-16MLLJ issues a flow control frame (Xoff, or transmitter off), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8851-16MLLJ sends out the another flow control frame (Xon, or transmitter on) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

Half-Duplex Backpressure

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8851-16MLLJ sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8851-16MLLJ discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

Address Filtering Function

The KSZ8851-16MLLJ supports 11 different address filtering schemes as shown in the following Table 3. The Ethernet destination address (DA) field inside the packet is the first 6-byte field which uses to compare with either the host MAC address registers (0x10 – 0x15) or the MAC address hash table registers (0xA0 – 0xA7) for address filtering operation. The first bit (bit 40) of the destination address (DA) in the Ethernet packet decides whether this is a physical address if bit 40 is “0” or a multicast address if bit 40 is “1”.

Item	Receive Control Register (0x74 – 0x75): RXCR1					Description
	Address Filtering Mode	RX ALL (Bit 4)	RX Inverse (Bit 1)	RX Physical Address	RX Multicast Address	
1	Perfect	0	0	1	1	All Rx frames are passed only if the DA exactly matches the MAC address in MARL, MARM and MARH registers.
2	Inverse perfect	0	1	1	1	All Rx frames are passed if the DA is not matching the MAC address in MARL, MARM and MARH registers.
3	Hash only	0	0	0	0	All Rx frames with either multicast or physical destination address are filtering against the MAC address hash table.
4	Inverse hash only	0	1	0	0	All Rx frames with either multicast or physical destination address are filtering not against the MAC address hash table. All Rx frames which are filtering out at item 3 (Hash only) only are passed in this mode.
5	Hash perfect (Default)	0	0	1	0	All Rx frames are passed with Physical address (DA) matching the MAC address and to enable receive multicast frames that pass the hash table when Multicast address is matching the MAC address hash table.
6	Inverse hash perfect	0	1	1	0	All Rx frames which are filtering out at item 5 (Hash perfect) only are passed in this mode.
7	Promiscuous	1	1	0	0	All Rx frames are passed without any conditions.
8	Hash only with Multicast address passed	1	0	0	0	All Rx frames are passed with Physical address (DA) matching the MAC address hash table and with Multicast address without any conditions.
9	Perfect with Multicast address passed	1	0	1	1	All Rx frames are passed with Physical address (DA) matching the MAC address and with Multicast address without any conditions.
10	Hash only with Physical address passed	1	0	1	0	All Rx frames are passed with Multicast address matching the MAC address hash table and with Physical address without any conditions.
11	Perfect with Physical address passed	1	0	0	1	All Rx frames are passed with Multicast address matching the MAC address and with Physical address without any conditions.

Notes:
1. Bit 0 (RX Enable), Bit 5 (RX Unicast Enable) and Bit 6 (RX Multicast Enable) must set to 1 in RXCR1 register.
2. The KSZ8851-16MLLJ will discard frame with SA same as the MAC address if bit[0] is set in RXCR2 register.

Table 3. Address Filtering Scheme

Clock Generator

The X1 and X2 pins are connected to a 25MHz crystal. X1 can also serve as the connector to a 3.3V, 25MHz oscillator (as described in the pin description).

Bus Interface Unit (BIU)

The BIU host interface is a generic shared data bus interface, designed to communicate with embedded processors. No glue logic is required when it talks to various standard asynchronous buses and processors.

Supported Transfers

In terms of transfer type, the BIU can support asynchronous transfer or SRAM-like slave mode. To support the data transfers, the BIU provides a group of signals:

Shared Data bus SD[15:0] for Address, Data and Byte Enable, Command (CMD), Chip Select Enable (CSN), Read (RDN), Write (WRN) and Interrupt (INTRN).

Physical Data Bus Size

The BIU supports an 8-bit or 16-bit host standard data bus. Depending on the size of the physical data bus, the KSZ8851-16MLLJ can support 8-bit or 16-bit data transfers.

For example,

For a 16-bit data bus mode, the KSZ8851-16MLLJ allows an 8-bit and 16-bit data transfer.

For an 8-bit data bus mode, the KSZ8851-16MLLJ only allows an 8-bit data transfer.

The KSZ8851-16MLLJ supports internal data byte-swap. This means that the system/host data bus HD[7:0] just connect to SD[7:0] for an 8-bit data bus interface. For a 16-bit data bus, the system/host data bus HD[15:8] and HD[7:0] only need to connect to SD[15:8] and SD[7:0] respectively.

Table 4 describes the BIU signal grouping.

Signal	Type	Function
SD[15:0]	I/O	**Shared Data Bus** Data D[15:0] -> SD[15:0] access when CMD=0. Address A[7:2] -> SD[7:2] and Byte Enable BE[3:0] -> SD[15:12] access when CMD=1 in 16-bit mode. Address A[7:0] -> SD[7:0] only access when CMD=1 in 8-bit mode (Shared data bus SD[15:8] must be tied to low in 8-bit bus mode).
CMD	Input	**Command Type** This command input decides the SD[15:0] shared data bus access cycle information.
CSN	Input	**Chip Select Enable** Chip Enable asserted (low) indicates that the shared data bus access is enabled.
INTRN	Output	**Interrupt** This pin is asserted to low when interrupt occurred.
RDN	Input	**Asynchronous Read** This pin is asserted to low during read cycle.
WRN	Input	**Asynchronous Write** This pin is asserted to low during write cycle.

Table 4. Bus Interface Unit Signal Grouping

Little and Big Endian Support

The KSZ8851-16MLLJ supports either Little- or Big-Endian microprocessor. The external strap pin 10 (EESK) is used to select between two modes. The KSZ8851-16MLLJ operates in Little Endian when this pin is pulled-down or in Big Endian when this pin is pulled-up.

When this pin 10 is no connect or tied to GND, the bit 11 (Endian mode selection) in RXFDPR register can be used to program either Little (bit11=0) Endian mode or Big (bit11=1) Endian mode.

Asynchronous Interface

For asynchronous transfers, the asynchronous interface uses RDN (read) and WRN (write) signal strobes for data latching. The host utilizes the rising edge of RDN to latch read data and the KSZ8851-16MLLJ will use falling edge of WRN to latch write data.

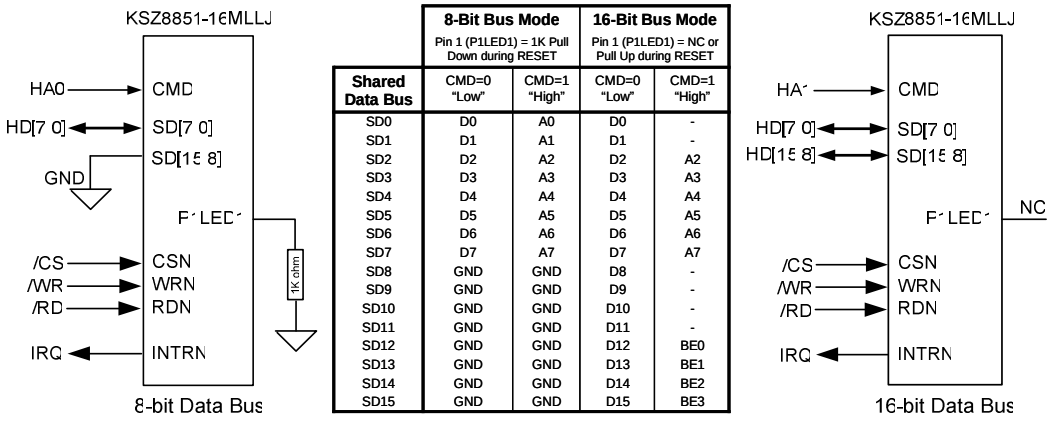
All asynchronous transfers are either single-data or burst-data transfers. Byte or word data bus access (transfers) is supported. The BIU, however, provides flexible asynchronous interfacing to communicate with various applications and architectures. No additional address latch is required. The BIU qualifies both CSN (Chip Select) pin and WRN (Write Enable) pin to write the Address A[7:2] and BE[3:0] value (in 16-bit mode) or Address A[7:0] value (in 8-bit mode) into KSZ8851-16MLLJ when CMD (Command type) pin is high. The BIU qualifies both CSN (Chip Select) pin and RDN (Read Enable) or WRN (Write Enable) pin to read or write the SD[15:0] data value from or to KSZ8851-16MLLJ when CMD (Command type) pin is low.

In order for software to read back the previous CMD register write value when CMD is “1”, the BIU qualifies both CSN (Chip Select) pin and RDN (Read Enable) pin to read the Address A[7:2] and BE[3:0] value (in 16-bit mode) or Address A[7:0] value (in 8-bit mode) back from KSZ8851-16MLLJ when CMD (Command type) pin is high.

BIU Summation

Figure 6 shows the connection for different data bus sizes. Also refer to reference schematics in hardware design package.

All of control and status registers in the KSZ8851-16MLLJ are accessed indirectly depending on CMD (Command type) pin. The command sequence to access the specified control or status register is to write the register’s address (when CMD=1) then read or write this register data (when CMD=0). If both RDN and WRN signals in the system are only used for KSZ8851-16MLLJ, the CSN pin can be forced to active low to simplify the system design. The CMD pin can be connected to host address line HA0 for 8-bit bus mode or HA1 for 16-bit bus mode.



Shared Data Bus	8-Bit Bus Mode Pin 1 (P1LED1) = 1K Pull Down during RESET		16-Bit Bus Mode Pin 1 (P1LED1) = NC or Pull Up during RESET	
	CMD=0 “Low”	CMD=1 “High”	CMD=0 “Low”	CMD=1 “High”
SD0	D0	A0	D0	-
SD1	D1	A1	D1	-
SD2	D2	A2	D2	A2
SD3	D3	A3	D3	A3
SD4	D4	A4	D4	A4
SD5	D5	A5	D5	A5
SD6	D6	A6	D6	A6
SD7	D7	A7	D7	A7
SD8	GND	GND	D8	-
SD9	GND	GND	D9	-
SD10	GND	GND	D10	-
SD11	GND	GND	D11	-
SD12	GND	GND	D12	BE0
SD13	GND	GND	D13	BE1
SD14	GND	GND	D14	BE2
SD15	GND	GND	D15	BE3

Figure 6. KSZ8851-16MLLJ 8-Bit and 16-Bit Data Bus Connections

Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic between the MAC/PHY interface and the system host. It has built-in packet memory for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). Each queue contains 12KB for RXQ and 6KB for TXQ of memory with back-to-back, non-blocking frame transfer performance. It provides a group of control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

Transmit Queue (TXQ) Frame Format

The frame format for the transmit queue is shown in the following Table 5. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled in TXCR (bit 1) register.

Multiple frames can be pipelined in both the transmit queue and receive queue as long as there is enough queue memory, thus avoiding overrun. For each transmitted frame, the transmit status information for the frame is located in the TXSR (0x72) register.

Packet Memory Address Offset	Bit 15 Bit 0 2nd Byte 1st Byte
0	Control Word (High byte and low byte need to swap in Big-Endian mode)
2	Byte Count (High byte and low byte need to swap in Big-Endian mode)
4 - up	Transmit Packet Data (maximum size is 2000)

Table 5. Frame Format for Transmit Queue

Since multiple packets can be pipelined into the TX packet memory for transmit, the transmit status reflects the status of the packet that is currently being transferred on the MAC interface, which may or may not be the last queued packet in the TX queue.

The transmit control word is the first 16-bit word in the TX packet memory, followed by a 16-bit byte count. It must be word aligned. Each control word corresponds to one TX packet. Table 6 gives the transmit control word bit fields.

Bit	Description
15	**TXIC Transmit Interrupt on Completion** When this bit is set, the KSZ8851-16MLLJ sets the transmit interrupt after the present frame has been transmitted.
14-6	Reserved.
5-0	**TXFID Transmit Frame ID** This field specifies the frame ID that is used to identify the frame and its associated status information in the transmit status register.

Table 6. Transmit Control Word Bit Fields

The transmit Byte Count specifies the total number of bytes to be transmitted from the TXQ. Its format is given in Table 7.

Bit	Description
15-11	Reserved.
10-0	**TXBC Transmit Byte Count** Transmit Byte Count. Hardware uses the byte count information to conserve the TX buffer memory for better utilization of the packet memory. Note: The hardware behavior is unknown if an incorrect byte count information is written to this field. Writing a 0 value to this field is not permitted.

Table 7. Transmit Byte Count Format

The data area contains six bytes of Destination Address (DA) followed by six bytes of Source Address (SA), followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The KSZ8851-16MLLJ does not insert its own SA. The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the KSZ8851-16MLLJ. It is treated transparently as data both for transmit operations.

Frame Transmitting Path Operation in TXQ

This section describes the typical register settings for transmitting packets from host processor to KSZ8851-16MLLJ with generic bus interface. User can use the default value for most of the transmit registers. The following Table 8 describes all registers which need to be set and used for transmitting single or multiple frames.

Register Name [bit](offset)	Description
TXCR[3:0](0x70) TXCR[8:5](0x70)	Set transmit control function as below: Set bit 3 to enable transmitting flow control. Set bit 2 to enable transmitting padding. Set bit 1 to enable transmitting CRC. Set bit 0 to enable transmitting block operation. Set transmit checksum generation for ICMP, UDP, TCP and IP packet.
TXMIR[12:0](0x78)	The amount of free transmit memory available is represented in units of byte. The TXQ memory (6 KByte) is used for both frame payload and control word.
TXQCR[0](0x80)	For single frame to transmit, set this bit 0 = 1(manual enqueue). the KSZ8851-16MLLJ will enable current TX frame prepared in the TX buffer is queued for transmit, this is only transmit one frame at a time. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.
TXQCR[1](0x80)	When this bit is written as 1, the KSZ8851-16MLLJ will generate interrupt (bit 6 in ISR register) to CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at TXNTFSR (0x9E) register. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before set to 1 again
TXQCR[2](0x80)	For multiple frames to transmit, set this bit 2 = 1 (auto-enqueue). the KSZ8851-16MLLJ will enable current all TX frames prepared in the TX buffer are queued to transmit automatically.
RXQCR[3](0x82)	Set bit 3 to start DMA access from host CPU either read (receive frame data) or write (transmit data frame)
TXFDPR[14](0x84)	Set bit 14 to enable TXQ transmit frame data pointer register increments automatically on accesses to the data register.
IER[14][6](0x90)	Set bit 14 to enable transmit interrupt in Interrupt Enable Register Set bit 6 to enable transmit space available interrupt in Interrupt Enable Register.
ISR[15:0](0x92)	Write 1 (0xFFFF) to clear all interrupt status bits after interrupt occurred in Interrupt Status Register.
TXNTFSR[15:0](0x9E)	The host CPU is used to program the total amount of TXQ buffer space which is required for next total transmit frames size in double-word count.

Table 8. Registers Setting for Transmit Function Block

Driver Routine for Transmit Packet from Host Processor to KSZ8851-16MLLJ

The transmit routine is called by the upper layer to transmit a contiguous block of data through the Ethernet controller. It is user's choice to decide how the transmit routine is implemented. If the Ethernet controller encounters an error while transmitting the frame, it's the user's choice to decide whether the driver should attempt to retransmit the same frame or discard the data. The following Figures 7 and 8 shows the step-by-step for single and multiple transmit packets from host processor to KSZ8851-16MLLJ.

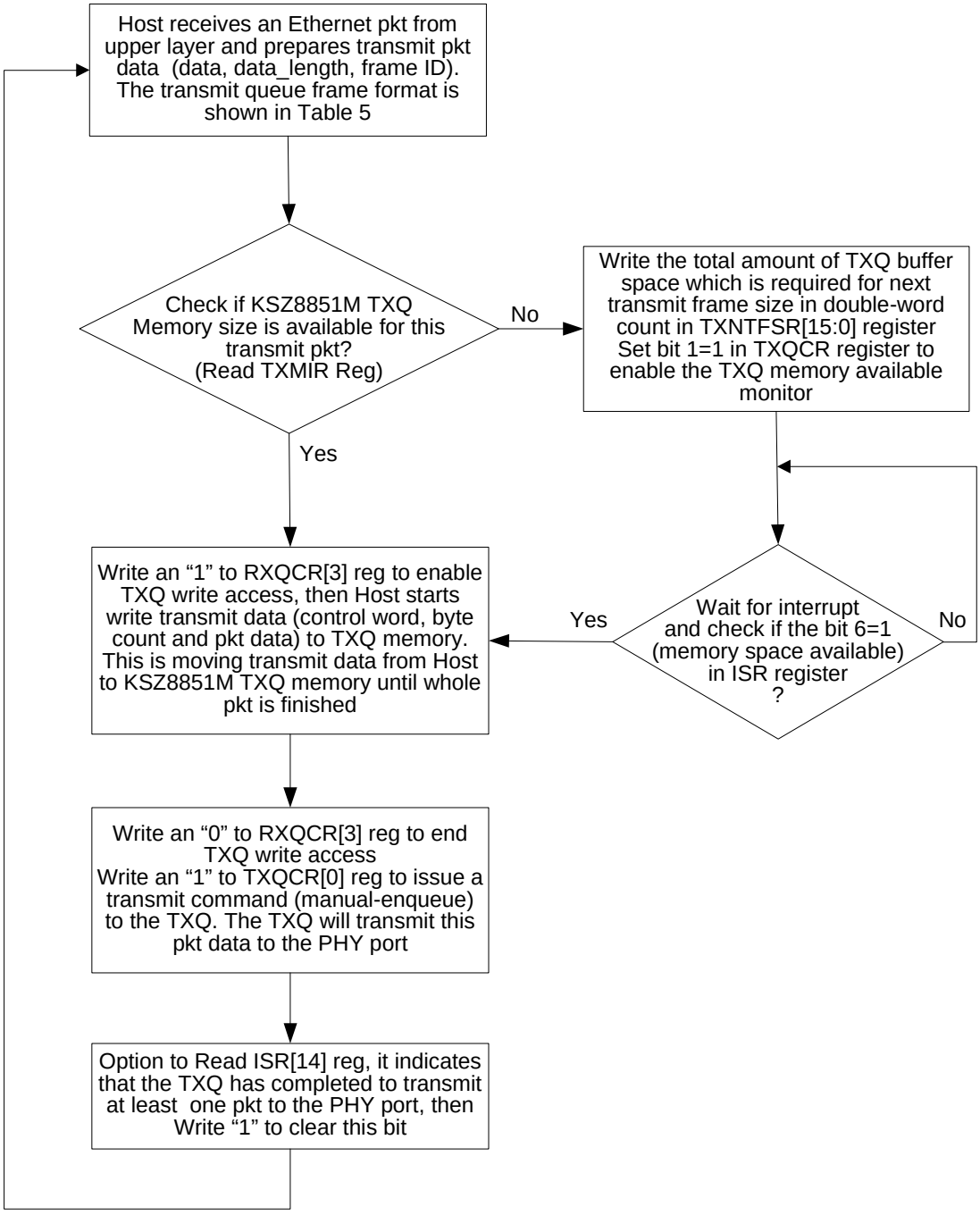


Figure 7. Host TX Single Frame in Manual Enqueue Flow Diagram

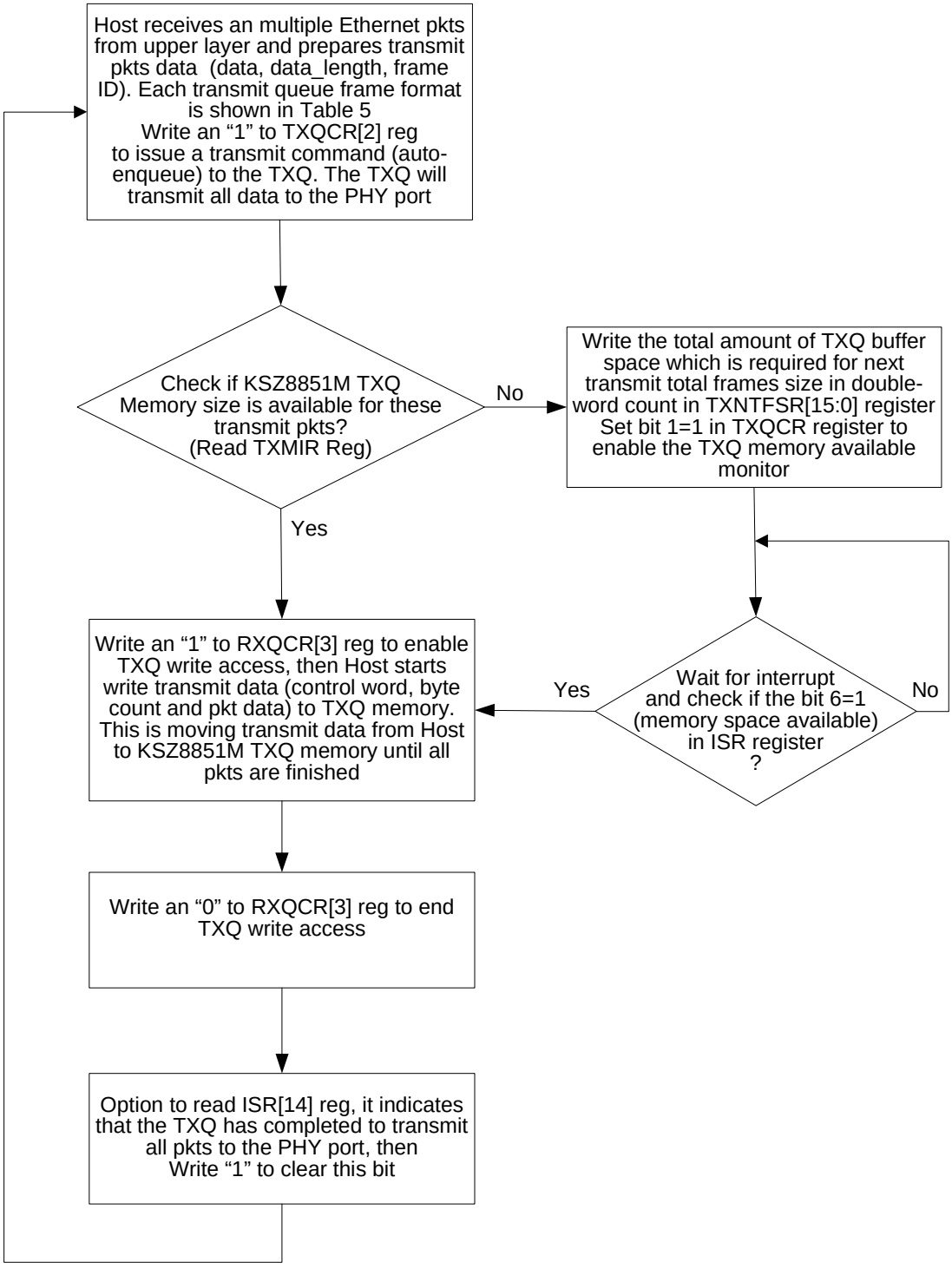


Figure 8. Host TX Multiple Frames in Auto- Enqueue Flow Diagram

Receive Queue (RXQ) Frame Format

The frame format for the receive queue is shown in Table 9. The first word contains the status information for the frame received. The second word is the total number of bytes of the RX frame. Following that is the packet data area. The packet data area holds the frame itself. It includes the CRC checksum.

Packet Memory Address Offset	Bit 15 2nd Byte / Bit 0 1st Byte
0	Status Word (High byte and low byte need to swap in Big-Endian mode. Also see description in RXFHSR register)
2	Byte Count (High byte and low byte need to swap in Big-Endian mode. Also see description in RXFHBCR register)
4 - up	Receive Packet Data (maximum size is 2000)

Table 9. Frame Format for Receive Queue

Frame Receiving Path Operation in RXQ

This section describes the typical register settings for receiving packets from KSZ8851-16MLLJ to host processor with generic bus interface. User can use the default value for most of the receive registers. The following Table 10 describes all registers which need to be set and used for receiving single or multiple frames.

Register Name[bit](offset)	Description
RXCR1(0x74) RXCR2(0x76)	Set receive control function as below: Set RXCR1[10] to enable receiving flow control. Set RXCR1[0] to enable receiving block operation. Set receive checksum check for ICMP, UDP, TCP and IP packet. Set receive address filtering scheme as shown in the Table 3.
RXFHSR[15:0](0x7C)	This register (read only) indicates the current received frame header status information.
RXFHBCR[11:0](0x7E)	This register (read only) indicates the current received frame header byte count information.
RXQCR[12:3](0x82)	Set RXQ control function as below: Set bit 3 to start DMA access from host CPU either read (receive frame data) or write (transmit data frame). Set bit 4 to automatically enable RXQ frame buffer dequeue. Set bit 5 to enable RX frame count threshold and read bit 10 for status. Set bit 6 to enable RX data byte count threshold and read bit 11 for status. Set bit 7 to enable RX frame duration timer threshold and read bit 12 for status. Set bit 9 enable RX IP header two-byte offset.
RXFDPR[14](0x86)	Set bit 14 to enable RXQ address register increments automatically on accesses to the data register.
RXDTTR[15:0](0x8C)	To program received frame duration timer value. When Rx frame duration in RXQ exceeds this threshold in 1uS interval count and bit 7 of RXQCR register is set to 1, the KSZ8851-16MLLJ will generate RX interrupt in ISR[13] and indicate the status in RXQCR[12].
RXDBCTR[15:0](0x8E)	To program received data byte count value. When the number of received bytes in RXQ exceeds this threshold in byte count and bit 6 of RXQCR register is set to 1, the KSZ8851-16MLLJ will generate RX interrupt in ISR[13] and indicate the status in RXQCR[11].
IER[13](0x90)	Set bit 13 to enable receive interrupt in Interrupt Enable Register.
ISR[15:0](0x92)	Write 1 (0xFFFF) to clear all interrupt status bits after interrupt occurred in Interrupt Status Register.
RXFCTR[15:8](0x9C)	Rx frame count read only. To indicate the total received frame in RXQ frame buffer when receive interrupt (bit 13 in ISR) occurred.
RXFCTR[7:0](0x9C)	To program received frame count value. When the number of received frames in RXQ exceeds this threshold value and bit 5 of RXQCR register is set to 1, the KSZ8851-16MLLJ will generate RX interrupt in ISR[13] and indicate the status in RXQCR[10].

Table 10. Registers Setting for Receive Function Block

Driver Routine for Receive Packet from KSZ8851-16MLLJ to Host Processor

The software driver receives data packet frames from the KSZ8851-16MLLJ device either as a result of polling or an interrupt based service. When an interrupt is received, the OS invokes the interrupt service routine that is in the interrupt vector table.

If your system has OS support, to minimize interrupt lockout time, the interrupt service routine should handle at interrupt level only those tasks that require minimum execution time, such as error checking or device status change. The routine should queue all the time-consuming work to transfer the packet from the KSZ8851-16MLLJ RXQ into system memory at task level. The following Figure 9 shows the step-by-step for receive packets from KSZ8851-16MLLJ to host processor.

Note: Each DMA read operation from the host CPU to read RXQ frame buffer, the first read data (byte in 8-bit bus mode, word in 16-bit bus mode and double word in 32-bit bus mode) is dummy data and must be discarded by host CPU. Afterward, host CPU must read each frame data to align with double word boundary at end. For example, the host CPU has to read up to 68 bytes if received frame is 65 bytes.

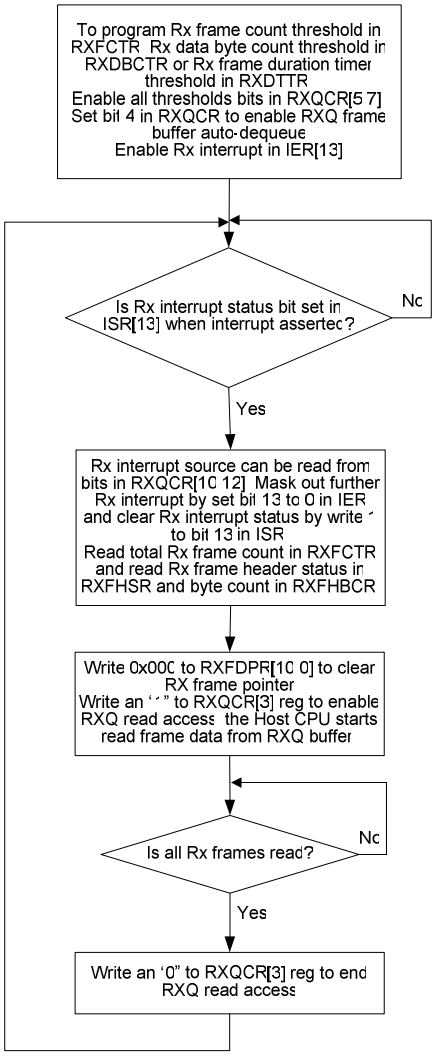


Figure 9. Host RX Single or Multiple Frames in Auto-Dequeue Flow Diagram

In order to read received frames from RXQ without error, the software driver must use following steps:

1. When receive interrupt occurred and software driver writes “1” to clear the RX interrupt in ISR register; the KSZ8851 will update Receive Frame Counter (RXFCTR) Register for this interrupt.
2. When software driver reads back Receive Frame Count (RXFCTR) Register; the KSZ8851 will update both Receive Frame Header Status and Byte Count Registers (RXFHSR/RXFHBCR).
3. When software driver reads back both Receive Frame Header Status and Byte Count Registers (RXFHSR/RXFHBCR); the KSZ8851 will update next receive frame header status and byte count registers (RXFHSR/RXFHBCR).

EEPROM Interface

It is optional in the KSZ8851-16MLLJ to use an external EEPROM. The EED_IO (pin 9) must be pulled high to use external EEPROM otherwise this pin pulled low or floating without EEPROM.

An external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address. The KSZ8851-16MLLJ can detect if the EEPROM is a 1KB (93C46) or 4KB (93C66) EEPROM device (the 93C46 and the 93C66 are typical EEPROM devices). The EEPROM must be organized as 16-bit mode.

If the EED_IO pin is pulled high, then the KSZ8851-16MLLJ performs an automatic read of the external EEPROM words 0H to 3H after the de-assertion of Reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR (0x22) registers.

The KSZ8851-16MLLJ EEPROM format is given in Table 11.

WORD	**15 8**	**7 0**
0H	Reserved	
1H	Host MAC Address Byte 2	Host MAC Address Byte 1
2H	Host MAC Address Byte 4	Host MAC Address Byte 3
3H	Host MAC Address Byte 6	Host MAC Address Byte 5
4H – 6H	Reserved	
7H-3FH	Not used for KSZ8851-16MLLJ (available for user to use)	

Table 11. KSZ8851-16MLLJ EEPROM Format

Loopback Support

The KSZ8851-16MLLJ provides two loopback modes, one is Near-end (Remote) loopback to support for remote diagnostic of failure at line side, and the other is Far-end (Local) loopback to support for local diagnostic of failure at host side. In loopback mode, the speed at the PHY port will be set to 100BASE-TX full-duplex mode.

Near-End (Remote) Loopback

Near-end (Remote) loopback is conducted at PHY port 1 of the KSZ8851-16MLLJ. The loopback path starts at the PHY port's receive inputs (RXP1/RXM1), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXP1/TXM1).

Bit [9] of register P1SCLMD (0xF4) is used to enable near-end loopback. The ports 1 near-end loopback path is illustrated in the following Figure 10.

Far-End (Local) Loopback

Far-end (Local) loopback is conducted at Host of the KSZ8851-16MLLJ. The loopback path starts at the host port's transmit inputs (Tx data), wraps around at the PHY port's PMD/PMA, and ends at the host port's receive outputs (Rx data)

Bit [14] of register P1MBCR (0xE4) is used to enable far-end loopback at host side. The host far-end loopback path is illustrated in the following Figure 10.

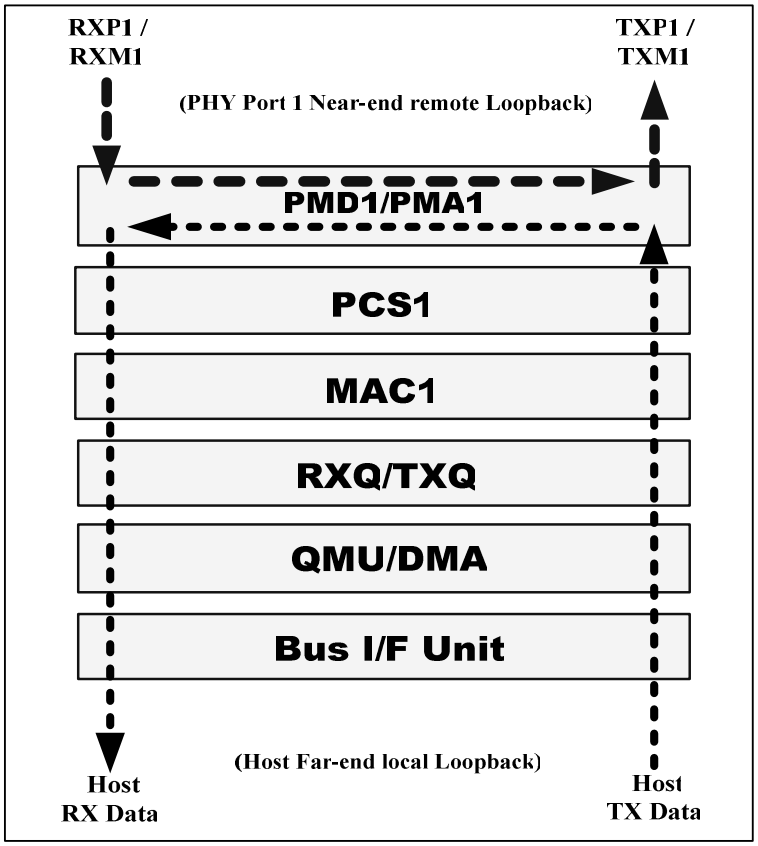


Figure 10. PHY Port 1 Near-End (Remote) and Host Far-End (Local) Loopback Paths

CPU Interface I/O Registers

The KSZ8851-16MLLJ provides an SRAM-like asynchronous bus interface for the CPU to access its internal I/O registers. I/O registers serve as the address that the microprocessor uses when communicating with the device. This is used for configuring operational settings, reading or writing control, status information, and transferring packets. The KSZ8851-16MLLJ can be programmed to interface with either Big-Endian or Little-Endian processor.

I/O Registers

The following I/O Space Mapping Tables apply to 8 or 16-bit bus interface. Depending upon the bus mode selected, each I/O access can be performed the following operations:

In 8-bit bus mode, there are 256 address locations which is based on SD[7:0] for address when CMD=1. The SD[7:0] is for data when CMD=0.

In 16-bit bus mode, there are 64 address locations which is based on SD[7:2] ([1:0] is “don’t care”) for address and SD[15:12] for Byte Enable BE[3:0] (either one byte or two bytes) when CMD=1. The SD[15:0] is for data when CMD=0.

Internal I/O Registers Space Mapping

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x00 - 0x01	0x00 0x01	Reserved	Don't care	None
0x02 - 0x03	0x02 0x03			
0x04 - 0x05	0x04 0x05	Reserved	Don't care	None
0x06 - 0x07	0x06 0x07			
0x08 - 0x09	0x08 0x09	CCR	Read only	Chip Configuration Register [7:0] Chip Configuration Register [15:8]
0x0A - 0x0B	0x0A 0x0B	Reserved	Don't care	None
0x0C - 0x0D	0x0C 0x0D	Reserved	Don't care	None
0x0E - 0x0F	0x0E 0x0F			
0x10 - 0x11	0x10 0x11	MARL	-	MAC Address Register Low [7:0] MAC Address Register Low [15:8]
0x12 - 0x13	0x12 0x13	MARM	-	MAC Address Register Middle [7:0] MAC Address Register Middle [15:8]
0x14 - 0x15	0x14 0x15	MARH	-	MAC Address Register High [7:0] MAC Address Register High [15:8]
0x16 - 0x17	0x16 0x17	Reserved	Don't care	None
0x18 - 0x19	0x18 0x19	Reserved	Don't care	None
0x1A - 0x1B	0x1A 0x1B			
0x1C - 0x1D	0x1C 0x1D	Reserved	Don't care	None
0x1E - 0x1F	0x1E 0x1F			
0x20 - 0x21	0x20 0x21	OBCR	0x0000	On-Chip Bus Control Register [7:0] On-Chip Bus Control Register [15:8]
0x22 - 0x23	0x22 0x23	EEPCR	0x0000	EEPROM Control Register [7:0] EEPROM Control Register [15:8]
0x24 - 0x25	0x24 0x25	MBIR	0x1010	Memory BIST Info Register [7:0] Memory BIST Info Register [15:8]
0x26 - 0x27	0x26 0x27	GRR	0x0000	Global Reset Register [7:0] Global Reset Register [15:8]
0x28 - 0x29	0x28 0x29	Reserved	Don't care	None
0x2A - 0x2B	0x2A 0x2B	WFCR	0x0000	Wakeup Frame Control Register [7:0] Wakeup Frame Control Register [15:8]

Internal I/O Registers Space Mapping (Continued)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x2C - 0x2D	0x2C 0x2D	Reserved	Don't care	
0x2E - 0x2F	0x2E 0x2F			
0x30 - 0x31	0x30 0x31	WF0CRC0	0x0000	Wakeup Frame 0 CRC0 Register [7:0] Wakeup Frame 0 CRC0 Register [15:8]
0x32 - 0x33	0x32 0x33	WF0CRC1	0x0000	Wakeup Frame 0 CRC1 Register [7:0] Wakeup Frame 0 CRC1 Register [15:8]
0x34 - 0x35	0x34 0x35	WF0BM0	0x0000	Wakeup Frame 0 Byte Mask 0 Register [7:0] Wakeup Frame 0 Byte Mask 0 Register [15:8]
0x36 - 0x37	0x36 0x37	WF0BM1	0x0000	Wakeup Frame 0 Byte Mask 1 Register [7:0] Wakeup Frame 0 Byte Mask 1 Register [15:8]
0x38 - 0x39	0x38 0x39	WF0BM2	0x0000	Wakeup Frame 0 Byte Mask 2 Register [7:0] Wakeup Frame 0 Byte Mask 2 Register [15:8]
0x3A - 0x3B	0x3A 0x3B	WF0BM3	0x0000	Wakeup Frame 0 Byte Mask 3 Register [7:0] Wakeup Frame 0 Byte Mask 3 Register [15:8]
0x3C - 0x3D	0x3C 0x3D	Reserved	Don't care	None
0x3E - 0x3F	0x3E 0x3F			
0x40 - 0x41	0x40 0x41	WF1CRC0	0x0000	Wakeup Frame 1 CRC0 Register [7:0] Wakeup Frame 1 CRC0 Register [15:8]
0x42 - 0x43	0x42 0x43	WF1CRC1	0x0000	Wakeup Frame 1 CRC1 Register [7:0] Wakeup Frame 1 CRC1 Register [15:8]
0x44 - 0x45	0x44 0x45	WF1BM0	0x0000	Wakeup Frame 1 Byte Mask 0 Register [7:0] Wakeup Frame 1 Byte Mask 0 Register [15:8]
0x46 - 0x47	0x46 0x47	WF1BM1	0x0000	Wakeup Frame 1 Byte Mask 1 Register [7:0] Wakeup Frame 1 Byte Mask 1 Register [15:8]
0x48 - 0x49	0x48 0x49	WF1BM2	0x0000	Wakeup Frame 1 Byte Mask 2 Register [7:0] Wakeup Frame 1 Byte Mask 2 Register [15:8]
0x4A - 0x4B	0x4A 0x4B	WF1BM3	0x0000	Wakeup Frame 1 Byte Mask 3 Register [7:0] Wakeup Frame 1 Byte Mask 3 Register [15:8]
0x4C - 0x4D	0x4C 0x4D	Reserved	Don't care	None
0x4E - 0x4F	0x4E 0x4F			
0x50 - 0x51	0x50 0x51	WF2CRC0	0x0000	Wakeup Frame 2 CRC0 Register [7:0] Wakeup Frame 2 CRC0 Register [15:8]
0x52 - 0x53	0x52 0x53	WF2CRC1	0x0000	Wakeup Frame 2 CRC1 Register [7:0] Wakeup Frame 2 CRC1 Register [15:8]
0x54 - 0x55	0x54 0x55	WF2BM0	0x0000	Wakeup Frame 2 Byte Mask 0 Register [7:0] Wakeup Frame 2 Byte Mask 0 Register [15:8]
0x56 - 0x57	0x56 0x57	WF2BM1	0x0000	Wakeup Frame 2 Byte Mask 1 Register [7:0] Wakeup Frame 2 Byte Mask 1 Register [15:8]
0x58 - 0x59	0x58 0x59	WF2BM2	0x0000	Wakeup Frame 2 Byte Mask 2 Register [7:0] Wakeup Frame 2 Byte Mask 2 Register [15:8]

Internal I/O Registers Space Mapping (Continued)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x5A - 0x5B	0x5A 0x5B	WF2BM3	0x0000	Wakeup Frame 2 Byte Mask 3 Register [7:0] Wakeup Frame 2 Byte Mask 3 Register [15:8]
0x5C - 0x5D	0x5C 0x5D	Reserved	Don't care	None
0x5E - 0x5F	0x5E 0x5F			
0x60 - 0x61	0x60 0x61	WF3CRC0	0x0000	Wakeup Frame 3 CRC0 Register [7:0] Wakeup Frame 3 CRC0 Register [15:8]
0x62 - 0x63	0x62 0x63	WF3CRC1	0x0000	Wakeup Frame 3 CRC1 Register [7:0] Wakeup Frame 3 CRC1 Register [15:8]
0x64 - 0x65	0x64 0x65	WF3BM0	0x0000	Wakeup Frame 3 Byte Mask 0 Register [7:0] Wakeup Frame 3 Byte Mask 0 Register [15:8]
0x66 - 0x67	0x66 0x67	WF3BM1	0x0000	Wakeup Frame 3 Byte Mask 1 Register [7:0] Wakeup Frame 3 Byte Mask 1 Register [15:8]
0x68 - 0x69	0x68 0x69	WF3BM2	0x0000	Wakeup Frame 3 Byte Mask 2 Register [7:0] Wakeup Frame 3 Byte Mask 2 Register [15:8]
0x6A - 0x6B	0x6A 0x6B	WF3BM3	0x0000	Wakeup Frame 3 Byte Mask 3 Register [7:0] Wakeup Frame 3 Byte Mask 3 Register [15:8]
0x6C - 0x6D	0x6C 0x6D	Reserved	Don't care	None
0x6E - 0x6F	0x6E 0x6F			
0x70 - 0x71	0x70 0x71	TXCR	0x0000	Transmit Control Register [7:0] Transmit Control Register [15:8]
0x72 - 0x73	0x72 0x73	TXSR	0x0000	Transmit Status Register [7:0] Transmit Status Register [15:8]
0x74 - 0x75	0x74 0x75	RXCR1	0x0800	Receive Control Register 1 [7:0] Receive Control Register 1 [15:8]
0x76 - 0x77	0x76 0x77	RXCR2	0x0004	Receive Control Register 2 [7:0] Receive Control Register 2 [15:8]
0x78 - 0x79	0x78 0x79	TXMIR	0x0000	TXQ Memory Information Register [7:0] TXQ Memory Information Register [15:8]
0x7A - 0x7B	0x7A 0x7B	Reserved	Don't care	None
0x7C - 0x7D	0x7C 0x7D	RXFHSR	0x0000	Receive Frame Header Status Register [7:0] Receive Frame Header Status Register [15:8]
0x7E - 0x7F	0x7E 0x7F	RXFHBCR	0x0000	Receive Frame Header Byte Count Register [7:0] Receive Frame Header Byte Count Register [15:8]
0x80 - 0x81	0x80 0x81	TXQCR	0x0000	TXQ Command Register [7:0] TXQ Command Register [15:8]
0x82 - 0x83	0x82 0x83	RXQCR	0x0000	RXQ Command Register [7:0] RXQ Command Register [15:8]
0x84 - 0x85	0x84 0x85	TXFDPR	0x0000	TX Frame Data Pointer Register [7:0] TX Frame Data Pointer Register [15:8]

Internal I/O Registers Space Mapping (Continued)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x86 - 0x87	0x86 0x87	RXFDPR	0x0000	RX Frame Data Pointer Register [7:0] RX Frame Data Pointer Register [15:8]
0x88 - 0x89	0x88 0x89	Reserved	Don't care	None
0x8A - 0x8B	0x8A 0x8B			
0x8C - 0x8D	0x8C 0x8D	RXDTTR	0x0000	RX Duration Timer Threshold Register [7:0] RX Duration Timer Threshold Register [15:8]
0x8E - 0x8F	0x8E 0x8F	RXDBCTR	0x0000	RX Data Byte Count Threshold Register [7:0] RX Data Byte Count Threshold Register [15:8]
0x90 - 0x91	0x90 0x91	IER	0x0000	Interrupt Enable Register [7:0] Interrupt Enable Register [15:8]
0x92 - 0x93	0x92 0x93	ISR	0x0300	Interrupt Status Register [7:0] Interrupt Status Register [15:8]
0x94 - 0x95	0x94 0x95	Reserved	Don't care	None
0x96 - 0x97	0x96 0x97			
0x98 - 0x99	0x98 0x99	Reserved	Don't care	None
0x9A - 0x9B	0x9A 0x9B			
0x9C - 0x9D	0x9C 0x9D	RXFCTR	0x0000	RX Frame Count & Threshold Register [7:0] RX Frame Count & Threshold Register [15:8]
0x9E - 0x9F	0x9E 0x9F	TXNTFSR	0x0000	TX Next Total Frames Size Register [7:0] TX Next Total Frames Size Register [15:8]
0xA0 - 0xA1	0xA0 0xA1	MAHTR0	0x0000	MAC Address Hash Table Register 0 [7:0] MAC Address Hash Table Register 0 [15:8]
0xA2 - 0xA3	0xA2 0xA3	MAHTR1	0x0000	MAC Address Hash Table Register 1 [7:0] MAC Address Hash Table Register 1 [15:8]
0xA4 - 0xA5	0xA4 0xA5	MAHTR2	0x0000	MAC Address Hash Table Register 2 [7:0] MAC Address Hash Table Register 2 [15:8]
0xA6 - 0xA7	0xA6 0xA7	MAHTR3	0x0000	MAC Address Hash Table Register 3 [7:0] MAC Address Hash Table Register 3 [15:8]
0xA8 - 0xA9	0xA8 0xA9	Reserved	Don't care	None
0xAA - 0xAB	0xAA 0xAB			
0xAC - 0xAD	0xAC 0xAD	Reserved	Don't care	None
0xAE - 0xAF	0xAE 0xAF			
0xB0 - 0xB1	0xB0 0xB1	FCLWR	0x0500	Flow Control Low Watermark Register [7:0] Flow Control Low Watermark Register [15:8]
0xB2 - 0xB3	0xB2 0xB3	FCHWR	0x0300	Flow Control High Watermark Register [7:0] Flow Control High Watermark Register [15:8]

Internal I/O Registers Space Mapping (Continued)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0xB4 - 0xB5	0xB4 0xB5	FCOWR	0x0040	Flow Control Overrun Watermark Register [7:0] Flow Control Overrun Watermark Register [15:8]
0xB6 - 0xB7	0xB6 0xB7	Reserved	Don't care	None
0xB8 - 0xB9	0xB8 0xB9	Reserved	Don't care	None
0xBA - 0xBB	0xBA 0xBB			
0xBC - 0xBD	0xBC 0xBD	Reserved	Don't care	None
0xBE - 0xBF	0xBE 0xBF			
0xC0 - 0xC1	0xC0 0xC1	CIDER	0x8870	Chip ID and Enable Register [7:0] Chip ID and Enable Register [15:8]
0xC2 - 0xC3	0xC2 0xC3	Reserved	Don't care	None
0xC4 - 0xC5	0xC4 0xC5	Reserved	Don't care	None
0xC6 - 0xC7	0xC6 0xC7	CGCR	0x0835	Chip Global Control Register [7:0] Chip Global Control Register [15:8]
0xC8 - 0xC9	0xC8 0xC9	IACR	0x0000	Indirect Access Control Register [7:0] Indirect Access Control Register [15:8]
0xCA - 0xCB	0xCA 0xCB	Reserved	Don't care	None
0xCC - 0xCD	0xCC 0xCD	Reserved	Don't care	None
0xCE - 0xCF	0xCE 0xCF			
0xD0 - 0xD1	0xD0 0xD1	IADLR	0x0000	Indirect Access Data Low Register [7:0] Indirect Access Data Low Register [15:8]
0xD2 - 0xD3	0xD2 0xD3	IADHR	0x0000	Indirect Access Data High Register [7:0] Indirect Access Data High Register [15:8]
0xD4 - 0xD5	0xD4 0xD5	PMECR	0x0080	Power Management Event Control Register [7:0] Power Management Event Control Register [15:8]
0xD6 - 0xD7	0xD6 0xD7	GSWUTR	0X080C	Go-Sleep & Wake-Up Time Register [7:0] Go-Sleep & Wake-Up Time Register [15:8]
0xD8 - 0xD9	0xD8 0xD9	PHYRR	0x0000	PHY Reset Register [7:0] PHY Reset Register [15:8]
0xDA - 0xDB	0xDA 0xDB	Reserved	Don't care	None
0xDC - 0xDD	0xDC 0xDD	Reserved	Don't care	None
0xDE - 0xDF	0xDE 0xDF			

Internal I/O Registers Space Mapping (Continued)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0xE0 - 0xE1	0xE0 0xE1	Reserved	Don't care	None
0xE2 - 0xE3	0xE2 0xE3			
0xE4 - 0xE5	0xE4 0xE5	P1MBCR	0x3120	PHY 1 MII-Register Basic Control Register [7:0] PHY 1 MII-Register Basic Control Register [15:8]
0xE6 - 0xE7	0xE6 0xE7	P1MBSR	0x7808	PHY 1 MII-Register Basic Status Register [7:0] PHY 1 MII-Register Basic Status Register [15:8]
0xE8 - 0xE9	0xE8 0xE9	PHY1ILR	0x1430	PHY 1 PHY ID Low Register [7:0] PHY 1 PHY ID Low Register [15:8]
0xEA - 0xEB	0xEA 0xEB	PHY1IHR	0x0022	PHY 1 PHY ID High Register [7:0] PHY 1 PHY ID High Register [15:8]
0xEC - 0xED	0xEC 0xED	P1ANAR	0x05E1	PHY 1 Auto-Negotiation Advertisement Register [7:0] PHY 1 Auto-Negotiation Advertisement Register [15:8]
0xEE - 0xEF	0xEE 0xEF	P1ANLPR	0x0001	PHY 1 Auto-Negotiation Link Partner Ability Register [7:0] PHY 1 Auto-Negotiation Link Partner Ability Register [15:8]
0xF0 - 0xF1	0xF0 0xF1	Reserved	Don't care	None
0xF2 - 0xF3	0xF2 0xF3			
0xF4 - 0xF5	0xF4 0xF5	P1SCLMD	0x0000	Port 1 PHY Special Control/Status, LinkMD® [7:0] Port 1 PHY Special Control/Status, LinkMD® [15:8]
0xF6 - 0xF7	0xF6 0xF7	P1CR	0x00FF	Port 1 Control Register [7:0] Port 1 Control Register [15:8]
0xF8 - 0xF9	0xF8 0xF9	P1SR	0x8080	Port 1 Status Register [7:0] Port 1 Status Register [15:8]
0xFA - 0xFB	0xFA 0xFB	Reserved	Don't care	None
0xFC - 0xFD	0xFC 0xFD	Reserved	Don't care	None
0xFE - 0xFF	0xFE 0xFF			

Register Map: MAC, PHY and QMU

Do not write to bit values or to registers defined as Reserved. Manipulating reserved bits or registers causes unpredictable and often fatal results. If the user wants to write to these reserved bits, the user has to read back these reserved bits (RO or RW) first, then "OR" with the read value of the reserved bits and write back to these reserved bits.

Bit Type Definition

RO = Read only.

WO = Write only.

RW = Read/Write.

W1C = Write 1 to Clear (writing an "1" to clear this bit).

0x00 – 0x07: Reserved

Chip Configuration Register (0x08 – 0x09): CCR

This register indicates the chip configuration mode based on strapping and bonding options.

Bit	Default Value	R/W	Description
15-11	-	RO	**Reserved**.
10	-	RO	**Bus Endian mode** The EESK (pin 10) value is latched into this bit druing power-up/reset. 0: Bus in Big Endian mode, 1: Bus in Little Endian mode.
9	-	RO	**EEPROM presence** The EED_IO (pin 9) value is latched into this bit druing power-up/reset. 0: No external EEPROM, 1: Use external EEPROM.
8	0	RO	**Reserved**.
7	-	RO	**8-Bit data bus width** This bit value is loaded from P1LED1 (pin 1) 0: Not in 8-bit bus mode operation, 1: In 8-bit bus mode operation.
6	-	RO	**16-Bit data bus width** This bit value is loaded from P1LED1 (pin 1) 0: Not in 16-bit bus mode operation, 1: In 16-bit bus mode operation.
5	0	RO	**Reserved**.
4	-	RO	**Shared data bus mode for data and address** 0: Data and address bus are seperated. 1: Data and address bus are shared.
3	0	RO	**Reserved**.
2	0	RO	**Reserved**.
1	-	RO	**48-Pin Chip Package** To indicate chip package is 48-pin. 0: No, 1: Yes.
0	0	RO	**Reserved**.

0x0A – 0x0F: Reserved

Host MAC Address Registers: MARL, MARM and MARH

These Host MAC address registers are loaded starting at word location 0x1 of the EEPROM upon hardware reset. The software driver can read or write these registers value, but it will not modify the original Host MAC address value in the EEPROM. These six bytes of Host MAC address in external EEPROM are loaded to these three registers as mapping below:

MARL[15:0] = EEPROM 0x1(MAC Byte 2 and 1)

MARM[15:0] = EEPROM 0x2(MAC Byte 4 and 3)

MARH[15:0] = EEPROM 0x3(MAC Byte 6 and 5)

The Host MAC address is used to define the individual destination address that the KSZ8851-16MLLJ responds to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received from right to left (LSB to MSB). For example, the actual transmitted and received bits are on the order of 10000000 11000100 10100010 11100110 10010001 11010101. These three registers value for Host MAC address 01:23:45:67:89:AB will be held as below:

MARL[15:0] = 0x89AB

MARM[15:0] = 0x4567

MARH[15:0] = 0x0123

Host MAC Address Register Low (0x10 – 0x11): MARL

The following table shows the register bit fields for Low word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARL MAC Address Low** The least significant word of the MAC address.

Host MAC Address Register Middle (0x12 – 0x13): MARM

The following table shows the register bit fields for middle word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARM MAC Address Middle** The middle word of the MAC address.

Host MAC Address Register High (0x14 – 0x15): MARH

The following table shows the register bit fields for high word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARH MAC Address High** The Most significant word of the MAC address.

0x16 – 0x1F: Reserved

On-Chip Bus Control Register (0x20 – 0x21): OBCR

This register controls the on-chip bus clock speed for the KSZ8851-16MLLJ. The default of the on-chip bus clock speed is 125MHz. When the external host CPU is running at a higher clock rate, the on-chip bus should be adjusted for the best performance.

Bit	Default Value	R/W	Description
15-7	-	RW	**Reserved**.
6	0	RW	**Output Pin Drive Strength** Bi-directional or output pad drive strength selection. 0: 8 mA; 1: 16 mA
5-3	-	RW	**Reserved**.
2	0	RW	**On-Chip Bus Clock Selection** 0: 125MHz (default setting is divided by 1, Bit[1:0]=00) 1: NA (reserved)
1-0	0x0	RW	**On-Chip Bus Clock Divider Selection** 00: Divided by 1; 01: Divided by 2; 10: Divided by 3; 11: NA (reserved). For example to contol the bus clock speed as below: If Bit 2 = 0 and this value is set 00 to select 125 MHz. If Bit 2 = 0 and this value is set 01 to select 62.5 MHz.

EEPROM Control Register (0x22 – 0x23): EEPCR

To support an external EEPROM, pulled-up the EED_IO pin to High; otherwise, it is pulled-down to Low. If an external EEPROM is not used, the software programs the host MAC address. If an EEPROM is used in the design, the chip host MAC address is loaded from the EEPROM immediately after reset. The KSZ8851-16MLLJ allows the software to access (read and write) the EEPROM directly; that is, the EEPROM access timing can be fully controlled by the software if the EEPROM Software Access bit is set.

Bit	Default Value	R/W	Description
15-6	-	RO	**Reserved**.
5	0	WO	**EESRWA EEPROM Software Read or Write Access** 0: software read enable to access EEPROM when software access enabled (bit4=1) 1: software write enable to access EEPROM when software access enabled (bit4=1).
4	0	RW	**EESA EEPROM Software Access** 1: enable software to access EEPROM through bit 3 to bit 0. 0: disable software to access EEPROM.
3	-	RO	**EESB EEPROM Status Bit** Data Receive from EEPROM. This bit directly reads the EED_IO pin.
2-0	0x0	RW	**EECB EEPROM Control Bits** Bit 2: Data Transmit to EEPROM. This bit directly controls the device's EED_IO pin. Bit 1: Serial Clock. This bit directly controls the device's EESK pin. Bit 0: Chip Select for EEPROM. This bit directly controls the device's EECS pin.

Memory BIST Info Register (0x24 – 0x25): MBIR

This register indicates the build-in self test result for both TX and RX memories after power-up/reset.

Bit	Default Value	R/W	Description
15-13	0x0	RO	**Reserved**.
12	-	RO	**TXMBF TX Memory BIST Test Finish** When set, it indicates the Memory Built In Self Test completion for the TX Memory.
11	-	RO	**TXMBFA TX Memory BIST Test Fail** When set, it indicates the TX Memory Built In Self Test has failed.
10-8	-	RO	**TXMBFC TX Memory BIST Test Fail Count** To indicate the TX Memory Built In Self Test failed count
7-5	-	RO	**Reserved**.
4	-	RO	**RXMBF RX Memory Bist Finish** When set, it indicates the Memory Built In Self Test completion for the RX Memory.
3	-	RO	**RXMBFA RX Memory Bist Fail** When set, it indicates the RX Memory Built In Self Test has failed.
2-0	-	RO	**RXMBFC RX Memory BIST Test Fail Count** To indicate the RX Memory Built In Self Test failed count.

Global Reset Register (0x26 – 0x27): GRR

This register controls the global and QMU reset functions with information programmed by the CPU.

Bit	Default Value	R/W	Description
15-2	0x0000	RO	**Reserved**.
1	0	RW	**QMU Module Soft Reset** 1: Software reset is active to clear both TXQ and RXQ memories. 0: Software reset is inactive. QMU software reset will flush out all TX/RX packet data inside the TXQ and RXQ memories and reset all QMU registers to default value.
0	0	RW	**Global Soft Reset** 1: Software reset is active. 0: Software reset is inactive. Global software reset will affect PHY, MAC, QMU, DMA, and the switch core, all registers value are set to default value.

0x28 – 0x29: Reserved

Wakeup Frame Control Register (0x2A – 0x2B): WFCR

This register holds control information programmed by the CPU to control the wake up frame function.

Bit	Default Value	R/W	Description
15-8	0x00	RO	**Reserved**.
7	0	RW	**MPRXE** Magic Packet RX Enable When set, it enables the magic packet pattern detection. When reset, the magic packet pattern detection is disabled.
6-4	0x0	RO	**Reserved**.
3	0	RW	**WF3E** Wake up Frame 3 Enable When set, it enables the Wake up frame 3 pattern detection. When reset, the Wake up frame 3 pattern detection is disabled.
2	0	RW	**WF2E** Wake up Frame 2 Enable When set, it enables the Wake up frame 2 pattern detection. When reset, the Wake up frame 2 pattern detection is disabled.
1	0	RW	**WF1E** Wake up Frame 1 Enable When set, it enables the Wake up frame 1 pattern detection. When reset, the Wake up frame 1 pattern detection is disabled.
0	0	RW	**WF0E** Wake up Frame 0 Enable When set, it enables the Wake up frame 0 pattern detection. When reset, the Wake up frame 0 pattern detection is disabled.

0x2C – 0x2F: Reserved

Wakeup Frame 0 CRC0 Register (0x30 – 0x31): WF0CRC0

This register contains the expected CRC values of the Wake up frame 0 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0CRC0** Wake up Frame 0 CRC (lower 16 bits) The expected CRC value of a Wake up frame 0 pattern.

Wakeup Frame 0 CRC1 Register (0x32 – 0x33): WF0CRC1

This register contains the expected CRC values of the Wake up frame 0 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0CRC1** Wake up Frame 0 CRC (upper 16 bits). The expected CRC value of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 0 Register (0x34 – 0x35): WF0BM0

This register contains the first 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the first byte of the Wake up frame 0, setting bit 15 selects the 16th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0BM0** Wake up Frame 0 Byte Mask 0 The first 16 bytes mask of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 1 Register (0x36 – 0x37): WF0BM1

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 0. Setting bit 15 selects the 32nd byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0BM1** Wake up Frame 0 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 2 Register (0x38 – 0x39): WF0BM2

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 0. Setting bit 15 selects the 48th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0BM2** Wake-up Frame 0 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 0 pattern.

Wakeup Frame 0 Byte Mask 3 Register (0x3A – 0x3B): WF0BM3

This register contains the last 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 0. Setting bit 15 selects the 64th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0BM3** Wake-up Frame 0 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 0 pattern.

0x3C – 0x3F: Reserved

Wakeup Frame 1 CRC0 Register (0x40 – 0x41): WF1CRC0

This register contains the expected CRC values of the Wake up frame 1 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1CRC0** Wake-up frame 1 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Wakeup Frame 1 CRC1 Register (0x42 – 0x43): WF1CRC1

This register contains the expected CRC values of the Wake up frame 1 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1CRC1** Wake-up frame 1 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 0 Register (0x44 – 0x45): WF1BM0

This register contains the first 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the first byte of the Wake up frame 1, setting bit 15 selects the 16th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1BM0** Wake-up frame 1 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 1 Register (0x46 – 0x47): WF1BM1

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 1. Setting bit 15 selects the 32nd byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1BM1** Wake-up frame 1 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 2 Register (0x48 – 0x49): WF1BM2

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 1. Setting bit 15 selects the 48th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1BM2** Wake-up frame 1 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 3 Register (0x4A – 0x4B): WF1BM3

This register contains the last 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 1. Setting bit 15 selects the 64th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF1BM3** Wake-up frame 1 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 1 pattern.

0x4C – 0x4F: Reserved

Wakeup Frame 2 CRC0 Register (0x50 – 0x51): WF2CRC0

This register contains the expected CRC values of the Wake up frame 2 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF2CRC0** Wake-up frame 2 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Wakeup Frame 2 CRC1 Register (0x52 – 0x53): WF2CRC1

This register contains the expected CRC values of the wake-up frame 2 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF2CRC1** Wake-up frame 2 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 0 Register (0x54 – 0x55): WF2BM0

This register contains the first 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the first byte of the Wake up frame 2, setting bit 15 selects the 16th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF2BM0** Wake-up frame 2 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 1 Register (0x56 – 0x57): WF2BM1

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 2. Setting bit 15 selects the 32nd byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF2BM1** Wake-up frame 2 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 2 Register (0x58 – 0x59): WF2BM2

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 2. Setting bit 15 selects the 48th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM2** Wake-up frame 2 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 3 Register (0x5A – 0x5B): WF2BM3

This register contains the last 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 2. Setting bit 15 selects the 64th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM3** Wake-up frame 2 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 2 pattern.

0x5C – 0x5F: Reserved

Wakeup Frame 3 CRC0 Register (0x60 – 0x61): WF3CRC0

This register contains the expected CRC values of the Wake up frame 3 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake-up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3CRC0** Wake-up frame 3 CRC (lower 16 bits). The expected CRC value of a Wake up frame 3 pattern.

Wakeup Frame 3 CRC1 Register (0x62 – 0x63): WF3CRC1

This register contains the expected CRC values of the Wake up frame 3 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake-up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3CRC1** Wake-up frame 3 CRC (upper 16 bits). The expected CRC value of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 0 Register (0x64 – 0x65): WF3BM0

This register contains the first 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the first byte of the Wake up frame 3, setting bit 15 selects the 16th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM0** Wake up Frame 3 Byte Mask 0. The first 16 byte mask of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 1 Register (0x66 – 0x67): WF3BM1

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 3. Setting bit 15 selects the 32nd byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM1** Wake up Frame 3 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 2 Register (0x68 – 0x69): WF3BM2

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 3. Setting bit 15 selects the 48th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM2** Wake up Frame 3 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 3 Register (0x6A – 0x6B): WF3BM3

This register contains the last 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 3. Setting bit 15 selects the 64th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM3** Wake up Frame 3 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake up frame 3 pattern.

0x6C – 0x6F: Reserved

Transmit Control Register (0x70 – 0x71): TXCR

This register holds control information programmed by the CPU to control the QMU transmit module function.

Bit	Default Value	R/W	Description
15-9	-	RO	**Reserved**.
8	0x0	RW	**TCGICMP Transmit Checksum Generation for ICMP** When this bit is set, The KSZ8851-16MLLJ is enabled to transmit ICMP frame (only for non-fragment frame) checksum generation.
7	0x0	RO	**Reserved**.
6	0x0	RW	**TCGTCP Transmit Checksum Generation for TCP** When this bit is set, The KSZ8851-16MLLJ is enabled to transmit TCP frame checksum generation.
5	0x0	RW	**TCGIP Transmit Checksum Generation for IP** When this bit is set, The KSZ8851-16MLLJ is enabled to transmit IP header checksum generation.
4	0x0	RW	**FTXQ Flush Transmit Queue** When this bit is set, The transmit queue memory is cleared and TX frame pointer is reset. Note: Disable the TXE transmit enable bit[0] first before set this bit, then clear this bit to normal operation.
3	0x0	RW	**TXFCE Transmit Flow Control Enable** When this bit is set and the KSZ8851-16MLLJ is in full-duplex mode, flow control is enabled. The KSZ8851-16MLLJ transmits a PAUSE frame when the Receive Buffer capacity reaches a threshold level that will cause the buffer to overflow. When this bit is set and the KSZ8851-16MLLJ is in half-duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
2	0x0	RW	**TXPE Transmit Padding Enable** When this bit is set, the KSZ8851-16MLLJ automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit requires enabling the add CRC feature (bit1=1) to avoid CRC errors for the transmit packet.
1	0x0	RW	**TXCE Transmit CRC Enable** When this bit is set, the KSZ8851-16MLLJ automatically adds a 32-bit CRC checksum field to the end of a transmit frame.
0	0x0	RW	**TXE Transmit Enable** When this bit is set, the transmit module is enabled and placed in a running state. When reset, the transmit process is placed in the stopped state after the transmission of the current frame is completed.

Transmit Status Register (0x72 – 0x73): TXSR

This register keeps the status of the last transmitted frame.

Bit	Default Value	R/W	Description
15-14	0x0	RO	**Reserved**.
13	0x0	RO	**TXLC Transmit Late Collision** This bit is set when a transmit Late Collision occurs.
12	0x0	RO	**TXMC Transmit Maximum Collision** This bit is set when a transmit Maximum Collision is reached.
11-6	-	RO	**Reserved**.
5-0	-	RO	**TXFID Transmit Frame ID** This field identifies the transmitted frame. All of the transmit status information in this register belongs to the frame with this ID.

Receive Control Register 1 (0x74 – 0x75): RXCR1

This register holds control information programmed by the CPU to control the receive function.

Bit	Default Value	R/W	Description
15	0x0	RW	**FRXQ Flush Receive Queue** When this bit is set, The receive queue memory is cleared and RX frame pointer is reset. Note: Disable the RXE receive enable bit[0] first before set this bit, then clear this bit to normal operation.
14	0x0	RW	**RXUDPFCC Receive UDP Frame Checksum Check Enable** When this bit is set, the KSZ8851 will check for correct UDP checksum for incoming UDP frames. Any received UDP frames with incorrect checksum will be discarded.
13	0x0	RW	**RXTCPFCC Receive TCP Frame Checksum Check Enable** When this bit is set, the KSZ8851 will check for correct TCP checksum for incoming TCP frames. Any received TCP frames with incorrect checksum will be discarded.
12	0x0	RW	**RXIPFCC Receive IP Frame Checksum Check Enable** When this bit is set, the KSZ8851 will check for correct IP header checksum for incoming IP frames. Any received IP frames with incorrect checksum will be discarded.
11	0x1	RW	**RXPAFMA Receive Physical Address Filtering with MAC Address Enable** When this bit is set, this bit enables the RX function to receive physical address that pass the MAC address filtering mechanism (see Address Filtering Scheme in Table 3 for detail).
10	0x0	RW	**RXFCE Receive Flow Control Enable** When this bit is set and the KSZ8851-16MLLJ is in full-duplex mode, flow control is enabled, and the KSZ8851-16MLLJ will acknowledge a PAUSE frame from the receive interface; i.e., the outgoing packets are pending in the transmit buffer until the PAUSE frame control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, flow control is not enabled.
9	0x0	RW	**RXEFE Receive Error Frame Enable** When this bit is set, CRC error frames are allowed to be received into the RX queue. When this bit is cleared, all CRC error frames are discarded.
8	0x0	RW	**RXMAFMA Receive Multicast Address Filtering with MAC Address Enable** When this bit is set, this bit enables the RX function to receive multicast address that pass the MAC address filtering mechanism (see Address Filtering Scheme in Table 3 for detail).

Receive Control Register 1 (0x74 – 0x75): RXCR1 (Continued)

Bit	Default Value	R/W	Description
7	0x0	RW	**RXBE Receive Broadcast Enable** When this bit is set, the RX module receives all the broadcast frames.
6	0x0	RW	**RXME Receive Multicast Enable** When this bit is set, the RX module receives all the multicast frames (including broadcast frames).
5	0x0	RW	**RXUE Receive Unicast Enable** When this bit is set, the RX module receives unicast frames that match the 48-bit Station MAC address of the module.
4	0x0	RW	**RXAE Receive All Enable** When this bit is set, the KSZ8851-16MLLJ receives all incoming frames, regardless of the frame's destination address (see Address Filtering Scheme in Table 3 for detail).
3	0x0	RW	**Reserved**
2	0x0	RW	**Reserved**
1	0x0	RW	**RXINVF Receive Inverse Filtering** When this bit is set, the KSZ8851-16MLLJ receives function with address check operation in inverse filtering mode (see Address Filtering Scheme in Table 3 for detail).
0	0x0	RW	**RXE Receive Enable** When this bit is set, the RX block is enabled and placed in a running state. When this bit is cleared, the receive process is placed in the stopped state upon completing reception of the current frame.

Receive Control Register 2 (0x76 – 0x77): RXCR2

This register holds control information programmed by the CPU to control the receive function.

Bit	Default Value	R/W	Description
15-5	-	RO	**Reserved**.
4	0x0	RW	**IUFFP IPV4/IPV6/UDP Fragment Frame Pass** When this bit is set, the KSZ8851-16MLLJ will pass the checksum check at receive side for IPv4/IPv6 UDP frame with fragment extension header. When this bit is cleared, the KSZ8851-16MLLJ will perform checksum operation based on configuration and doesn't care whether it's a fragment frame or not.
3	0x0	RW	**RXIUFCEZ Receive IPV4/IPV6/UDP Frame Checksum Equal Zero** When this bit is set, the KSZ8851-16MLLJ will pass the filtering for IPv4/IPv6 UDP frame with UDP checksum equal to zero. When this bit is cleared, the KSZ8851-16MLLJ will drop IPv4/IPv6 UDP packet with UDP checksum equal to zero.
2	0x1	RW	**UDPLFE UDP Lite Frame Enable** When this bit is set, the KSZ8851-16MLLJ will check the checksum at receive side and generate the checksum at transmit side for UDP Lite frame. When this bit is cleared, the KSZ8851-16MLLJ will pass the checksum check at receive side and skip the checksum generation at transmit side for UDP Lite frame.
1	0x0	RW	**RXICMPFCC Receive ICMP Frame Checksum Check Enable** When this bit is set, the KSZ8851 will check for correct ICMP checksum for incoming ICMP frames (only for non-fragment frame). Any received ICMP frames with incorrect checksum will be discarded.
0	0x0	RW	**RXSAF Receive Source Address Filtering** When this bit is set, the KSZ8851-16MLLJ will drop the frame if the source address is same as MAC address in MARL, MARM, MARH registers.

TXQ Memory Information Register (0x78 – 0x79): TXMIR

This register indicates the amount of free memory available in the TXQ of the QMU module.

Bit	Default Value	R/W	Description
15-13	-	RO	**Reserved**.
12-0	-	RO	**TXMA Transmit Memory Available** The amount of memory available is represented in units of byte. The TXQ memory is used for both frame payload, control word. Note: Software must be written to ensure that there is enough memory for the next transmit frame including control information before transmit data is written to the TXQ.

0x7A – 0x7B: Reserved

Receive Frame Header Status Register (0x7C – 0x7D): RXFHSR

This register indicates the received frame header status information, the received frames are reported in RXFCTR register. This register contains the status information for the frame received and the CPU can read so many times same as the frame count value in the RXFCTR.

Bit	Default Value	R/W	Description
15	-	RO	**RXFV Receive Frame Valid** When this bit is set, it indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When clear, it indicates that there is either no pending receive frame or that the current frame is still in the process of receiving.
14	-	RO	**Reserved**
13	-	RO	**RXICMPFCS Receive ICMP Frame Checksum Status** When this bit is set, the KSZ8851 received ICMP frame checksum field is incorrect.
12	-	RO	**RXIPFCS Receive IP Frame Checksum Status** When this bit is set, the KSZ8851 received IP header checksum field is incorrect.
11	-	RO	**RXTCPFCS Receive TCP Frame Checksum Status** When this bit is set, the KSZ8851 received TCP frame checksum field is incorrect.
10	-	RO	**RXUDPFCS Receive UDP Frame Checksum Status** When this bit is set, the KSZ8851 received UDP frame checksum field is incorrect.
9-8	-	RO	**Reserved**
7	-	RO	**RXBF Receive Broadcast Frame** When this bit is set, it indicates that this frame has a broadcast address.
6	-	RO	**RXMF Receive Multicast Frame** When this bit is set, it indicates that this frame has a multicast address (including the broadcast address).
5	-	RO	**RXUF Receive Unicast Frame** When this bit is set, it indicates that this frame has a unicast address.
4	-	RO	**RXMR Receive MII Error** When set, it indicates that there is an MII symbol error on the received frame.
3	-	RO	**RXFT Receive Frame Type** When this bit is set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.

Receive Frame Header Status Register (0x7C – 0x7D): RXFHSR (Continued)

2	-	RO	**RXFTL Receive Frame Too Long** When this bit is set, it indicates that the frame length exceeds the maximum size of 2000 bytes. Frames that are too long are passed to the host only if the pass bad frame bit is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
1	-	RO	**RXRF Receive Runt Frame** When this bit is set, it indicates that a frame was damaged by a collision or had a premature termination before the collision window passed. Runt frames are passed to the host only if the pass bad frame bit is set.
0	-	RO	**RXCE Receive CRC Error** When this bit is set, it indicates that a CRC error has occurred on the current received frame. CRC error frames are passed to the host only if the pass bad frame bit is set.

Receive Frame Header Byte Count Register (0x7E – 0x7F): RXFHBCR

This register indicates the received frame header byte count information, the received frames are reported in RXFCTR register. This register contains the total number of bytes information for the frame received and the CPU can read so many times same as the frame count value in the RXFCTR.

Bit	Default Value	R/W	Description
15-12	-	RO	**Reserved**.
11-0	-	RO	**RXBC Receive Byte Count** This field indicates the present received frame byte size. Note: Always read low byte first for 8-bit mode opearation.

TXQ Command Register (0x80 – 0x81): TXQCR

This register is programmed by the Host CPU to issue a transmit command to the TXQ. The present transmit frame in the TXQ memory is queued for transmit.

Bit	Default Value	R/W	Description
15-3	-	RW	**Reserved**
2	0x0	RW	**AETFE Auto-Enqueue TXQ Frame Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable current all TX frames prepared in the TX buffer are queued to transmit automatically. The bit 0 METFE has to be set 0 when this bit is set to 1 in this register.
1	0x0	RW	**TXQMAM TXQ Memory Available Monitor** When this bit is written as 1, the KSZ8851-16MLLJ will generate interrupt (bit 6 in ISR register) to CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at TXNTFSR (0x9E) register. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before set to 1 again.
0	0x0	RW	**METFE Manual Enqueue TXQ Frame Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable current TX frame prepared in the TX buffer is queued for transmit, this is only transmit one frame at a time. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.

RXQ Command Register (0x82 – 0x83): RXQCR

This register is programmed by the Host CPU to issue DMA read or write command to the RXQ and TXQ. This register also is used to control all RX thresholds enable and status.

Bit	Default Value	R/W	Description
15-13	-	RW	**Reserved**.
12	-	RO	**RXDTTS RX Duration Timer Threshold Status** When this bit is set, it indicates that RX interrupt is due to the time start at first received frame in RXQ buffer exceeds the threshold set in RX Duration Timer Threshold Register (0x8C, RXDTT). This bit will be updated when write 1 to bit 13 in ISR register.
11	-	RO	**RXDBCTS RX Data Byte Count Threshold Status** When this bit is set, it indicates that RX interrupt is due to the number of received bytes in RXQ buffer exceeds the threshold set in RX Data Byte Count Threshold Register (0x8E, RXDBCT). This bit will be updated when write 1 to bit 13 in ISR register.
10	-	RO	**RXFCTS RX Frame Count Threshold Status** When this bit is set, it indicates that RX interrupt is due to the number of received frames in RXQ buffer exceeds the threshold set in RX Frame Count Threshold Register (0x9C, RXFCT). This bit will be updated when write 1 to bit 13 in ISR register.
9	0x0	RW	**RXIPHTOE RX IP Header Two-Byte Offset Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable to add two bytes before frame header in order for IP header inside the frame contents to be aligned with double word boundary to speed up software operation.
8	-	RW	**Reserved**.
7	0x0	RW	**RXDTTE RX Duration Timer Threshold Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable RX interrupt (bit 13 in ISR) when the time start at first received frame in RXQ buffer exceeds the threshold set in RX Duration Timer Threshold Register (0x8C, RXDTT).
6	0x0	RW	**RXDBCTE RX Data Byte Count Threshold Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable RX interrupt (bit 13 in ISR) when the number of received bytes in RXQ buffer exceeds the threshold set in RX Data Byte Count Threshold Register (0x8E, RXDBCT).
5	0x0	RW	**RXFCTE RX Frame Count Threshold Enable** When this bit is written as 1, the KSZ8851-16MLLJ will enable RX interrupt (bit 13 in ISR) when the number of received frames in RXQ buffer exceeds the threshold set in RX Frame Count Threshold Register (0x9C, RXFCT).
4	0x0	RW	**ADRFE Auto-Dequeue RXQ Frame Enable** When this bit is written as 1, the KSZ8851-16MLLJ will automatically enable RXQ frame buffer dequeue. The read pointer in RXQ frame buffer will be automatically adjusted to next received frame location after current frame is completely read by the host.
3	0x0	WO	**SDA Start DMA Access** When this bit is written as 1, the KSZ8851-16MLLJ allows a DMA operation from the host CPU to access either read RXQ frame buffer or write TXQ frame buffer with CSN and RDN or WRN signals while the CMD pin is low. All registers access are disabled except this register during this DMA operation. This bit must be set to 0 when DMA operation is finished in order to access the rest of registers.

RXQ Command Register (0x82 – 0x83): RXQCR (Continued)

Bit	Default Value	R/W	Description
2-1	-	RW	**Reserved.**
0	0x0	RW	**RRXEF Release RX Error Frame** When this bit is written as 1, the current RX error frame buffer is released. Note: This bit is self-clearing after the frame memory is released. The software should wait for the bit to be cleared before processing new RX frame.

TX Frame Data Pointer Register (0x84 – 0x85): TXFDPR

The value of this register determines the address to be accessed within the TXQ frame buffer. When the AUTO increment is set, It will automatically increment the pointer value on write accesses to the data register.

The counter is incremented by one for every byte access, by two for every word access, and by four for every double word access.

Bit	Default Value	R/W	Description
15	-	RO	**Reserved**.
14	0x0	RW	**TXFPAI TX Frame Data Pointer Auto Increment** When this bit is set, the TX Frame data pointer register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every doubleword access. When this bit is reset, the TX frame data pointer is manually controlled by user to access the TX frame location.
13-11	-	RO	**Reserved**.
10-0	0x000	RO	**TXFP TX Frame Pointer** TX Frame Pointer index to the Frame Data register for access. This field reset to next available TX frame location when the TX Frame Data has been enqueued through the TXQ command register.

RX Frame Data Pointer Register (0x86 – 0x87): RXFDPR

The value of this register determines the address to be accessed within the RXQ frame buffer. When the Auto Increment is set, it will automatically increment the RXQ Pointer on read accesses to the data register.

The counter is incremented is by one for every byte access, by two for every word access, and by four for every double word access.

Bit	Default Value	R/W	Description
15	-	RO	**Reserved**.
14	0x0	RW	**RXFPAI RX Frame Pointer Auto Increment** When this bit is set, the RXQ Address register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every double word access. When this bit is reset, the RX frame data pointer is manually controlled by user to access the RX frame location.
13	-	RO	**Reserved**.
12	0x0	RW	**WST Write Sample Time** This bit is used to select the WRN active to write data valid time as shown in Figure 11. 0: WRN active to write data valid sample time is range of 8nS (min) to 16nS (max). 1: WRN active to write data valid sample time is 4nS (max).
11	0x0	WO (Read back is "0")	**EMS Endian Mode Selection** This bit is used to select either Big or Little Endian mode when Endian mode select strapping pin (10) is NC or tied to GND. 0: is set to Little Endian Mode 1: is set to Big Endian Mode
10-0	0x000	WO	**RXFP RX Frame Pointer** RX Frame data pointer index to the Data register for access. This pointer value must reset to 0x000 before each DMA operation from the host CPU to read RXQ frame buffer.

0x88 – 0x8B: Reserved

RX Duration Timer Threshold Register (0x8C – 0x8D): RXDTTR

This register is used to program the received frame duration timer threshold.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**RXDTT Receive Duration Timer Threshold** To program received frame duration timer threshold value in 1us interval. The maximum value is 0xCFFF. When bit 7 set to 1 in RXQCR register, the KSZ8851-16MLLJ will set RX interrupt (bit 13 in ISR) after the time starts at first received frame in RXQ buffer and exceeds the threshold set in this register.

RX Data Byte Count Threshold Register (0x8E – 0x8F): RXDBCTR

This register is used to program the received data byte count threshold.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**RXDBCT Receive Data Byte Count Threshold** To program received data byte threshold value in byte count. When bit 6 set to 1 in RXQCR register, the KSZ8851-16MLLJ will set RX interrupt (bit 13 in ISR) when the number of received bytes in RXQ buffer exceeds the threshold set in this register.

Interrupt Enable Register (0x90 – 0x91): IER

This register enables the interrupts from the QMU and other sources.

Bit	Default Value	R/W	Description
15	0x0	RW	**LCIE Link Change Interrupt Enable** When this bit is set, the link change interrupt is enabled. When this bit is reset, the link change interrupt is disabled.
14	0x0	RW	**TXIE Transmit Interrupt Enable** When this bit is set, the transmit interrupt is enabled. When this bit is reset, the transmit interrupt is disabled.
13	0x0	RW	**RXIE Receive Interrupt Enable** When this bit is set, the receive interrupt is enabled. When this bit is reset, the receive interrupt is disabled.
12	0x0	RW	**Reserved**
11	0x0	RW	**RXOIE Receive Overrun Interrupt Enable** When this bit is set, the Receive Overrun interrupt is enabled. When this bit is reset, the Receive Overrun interrupt is disabled.
10	0x0	RW	**Reserved**
9	0x0	RW	**TXPSIE Transmit Process Stopped Interrupt Enable** When this bit is set, the Transmit Process Stopped interrupt is enabled. When this bit is reset, the Transmit Process Stopped interrupt is disabled.
8	0x0	RW	**RXPSIE Receive Process Stopped Interrupt Enable** When this bit is set, the Receive Process Stopped interrupt is enabled. When this bit is reset, the Receive Process Stopped interrupt is disabled.
7	0x0	RW	**Reserved**
6	0x0	RW	**TXSAIE Transmit Space Available Interrupt Enable** When this bit is set, the Transmit memory space available interrupt is enabled. When this bit is reset, the Transmit memory space available interrupt is disabled.
5	0x0	RW	**RXWFDIE Receive Wake-up Frame Detect Interrupt Enable** When this bit is set, the Receive wakeup frame detect interrupt is enabled. When this bit is reset, the Receive wakeup frame detect interrupt is disabled.
4	0x0	RW	**RXMPDIE Receive Magic Packet Detect Interrupt Enable** When this bit is set, the Receive magic packet detect interrupt is enabled. When this bit is reset, the Receive magic packet detect interrupt is disabled.
3	0x0	RW	**LDIE Linkup Detect Interrupt Enable** When this bit is set, the wake-up from linkup detect interrupt is enabled. When this bit is reset, the linkup detect interrupt is disabled.

Interrupt Enable Register (0x90 – 0x91): IER (Continued)

Bit	Default Value	R/W	Description
2	0x0	RW	**EDIE Energy Detect Interrupt Enable** When this bit is set, the wake-up from energy detect interrupt is enabled. When this bit is reset, the energy detect interrupt is disabled.
1	0x0	RO	**Reserved**.
0	0x0	RW	**DEDIE Delay Energy Detect Interrupt Enable** When this bit is set, the delay energy detect interrupt is enabled. When this bit is reset, the delay energy detect interrupt is disabled. Note: the delay energy detect interrupt till device is ready for host access.

Interrupt Status Register (0x92 – 0x93): ISR

This register contains the status bits for all QMU and other interrupt sources.

When the corresponding enable bit is set, it causes the interrupt pin to be asserted.

This register is usually read by the host CPU and device drivers during interrupt service routine or polling. The register bits are not cleared when read. The user has to write “1” to clear.

Bit	Default Value	R/W	Description
15	0x0	RO (W1C)	**LCIS Link Change Interrupt Status** When this bit is set, it indicates that the link status has changed from link up to link down, or link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
14	0x0	RO (W1C)	**TXIS Transmit Interrupt Status** When this bit is set, it indicates that the TXQ MAC has transmitted at least a frame on the MAC interface and the QMU TXQ is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
13	0x0	RO (W1C)	**RXIS Receive Interrupt Status** When this bit is set, it indicates that the QMU RXQ has received at least a frame from the MAC interface and the frame is ready for the host CPU to process. This edge-triggered interrupt status is cleared by writing 1 to this bit.
12	0x0	RO	**Reserved**
11	0x0	RO (W1C)	**RXOIS Receive Overrun Interrupt Status** When this bit is set, it indicates that the Receive Overrun status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
10	0x0	RO	**Reserved**
9	0x1	RO (W1C)	**TXPSIS Transmit Process Stopped Interrupt Status** When this bit is set, it indicates that the Transmit Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
8	0x1	RO (W1C)	**RXPSIS Receive Process Stopped Interrupt Status** When this bit is set, it indicates that the Receive Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
7	0x0	RO	**Reserved**
6	0x0	RO (W1C)	**TXSAIS Transmit Space Available Interrupt Status** When this bit is set, it indicates that Transmit memory space available status has occurred. When this bit is reset, the Transmit memory space available interrupt is disabled.

Interrupt Status Register (0x92 – 0x93): ISR (Continued)

Bit	Default Value	R/W	Description
5	0x0	RO	**RXWFDIS Receive Wakeup Frame Detect Interrupt Status** When this bit is set, it indicates that Receive wakeup frame detect status has occurred. Write “1000” to PMECR[5:2] to clear this bit
4	0x0	RO	**RXMPDIS Receive Magic Packet Detect Interrupt Status** When this bit is set, it indicates that Receive magic packet detect status has occurred. Write “0100” to PMECR[5:2] to clear this bit.
3	0x0	RO	**LDIS Linkup Detect Interrupt Status** When this bit is set, it indicates that wake-up from linkup detect status has occurred. Write “0010” to PMECR[5:2] to clear this bit.
2	0x0	RO	**EDIS Energy Detect Interrupt Status** When this bit is set and bit 2=1, bit 0=0 in IER register, it indicates that wake-up from energy detect status has occurred. When this bit is set and bit 2, 0=1 in IER register, it indicates that wake-up from delay energy detect status has occurred. Write “0001” to PMECR[5:2] to clear this bit.
1	0x0	RO	**Reserved**.
0	0x0	RO	**Reserved**

0x94 – 0x9B: Reserved

RX Frame Count & Threshold Register (0x9C – 0x9D): RXFCTR

This register indicates the current total amount of received frame count in RXQ frame buffer and also is used to program the received frame count threshold.

Bit	Default Value	R/W	Description
15-8	0x00	RO	**RXFC RX Frame Count** To indicate the total received frames in RXQ frame buffer when receive interrupt (bit13=1 in ISR) occurred and write “1” to clear this bit 13 in ISR. The host CPU can start to read the updated receive frame header information in RXFHSR/RXFHBCR registers after read this RX frame count register.
7-0	0x00	RW	**RXFCT Receive Frame Count Threshold** To program received frame count threshold value. When bit 5 set to 1 in RXQCR register, the KSZ8851-16MLLJ will set RX interrupt (bit 13 in ISR) when the number of received frames in RXQ buffer exceeds the threshold set in this register.

TX Next Total Frames Size Register (0x9E – 0x9F): TXNTFSR

This register is used by the host CPU to program the total amount of TXQ buffer space requested for the next transmit.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**TXNTFS TX Next Total Frames Size** The host CPU is used to program the total amount of TXQ buffer space which is required for next total transmit frames size in double-word count. When bit 1 (TXQ memory available monitor) is set to 1 in TXQCR register, the KSZ8851-16MLLJ will generate interrupt (bit 6 in ISR register) to CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at this register.

MAC Address Hash Table Register 0 (0xA0 – 0xA1): MAHTR0

The 64-bit MAC address table is used for group address filtering and it is enabled by selecting item 5 “Hash perfect” mode in Table 3 (Address Filtering Scheme). This value is defined as the six most significant bits from CRC circuit calculation result that is based on 48-bit of DA input. The two most significant bits select one of the four registers to be used, while the others determine which bit within the register.

Multicast table register 0.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**HT0 Hash Table 0** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop.

MAC Address Hash Table Register 1 (0xA2 – 0xA3): MAHTR1

Multicast table register 1.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**HT1 Hash Table 1** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXAE) or receive multicast (RXME) bit is set in the RXCR1, all multicast addresses are received regardless of the multicast table value.

MAC Address Hash Table Register 2 (0xA4 – 0xA5): MAHTR2

Multicast table register 2.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**HT2 Hash Table 2** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXAE) or receive multicast (RXME) bit is set in the RXCR1, all multicast addresses are received regardless of the multicast table value.

MAC Address Hash Table Register 3 (0xA6 – 0xA7): MAHTR3

Multicast table register 3.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**HT3 Hash Table 3** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXAE) or receive multicast (RXME) bit is set in the RXCR1, all multicast addresses are received regardless of the multicast table value.

0xA8 – 0xAF: Reserved

Flow Control Low Watermark Register (0xB0 – 0xB1): FCLWR

This register is used to control the flow control for low watermark in QMU RX queue.

Bit	Default Value	R/W	Description
15-12	-	RW	**Reserved**
11-0	0x0500	RW	FCLWC Flow Control Low Watermark Configuration These bits are used to define the QMU RX queue low watermark configuration. It is in double words count and default is 5.12 KByte available buffer space out of 12 KByte.

Flow Control High Watermark Register (0xB2 – 0xB3): FCHWR

This register is used to control the flow control for high watermark in QMU RX queue.

Bit	Default Value	R/W	Description
15-12	-	RW	**Reserved**
11-0	0x0300	RW	FCHWC Flow Control High Watermark Configuration These bits are used to define the QMU RX queue high watermark configuration. It is in double words count and default is 3.072 K Byte available buffer space out of 12 KByte.

Flow Control Overrun Watermark Register (0xB4 – 0xB5): FCOWR

This register is used to control the flow control for overrun watermark in QMU RX queue

Bit	Default Value	R/W	Description
15-12	-	RW	**Reserved**
11-0	0x0040	RW	FCLWC Flow Control Overrun Watermark Configuration These bits are used to define the QMU RX queue overrun watermark configuration. It is in double words count and default is 256 Bytes available buffer space out of 12 Kbyte.

0xB6 – 0xBF: Reserved

Chip ID and Enable Register (0xC0 – 0xC1): CIDER

This register contains the chip ID and the chip enable bit.

Bit	Default	R/W	Description
15-8	0x88	RO	**Family ID** Chip family ID
7-4	0x7	RO	**Chip ID** 0x7 is assigned to KSZ8851-16MLLJ
3-1	0x1	RO	**Revision ID**
0	0x0	RW	**Reserved**

0xC2 – 0xC5: Reserved

Chip Global Control Register (0xC6 – 0xC7): CGCR

This register contains the global control for the chip function.

Bit	Default	R/W	Description
15-12	0x0	RW	**Reserved.**
11-10	0x2	RW	**Reserved.**
9	0x0	RW	**LEDSEL0** This bit sets the LEDSEL0 selection for P1LED1 and P1LED0. PHY port LED indicators, defined as below: LEDSEL0 (bit9): 0 / 1 P1LED1: 100BT / ACT P1LED0: LINK/ACT / LINK
8	0x0	R/W	**Reserved.**
7-0	0x35	RW	**Reserved.**

Indirect Access Control Register (0xC8 – 0xC9): IACR

This register contains the indirect control for the MIB counter (Write IACR triggers a command. Read access is determined by bit 12).

Bit	Default	R/W	Description
15-13	0x0	RW	**Reserved**.
12	0x0	RW	**Read Enable.** 1 = Read cycle is enabled (MIB counter will clear after read). 0 = No operation.
11-10	0x0	RW	**Table Select** 00 = reserved. 01 = reserved. 10 = reserved. 11 = MIB counter selected.
9-5	-	RW	**Reserved.**
4-0	0x00	RW	**Indirect Address** Bit 4-0 of indirect address for 32 MIB counter locations.

0xCA – 0xCF: Reserved

Indirect Access Data Low Register (0xD0 – 0xD1): IADLR

This register contains the indirect data (low word) for MIB counter.

Bit	Default	R/W	Description
15-0	0x0000	RW	**Indirect Low Word Data** Bit 15-0 of indirect data.

Indirect Access Data High Register (0xD2 – 0xD3): IADHR

This register contains the indirect data (high word) for MIB counter.

Bit	Default	R/W	Description
15-0	0x0000	RW	**Indirect High Word Data** Bit 31-16 of indirect data.

Power Management Event Control Register (0xD4 – 0xD5): PMECR

This register is used to control the KSZ8851-16MLLJ power management event, capabilities and status.

Bit	Default Value	R/W	Description
15	-	RO	**Reserved**.
14	0	RW	**PME Delay Enable** This bit is used to enable the delay of PME output pin assertion. When this bit is set to 1, the device will not assert the PME output till the device's all clocks are running and ready for host access. When this bit is set to 0, the device will assert the PME output without delay. This bit is only valid when Auto Wake-Up Enable (bit7) is set to 1 in this register.
13	0	RW	**Reserved**
12	0	RW	**PME Output Polarity** This bit is used to control the PME output pin polarity. When this bit is set to 1, the PME output pin is active high. When this bit is set to 0, the PME output pin is active low.
11-8	0x0	RW	**Wake-on-LAN to PME Output Enable** These four bits are used to enable the PME output pin asserted when one of these wake-on-LAN events is detected: Bit 11: is corresponding to receive wake-up frame. Bit 10: is corresponding to receive magic packet. Bit 9: is corresponding to link change from down to up. Bit 8: is corresponding to signal energy detected. When the bit is set to 1, the PME pin will be asserted when a corresponding wake-on-LAN event is occurred. When this bit is set to 0, the PME pin will be not asserted when a corresponding wake-on-LAN event is occurred.
7	0	RW	**Auto Wake-Up Enable** This bit is used to enable automatically wake-up from low power state to normal power state in energy detect mode if carrier (signal energy) is present more than wake-up time in GSWUTR register. During the normal power state, the device can receive and transmit packets. When this bit is set to 1, the auto wake-up is enabled in energy detect mode. When this bit is set to 0, the auto wake-up is disabled in energy detect mode.
6	0	RW	**Wake-Up to Normal Operation Mode** This bit is used to control the device wake-up from low power state in energy detect mode to normal operation mode if signal energy is detected longer than the programmed wake-up time in GSWUTR register. When this bit is set to 1, the device will automatically go to the normal operation mode from energy detect mode. When this bit is set to 0, the device will not automatically go to the normal mode from energy detect mode. This bit is only valid when Auto Wake-Up Enable (bit7) is set to 1.

Power Management Event Control Register (0xD4 – 0xD5): PMECR (Continued)

Bit	Default Value	R/W	Description
5-2	0x0	RO (W1C)	**Wake-Up Event Indication** These four bits are used to indicate the KSZ8851-16MLLJ wake-up event status as below: 0000: No wake-up event. 0001: Wake-up from energy event detected. (Bit 2 also set to 1 in ISR register) 0010: Wake-up from link up event detected. (Bit 3 also set to 1 in ISR register) 0100: Wake-up from magic packet event detected. 1000: Wake-up from wakeup frame event detected. If Wake-on-LAN to PME Output Enable bit[11:8] are set, the KSZ8851-16MLLJ also asserts the PME pin. These bits are cleared on power up reset or by write 1. It is not modified by either hardware or software reset. When these bits are cleared, the KSZ8851-16MLLJ deasserts the PME pin.
1-0	0x0	RW	**Power Management Mode** These two bits are used to control the KSZ8851-16MLLJ power management mode as below: 00: Normal Operation Mode. 01: Energy Detect Mode. (two states in this mode either low power or normal power) 10: Soft Power Down Mode. 11: Power Saving Mode. In energy detect mode under low power state, it can wake-up to normal operation mode either from line or host wake-up (host CPU issues a read cycle to GRR register). In soft power down mode, it can wake-up to normal operation mode only from host wake-up (host CPU issues a read cycle to GRR register).

Go-Sleep & Wake-Up Time Register (0xD6 – 0xD7): GSWUTR

This register contains the value which is used to control minimum Go-Sleep time period when the device from normal power state to low power state or to control minimum Wake-Up time period when the device from low power state to normal power state in energy detect mode.

Bit	Default	R/W	Description
15-8	0x08	RW	**Wake-up Time** This value is used to control the minimum period that the energy has to be detected consecutively before the device is waked-up from the low power state. The unit is 16 ms +/- 80%, the default wake-up time is 128 ms (16ms x 8). Zero time (0x00) is not allowed
7-0	0x0C	RW	**Go-sleep Time** This value is used to control the minimum period that the no energy event has to be detected consecutively before the device enters the low power state when the energy detect mode is on. The unit is 1 sec +/-80%, the default go-sleep time is 12 sec (1s x 12). Zero time (0x00) is not allowed

PHY Reset Register (0xD8 – 0xD9): PHYRR

This register contains a control bit to reset PHY block when write an “1”.

Bit	Default	R/W	Description
15-1	-	RW	**Reserved**.
0	0	WO (Self clear)	**PHY Reset Bit** This bit is write only and self clear after write an “1”, it is used to reset PHY block circuitry.

0xDA – 0xDF: Reserved

0xE0 – 0xE3: Reserved

PHY 1 MII-Register Basic Control Register (0xE4 – 0xE5): P1MBCR

This register contains Media Independent Interface (MII) register for port 1 as defined in the IEEE 802.3 specification.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Reserved**	
14	0	RW	**Local (far-end) loopback** (llb) 1 = perform local loopback at host (host Tx -> PHY -> host Rx, see Figure 10) 0 = normal operation	
13	1	RW	**Force 100** 1 = force 100Mbps if AN is disabled (bit 12) 0 = force 10Mbps if AN is disabled (bit 12)	Bit 6 in P1CR
12	1	RW	**AN Enable** 1 = auto-negotiation enabled. 0 = auto-negotiation disabled.	Bit 7 in P1CR
11-10	0	RW	**Reserved**	
9	0	RW	**Restart AN** 1 = restart auto-negotiation. 0 = normal operation.	Bit 13 in P1CR
8	1	RW	**Force Full Duplex** 1 = force full duplex 0 = force half duplex. if AN is disabled (bit 12) or AN is enabled but failed.	Bit 5 in P1CR
7-6	0	RO	**Reserved**	
5	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Micrel Auto MDI-X mode.	Bit 15 in P1SR
4	0	RW	**Force MDI-X** 1 = force MDI-X. 0 = normal operation.	Bit 9 in P1CR
3	0	RW	**Disable MDI-X** 1 = disable auto MDI-X. 0 = normal operation.	Bit 10 in P1CR
2	0	RW	**Reserved**.	
1	0	RW	**Disable Transmit** 1 = disable transmit. 0 = normal operation.	Bit 14 in P1CR
0	0	RW	**Disable LED** 1 = disable all LEDs. 0 = normal operation.	Bit 15 in P1CR

PHY 1 MII-Register Basic Status Register (0xE6 – 0xE7): P1MBSR

This register contains the MII register status for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**T4 Capable** 1 = 100 BASE-T4 capable. 0 = not 100 BASE-T4 capable.	
14	1	RO	**100 Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = not 100BASE-TX full duplex.capable.	
13	1	RO	**100 Half Capable** 1= 100BASE-TX half-duplex capable. 0= not 100BASE-TX half-duplex capable.	
12	1	RO	**10 Full Capable** 1 = 10BASE-T full-duplex capable. 0 = not 10BASE-T full-duplex capable.	
11	1	RO	**10 Half Capable** 1 = 10BASE-T half-duplex capable. 0 = not 10BASE-T half-duplex capable.	
10-7	0x0	RO	**Reserved.**	
6	0	RO	**Preamble suppressed** Not supported.	
5	0	RO	**AN Complete** 1 = auto-negotiation complete. 0 = auto-negotiation not completed.	Bit 6 in P1SR
4	0	RO	**Reserved**	
3	1	RO	**AN Capable** 1 = auto-negotiation capable. 0 = not auto-negotiation capable.	
2	0	RO	**Link Status** 1 = link is up; 0 = link is down.	Bit 5 in P1SR
1	0	RO	**Jabber test** Not supported.	
0	0	RO	**Extended Capable** 1 = extended register capable. 0 = not extended register capable.	

PHY 1 PHY ID Low Register (0xE8 – 0xE9): PHY1ILR

This register contains the PHY ID (low) for the chip.

Bit	Default	R/W	Description
15-0	0x1430	RO	**PHYID Low** Low order PHYID bits.

PHY 1 PHY ID High Register (0xEA – 0xEB): PHY1IHR

This register contains the PHY ID (high) for the chip.

Bit	Default	R/W	Description
15-0	0x0022	RO	**PHYID High** High order PHYID bits.

PHY 1 Auto-Negotiation Advertisement Register (0xEC – 0xED): P1ANAR

This register contains the auto-negotiation advertisement for the PHY function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Next page** Not supported.	
14	0	RO	**Reserved**	
13	0	RO	**Remote fault** Not supported.	
12-11	0x0	RO	**Reserved**	
10	1	RW	**Pause (flow control capability)** 1 = advertise pause capability. 0 = do not advertise pause capability.	Bit 4 in P1CR
9	0	RW	**Reserved**.	
8	1	RW	**Adv 100 Full** 1 = advertise 100 full-duplex capability. 0 = do not advertise 100 full-duplex capability	Bit 3 in P1CR
7	1	RW	**Adv 100 Half** 1= advertise 100 half-duplex capability. 0 = do not advertise 100 half-duplex capability.	Bit 2 in P1CR
6	1	RW	**Adv 10 Full** 1 = advertise 10 full-duplex capability. 0 = do not advertise 10 full-duplex capability.	Bit 1 in P1CR
5	1	RW	**Adv 10 Half** 1 = advertise 10 half-duplex capability. 0 = do not advertise 10 half-duplex capability.	Bit 0 in P1CR
4-0	0x01	RO	**Selector Field** 802.3	

PHY 1 Auto-Negotiation Link Partner Ability Register (0xEE – 0xEF): P1ANLPR

This register contains the auto-negotiation link partner ability for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Next page** Not supported.	
14	0	RO	**LP ACK** Not supported.	
13	0	RO	**Remote fault** Not supported.	
12-11	0x0	RO	**Reserved**	
10	0	RO	**Pause** Link partner pause capability.	Bit 4 in P1SR
9	0	RO	**Reserved**.	
8	0	RO	**Adv 100 Full** Link partner 100 full capability.	Bit 3 in P1SR
7	0	RO	**Adv 100 Half** Link partner 100 half capability.	Bit 2 in P1SR
6	0	RO	**Adv 10 Full** Link partner 10 full capability.	Bit 1 in P1SR
5	0	RO	**Adv 10 Half** Link partner 10 half capability.	Bit 0 in P1SR
4-0	0x01	RO	**Reserved**.	

0xF0 – 0xF3: Reserved

Port 1 PHY Special Control/Status, LinkMD (0xF4 – 0xF5): P1SCLMD

This register contains the special control, status and LinkMD information of PHY1.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Reserved**	
14-13	0x0	RO	**Vct_result** VCT result. [00] = normal condition. [01] = open condition has been detected in cable. [10] = short condition has been detected in cable. [11] = cable diagnostic test is failed.	
12	0	RW (Self-Clear)	**Vct_en** Vct enable. 1 = the cable diagnostic test is enabled. It is self-cleared after the VCT test is done. 0 = it indicates the cable diagnostic test is completed and the status information is valid for read.	

Port 1 PHY Special Control/Status, LinkMD (0xF4 – 0xF5): P1SCLMD (Continued)

11	0	RW	**Force_lnk** Force link. 1 = force link pass; 0 = normal operation.	
10	0	RO	**Reserved.**	
9	0	RW	**Remote (Near-end) loopback** (rlb) 1 = perform remote loopback at PHY (RXP1/RXM1 -> TXP1/TXM1, see Figure 10) 0 = normal operation	
8-0	0x000	RO	**Vct_fault_count** VCT fault count. Distance to the fault. It's approximately 0.4m*vct_fault_count.	

Port 1 Control Register (0xF6 – 0xF7): P1CR

This register contains the global per port control for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RW	**LED Off** 1 = Turn off all of the port 1 LEDs (P1LED3, P1LED2, P1LED1, P1LED0). These pins are driven high if this bit is set to one. 0 = normal operation.	Bit 0 in P1MBCR
14	0	RW	**Txids** 1 = disable the port's transmitter. 0 = normal operation.	Bit 1 in P1MBCR
13	0	RW	**Restart AN** 1 = restart auto-negotiation. 0 = normal operation.	Bit 9 in P1MBCR
12	0	RW	**Reserved**	
11	0	RW	**Reserved**	
10	0	RW	**Disable auto MDI/MDI-X** 1 = disable auto MDI/MDI-X function. 0 = enable auto MDI/MDI-X function.	Bit 3 in P1MBCR
9	0	RW	**Force MDI-X** 1= if auto MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = do not force PHY into MDI-X mode.	Bit 4 in P1MBCR
8	0	RW	**Reserved**	
7	1	RW	**Auto Negotiation Enable** 1 = auto negotiation is enabled. 0 = disable auto negotiation, speed, and duplex are decided by bits 6 and 5 of the same register.	Bit 12 in P1MBCR

Port 1 Control Register (0xF6 – 0xF7): P1CR (Continued)

6	1	RW	**Force Speed** 1 = force 100BT if AN is disabled (bit 7). 0 = force 10BT if AN is disabled (bit 7).	Bit 13 in P1MBCR
5	1	RW	**Force Duplex** 1 = force full duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = force half duplex if (1) AN is disabled or (2) AN is enabled but failed.	Bit 8 in P1MBCR
4	1	RW	**Advertised flow control capability** 1 = advertise flow control (pause) capability. 0 = suppress flow control (pause) capability from transmission to link partner.	Bit 10 in P1ANAR
3	1	RW	**Advertised 100BT full-duplex capability** 1 = advertise 100BT full-duplex capability. 0 = suppress 100BT full-duplex capability from transmission to link partner.	Bit 8 in P1ANAR
2	1	RW	**Advertised 100BT half-duplex capability** 1 = advertise 100BT half-duplex capability. 0 = suppress 100BT half-duplex capability from transmission to link partner.	Bit 7 in P1ANAR
1	1	RW	**Advertised 10BT full-duplex capability** 1 = advertise 10BT full-duplex capability. 0 = suppress 10BT full-duplex capability from transmission to link partner.	Bit 6 in P1ANAR
0	1	RW	**Advertised 10BT half-duplex capability** 1 = advertise 10BT half-duplex capability. 0 = suppress 10BT half-duplex capability from transmission to link partner.	Bit 5 in P1ANAR

Port 1 Status Register (0xF8 – 0xF9): P1SR

This register contains the PHY port status for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	1	RW	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Micrel Auto MDI-X mode.	Bit 5 in P1MBCR
14	0	RO	**Reserved**	
13	0	RO	**Polarity Reverse** 1 = polarity is reversed. 0 = polarity is not reversed.	
12-11	0	RO	**Reserved**	
10	0	RO	**Operation Speed** 1 = link speed is 100Mbps. 0 = link speed is 10Mbps.	
9	0	RO	**Operation Duplex** 1 = link duplex is full. 0 = link duplex is half.	
8	0	RO	**Reserved**	
7	1	RO	**MDI-X status** 1 = MDI. 0 = MDI-X.	
6	0	RO	**AN Done** 1 = AN done. 0 = AN not done.	Bit 5 in P1MBSR
5	0	RO	**Link Good** 1= link good. 0 = link not good.	Bit 2 in P1MBSR
4	0	RO	**Partner flow control capability** 1 = link partner flow control (pause) capable. 0 = link partner not flow control (pause) capable.	Bit 10 in P1ANLPR
3	0	RO	**Partner 100BT full-duplex capability** 1 = link partner 100BT full-duplex capable. 0 = link partner not 100BT full-duplex capable.	Bit 8 in P1ANLPR
2	0	RO	**Partner 100BT half-duplex capability** 1 = link partner 100BT half-duplex capable. 0= link partner not 100BT half-duplex capable.	Bit 7 in P1ANLPR
1	0	RO	**Partner 10BT full-duplex capability** 1= link partner 10BT full-duplex capable. 0 = link partner not 10BT full-duplex capable.	Bit 6 in P1ANLPR
0	0	RO	**Partner 10BT half-duplex capability** 1 = link partner 10BT half-duplex capable. 0 = link partner not 10BT half-duplex capable.	Bit 5 in P1ANLPR

0xFA – 0xFF: Reserved

MIB (Management Information Base) Counters

The KSZ8851-16MLLJ provides 32 MIB counters to monitor the port activity for network management. The MIB counters are formatted as shown in Table 12:

Bit	Name	R/W	Description	Default
31-0	Counter values	RO	Counter value (read clear)	0x00000000

Table 12. Format of MIB Counters

Ethernet port MIB counters are read using indirect memory access. The address offset range is 0x00 to 0x1F.

Offset	Counter Name	Description
0x0	RxByte	Rx octet count including bad packets
0x1	Reserved	Reserved.
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 bytes)
0x5	RxJabbers	Rx packets longer than 1536 bytes w/ either CRC errors, alignment errors, or symbol errors
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,2000) bytes w/ an integral number of bytes and a bad CRC
0x8	RxAlignmentError	Rx packets within (64,2000) bytes w/ a non-integral number of bytes and a bad CRC
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1521Octets	Total Rx packets (bad packets included) that are between 1024 and 1521 octets in length
0x14	Rx1522to2000Octets	Total Rx packets (bad packets included) that are between 1522 and 2000 octets in length
0x15	TxByte	Tx good octet count, including PAUSE packets
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

Table 13. Port 1 MIB Counters Indirect Memory Offsets

Example:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)

Write to reg. IACR (0xC8) with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADHR (MIB counter value 31-16)

Read reg. IADLR (MIB counter value 15-0)

Additional MIB Information

In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.

Absolute Maximum Ratings(1)

Supply Voltage (VDD_A3.3, VDD_IO) ..... –0.5V to +4.0V
Input Voltage (All Inputs) ..... –0.5V to +4.0V
Output Voltage (All Outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C
Maximum Junction Temperature (T_J) ..... +140°C
HBM ESD Rating 6KV

Operating Ratings(2)

Supply Voltage
VDD_A3.3 ..... +3.1V to +3.5V
VDD_IO (3.3V) ..... +3.1V to +3.5V
VDD_IO (2.5V) ..... +2.35V to +2.65V
VDD_IO (1.8V) ..... +1.7V to +1.9V
Ambient Operating Temperature (T_A)
Extended (MLLJ)……..-40°C to +125°C
Thermal Resistance(3)
Junction-to-Ambient (θ_{JA}) .....83.56°C/W
Junction-to-Case (θ_{JC}) .....35.90°C/W

Electrical Characteristics(4, 5)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current for 100BASE-TX Operation (Single Port@100% Utilization)						
I_{dd1}	100BASE-TX (analog core + PLL + digital core + transceiver + digital I/O)	VDD_A3.3, VDD_IO = 3.3V; Chip only (no transformer)		85		mA
		VDD_A3.3 = 3.3V, VDD_IO = 2.5V; Chip only (no transformer)		85		mA
		VDD_A3.3 = 3.3V, VDD_IO = 1.8V; Chip only (no transformer)		85		mA
Supply Current for 10BASE-T Operation (Single Port@100% Utilization)						
I_{dd2}	10BASE-T (analog core + PLL + digital core + transceiver + digital I/O)	VDD_A3.3, VDD_IO = 3.3V; Chip only (no transformer)		75		mA
		VDD_A3.3 = 3.3V, VDD_IO = 2.5V; Chip only (no transformer)		75		mA
		VDD_A3.3 = 3.3V, VDD_IO = 1.8V; Chip only (no transformer)		75		mA
Power Management Mode						
I_{dd3}	Power Saving Mode(6)	Ethernet cable disconnected & Auto-Neg		70		mA
I_{dd4}	Soft Power Down Mode	Set Bit [1:0] = 10 in PMECR register		2		mA
I_{dd5}	Energy Detect Mode	At low power state		2		mA
TTL Inputs (VDD_IO = 3.3V/2.5V/1.8V)						
V_{IH}	Input High Voltage		2.0/2.0 /1.3			V
V_{IL}	Input Low Voltage				0.8/0.6 /0.3	V
I_{IN}	Input Current	V_{IN} = GND ~ VDD_IO	-10		10	µA
TTL Outputs (VDD_IO = 3.3V/2.5V/1.8V)						
V_{OH}	Output High Voltage	I_{OH} = -8mA	2.4/1.9 /1.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4/0.4 /0.2	V
$\|I_{OZ}\|$	Output Tri-state Leakage				10	µA

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to a appropriate logic voltage level (Ground to VDD_IO).
3. No (HS) heat spreader in this package. The θ_{JC}/θ_{JA} is under air velocity 0m/s.

Electrical Characteristics[4, 5] (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BaseTX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination on the diff. output	±0.95		±1.05	V
V_{imb}	Output Voltage Imbalance	100Ω termination on the diff. output			2	%
t_r, / t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.5		V
	Output Jitter	Peak-to-peak		0.7	1.4	ns
10BaseT Receive						
V_{sq}	Squelch Threshold	5MHz square wave		400		mV
10BaseT Transmit (measured differentially after 1:1 transformer)						
V_p	Peak Differential Output Voltage	100Ω termination on the differential output	2.2	2.5	2.8	V
	Jitter Added	100Ω termination on the differential output (Peak-to-peak)		1.8	3.5	ns

Table 14. Electrical Characteristics

Notes:
4. T_A = 25°C. Specification for packaged product only.
5. Single Port's transformer consumes an additional 45mA @3.3V for 100BASE-TX and 70mA @3.3V for 10BASE-T.
6. Single Port's transformer consumes less than 1mA during the Power Saving Mode.

Timing Specifications

Asynchronous Read and Write Timing

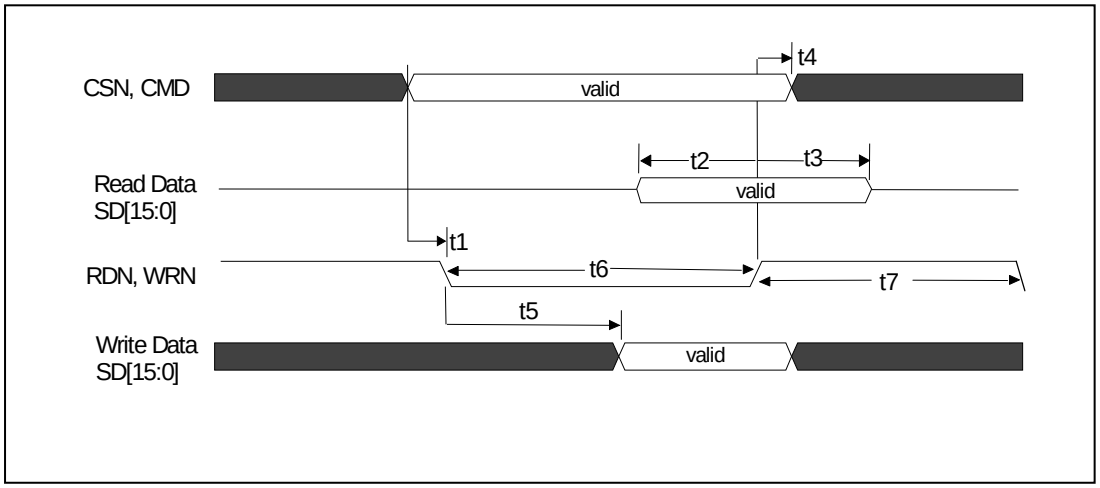


Figure 11. Asynchronous Cycle

Symbol	Parameter	Min	Typ	Max	Unit
t1	CSN, CMD valid to RDN, WRN active	0			ns
t2	Read Data SD[15:0] valid to RDN inactive	2			ns
t3	RDN inactive to Read data invalid	1		2	ns
t4	CSN, CMD hold after RDN, WRN inactive	0			ns
t5	WRN active to write data valid (bit12=0 in RXFDPR)	8		16	ns
	WRN active to write data valid (bit12=1 in RXFDPR)			4	ns
t6	RDN Read active time (low)	40			ns
	WRN Write active time (low)	40			ns
t7	RDN Read inactive time (high)	10			ns
	WRN Write inactive time (high)	10			ns

Table 15. Asynchronous Cycle Timing Parameters

Auto Negotiation Timing

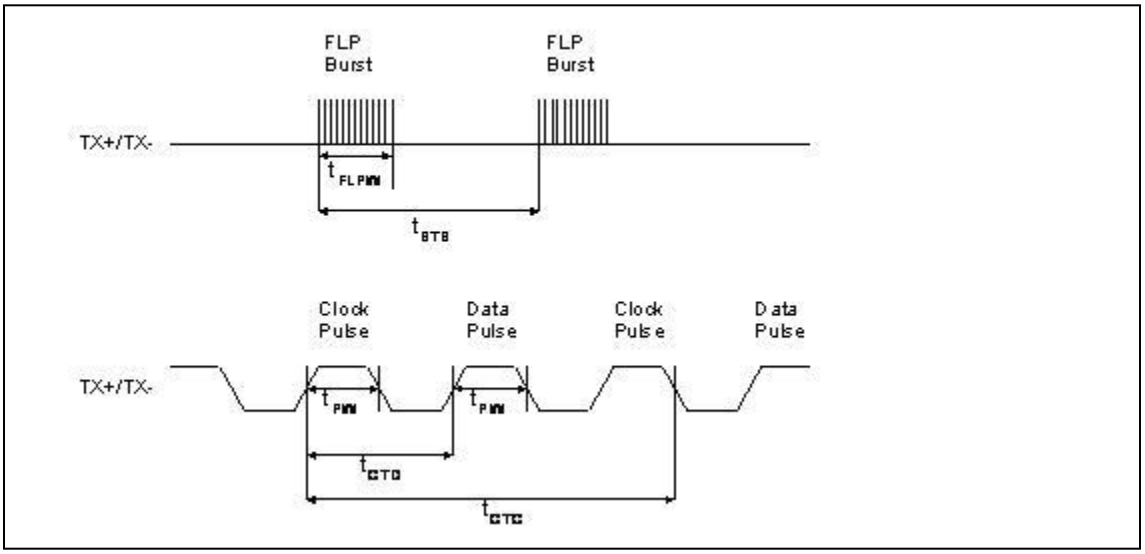


Figure 12. Auto Negotiation Timing

Timing Parameter	Description	Min.	Typ.	Max.	Unit.
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of Clock/Data pulses per burst	17		33	

Table 16. Auto Negotiation Timing Parameters

Reset Timing

As long as the stable supply voltages to reset High timing (minimum of 10ms) are met, there is no power-sequencing requirement for the KSZ8851-16MLLJ supply voltages (3.3V).

The reset timing requirement is summarized in the Figure 13 and Table 17.

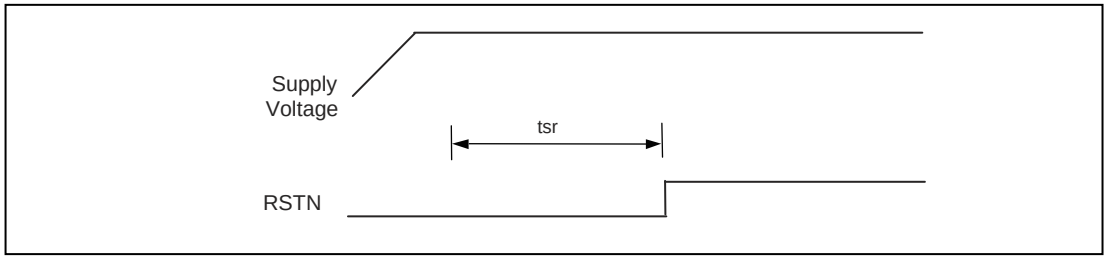


Figure 13. Reset Timing

Symbol	Parameter	Min	Max	Unit
tsr	Stable supply voltages to reset High	10		ms

Table 17. Reset Timing Parameters

EEPROM Timing

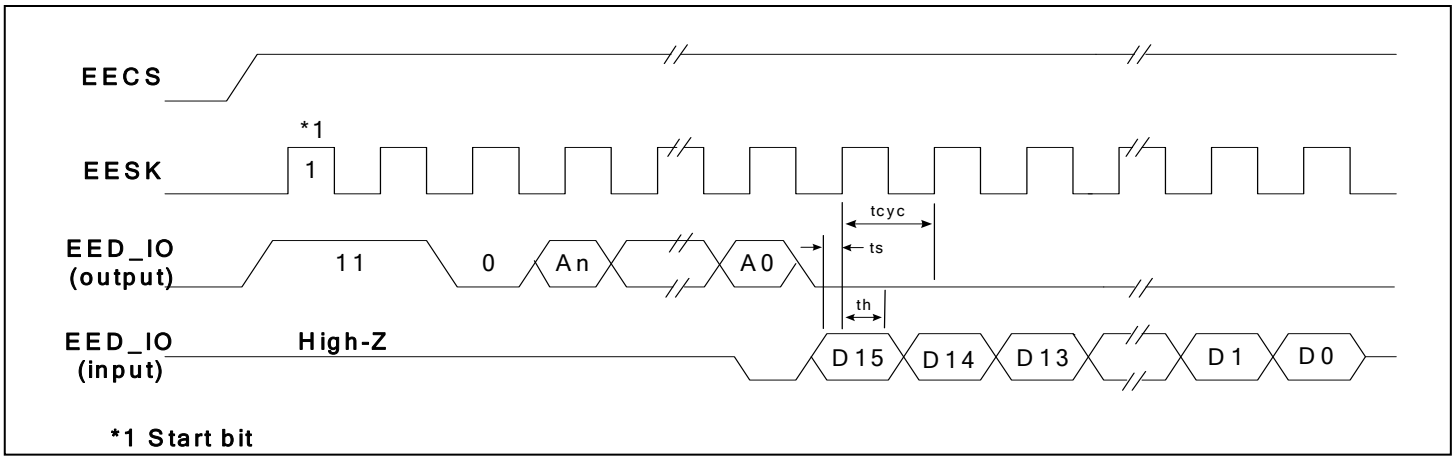


Figure 14. EEPROM Read Cycle Timing Diagram

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc	Clock cycle		0.8 (OBCR[1:0]=00 on-chip bus speed @ 125 MHz)		µs
ts	Setup time	20			ns
th	Hold time	20			ns

Table 18. EEPROM Timing Parameters

Selection of Isolation Transformers

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 19 gives recommended transformer characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min)	350μH	100mV, 100kHz, 8mA
Leakage inductance (max)	0.4μH	1MHz (min)
Inter-winding capacitance (max)	12pF	
D.C. resistance (max)	0.9Ω	
Insertion loss (max)	1.0dB	0MHz – 65MHz
HIPOT (min)	1500Vrms	

Table 19. Transformer Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

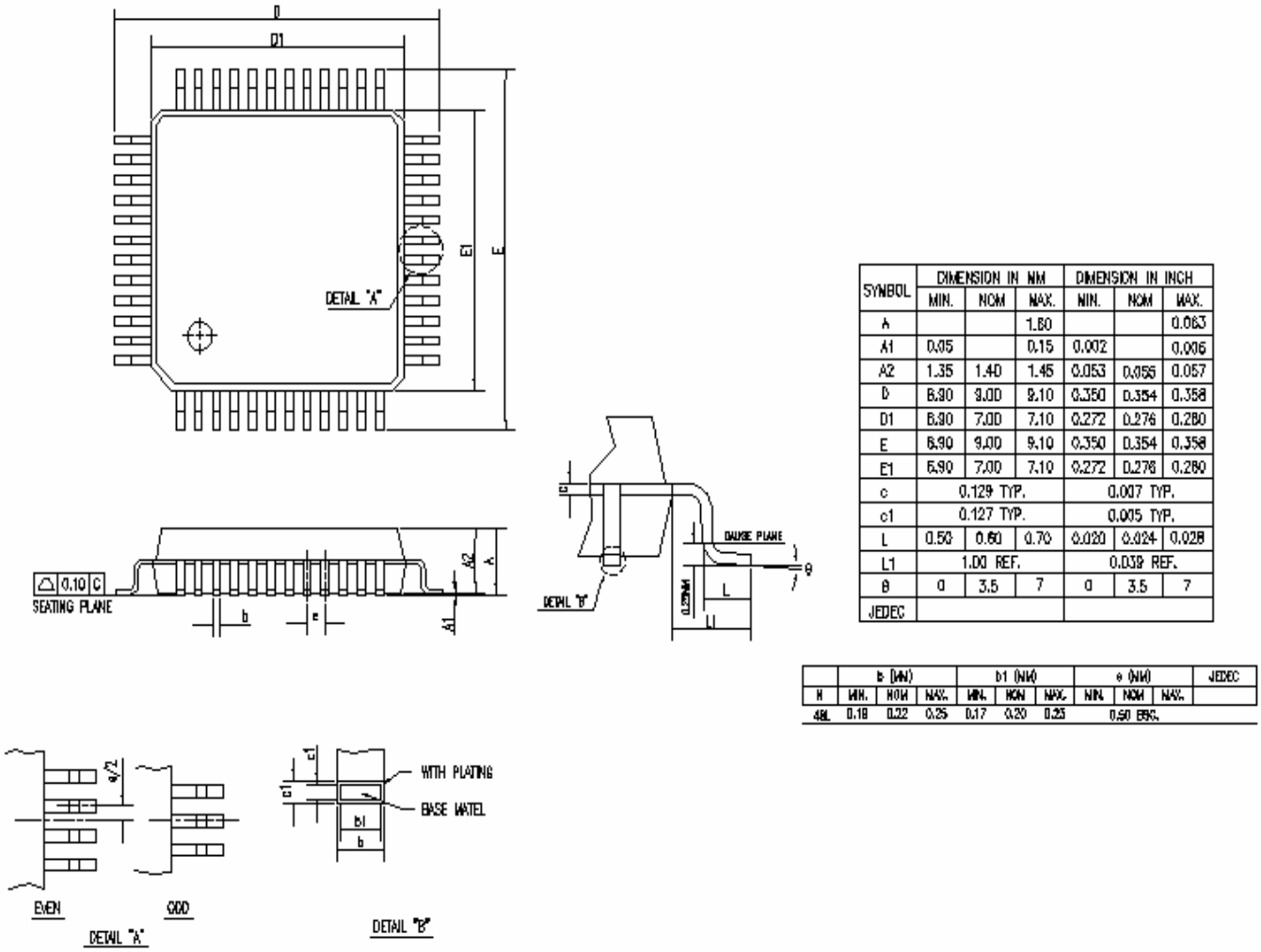
Table 20. Qualified Single Port Magnetics

Selection of Reference Crystal

Chacteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance (max)	20	pF
Series resistance	40	Ω

Table 21. Typical Reference Crystal Characteristics

Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.53	0.60	0.73	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.18	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

Figure 15. 48-Pin (7mm x 7mm) LQFP (V)

Acronyms and Glossary

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-through switch		A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EEPROM	Electronically Erasable Programmable Read-only Memory	A design in which memory on a chip can be erased by exposing it to an electrical charge.
EISA	Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI	Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
Jumbo Packet		A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.'

MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non Port VLAN ID	The Port VLAN ID value is used as a VLAN reference.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PME	Power Management Event	An occurrence that affects the directing of power to different components of a system.
QMU	Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA	Source Address	The address from which information has been sent.
TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal -- or part of the signal -- to return.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

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