

Feature

- Full diffusion process,capsule type ceramic package
- Distributed extension to amplify the gate structure
- Excellent dynamic characteristic
- Low switching loss,Doule-sided cooling
- Fast switching performance

Typical Application

- Inverter,Chopppe,Inductor
- Various types of forced converter

$I_{T(AV)}$	3000A
V_{DRM}/V_{RRM}	600-2500V
T_q	40-80us
I_{TSM}	44KA

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_J (°C)	VALUE		UNIT
				Min	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, THS=55°C	125		3000	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	$V_{DRM} \& V_{RRM} t_p=10ms$ $V_{DSM} \& V_{RSM}=V_{DRM} \& V_{RRM}+100V$	125	500	2500	V
I_{DRM} I_{RRM}	Repetitive peak current	$V_{DM}=V_{DRM}$ $V_{RM}=V_{RRM}$	125		250	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125		44	KA
I^2t	I^2t for fusing coordination	$V_R=0.6V_{RRM}$			9680	$A^2S \times 10$
V_{TO}	Threshold voltage				1.32	V
r_T	On-state slop resistance		125		0.14	mΩ
V_{TM}	Peak on-state voltage	$I_{TM}=5000A, F=15KN$	25		3.15	V
dv/dt	Critical rate of rise of-state voltage	$V_{DM}=0.67V_{DRM}$	125		1000	V/us
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\% V_{DRM}$ TO 1000A, Gate pulse $t_r \leq 0.5us$ $I_{GM}=1.5A$	125		250	A/us
I_{TM}	Reverse recovery current	$I_{TM}=5000A, t_q=1000us$ $Di/dt=-20A/us.$ $V_f=50V$	125	195		A
t_{rr}	Reverse recovery time			10.4		us
Q_{rr}	Recovery charge			1014	1100	uC
t_q	Circuit commutated turn-off time	$I_{TM}=5000A, t_q=1000us,$ $di/dt=20a/us$ $V_R=50V$	125	40	80	us
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	40	450	mA
V_{GT}	Gate trigger voltage			0.9	4.5	V
I_H	Holding current			20	1000	mA
V_{GD}	Npn-trigger gate voltage	$V_{DM}=0.67V_{DRM}$	125	0.3		V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180° sine double side cooled Clamping force 5.0kn			0.009	°C/W
F_M	Mounting force			70	85	KN
T_{stq}	Stored temperature			-40	140	°C
W_t	Weight					g
Outline						

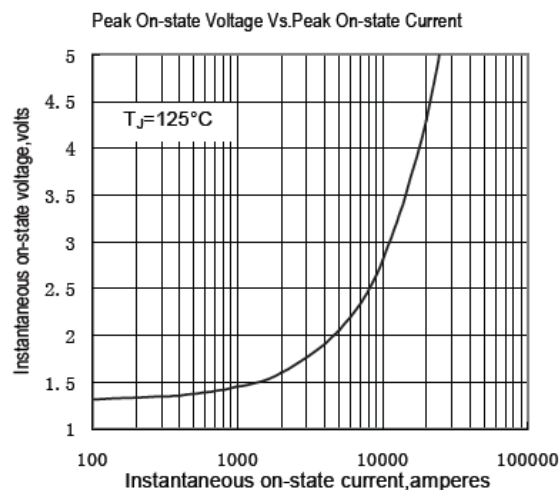


Fig.1

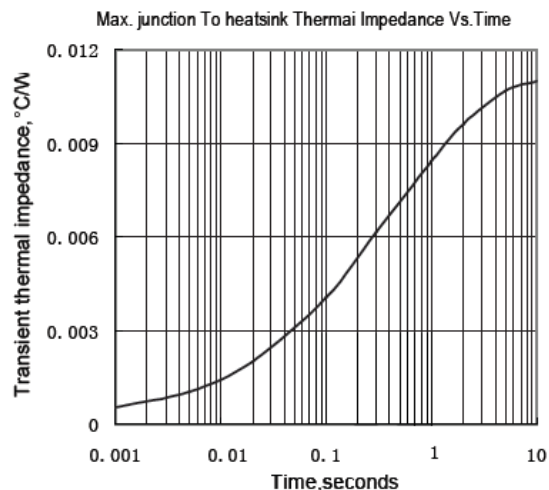


Fig.2

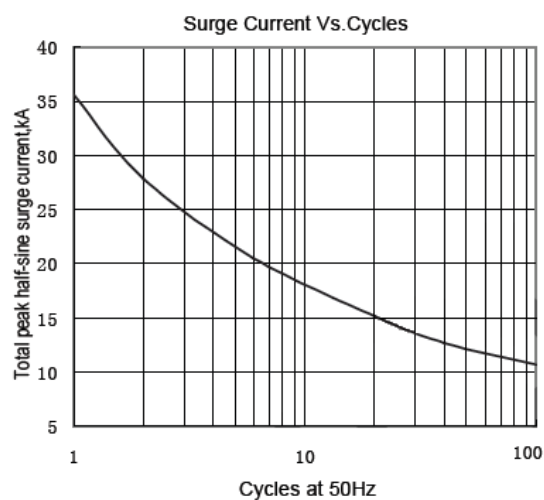


Fig.3

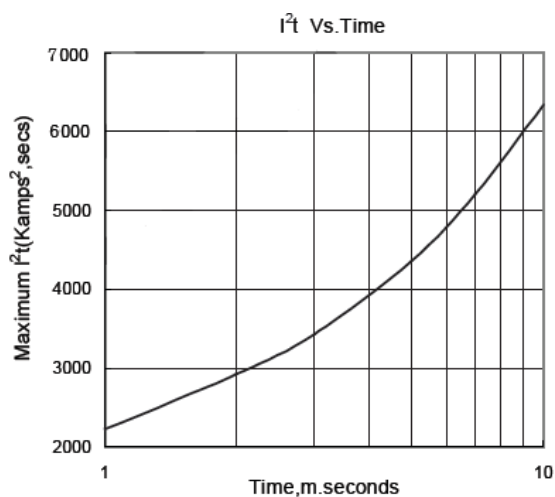


Fig.4

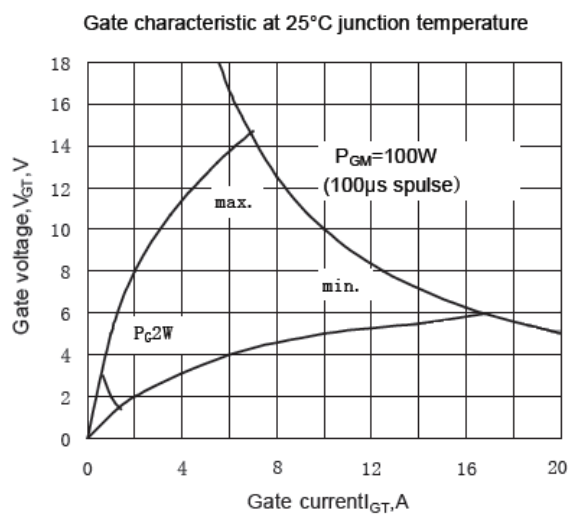


Fig.5

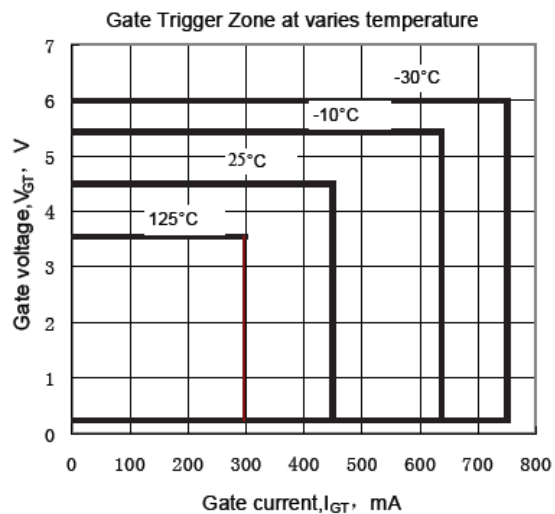
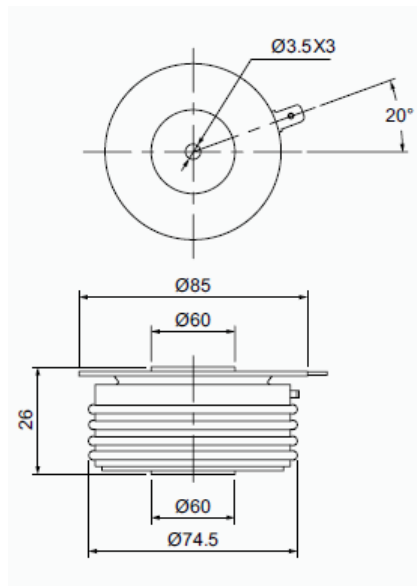
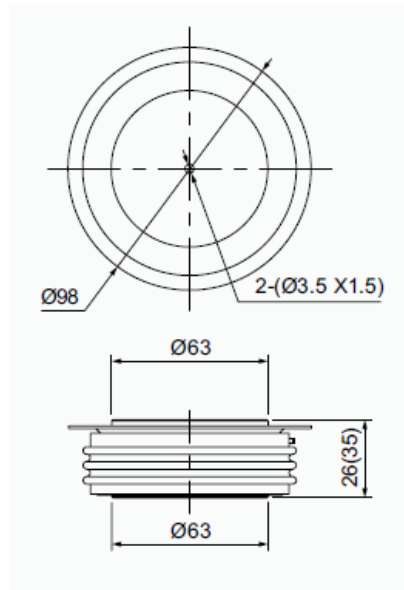


Fig.6

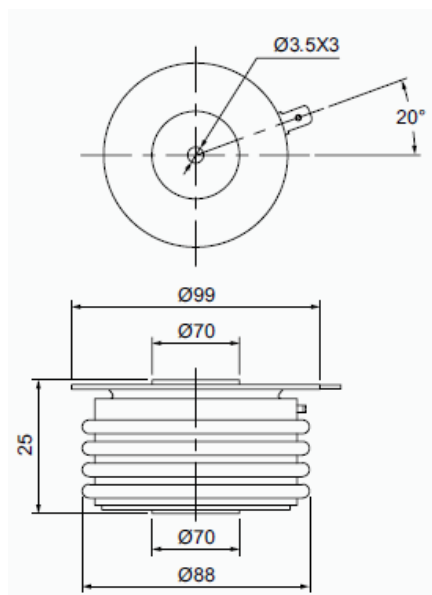
Outline:



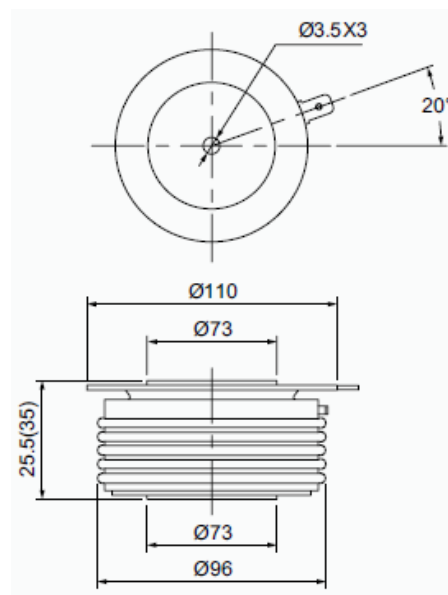
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