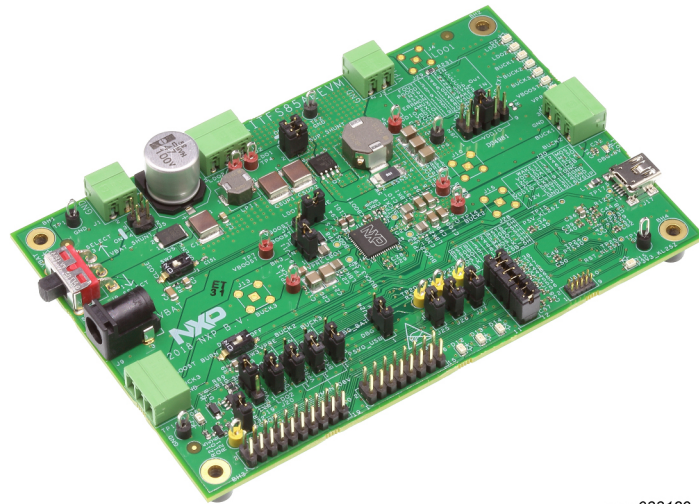


# UM11193

## KITFS85AEEVM evaluation board

Rev. 2.1 — 30 January 2019

User manual



aaa-033129

Figure 1. KITFS85AEEVM

### Important Notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY**. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and/or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Typical parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including Typical, must be validated for each customer application by customer's technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part.



## 1 Introduction

This document is the user guide for the KITFS85AEEVM evaluation board.

This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85AEEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

This kit is suitable for truck application running at 24 V nominal. It is able to sustain up to 60 V at  $V_{BAT}$ .

It is delivered with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. Burning the OTP three times, gives a good flexibility. The board contains a superset device (MC33FS8530AE0S), allowing tests on all the FS84/FS85 derivatives.

## 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for KITFS85AEEVM evaluation board is at <http://www.nxp.com/KITFS85AEEVM>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85AEEVM evaluation board, including the downloadable assets referenced in this document.

### 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

## 3 Getting ready

Working with the KITFS85AEEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

### 3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm

- Jumpers mounted on board

### 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

### 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

### 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <http://www.nxp.com/KITFS85AEEVM> or from the provided link.

- FlexGUI latest version
- FS85\_FS84\_OTP\_Config.xlsm
- Java installation <https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html>

## 4 Getting to know the hardware

The KITFS85AEEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/DC switcher node is mapped on test points. Digital signals (SPI, I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

This board can be operated in Emulation mode or in OTP mode. In emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

### 4.1 Kit overview

The KITFS85AEEVM is a hardware evaluation tool that allows performance test. The FS85xx part soldered on the board can be fused three times (see [Section 7.3 "Programming the device with an OTP configuration"](#)).

An Emulation mode is possible to test as many configurations as needed. The voltage monitoring hardware configuration is done through resistors. Note this configuration can be changed by selecting the appropriate bridges resistors:

- VMON1: assigned to VPRE, 4.1 V

- VMON2: assigned to EXT\_MON2, (VMON bridge for 3.3 V input)
- VMON3: assigned to BUCK3, 2.3 V
- VMON4: assigned to EXT\_MON4, (VMON bridge for 5.0 V input)

This configuration can be changed by installing appropriate bridge resistors. This board was designed to sustain up to 10 A total on VPRE. Layout is done using six layer PCB stack up.

The FS84/FS85 family can be evaluated with this board as it is populated with a superset part. The FS84xx supports ASIL B design, while FS85xx supports ASIL D design.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC/DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

#### 4.1.1 KITFS85AEEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 6.0 A (external MOSFET)
- VBUCK1/2 in Standalone (default) or Multiphase mode
- VBUCK3 up to 3.6 A peak
- VBOOST 5.0 V or 5.74 V, up to 400 mA
- LDO1 and LDO2, from 1.1 V to 5.0 V, up to 400 mA
- Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX\_OUT, regulators)
- LEDs that indicate signal or regulator status
- Support OTP fuse capabilities
- USB connection for register access, OTP emulation and programming

#### 4.1.2 VMON configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in [Figure 2](#).

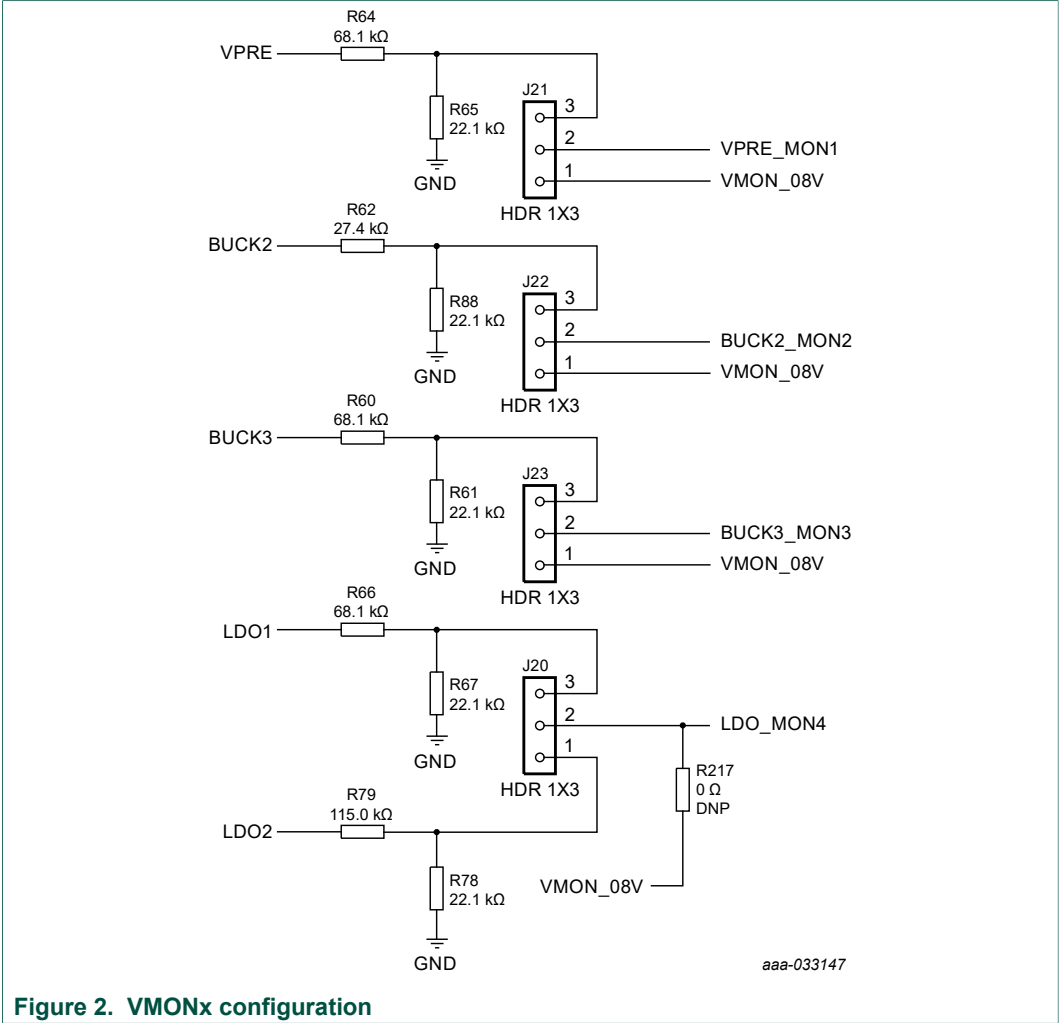
This configuration supports the following mapping:

- VPRE, assigned to VMON1; Bridge resistor set for 3.3 V
- BUCK2, assigned to VMON2; Bridge resistor set for 1.8 V
- BUCK3, assigned to VMON3; Bridge resistor set for 3.3 V
- LDO1, assigned to VMON4; Bridge resistor set for 3.3 V
- LDO2, assigned to VMON4; Bridge resistor set for 5.0 V

LDO1 and LDO2 use the same VMON, a reassignment is necessary to monitor both.

Due to the jumpers, VMONx can be tied to a 0.8 V to force a good voltage at pin level. This behaves like hardware disabling and makes debug easy in some cases.





4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.

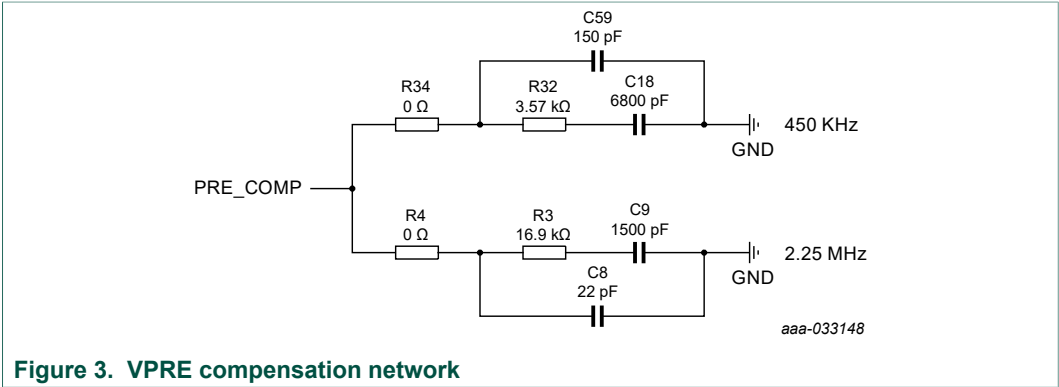
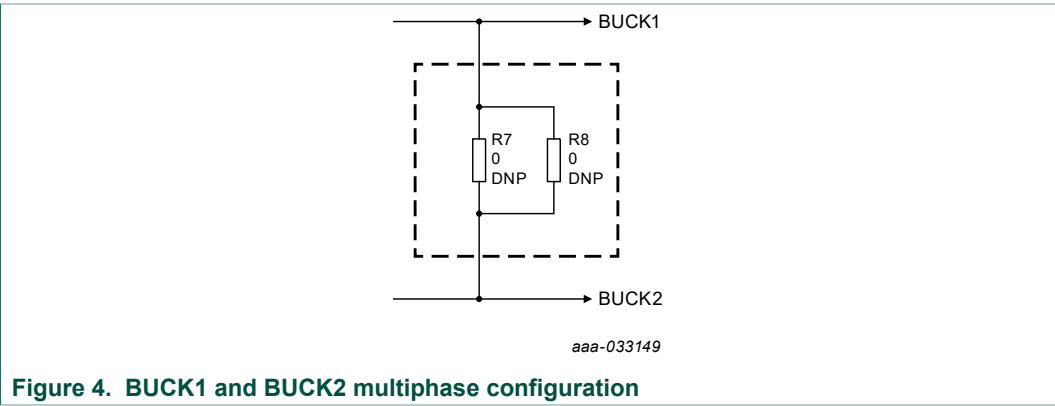


Table 1. Compensation network

| Components | VPRE 450 kHz     | VPRE 2.2 MHz             |
|------------|------------------|--------------------------|
| C18/C9     | 6.8 nF           | 1.5 nF                   |
| C59/C8     | 150 pF           | 22 pF                    |
| R32/R3     | 3.57 kΩ          | 16.9 kΩ                  |
| LPRE       | 4.7 μH or 6.8 μH | 1.5 μH, 2.2 μH or 4.7 μH |

4.1.4 BUCK1 and BUCK2 multiphase configuration

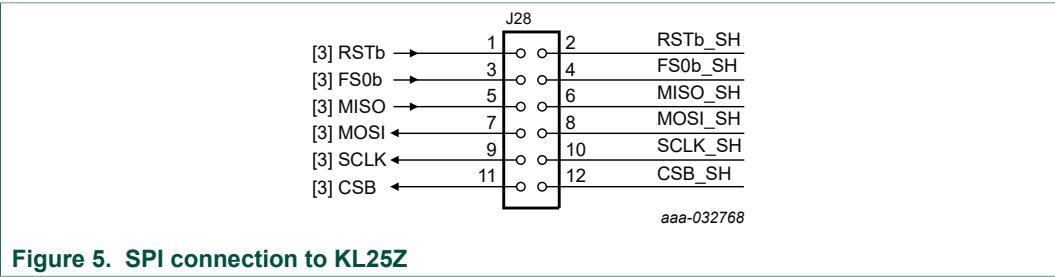
The board is designed to work independently with BUCK1 and BUCK2. Due to R7 and R8, it is possible to connect both connectors together and work in multiphase.



4.1.5 SPI/I2C

The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see [Section 8 "Using FlexGUI"](#)).

This kit uses a KL25Z MCU to communicate with FlexGUI. However, if the user wants to connect the SPI to another MCU, this is possible. In this case, remove J28 and appropriate jumpers to disconnect the KL25Z MCU (see [Figure 5](#)) and connect the external MCU on J30 connector as shown in [Figure 6](#). In addition to this change, make sure that the VDDIO voltage domain is the same on MCU side and SBC side.



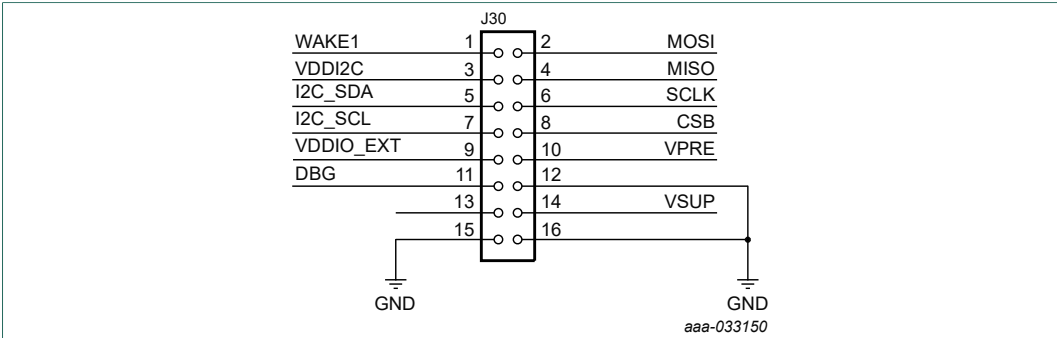


Figure 6. J30 SPI connection

4.1.6 VDDI2C

As an option, an external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.

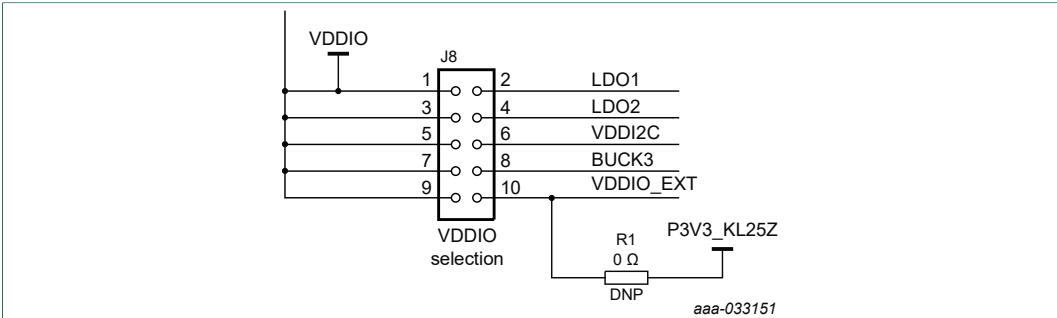


Figure 7. VDDIO selection

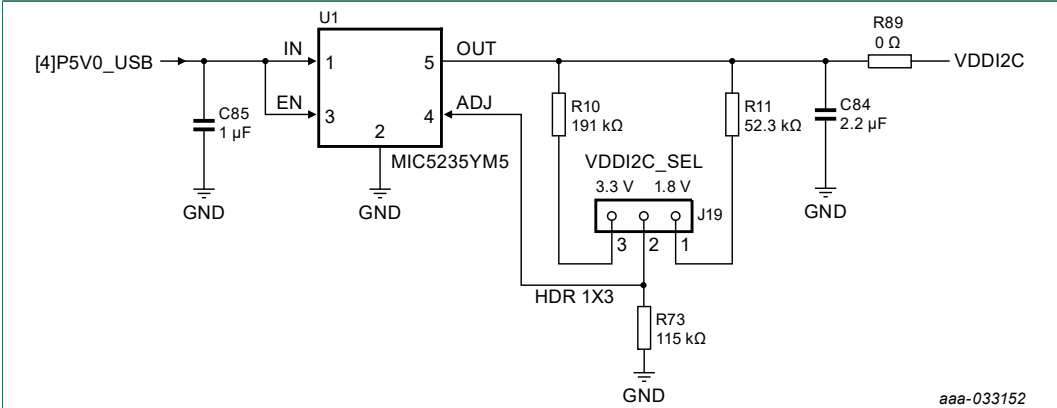


Figure 8. VDDI2C supply

4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This

impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

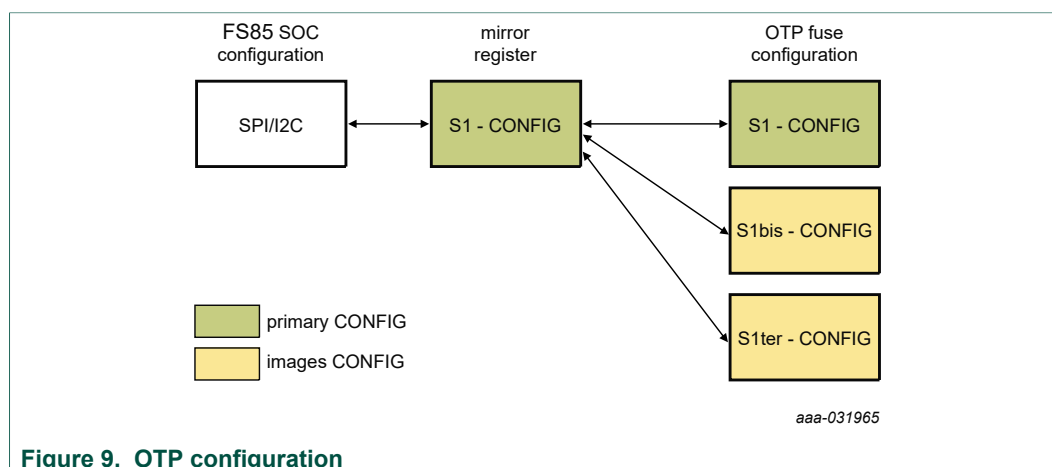
The OTP related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

#### 4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in [Figure 9](#) (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert back to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

**Note:** When device is operating in Emulation mode using configuration from mirror registers, few parameters must be overwritten by SPI/I2C. This concerns regulator TSD behaviors; VPRE slew rate high-side and low-side VBOOST slew rate. See [Section 8.4.10 "TestMode:Mirrors\\_Main and TestMode:Mirrors\\_Failsafe"](#) for additional details.



At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

#### 4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

[Figure 10](#) shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

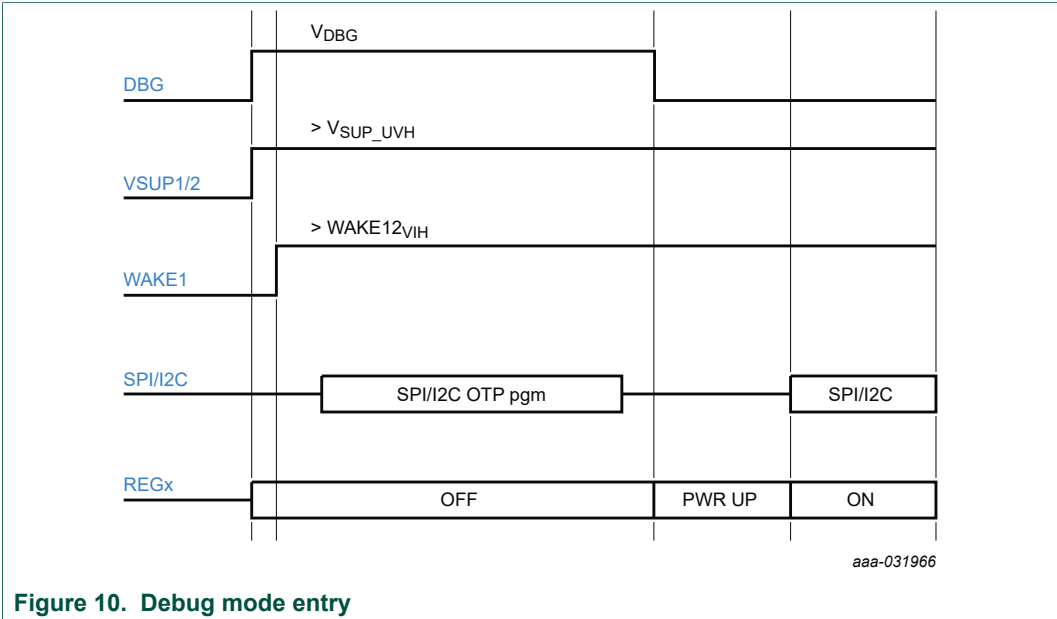


Figure 10. Debug mode entry

Figure 11 shows the hardware kit implementation.

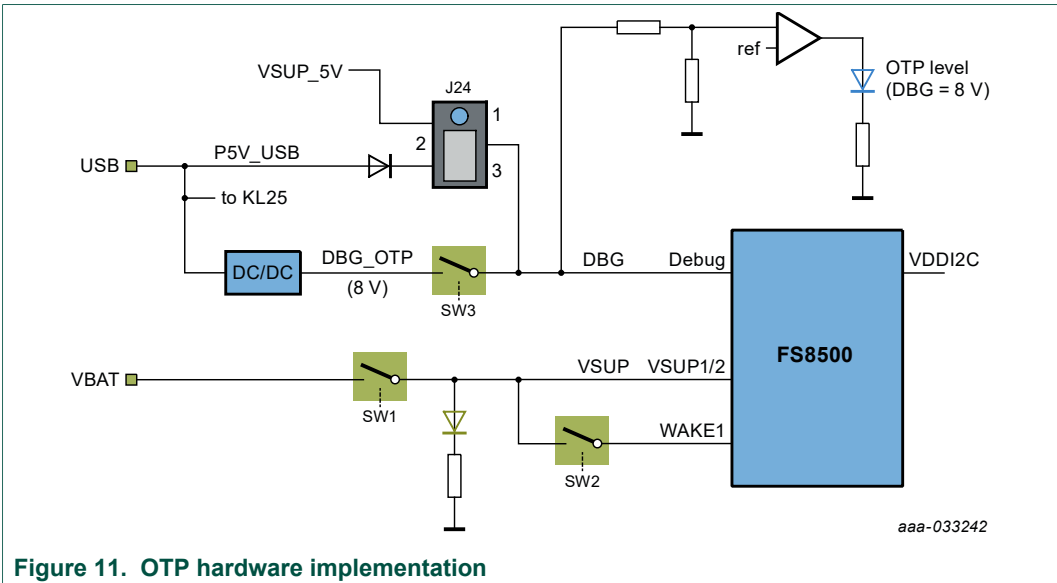


Figure 11. OTP hardware implementation

### 4.3 Kit featured components

Figure 12 identifies important components on the board and Table 2 provides additional details on these components.

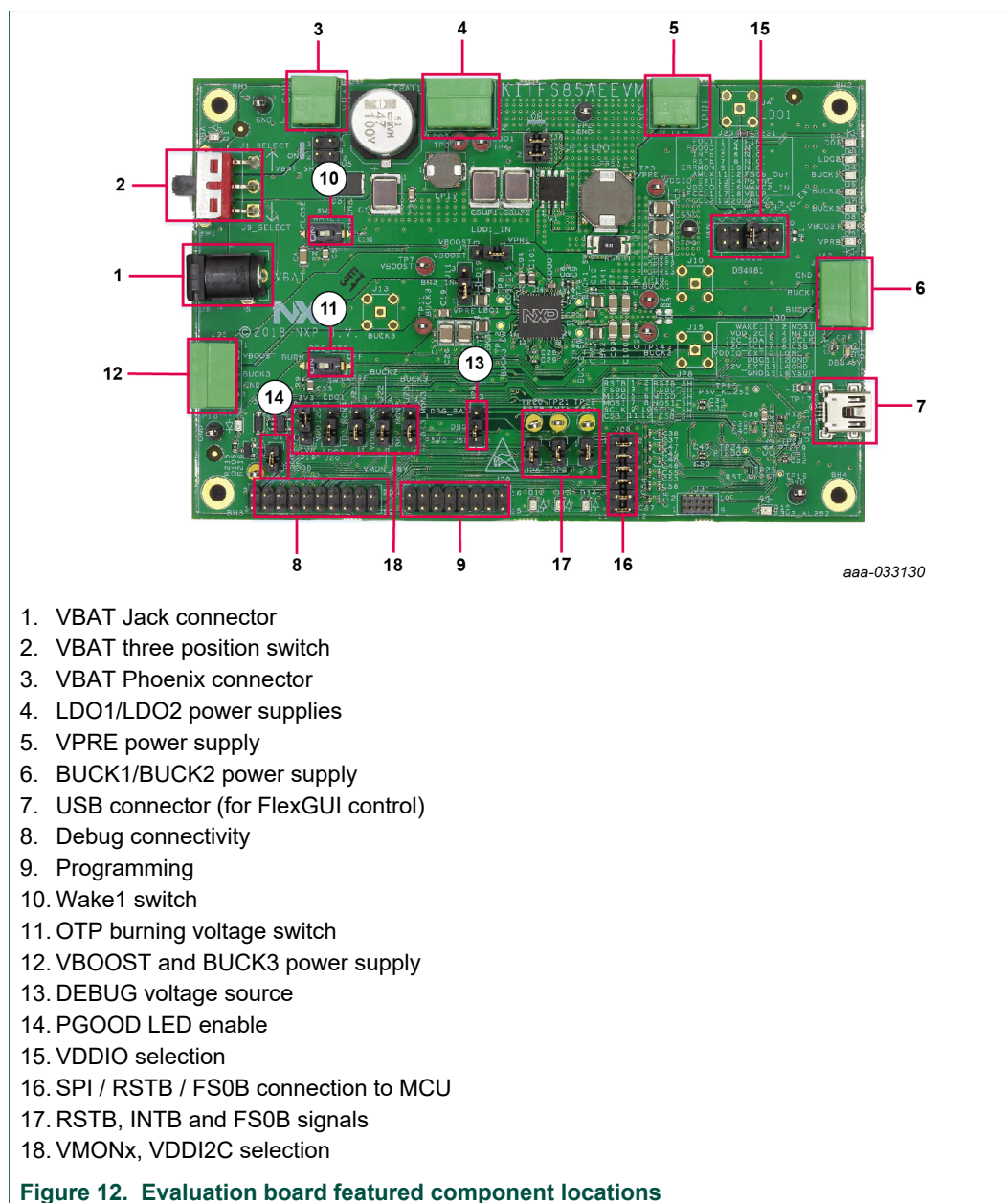


Table 2. Evaluation board board component descriptions

| Number | Description                                                                                                                                                                                                                            |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1      | VBAT Jack connector                                                                                                                                                                                                                    |
| 2      | VBAT three position switch <ul style="list-style-type: none"> <li>Left position: board supplied by Jack connector</li> <li>Middle position: board not supplied</li> <li>Right position: board supplied by Phoenix connector</li> </ul> |
| 3      | VBAT Phoenix connector                                                                                                                                                                                                                 |
| 4      | LDO1/LDO2 power supply                                                                                                                                                                                                                 |
| 5      | VPRE power supply                                                                                                                                                                                                                      |
| 6      | BUCK1/BUCK2 power supply                                                                                                                                                                                                               |



| Number | Description                                                                                                                                                                                                                   |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | USB connector (for FlexGUI control)                                                                                                                                                                                           |
| 8      | Debug connectivity. Access to: <ul style="list-style-type: none"> <li>• VSUP, GND</li> <li>• FOUT/FIN</li> <li>• PGOOD/RSTB/FS0B</li> <li>• FCCUx</li> <li>• WAKE2</li> <li>• PSYNC, ERRMON, AMUX</li> <li>• VMONx</li> </ul> |
| 9      | Programming <ul style="list-style-type: none"> <li>• SPI bus</li> <li>• I2C bus</li> <li>• Debug pin</li> <li>• VPRE, VSUP, GND</li> </ul>                                                                                    |
| 10     | Wake1 switch                                                                                                                                                                                                                  |
| 11     | OTP burning voltage switch                                                                                                                                                                                                    |
| 12     | VBOOST and BUCK3 power supply                                                                                                                                                                                                 |
| 13     | DEBUG voltage source either from USB (recommended) or from VSUP                                                                                                                                                               |
| 14     | PGOOD LED indicator (enabled when jumper is plugged)                                                                                                                                                                          |
| 15     | VDDIO source from device regulators or external sources                                                                                                                                                                       |
| 16     | SPI, RSTB or FS0B can be disconnected between device and MCU                                                                                                                                                                  |
| 17     | RSTB, INTB and FS0B signals available here (device pin level)                                                                                                                                                                 |
| 18     | Allows to select VMON from regulators or a fix 0.8 V<br>VDDI2C can be selected either 1.8 V or 3.3 V                                                                                                                          |

### 4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

#### 4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

#### 4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.

- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number:** low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10  $\mu$ A typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

### 4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

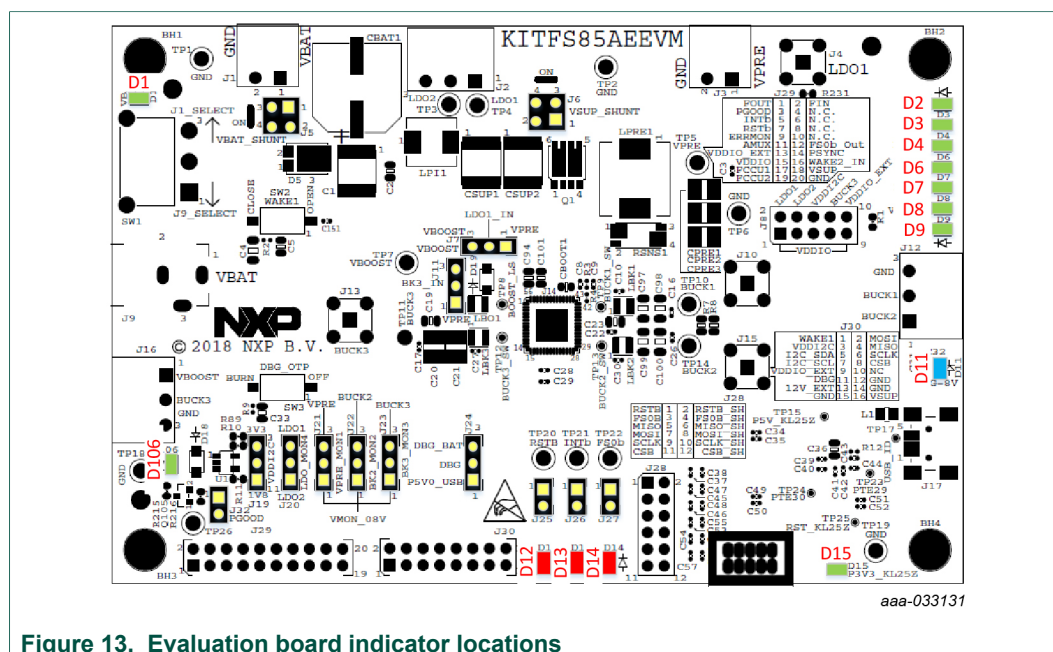


Figure 13. Evaluation board indicator locations

Table 3. Evaluation board indicator descriptions

| Label | Name | Color | Description |
|-------|------|-------|-------------|
| D1    | VBAT | Green | VBAT On     |
| D2    | LDO1 | Green | LDO1 On     |

| Label | Name        | Color | Description                               |
|-------|-------------|-------|-------------------------------------------|
| D3    | LDO2        | Green | LDO2 On                                   |
| D4    | BUCK1       | Green | BUCK1 On                                  |
| D6    | BUCK2       | Green | BUCK2 On                                  |
| D7    | BUCK3       | Green | BUCK3 On                                  |
| D8    | VBOOST      | Green | VBOOST On                                 |
| D9    | VPRE        | Green | VPRE On                                   |
| D11   | DBG > 8.0 V | Blue  | DBG pin voltage > 8.0 V (OTP programming) |
| D12   | RSTB        | Red   | RSTb asserted (logic level = 0)           |
| D13   | INTB        | Red   | INTB asserted (logic level = 0)           |
| D14   | FS0B        | Red   | FS0B asserted (logic level = 0)           |
| D15   | P3V3_KL25   | Green | P3V3_KL25 On                              |
| D106  | PGOOD       | Green | PGOOD released                            |

4.3.3 Connectors

Figure 14 shows the location of connectors on the board.

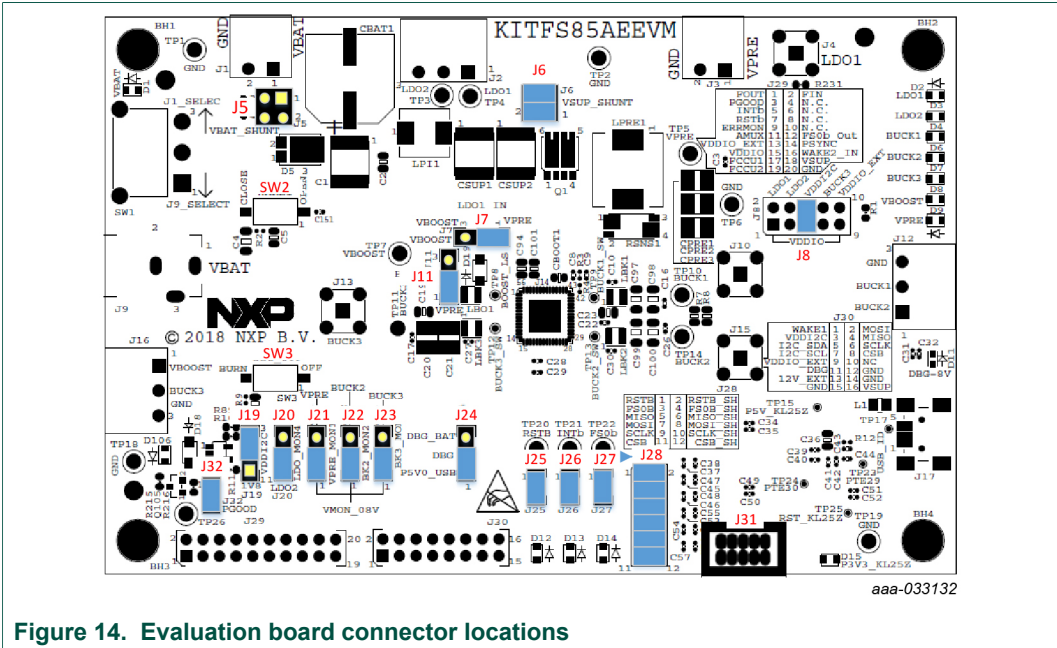


Figure 14. Evaluation board connector locations

4.3.3.1 VBAT connector (J1)

VBAT connects to the board through Phoenix connector (J1).

Table 4. V<sub>BAT</sub> Phoenix connector (J1)

| Schematic label | Signal name | Description                  |
|-----------------|-------------|------------------------------|
| J1-1            | VBAT        | Battery voltage supply input |
| J1-2            | GND         | Ground                       |

### 4.3.3.2 Output power supply connectors

**Table 5. BUCK1/BUCK2 connector (J14)**

| Schematic label | Signal name | Description               |
|-----------------|-------------|---------------------------|
| J14-1           | BUCK2       | BUCK2 power supply output |
| J14-2           | BUCK1       | BUCK1 power supply output |
| J14-3           | GND         | Ground                    |

**Table 6. VBOOST/BUCK3 connector (J16)**

| Schematic label | Signal name | Description               |
|-----------------|-------------|---------------------------|
| J16-1           | VBOOST      | VBOOST output             |
| J16-2           | BUCK3       | BUCK3 power supply output |
| J16-3           | GND         | Ground                    |

**Table 7. LDO1/LDO2 connector (J2)**

| Schematic label | Signal name | Description              |
|-----------------|-------------|--------------------------|
| J2-1            | LDO1        | LDO1 power supply output |
| J2-2            | LDO2        | LDO2 power supply output |
| J2-3            | GND         | Ground                   |

**Table 8. VPRE connector (J3)**

| Schematic label | Signal name | Description              |
|-----------------|-------------|--------------------------|
| J3-1            | VPRE        | VPRE power supply output |
| J3-2            | GND         | Ground                   |

### 4.3.3.3 Debug connector (J29)

**Table 9. Debug connector (J29)**

| Schematic label | Signal name | Description                      |
|-----------------|-------------|----------------------------------|
| J29-1           | FOUT        | Frequency synchronization output |
| J29-2           | FIN         | Frequency synchronization input  |
| J29-3           | PGOOD       | Power GOOD                       |
| J29-4           | n.c.        | not connected                    |
| J29-5           | INTB        | Interrupt, active low            |
| J29-6           | n.c.        | not connected                    |
| J29-7           | RSTB        | Reset, active low                |
| J29-8           | n.c.        | not connected                    |
| J29-9           | ERRMON      | Error monitoring                 |
| J29-10          | n.c.        | not connected                    |
| J29-11          | AMUX        | Analog multiplexer               |
| J29-12          | FS0B_Out    | Fail-safe, active low            |
| J29-13          | VDDIO_EXT   | VDDIO external reference         |

| Schematic label | Signal name | Description                    |
|-----------------|-------------|--------------------------------|
| J29-14          | PSYNC       | Power synchronization          |
| J29-15          | VDDIO       | VDDIO used by FS85             |
| J29-16          | WAKE2_IN    | Wake2 input                    |
| J29-17          | FCCU1       | Fault collector control unit 1 |
| J29-18          | VSUP        | VSUP power supply              |
| J29-19          | FCCU2       | Fault collector control unit 2 |
| J29-20          | GND         | Ground                         |

#### 4.3.3.4 Program connector (J30)

Table 10. Program connector (J30)

| Schematic label | Signal name | Description                            |
|-----------------|-------------|----------------------------------------|
| J30-1           | WAKE1       | WAKE1 input                            |
| J30-2           | MOSI        | SPI master output slave input          |
| J30-3           | VDDI2C      | VDDI2C voltage                         |
| J30-4           | MISO        | SPI master input slave output          |
| J30-5           | I2C_SDA     | I2C serial data                        |
| J30-6           | SCLK        | SPI clock                              |
| J30-7           | I2C_SCL     | I2C serial clock                       |
| J30-8           | CSB         | SPI chip select                        |
| J30-9           | VDDIO_EXT   | VDDIO supplied from external regulator |
| J30-10          | VPRE        | VPRE output                            |
| J30-11          | DBG         | Connected to Debug pin                 |
| J30-12          | GND         | Ground                                 |
| J30-13          | n.c.        | not connected                          |
| J30-14          | VSUP        | Connected to VSUP pin                  |
| J30-15          | GND         | Ground                                 |
| J30-16          | GND         | Ground                                 |

#### 4.3.4 Test points

The following test points provide access to various signals to and from the board.

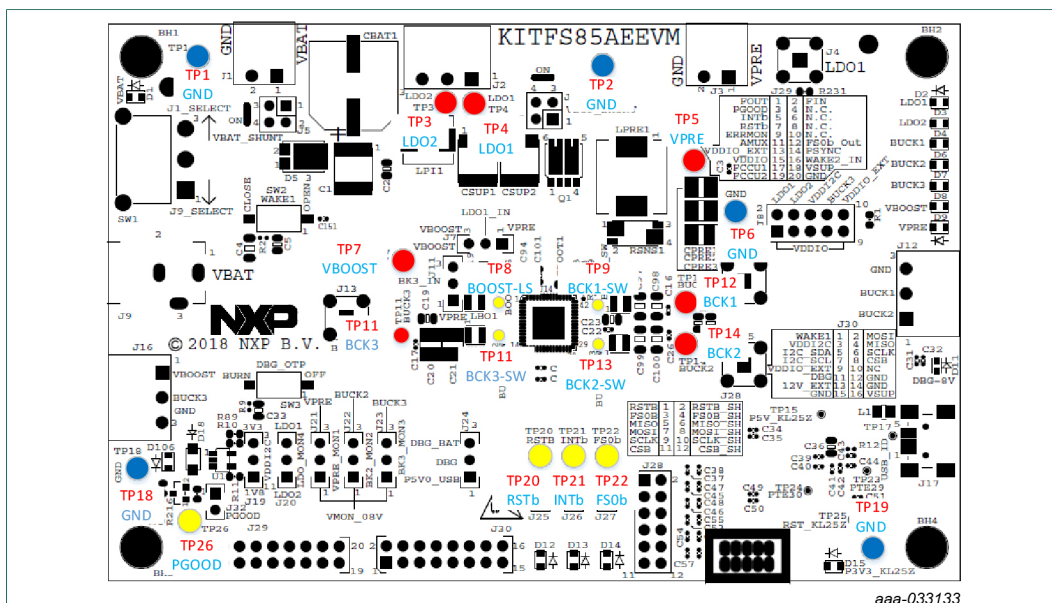


Figure 15. Evaluation board test points

Table 11. Evaluation board test point descriptions

| Test point name | Signal name | Description                  |
|-----------------|-------------|------------------------------|
| TP1             | GND         | Ground                       |
| TP2             | GND         | Ground                       |
| TP3             | LDO1        | LDO1 regulator output        |
| TP4             | LDO2        | LDO2 regulator output        |
| TP5             | VPRE        | VPRE DC/DC regulator output  |
| TP6             | GND         | Ground                       |
| TP7             | VBOOST      | VBOOST DC/DC output          |
| TP8             | BOOST_LS    | VBOOST low-side switcher     |
| TP9             | BUCK1_SW    | BUCK1 switcher               |
| TP10            | BUCK1       | BUCK1 DC/DC regulator output |
| TP11            | BUCK3       | BUCK3 DC/DC regulator output |
| TP12            | BUCK3_SW    | BUCK3 switcher               |
| TP13            | BUCK2_SW    | BUCK2 switcher               |
| TP14            | BUCK2       | BUCK2 DC/DC regulator output |
| TP19            | GND         | Ground                       |
| TP20            | RSTb        | Reset                        |
| TP21            | INTb        | Interruption                 |
| TP22            | FS0b        | Fail-safe output             |
| T26             | PGOOD       | Power GOOD                   |

### 4.3.5 Jumpers

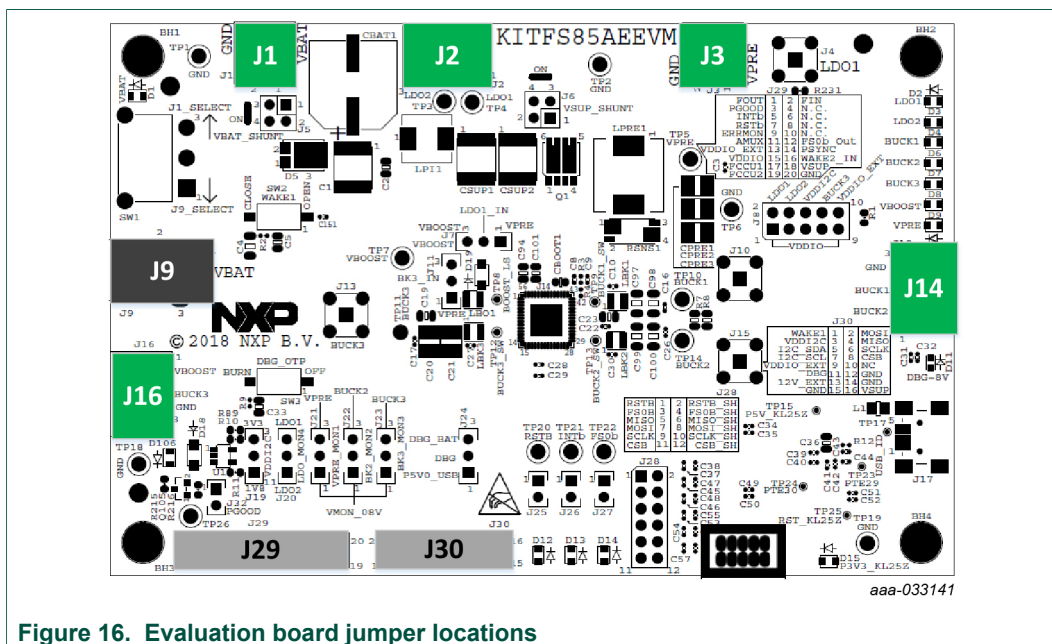


Figure 16. Evaluation board jumper locations

Table 12. Evaluation board jumper descriptions

| Name | Function        | Pin number | Jumper/pin function                                    |
|------|-----------------|------------|--------------------------------------------------------|
| J5   | VBAT shunt      | 1–2        | Shunt switch SW1 for current > 5.0 A                   |
|      |                 | 3–4        | Shunt switch SW1 for current > 5.0 A                   |
| J6   | VSUP shunt      | 1–2        | For current measurement (insert amperemeter)           |
|      |                 | 3–4        | For current measurement (insert amperemeter)           |
| J7   | LDO1 input      | 1–2        | LDO1_IN connected to VPRE                              |
|      |                 | 2–3        | LDO1_IN connected to VBOOST                            |
| J8   | VDDIO selection | 1–2        | VDDIO tied to LDO1                                     |
|      |                 | 3–4        | VDDIO tied to LDO2                                     |
|      |                 | 5–6        | VDDIO tied to VDDI2C (provided by external regulators) |
|      |                 | 7–8        | VDDIO tied to BUCK3                                    |
|      |                 | 9–10       | VDDIO tied to VDDIO external                           |
| J9   | VBAT Jack       | Jack       | Used for VBAT supply using jack connector              |
| J11  | BUCK3 input     | 1–2        | BUCK_INQ tied to VPRE                                  |
|      |                 | 2–3        | BUCK_INQ tied to VBOOST                                |
| J20  | VMON4           | 1–2        | VMON4 tied to LDO2                                     |
|      |                 | 2–3        | VMON4 tied to LDO1                                     |
| J21  | VMON1           | 1–2        | VMON1 tied to 0.8 V                                    |
|      |                 | 2–3        | VMON1 tied to VPRE                                     |
| J22  | VMON2           | 1–2        | VMON2 tied to 0.8 V                                    |
|      |                 | 2–3        | VMON2 tied to BUCK2                                    |
| J23  | VMON3           | 1–2        | VMON3 tied to 0.8 V                                    |
|      |                 | 2–3        | VMON3 tied to BUCK3                                    |



| Name | Function | Pin number | Jumper/pin function                                                                |
|------|----------|------------|------------------------------------------------------------------------------------|
| J24  | Debug    | 1-2        | Debug pin tied to P5V0_USB (5.0 V provided by USB connector)                       |
|      |          | 2-3        | Debug pin tied to VBAT (through external protection)<br>Do not use for OTP burning |
| J25  | RSTB     | 1-2        | Reset LED<br>Enabled when jumper is plugged                                        |
| J26  | INTB     | 1-2        | Interrupt LED<br>Enabled when jumper is plugged                                    |
| J27  | FS0B     | 1-2        | FS0B LED<br>Enabled when jumper is plugged                                         |
| J29  | —        | —          | —                                                                                  |
| J30  | —        | —          | —                                                                                  |
| J31  | —        | —          | Use only during board manufacturing                                                |
| J32  | PGOOD    | 1-2        | PGOOD LED<br>Enabled when jumper is plugged                                        |

#### 4.3.6 Switches

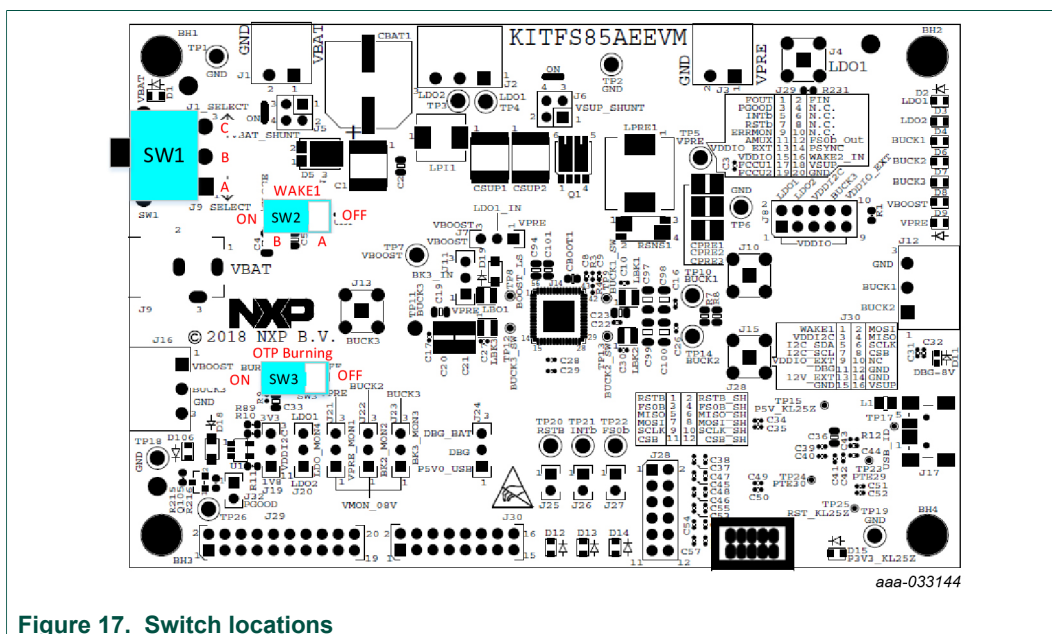


Figure 17. Switch locations

Table 13. SW3

| Position | Function            | Description                                                                    |
|----------|---------------------|--------------------------------------------------------------------------------|
| RIGHT    | OTP programming Off | OTP burning not possible                                                       |
| LEFT     | OTP programming On  | 8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state) |



Table 14. SW2

| Position | Function     | Description                                 |
|----------|--------------|---------------------------------------------|
| OFF      | WAKE1 open   | Wake1 pin not connected to V <sub>SUP</sub> |
| ON       | WAKE1 closed | Wake1 pin connected to V <sub>SUP</sub>     |

Table 15. SW1

| Position | Function | Description        |
|----------|----------|--------------------|
| TOP      | VBAT On  | VBAT from J1       |
| MIDDLE   | VBAT Off | Board not supplied |
| BOTTOM   | VBAT On  | VBAT from J9       |

## 4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85AEEVM evaluation board are available at <http://www.nxp.com/KITFS85AEEVM>.

# 5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

1. Install the appropriate Java SE Runtime Environment (JRE).
2. Install Windows 7 FlexGUI driver.
3. Install FlexGUI software package.

## 5.1 Installing the Java JRE

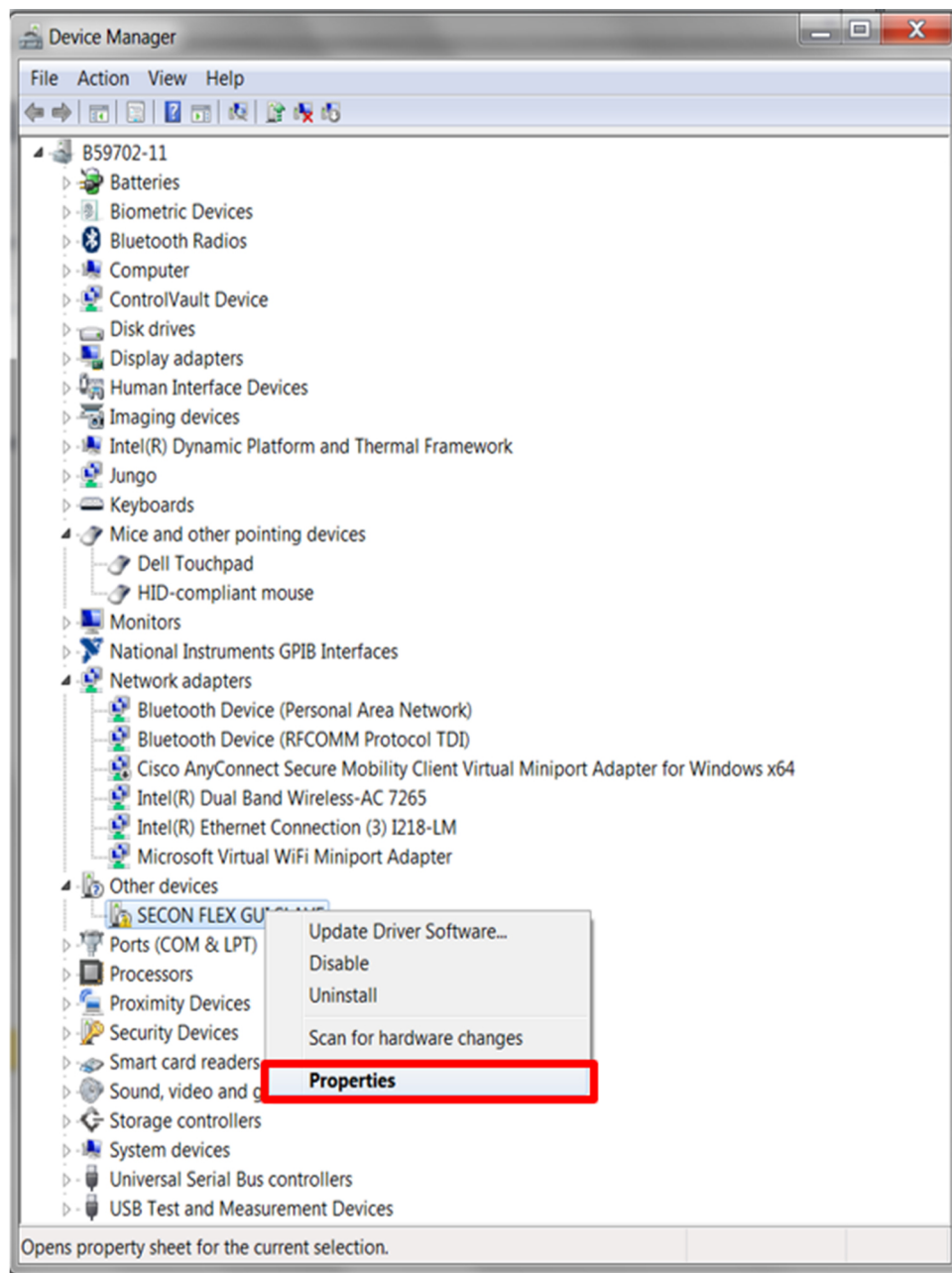
1. Download Java JRE (Java SE Runtime Environment), available at <http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html> (8u162 or newer).
2. Open the installer and follow the installation instructions.
3. Following the successful installation, restart the computer.

## 5.2 Installing Windows 7 FlexGUI driver

On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

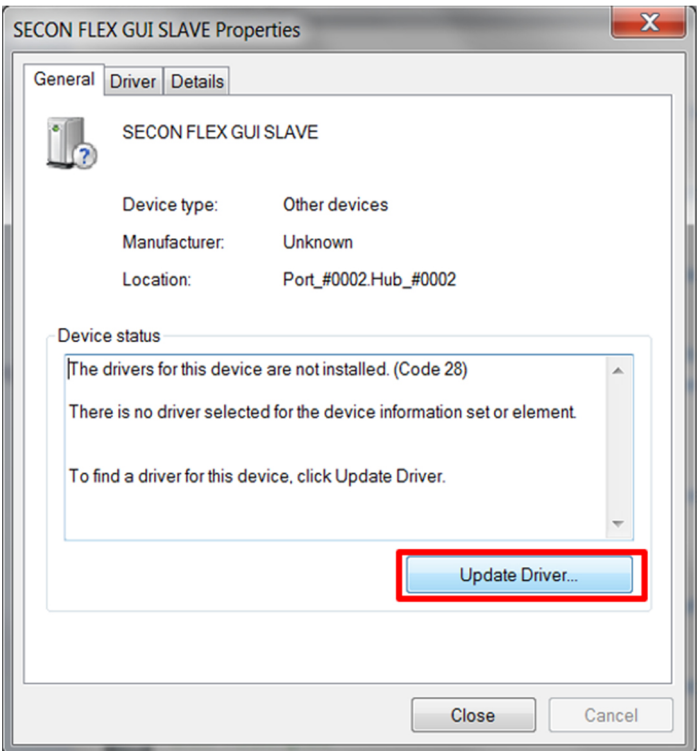
**Note:** On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

1. Connect the kit to the computer as described in [Section 6 "Configuring the hardware for startup"](#)
2. On the Windows PC, open the **Device Manager**.
3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.



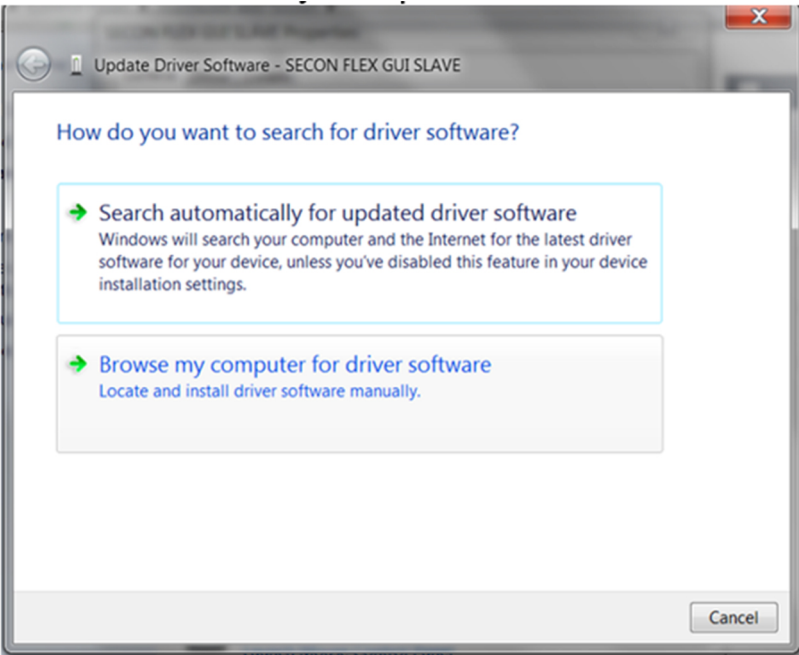
aaa-031982

4. In the **SECON FLEX GUI SLAVE Properties** window, click **Update Driver**.



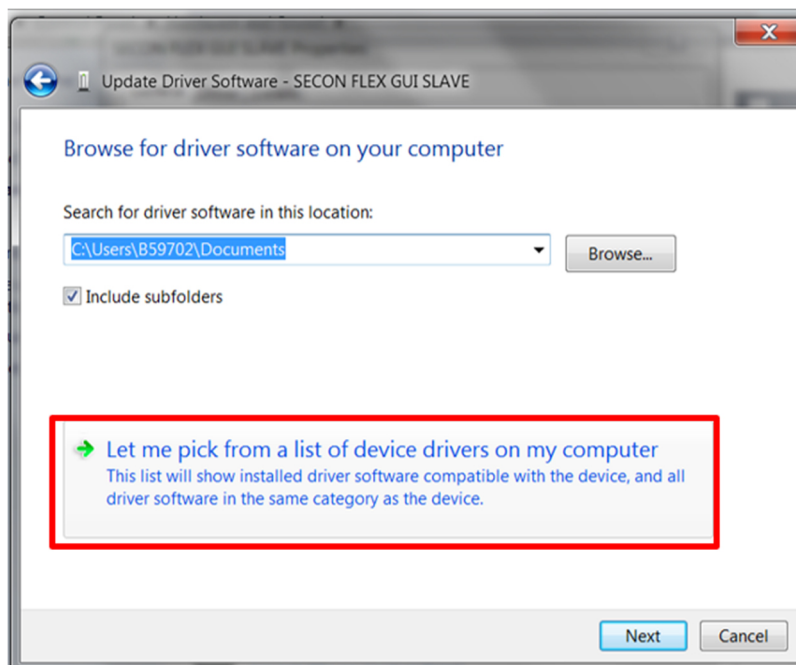
aaa-031983

5. in the **Update Software Driver** window, select **Browse my computer for driver software**.



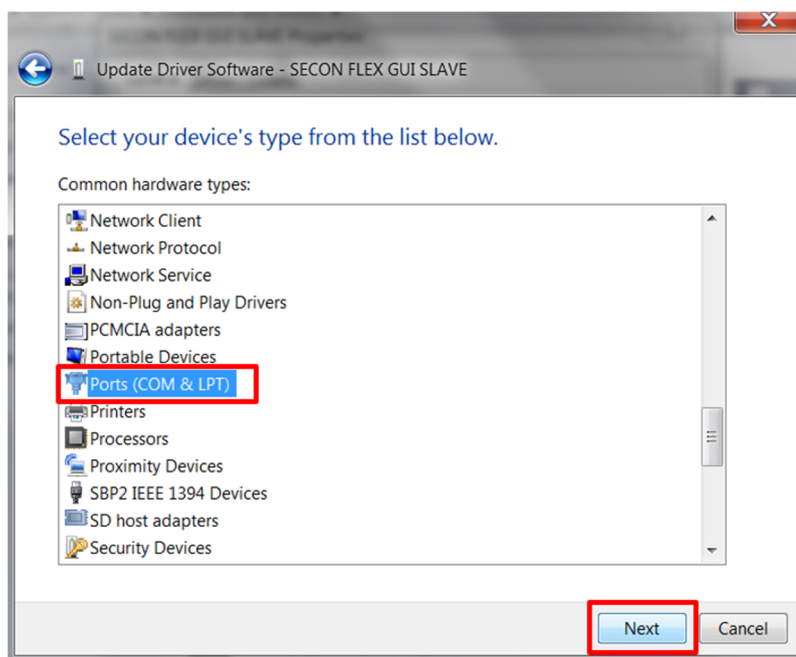
aaa-031984

6. Select **Let me pick from a list of device drivers on my computer**, and then click **Next**.



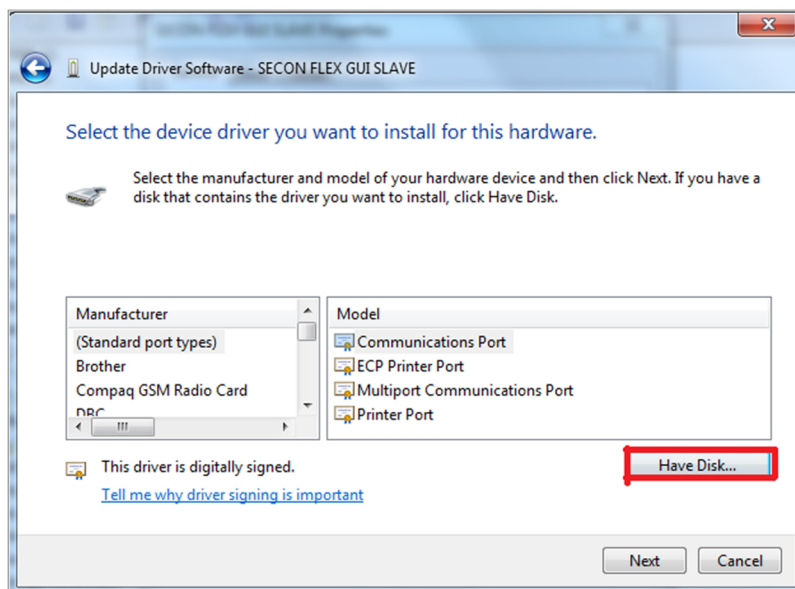
aaa-031985

7. Select **Ports (COM & LPT)** from the list, and then click **Next**.



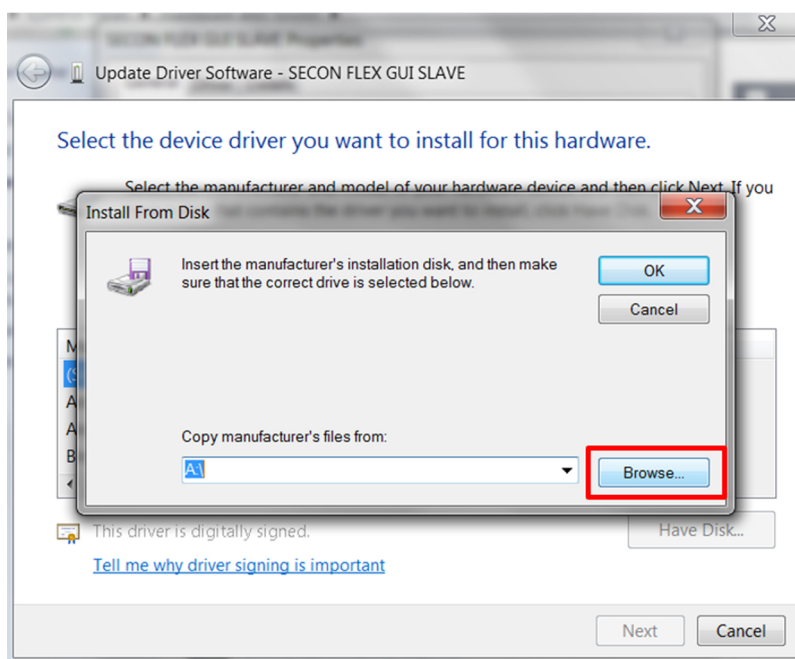
aaa-031986

8. Click **Have Disk**.



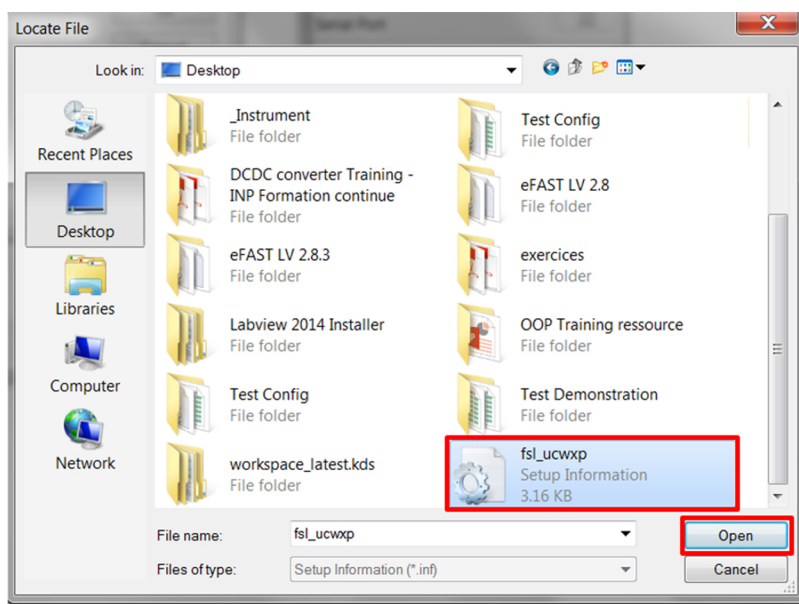
aaa-031987

9. Click **Browse**.



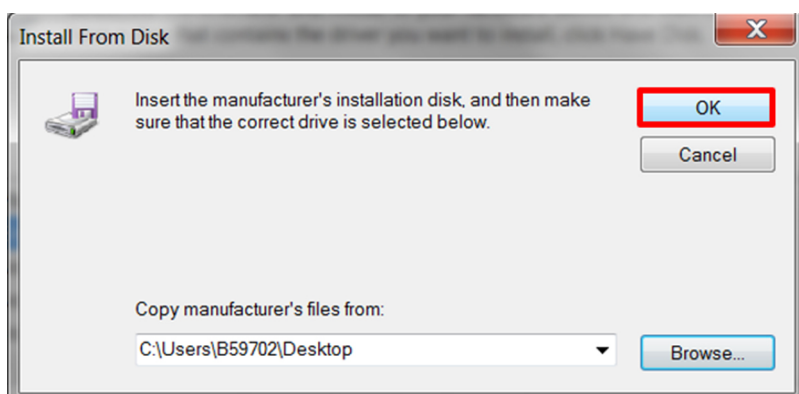
aaa-031988

10. In the **Locate File** window, locate and select **fsl\_ucwxp**, and then click **Open**.



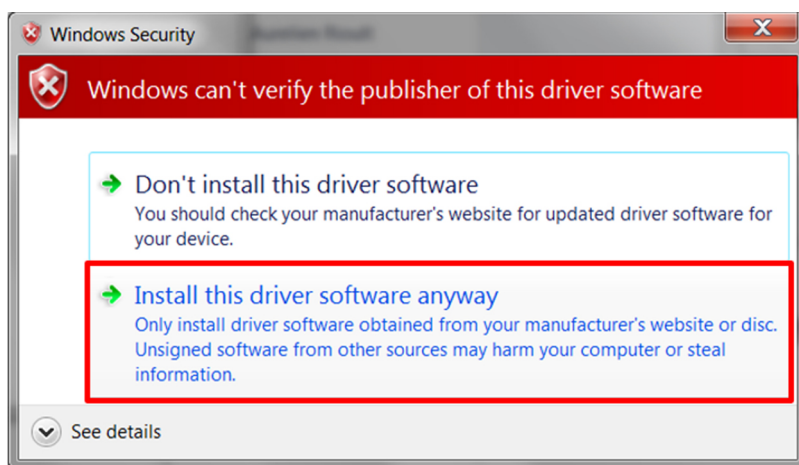
aaa-031989

11. In the **Install from Disk** window, click **OK**.

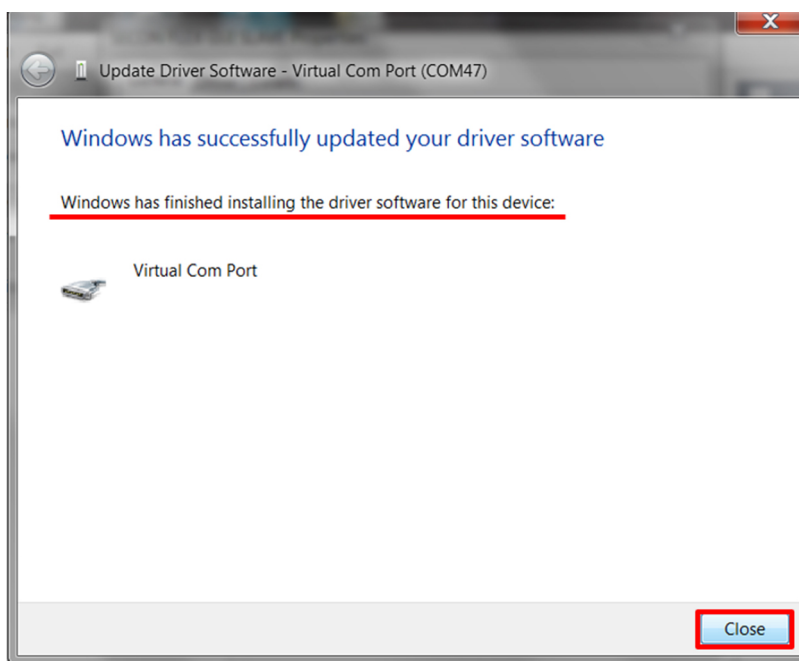


aaa-031990

12. If prompted, in the **Windows Security** window, click **Select this driver software anyway**.

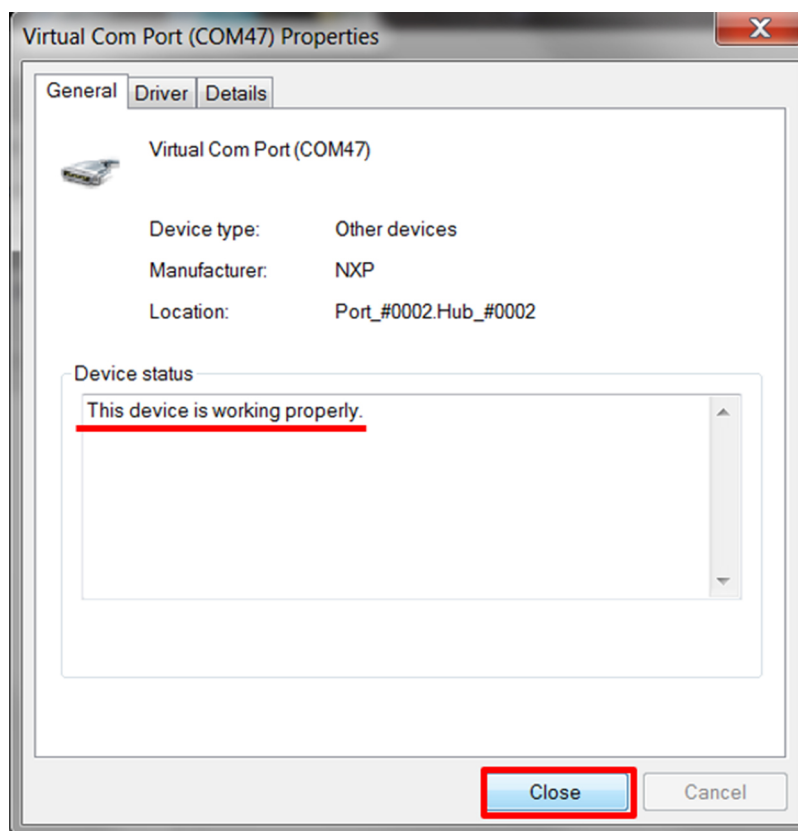


13. Close the window when the installation is complete.



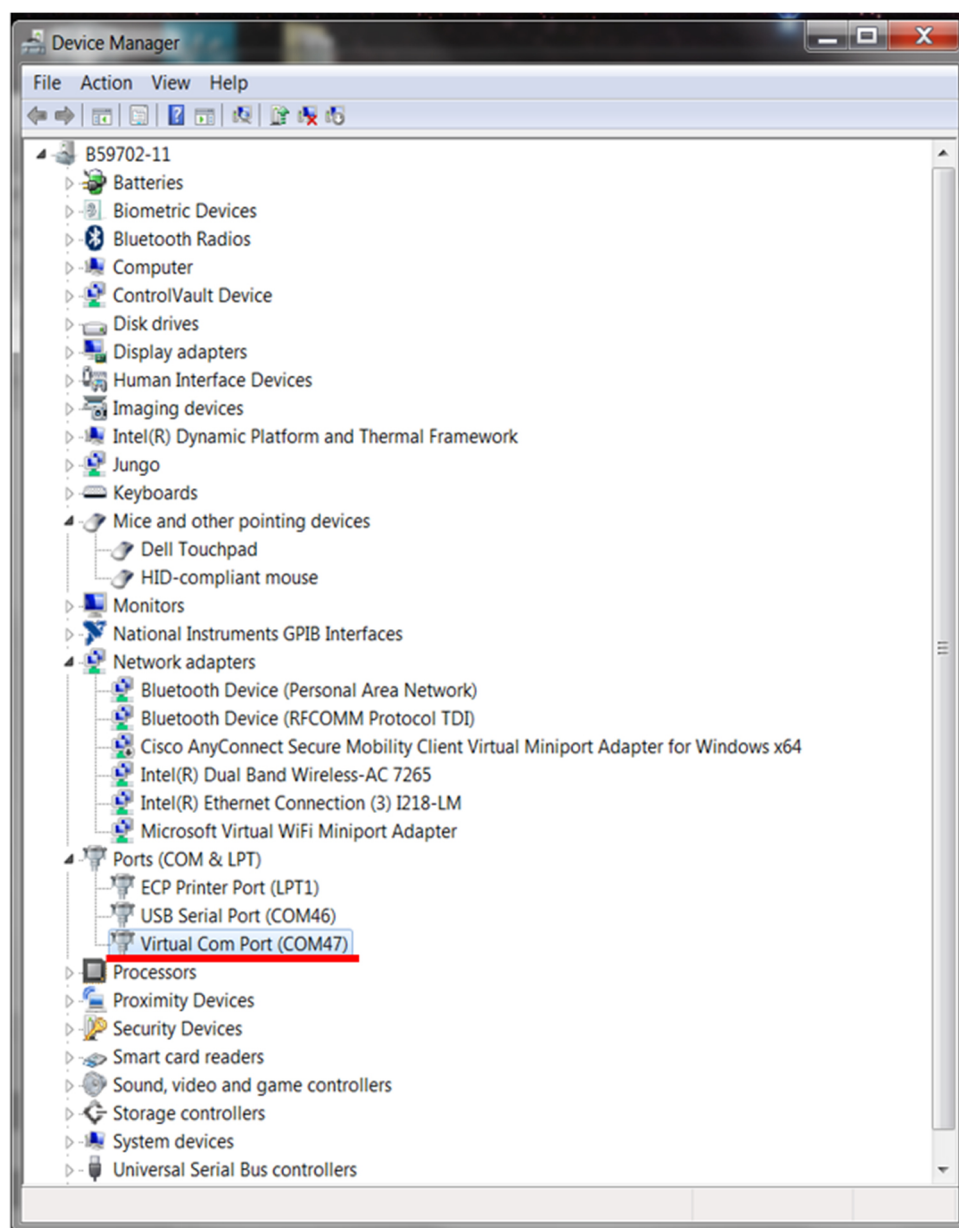
14. In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.





aaa-031993

The Virtual Com Port appears in the Device Manager window.



aaa-031994

### 5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
2. Download the latest FlexGUI (32-bit or 64-bit) version, available at <http://www.nxp.com/KITFS85AEEVM>.
3. Extract all the files to a desired location on your PC.  
FlexGUI is started by running the batch file, `bin\flexgui-app-fs85.bat`.

6 Configuring the hardware for startup

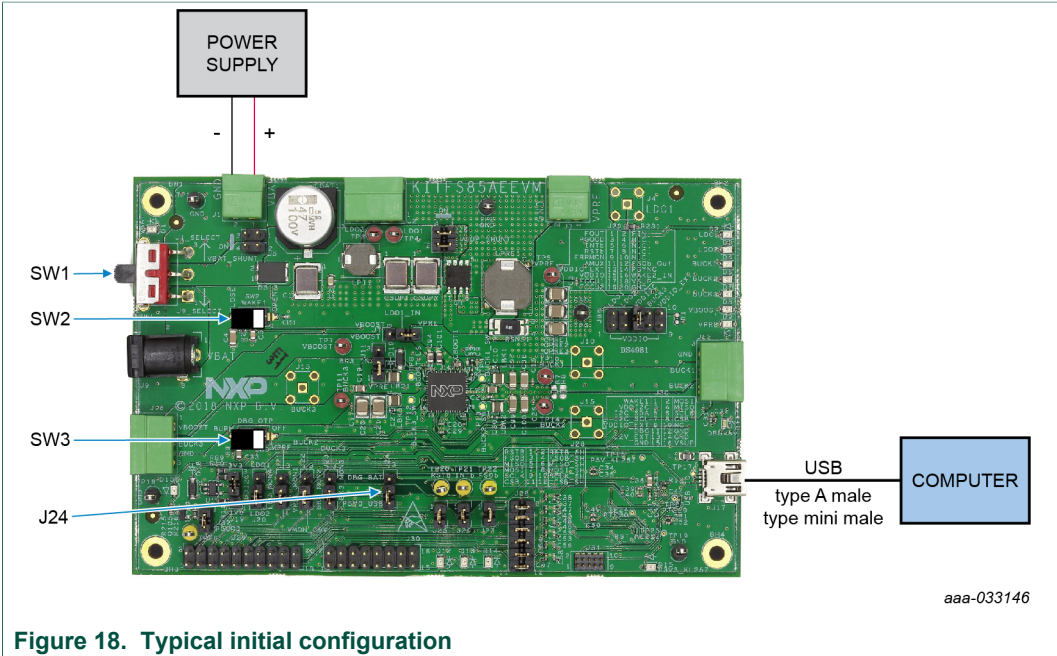


Figure 18. Typical initial configuration

Figure 18 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

To configure the hardware and workstation as illustrated in Figure 18, complete the following procedure:

- 1. Install jumpers for the configuration.

Table 16. Jumper configuration

| Jumper | Configuration                                       |
|--------|-----------------------------------------------------|
| J24    | connect 1-2 (connect 5.0 V on DBG pin from the USB) |

- 2. Configure switches for the configuration

Table 17. Switch configuration

| Switch | Configuration              |
|--------|----------------------------|
| SW1    | middle position (VBAT off) |
| SW2    | open (WAKE1)               |
| SW3    | open (OTP programming off) |

- 3. Connect the Windows PC USB port to the KITFS85AEEVM development board using the provided USB 2.0 cable.  
Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITFS85AEEVM VBAT Phoenix connector (J1).
- 4. Turn on the power supply.
- 5. Close SW2.

**Note:** At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J24 jumper is removed.

## 7 Using the KITFS85AEEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground.
- Debug mode is set by setting DBG voltage to 5.0 V.

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See [Section 4.2.1 "OTP and mirrors registers"](#) and [Section 8.3 "Working with the Script editor"](#) to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

### 7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85\_FS84\_OTP\_Config.xlsx*. This file allows configuring the device for parameters controlled by the the main state machine and the fail-safe state machine.

**Note:** You can avoid this step by using a trial script (*FS85\_UG\_Config.txt*) available on the website.

To generate the script:

1. Fill data in the **OTP\_conf\_main\_reg** sheet.

| MAIN OTP_REGISTERS |       |                |            |                  |               |            |             |            |             |          |          |
|--------------------|-------|----------------|------------|------------------|---------------|------------|-------------|------------|-------------|----------|----------|
| Register Name      | DDRES | BIT7           | BIT6       | BIT5             | BIT4          | BIT3       | BIT2        | BIT1       | BIT0        | Data_Bin | Data_Hex |
| OTP_CFG_VPRE_1     | 14    | -              | -          | -                | -             | VPRE[V5:0] | -           | -          | -           | 00100000 | 0x20     |
| OTP_CFG_VPRE_2     | 15    | 0              | 0          | -                | -             | VPRES[S:0] | -           | -          | -           | 00000011 | 0x07     |
| OTP_CFG_VPRE_3     | 16    | -              | VPRE[LM:0] | -                | VPRETOFF[1:0] | -          | VPRES[LS:0] | -          | VPRES[PH:0] | 10101100 | 0xAC     |
| OTP_CFG_BOOST_1    | 17    | -              | 10 - 120mV | -                | VPRE MODE     | Reserved   | VPRES[LS:0] | -          | VPRES[PH:0] | 00001101 | 0x0D     |
| OTP_CFG_BOOST_2    | 18    | BOOSTEN        | -          | VBSTCONTIME[1:0] | -             | VBST[SC:0] | -           | -          | -           | 10001100 | 0x8C     |
| OTP_CFG_BOOST_3    | 19    | VBSTRCOMP[1:0] | -          | VBSTCCOMP[1:0]   | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK1_1A   | 1A    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK1_1B   | 1B    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK2_1C   | 1C    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK2_1D   | 1D    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK2_1E   | 1E    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_BUCK2_1F   | 1F    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_LDO_1      | 20    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_SEQ_1      | 21    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_SEQ_2      | 22    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_SEQ_3      | 23    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CLOCK_1    | 24    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CLOCK_2    | 25    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CLOCK_3    | 26    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CLOCK_4    | 27    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_SM_1       | 28    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_SM_2       | 29    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_VSUP_U_1   | 2A    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_IC_1       | 2B    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_OV_1       | 2C    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_DEVID_1    | 2D    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CRC_LS_1   | 2E    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |
| OTP_CFG_CRC_MS_1   | 2F    | -              | -          | -                | -             | VBST[LM:0] | -           | VBST[SP:0] | -           | 00001101 | 0x0D     |

Figure 19. OTP\_conf\_main\_reg spreadsheet example

- Fill data in the OTP\_conf\_failsafe\_reg sheet.

| FAIL-SAFE OTP_REGISTERS |         |      |      |      |      |              |      |      |      |          |          |
|-------------------------|---------|------|------|------|------|--------------|------|------|------|----------|----------|
| Register Name           | ADDRESS | BIT7 | BIT6 | BIT5 | BIT4 | BIT3         | BIT2 | BIT1 | BIT0 | Data_Bin | Data_Hex |
| OTP_CFG_UVUV_1          | 0A      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 10001000 | 0x80     |
| OTP_CFG_UVUV_2          | 0B      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_3          | 0C      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_4          | 0D      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_5          | 0E      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_6          | 0F      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_7          | 10      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_UVUV_8          | 11      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_PGOOD           | 12      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_ABIST1          | 13      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_ASIL            | 14      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_IC_2            | 15      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_DGLT_DUR_1      | 16      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_DGLT_DUR_2      | 17      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_S1_CRC_LSB      | 18      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |
| OTP_CFG_S1_CRC_MSB      | 19      | -    | -    | -    | -    | VCORE_V[7:0] | -    | -    | -    | 11111111 | 0xFF     |

Figure 20. OTP\_conf\_failsafe\_reg spreadsheet example

- See the OTP\_conf\_summary sheet to review the complete configuration (main and fail-safe).

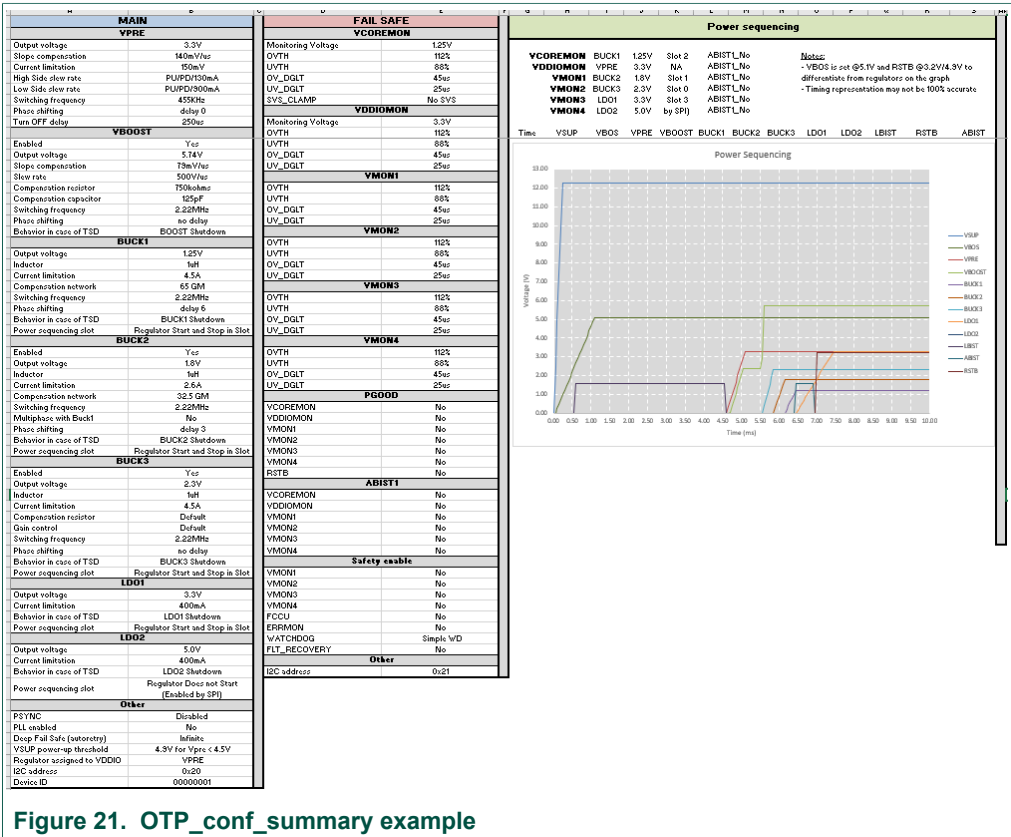


Figure 21. OTP\_conf\_summary example

4. Generate script in the **OTP\_conf\_file\_generation** sheet.
- Once the configuration is ready, the user can generate the script file. Go to **OTP\_conf\_file\_generation**, enter the path in the **File repository**, and then click **Write\_OTP\_File\_GUI**.

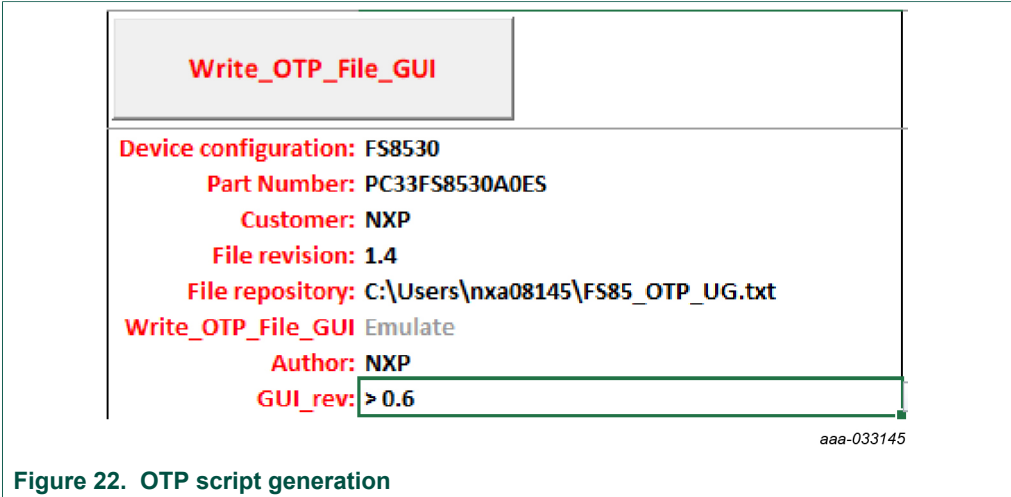


Figure 22. OTP script generation

7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP

emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

1. Configure the hardware. See [Section 6 "Configuring the hardware for startup"](#).
2. Launch the FlexGUI software.
3. Switch to Debug mode:
  - a. Place SW1 in TOP direction (VBAT switched On).
  - b. Close SW2 (WAKE1).
 While in Debug mode, all regulators are turned Off.
4. Load the mirror registers to work in OTP emulation mode. See [Section 8.3 "Working with the Script editor"](#).
5. Unplug jumper J24 1-2 to start the device with the mirror configuration setting.
  - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
  - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration is used, if it exists.
  - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD\_Answer, the WD does not start and regulators do not stay alive. Also, as long as Debug mode is not exited by writing FS\_STATES:[DBG\_EXIT] bit to 1, the FS0B pin cannot be released.

6. Use the FlexGUI software to evaluate the device configured. See [Section 8 "Using FlexGUI"](#).

### 7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring and releasing FS0B

The following script can be used to:

- Disable the WD (simple WD configuration is used here).
- Disable the FCCU monitoring.  
On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO, which is detected as error phase by default. Disabling the FCCU by SPI/I2C avoids safety issue at startup.
- Close the initialization phase.
- Exit the Debug mode.
- Release FS0B pin. This is valid only if WD is activated in OTP.  
Seven good consecutive WD answers are required to have the FLT\_ERR\_CNTR back to 0. This is one of the conditions to allow FS0B release.

**Table 18. FS85 starting sequence example**

| Step | Register name        | Value  | Description                                                                                            |
|------|----------------------|--------|--------------------------------------------------------------------------------------------------------|
| 1    | FS_WD_WINDOW         | 0x0200 | WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled                                                            |
| 2    | FS_NOT_WD_WINDOW     | 0xF50F | NOT of FS_WD_WINDOW                                                                                    |
| 3    | FS_I_SAFE_INPUTS     | 0x51C6 | FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair<br>FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault |
| 4    | FS_I_NOT_SAFE_INPUTS | 0xAC18 | NOT of FS_I_SAFE_INPUTS                                                                                |
| 5    | FS_WD_ANSWER         | 0x5AB2 | 1st good WD answer (for simple WD selection in OTP)<br>Close the initialization phase                  |
| 6    | FS_STATES            | 0x4000 | DBG_EXIT[0]=1 => Exit Debug mode                                                                       |

| Step | Register name     | Value  | Description                                     |
|------|-------------------|--------|-------------------------------------------------|
| 7    | FS_WD_ANSWER      | 0x5AB2 | 2nd good WD answer                              |
| 8    | FS_WD_ANSWER      | 0x5AB2 | 3rd good WD answer                              |
| 9    | FS_WD_ANSWER      | 0x5AB2 | 4th good WD answer                              |
| 10   | FS_WD_ANSWER      | 0x5AB2 | 5th good WD answer                              |
| 11   | FS_WD_ANSWER      | 0x5AB2 | 6th good WD answer                              |
| 12   | FS_WD_ANSWER      | 0x5AB2 | 7th good WD answer                              |
| 13   | FS_RELEASE_FS0B   | 0xB2A5 | FS0B pin released (pulled to high level)        |
| 14   | MFLAG2            | 0x40F1 | Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG |
| 15   | FS_OVUVREG_STATUS | 0x4550 | Clear UV status flags                           |

This sequence can be sent using a script built with FlexGUI. See [Section 8.3.2 "Script sequence files"](#).

### 7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see [Section 4.2.1 "OTP and mirrors registers"](#)). The programming steps are exactly the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See [Section 8.4.8 "OTP programming"](#). Follow the instructions on the screen to proceed.

## 8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see [Section 7.2 "Working in OTP emulation mode"](#)).

**Note:** It is recommended to use the latest version of FlexGUI.

### 8.1 Starting the FlexGUI application

After FlexGUI is launched with the `flexgui-app.bat` file, the FlexGUI launcher displays available kits.

Communication bus, SPI or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see [Section 8.2 "Establishing the connection between FlexGUI and the hardware"](#)).



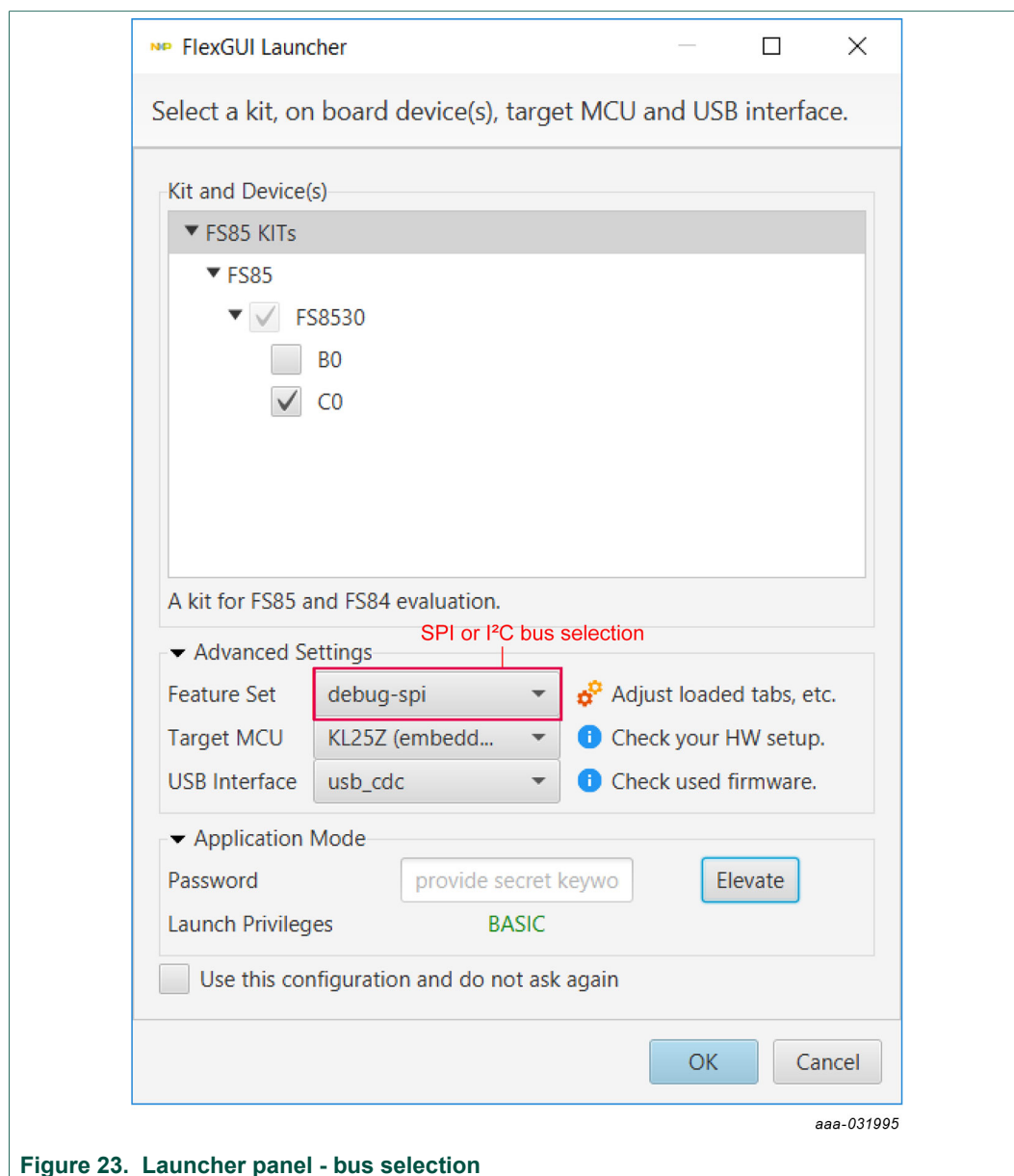


Figure 23. Launcher panel - bus selection

When the configuration is selected, click **OK**.

## 8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click **Start** to enable the connection.

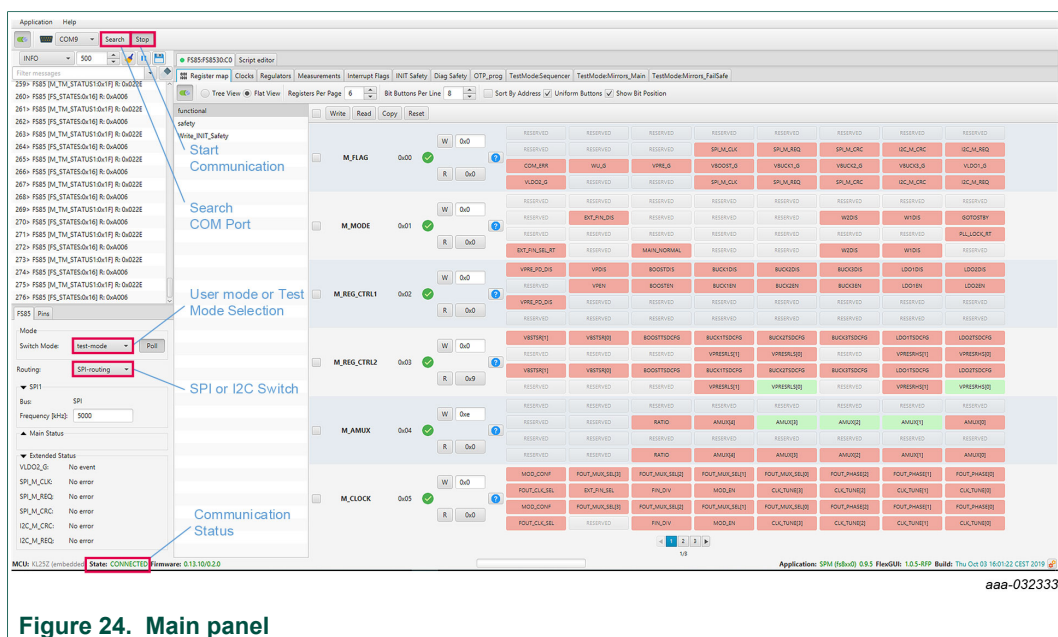


Figure 24. Main panel

Figure 24 shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (e.g.  $V_{SUP}$  is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode

- Debug mode :
  - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for fail-safe.
  - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
  - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

The current operating mode is refreshed periodically by default at FlexGUI startup. This automatic refresh can be disabled by disabling Poll button as shown in Figure 25.

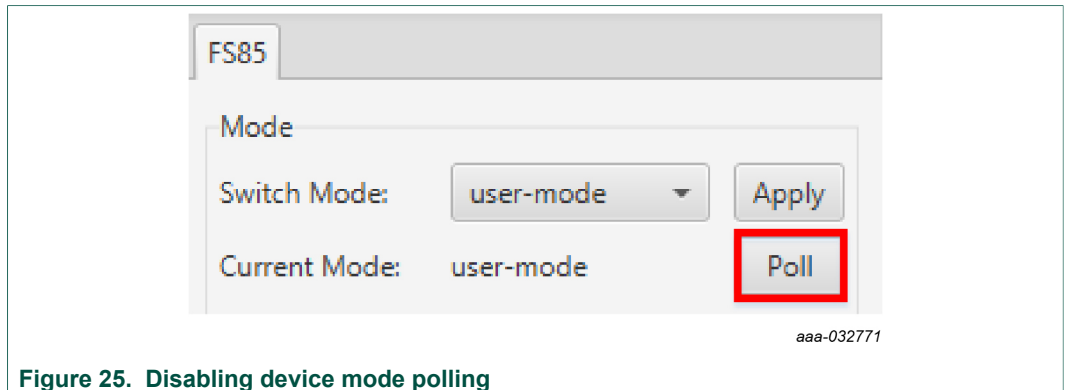


Figure 25. Disabling device mode polling

To move from one mode to the other, select the mode with switch mode drop-down button and click **Apply** to validate. At this time, the current mode is updated at the condition that Poll button is enabled.

### 8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

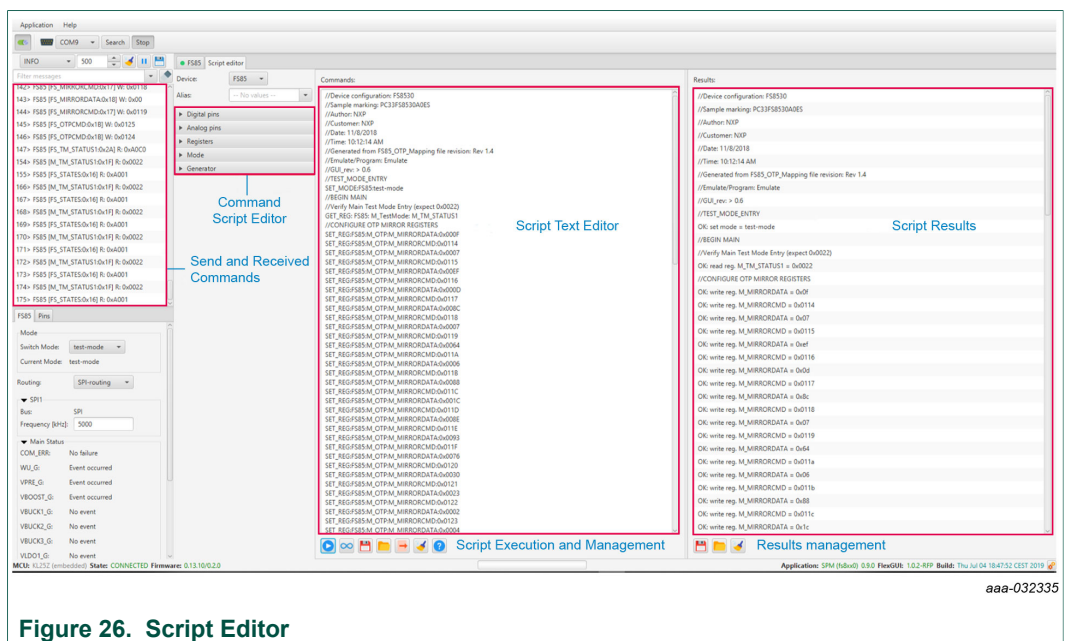


Figure 26. Script Editor

The main subareas of this panel are:

- **Send and receive command:** displays a summary of commands sent and received from the device
- **Command script editor:** builds commands to be sent to the device
- **Script text editor:** sends a sequence of register configurations from a text file or from command edited directly in this area
- **Script results:** displays result status of each command sent to the device

### 8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

#### List of commands

- **SET\_REG**: sets value of a selected register.
- **READ\_REG**: reads value of a selected register.
- **SET\_DPIN**: sets value of a selected digital pin.
- **GET\_DPIN**: gets value of a selected digital pin.
- **GET\_APIN**: gets value of a selected analog pin. Returned value is in mV.
- **PAUSE**: shows a dialog with user defined message. The script is paused until the user confirms the dialog.
- **EXIT**: stops execution of the script.
- **SET\_MODE**: sets device mode. List of modes depends on a device.

#### Command format

The following table describes command parameters. All parameters are mandatory.

|          | 1st parameter | 2nd parameter | 3rd parameter               | 4th parameter | 5th parameter |
|----------|---------------|---------------|-----------------------------|---------------|---------------|
| SET_REG  | Device        | Reg. set      | Reg. name /<br>Reg. address | Reg. value    | -             |
| GET_REG  | Device        | Reg. set      | Reg. name /<br>Reg. address | -             | -             |
| SET_DPIN | Device        | Pin name      | Dig. pin value              | -             | -             |
| GET_DPIN | Device        | Pin name      | -                           | -             | -             |
| GET_APIN | Device        | Pin name      | -                           | -             | -             |
| PAUSE    | Message       | -             | -                           | -             | -             |
| EXIT     | -             | -             | -                           | -             | -             |

Description of command parameters mentioned in the table above:

- **Device**: device name (alias used in application).
- **Reg. set**: register set name. Register sets allows to associate registers which have similar function.
- **Reg. name**: register name as defined in datasheet.
- **Reg. address**: register address in decimal or hexadecimal (with 0x prefix) format.
- **Reg. value**: register value in decimal or hexadecimal (with 0x prefix) format.
- **Pin name**: name of digital or analog pin as defined in device datasheet.
- **Dig. pin value**: value of digital pin. Allowed strings are 'low' and 'high'.
- **Message**: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of parameters.
- **Mode**: name of a device mode.

[Figure 27](#) shows an example to build a command from the panel.

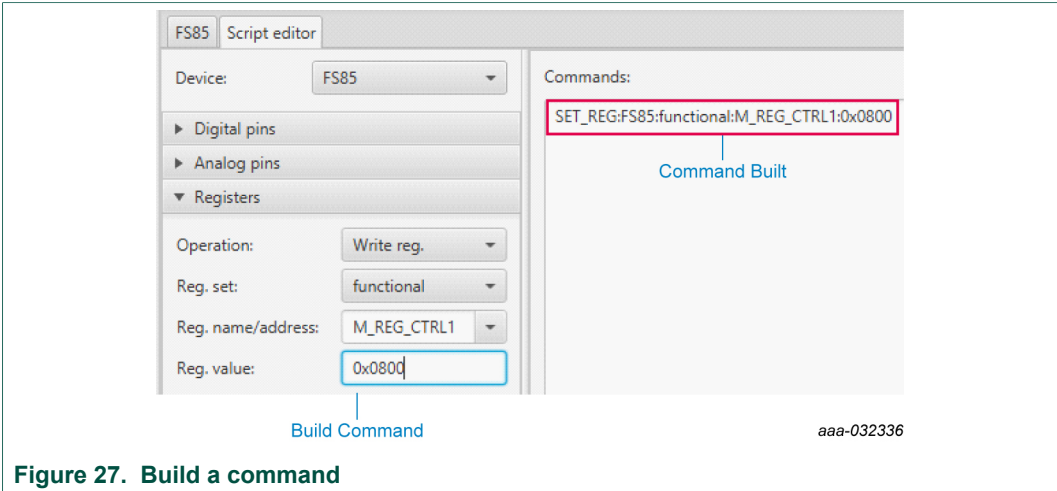


Figure 27. Build a command

The value 0x0800 is sent to the register M\_REG\_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see [Figure 28](#)).

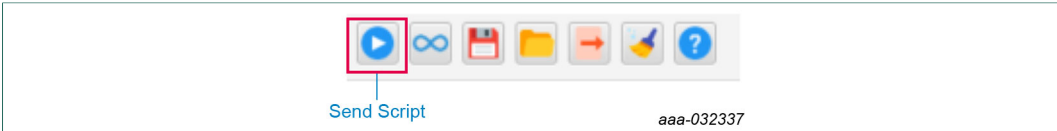


Figure 28. Send script

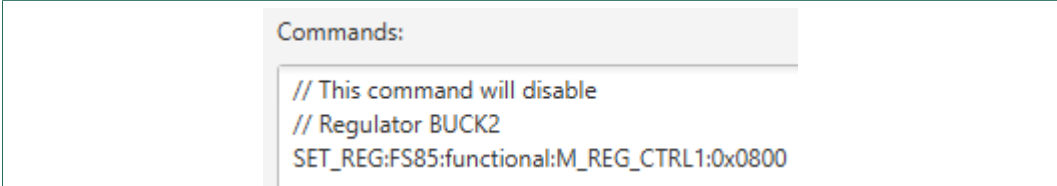


Figure 29. Correct format

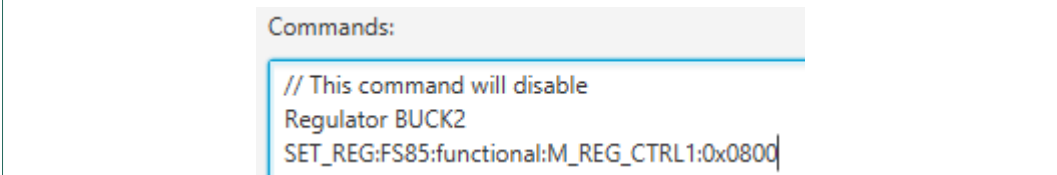


Figure 30. Wrong format (“//” missing in second line)

### 8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:Write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_STATES:0x4000
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_RELEASE_FS0B:0xB2A5
```

**Note:** Comments can be added with a // prefix.

## 8.4 Understanding the FS85 workspace

The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- Register map
- Clocks
- Regulators
- Measurements
- Interrupt flags
- INIT safety
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

### 8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

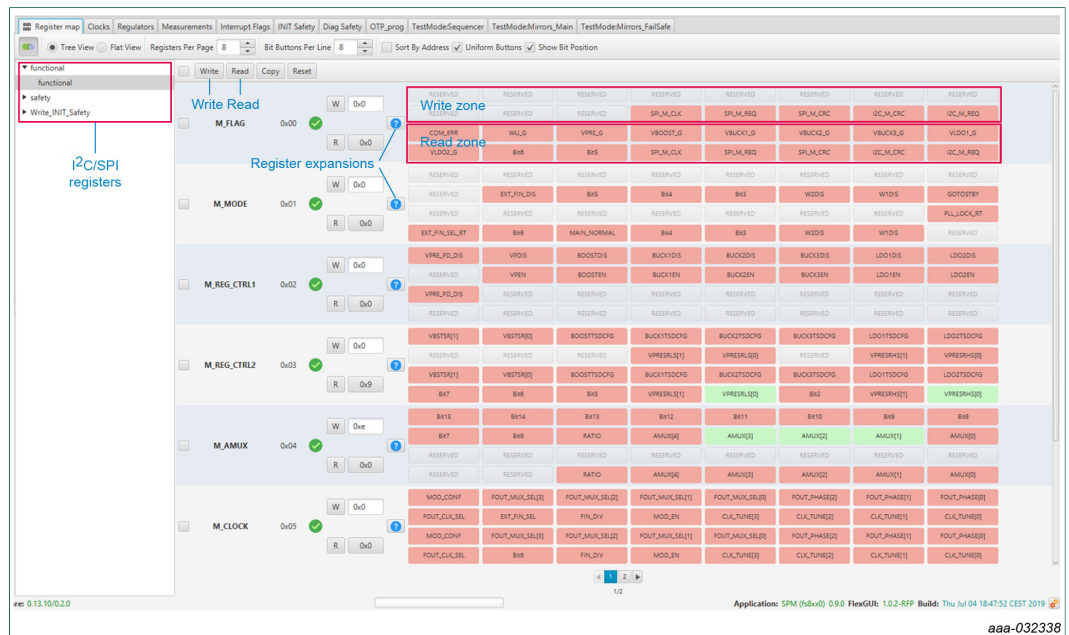


Figure 31. Register map

- **Register map:** allows access to functional register, safety register and write init register which are accessible only during initialization phase
- **Read:** allows you to read any register either individually or by bank
- **Write:** allows you to write any register either individually or by bank
- **Register expansion:** displays the value of each device parameter

## 8.4.2 Clocks

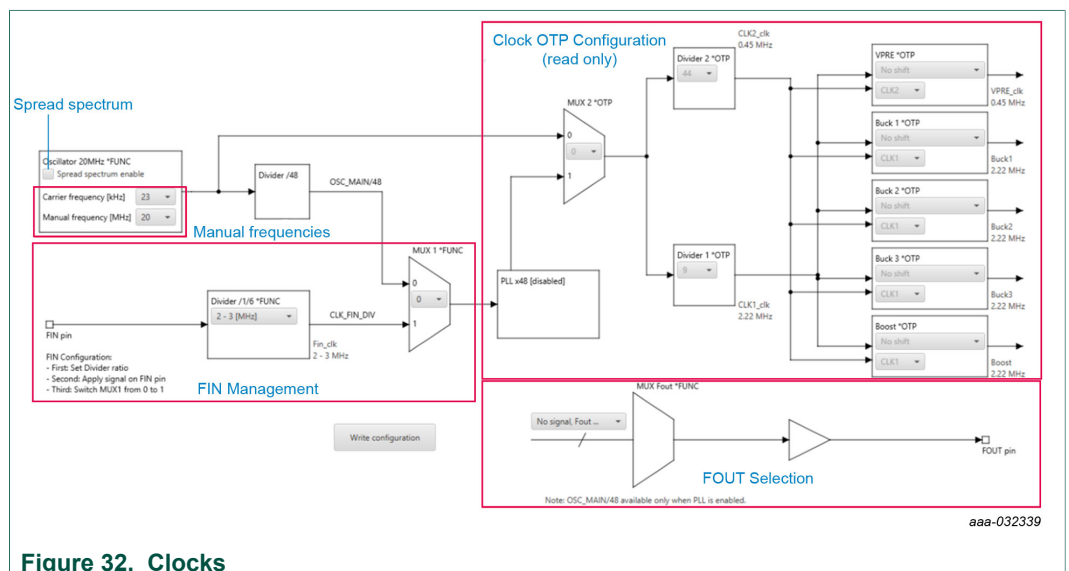


Figure 32. Clocks

This tab allows:

OTP:

- Read current OTP configuration (write operation is not possible). To display the accurate data, the device needs to operate in Test mode.



SPI/I2C:

- Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

### 8.4.3 Regulators

The regulator has two main areas:

- Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

**Low Voltage Regulators**

| LV Buck1                                    | LV Buck2                                    |
|---------------------------------------------|---------------------------------------------|
| State in normal mode: Disable               | State in normal mode: Disable               |
| Behavior in case of TSD: Regulator_Shutdown | Behavior in case of TSD: Regulator_Shutdown |

| LV Buck3                                    | LDO1                                        |
|---------------------------------------------|---------------------------------------------|
| State in normal mode: Disable               | State in normal mode: Disable               |
| Behavior in case of TSD: Regulator_Shutdown | Behavior in case of TSD: Regulator_Shutdown |

| LDO2                                        | VBOOST                                      |
|---------------------------------------------|---------------------------------------------|
| State in normal mode: Disable               | State in normal mode: Disable               |
| Behavior in case of TSD: Regulator_Shutdown | Behavior in case of TSD: Regulator_Shutdown |

Write

**VPRE compensation network calculation**

VPRE [V]

VPRE ILIM [mV]

Switching Frequency [KHz]

Rshunt [mOhm]

Cout [uF]

Lvpri [uH]

Rcomp [KOhm] N/A

Ccomp [nF] N/A

Chf [pF] N/A

Current limit [A] N/A

Slope compensation [mV/us] N/A

Calculate

aaa-032340

Figure 33. Regulators

### 8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary



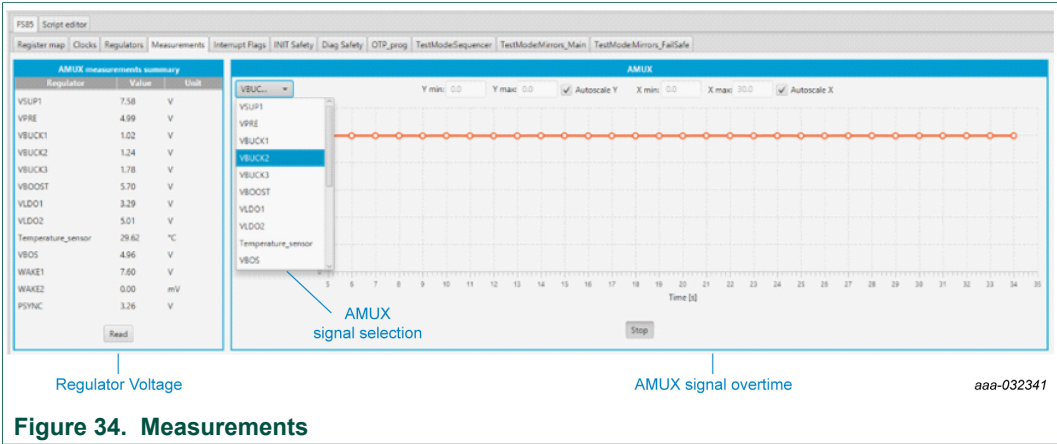


Figure 34. Measurements

8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

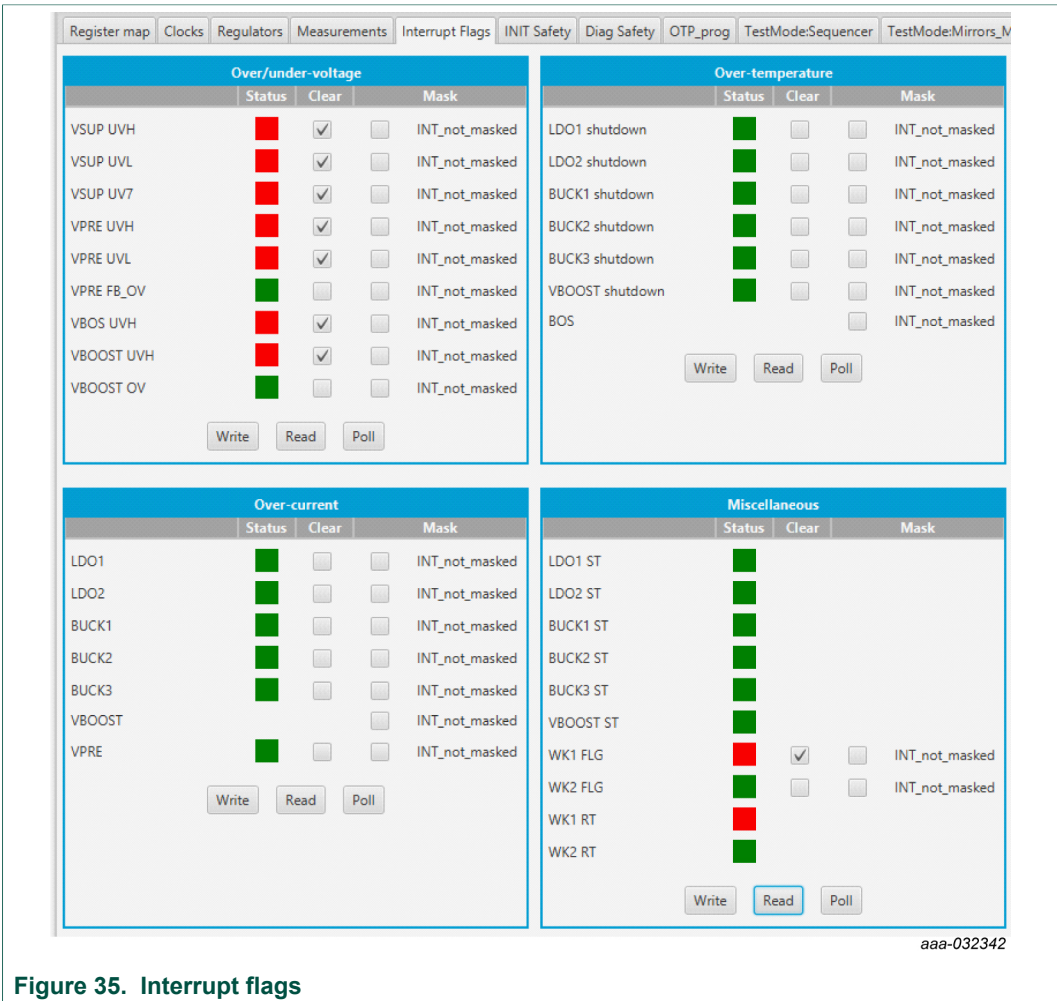


Figure 35. Interrupt flags

8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. Note that the initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

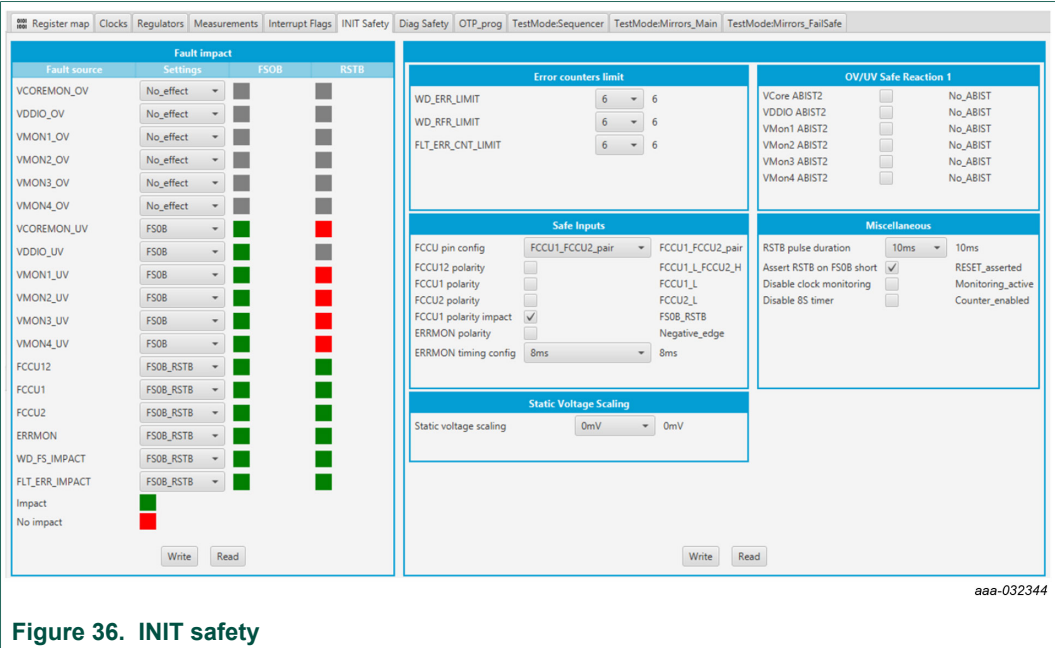
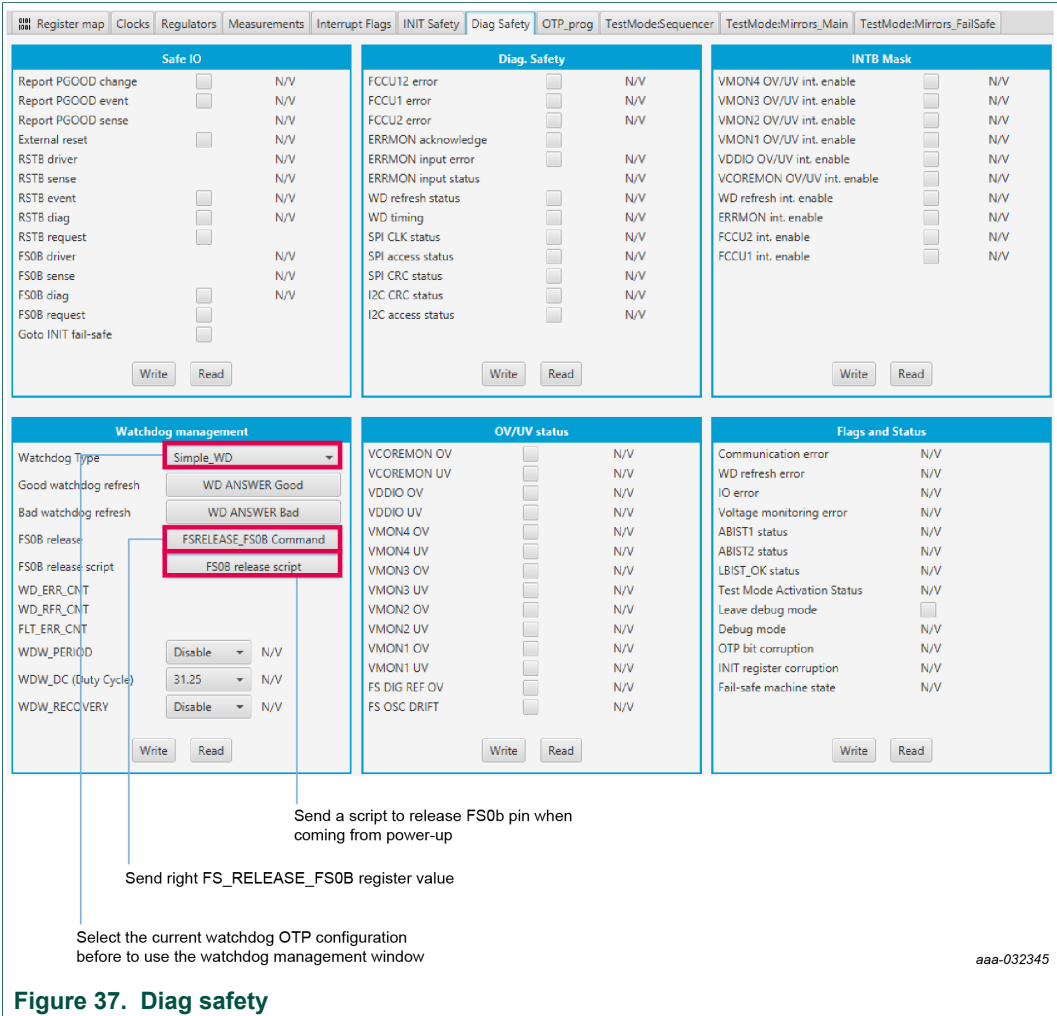


Figure 36. INIT safety

8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the drop-down list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors\_Failsafe and Miscellaneous tabs.



The FS\_Release\_FS0B command calculates and sends the right secure16-bit word to release FS0B.

A simplified way to release FS0B after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0B Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0B.

8.4.8 OTP programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see [Section 7.1 "Generating the OTP configuration file "](#)).

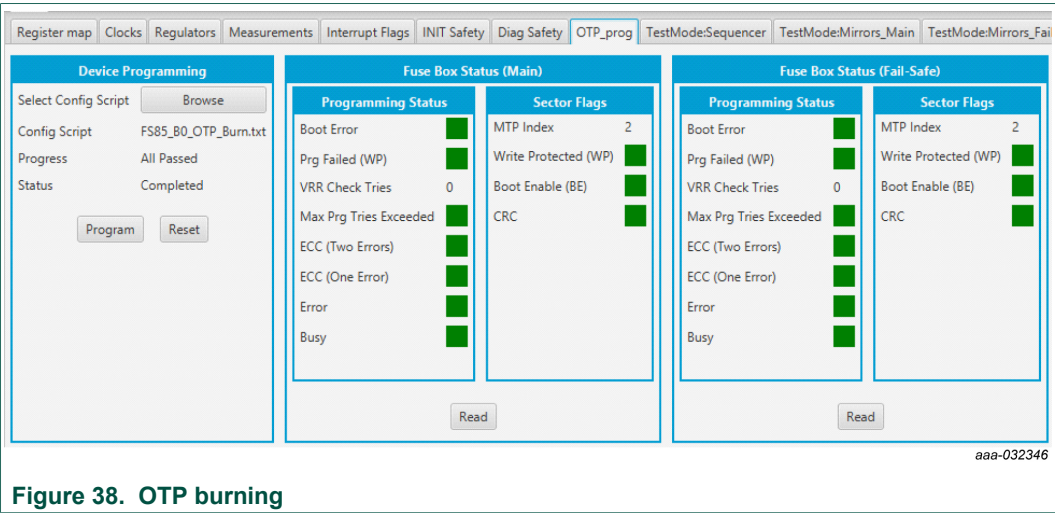


Figure 38. OTP burning

To set up the hardware before OTP burning, see [Section 7.3 "Programming the device with an OTP configuration"](#).

See [Figure 38](#) and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click **Program**.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE and CRC flags are green.

The Sector Flags area provides status [Table 19](#) provides the state of main flags after a read. This helps to determine how many times the part was burned.

Table 19. OTP burning flag status

| OTP burning step               | BE    | WP    | CRC   | MTP Index |
|--------------------------------|-------|-------|-------|-----------|
| OTP not burn<br>Mirrors Empty  | Red   | Red   | Red   | 1         |
| OTP not Burn<br>Mirrors Filled | Red   | Red   | Green | 1         |
| 1                              | Green | Green | Green | 1         |
| 2                              | Green | Green | Green | 2         |
| 3                              | Green | Green | Green | 3         |

Example shown in [Figure 38](#) corresponds to the OTP burning step 2 from [Table 19](#).

To check if a valid OTP configuration is already burned, switch V<sub>BAT</sub> Off, then On, and start the device. The device starts with the OTP configuration.

8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at start up with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.

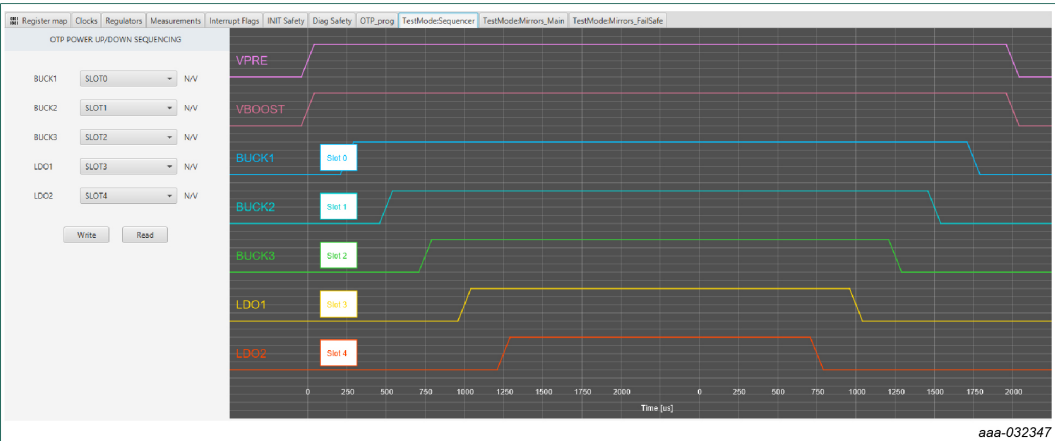


Figure 39. TestMode:Sequencer

Use the drop-down button (see [Figure 40](#)) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.

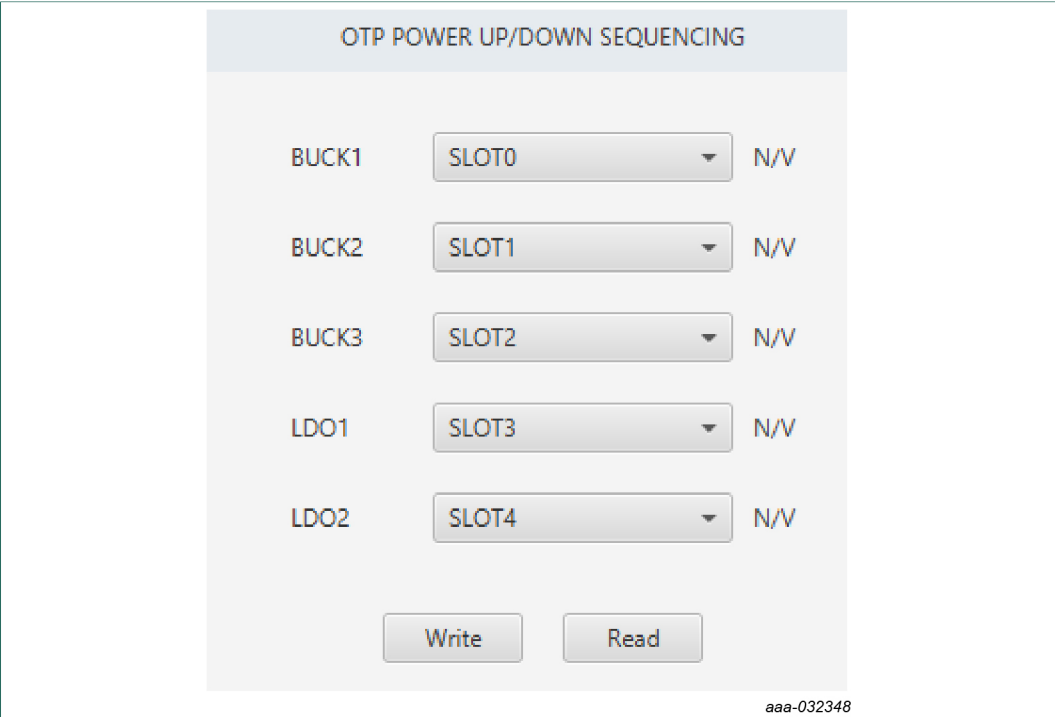


Figure 40. Slot management

8.4.10 TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

The TestModeMirrors\_Main and TestModeMirrors\_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

VPRE mode

Force PWM

Force PWM

Output voltage

17

17

Slope compensation

170mV/us

170mV/us

Current limitation threshold

50mV

50mV

Low Side slew rate control

130mA

130mA

High Side slew rate control

260mA

260mA

VPRE phase (delay) selection

Delay2

Delay2

Delay to turn OFF VPRE at device power down

32ms

32ms

VPRE clock selection

CLK\_DIV1

CLK\_DIV1

Write

Read

BOOST

Output voltage

1

1

BOOST enable

Disabled

Disabled

BOOST minimum ON time

60ms

60ms

VBOOST slope compensation

17

17

Compensation Network Resistor R<sub>comp</sub>

750Kohms

750Kohms

Compensation Network Capacitor C<sub>comp</sub>

1

1

VBOOST current limitation

0

0

VBOOST Low Side slew rate control

1

1

BOOST phase (delay) selection

Delay1

Delay1

BOOST clock selection

CLK\_DIV2

CLK\_DIV2

BOOST shutdown

BOOST shut...

BOOST shut...

Write

Read

LDOs

VLD02 current limitation

400mA

400mA

VLD02 output voltage

1.2V

1.2V

LDO2 sequencing slot

Slot2

Slot2

Regulator behavior in case o...

LDO2 shutdown + ...

LDO2 shutdown + ...

VLD01 current limitation

400mA

400mA

VLD01 output voltage

1.2V

1.2V

LDO1 sequencing slot

Slot1

Slot1

Regulator behavior in case o...

LDO1 shutdown

LDO1 shutdown

Write

Read

BUCK1

VBUCK1 output voltage

17

17

BUCK1 inductor selection

1.5uH

1.5uH

VBUCK1 current limitation

0

0

VBUCK1 & VBUCK2 multiphase operation

Enabled

Enabled

BUCK1 Compensation Network

65GM

65GM

BUCK1 sequencing slot

Slot1

Slot1

BUCK1 phase (delay) selection

Delay2

Delay2

BUCK1 clock selection

CLK\_DIV1

CLK\_DIV1

Regulator behavior in case of TSD

BUCK1 shutdown + ...

BUCK1 shutdown + ...

BUCK1 and BUCK2 Soft start/stop configura...

7.81mV/us

7.81mV/us

Write

Read

BUCK2

VBUCK2 output voltage

17

17

BUCK2 inductor selection

1uH

1uH

BUCK2 enable

Enabled

Enabled

VBUCK2 current limitation

0

0

BUCK2 compensation network

0

0

BUCK2 sequencing slot

Slot2

Slot2

BUCK2 phase (delay) selection

Delay1

Delay1

BUCK2 clock selection

CLK\_DIV1

CLK\_DIV1

Regulator behavior in case of TSD

BUCK2 shutdown

BUCK2 shutdown

Write

Read

BUCK3

VBUCK3 output voltage

2.8V

2.8V

BUCK3 enable

Disabled

Disabled

BUCK3 inductor selection

1uH

1uH

VBUCK3 current limitation

2.6A

2.6A

BUCK3 compensation resistor

Default

Default

BUCK3 gain control

1

1

BUCK3 sequencing slot

Slot1

Slot1

BUCK3 phase (delay) selection

Delay2

Delay2

BUCK3 clock selection

CLK\_DIV1

CLK\_DIV1

Regulator behavior in case of ...

BUCK3 shutdown

BUCK3 shutd...

Soft start/stop configurability

3.47mV/us

3.47mV/us

Write

Read

CLOCK

PLL enable

Disabled

Disabled

Divider 1 setting

Divide8

Divide8

Divider 2 setting

Divide10

Divide10

Write

Read

SM

Deep Fail-safe infinite autoretry enable

Disabled

Disabled

Deep Fail-safe autoretry enable

Disabled

Disabled

Synchronization with 1x FS85 or 1x PF82

2xFS85

2xFS85

Synchronization with 2 devices

Enabled

Enabled

Device I2C address

D1

D1

Write

Read

VSUP UV/I2V

VSUP Under Voltage Threshold Configuration

6.2V

6.2V

Regulator assigned to VDDIO (OV)

VPRE

VPRE

Write

Read

aaa-032350

Figure 41. TestMode: Mirrors\_Main



The screenshot displays the 'TestMode: Mirrors\_FailSafe' configuration window. It features a tabbed interface with the following sections:

- VMON1, VMON2, VMON3, VMON4:** Each section contains:
  - Overvoltage threshold [%]: 112
  - Overvoltage Filtering Timing [us]: 45
  - Undervoltage threshold [%]: 88
  - Undervoltage Filtering Timing [us]: 25
  - Assignment to PGOOD: Not\_Assigned
  - Assignment to ABIST1: Not\_Assigned
  - Monitoring: Disabled
- VDDIO:**
  - Overvoltage threshold [%]: 112
  - Overvoltage Filtering Timing [us]: 45
  - Undervoltage threshold [%]: 88
  - Undervoltage Filtering Timing [us]: 25
  - Assignment to PGOOD: Not\_Assigned
  - Assignment to ABIST1: Not\_Assigned
  - Voltage selection: 3.3V
- VCORE:**
  - Overvoltage threshold (BUCK1) [%]: 112
  - Overvoltage Filtering Timing [us]: 45
  - Undervoltage threshold [%]: 88
  - Undervoltage Filtering Timing [us]: 25
  - Assignment to PGOOD: Not\_Assigned
  - Assignment to ABIST1: Not\_Assigned
  - Monitoring voltage (VBUCK1): 1.25V
- Miscellaneous:**
  - SVS max value allowed: NoSVS
  - RSTB assignment to PGOOD: Not\_Assigned
  - Watchdog monitoring: Enabled
  - Watchdog mode: Simple\_WD
  - ERRMON monitoring: Disabled
  - FCCU monitoring: Disabled
  - Fault recovery strategy: Disabled
  - Device I2C address: D0

Each section has 'write' and 'read' buttons at the bottom.

aaa-032351

Figure 42. TestMode: Mirrors\_FailSafe

The Read button provides the current status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

## 9 References

- [1] **KITFS85AEEVM** — detailed information on this board, including documentation, downloads, and software and tools  
<http://www.nxp.com/KITFS85AEEVM>
- [2] **FS8500** — product information on FS8500, Safety system basis chip for S32 microcontrollers, ASIL D capable  
<http://www.nxp.com/FS8500>
- [3] **FS8400** — product information on FS8400, Safety system basis chip for S32 microcontrollers, ASIL B capable  
<http://www.nxp.com/FS8400>
- [4] **FS85\_FS84\_OTP\_Config.xlsm** — OTP configuration file



## 10 Revision history

### Revision history

| Rev   | Date     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| v.2.1 | 20200130 | <ul style="list-style-type: none"><li>• <a href="#">Section 2</a>, <a href="#">Section 3.4</a>, <a href="#">Section 4.4</a>: fixed links (tool summary)</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| v.2   | 20191206 | <ul style="list-style-type: none"><li>• <a href="#">Section 8.1</a>: updated <a href="#">Figure 23</a></li><li>• <a href="#">Section 8.2</a>: updated description and <a href="#">Figure 24</a></li><li>• <a href="#">Section 8.3</a>: updated <a href="#">Figure 26</a></li><li>• <a href="#">Section 8.3.1</a>: updated <a href="#">Figure 28</a></li><li>• <a href="#">Section 8.4.1</a>: updated <a href="#">Figure 31</a></li><li>• <a href="#">Section 8.4.2</a>: updated <a href="#">Figure 32</a></li><li>• <a href="#">Section 8.4.6</a>: updated <a href="#">Figure 36</a></li><li>• <a href="#">Section 8.4.3</a>: updated <a href="#">Figure 33</a></li><li>• <a href="#">Section 8.4.10</a>: updated <a href="#">Figure 41</a></li></ul> |
| v.1   | 20190220 | Initial version                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## 11 Legal information

### 11.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 11.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a

default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 11.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** — is a trademark of NXP B.V.

**SMARTMOS** — is a trademark of NXP B.V.

## Tables

|         |                                                     |    |          |                                                |    |
|---------|-----------------------------------------------------|----|----------|------------------------------------------------|----|
| Tab. 1. | Compensation network .....                          | 6  | Tab. 10. | Program connector (J30) .....                  | 15 |
| Tab. 2. | Evaluation board board component descriptions ..... | 10 | Tab. 11. | Evaluation board test point descriptions ..... | 16 |
| Tab. 3. | Evaluation board indicator descriptions .....       | 12 | Tab. 12. | Evaluation board jumper descriptions .....     | 17 |
| Tab. 4. | VBAT Phoenix connector (J1) .....                   | 13 | Tab. 13. | SW3 .....                                      | 18 |
| Tab. 5. | BUCK1/BUCK2 connector (J14) .....                   | 14 | Tab. 14. | SW2 .....                                      | 19 |
| Tab. 6. | VBOOST/BUCK3 connector (J16) .....                  | 14 | Tab. 15. | SW1 .....                                      | 19 |
| Tab. 7. | LDO1/LDO2 connector (J2) .....                      | 14 | Tab. 16. | Jumper configuration .....                     | 28 |
| Tab. 8. | VPRE connector (J3) .....                           | 14 | Tab. 17. | Switch configuration .....                     | 28 |
| Tab. 9. | Debug connector (J29) .....                         | 14 | Tab. 18. | FS85 starting sequence example .....           | 32 |
|         |                                                     |    | Tab. 19. | OTP burning flag status .....                  | 45 |

## Figures

|          |                                                     |    |          |                                                  |    |
|----------|-----------------------------------------------------|----|----------|--------------------------------------------------|----|
| Fig. 1.  | KITFS85AEEVM .....                                  | 1  | Fig. 21. | OTP_conf_summary example .....                   | 31 |
| Fig. 2.  | VMONx configuration .....                           | 5  | Fig. 22. | OTP script generation .....                      | 31 |
| Fig. 3.  | VPRE compensation network .....                     | 5  | Fig. 23. | Launcher panel - bus selection .....             | 34 |
| Fig. 4.  | BUCK1 and BUCK2 multiphase configuration .....      | 6  | Fig. 24. | Main panel .....                                 | 35 |
| Fig. 5.  | SPI connection to KL25Z .....                       | 6  | Fig. 25. | Disabling device mode polling .....              | 36 |
| Fig. 6.  | J30 SPI connection .....                            | 7  | Fig. 26. | Script Editor .....                              | 36 |
| Fig. 7.  | VDDIO selection .....                               | 7  | Fig. 27. | Build a command .....                            | 38 |
| Fig. 8.  | VDDI2C supply .....                                 | 7  | Fig. 28. | Send script .....                                | 38 |
| Fig. 9.  | OTP configuration .....                             | 8  | Fig. 29. | Correct format .....                             | 38 |
| Fig. 10. | Debug mode entry .....                              | 9  | Fig. 30. | Wrong format ("//" missing in second line) ..... | 38 |
| Fig. 11. | OTP hardware implementation .....                   | 9  | Fig. 31. | Register map .....                               | 40 |
| Fig. 12. | Evaluation board featured component locations ..... | 10 | Fig. 32. | Clocks .....                                     | 40 |
| Fig. 13. | Evaluation board indicator locations .....          | 12 | Fig. 33. | Regulators .....                                 | 41 |
| Fig. 14. | Evaluation board connector locations .....          | 13 | Fig. 34. | Measurements .....                               | 42 |
| Fig. 15. | Evaluation board test points .....                  | 16 | Fig. 35. | Interrupt flags .....                            | 42 |
| Fig. 16. | Evaluation board jumper locations .....             | 17 | Fig. 36. | INIT safety .....                                | 43 |
| Fig. 17. | Switch locations .....                              | 18 | Fig. 37. | Diag safety .....                                | 44 |
| Fig. 18. | Typical initial configuration .....                 | 28 | Fig. 38. | OTP burning .....                                | 45 |
| Fig. 19. | OTP_conf_main_reg spreadsheet example ....          | 30 | Fig. 39. | TestMode:Sequencer .....                         | 46 |
| Fig. 20. | OTP_conf_failsafe_reg spreadsheet example .....     | 30 | Fig. 40. | Slot management .....                            | 46 |
|          |                                                     |    | Fig. 41. | TestMode: Mirrors_Main .....                     | 47 |
|          |                                                     |    | Fig. 42. | TestMode: Mirrors_FailSafe .....                 | 48 |

## Contents

|          |                                                                                                  |           |            |                                                                    |           |
|----------|--------------------------------------------------------------------------------------------------|-----------|------------|--------------------------------------------------------------------|-----------|
| <b>1</b> | <b>Introduction .....</b>                                                                        | <b>2</b>  | <b>8.2</b> | Establishing the connection between FlexGUI and the hardware ..... | 34        |
| <b>2</b> | <b>Finding kit resources and information on the NXP web site .....</b>                           | <b>2</b>  | <b>8.3</b> | Working with the Script editor .....                               | 36        |
| 2.1      | Collaborate in the NXP community .....                                                           | 2         | 8.3.1      | Script text editor .....                                           | 37        |
| <b>3</b> | <b>Getting ready .....</b>                                                                       | <b>2</b>  | 8.3.2      | Script sequence files .....                                        | 39        |
| 3.1      | Kit contents .....                                                                               | 2         | 8.4        | Understanding the FS85 workspace .....                             | 39        |
| 3.2      | Additional hardware .....                                                                        | 3         | 8.4.1      | Register map .....                                                 | 39        |
| 3.3      | Windows PC workstation .....                                                                     | 3         | 8.4.2      | Clocks .....                                                       | 40        |
| 3.4      | Software .....                                                                                   | 3         | 8.4.3      | Regulators .....                                                   | 41        |
| <b>4</b> | <b>Getting to know the hardware .....</b>                                                        | <b>3</b>  | 8.4.4      | Measurements .....                                                 | 41        |
| 4.1      | Kit overview .....                                                                               | 3         | 8.4.5      | Interrupt flags .....                                              | 42        |
| 4.1.1    | KITFS85AEEVM features .....                                                                      | 4         | 8.4.6      | INIT safety .....                                                  | 43        |
| 4.1.2    | VMON configuration .....                                                                         | 4         | 8.4.7      | Diag safety .....                                                  | 43        |
| 4.1.3    | VPRE compensation network .....                                                                  | 5         | 8.4.8      | OTP programming .....                                              | 45        |
| 4.1.4    | BUCK1 and BUCK2 multiphase configuration .....                                                   | 6         | 8.4.9      | TestMode:Sequencer .....                                           | 46        |
| 4.1.5    | SPI/I2C .....                                                                                    | 6         | 8.4.10     | TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe .....          | 47        |
| 4.1.6    | VDDI2C .....                                                                                     | 7         | <b>9</b>   | <b>References .....</b>                                            | <b>48</b> |
| 4.2      | Device OTP user configuration .....                                                              | 7         | <b>10</b>  | <b>Revision history .....</b>                                      | <b>49</b> |
| 4.2.1    | OTP and mirrors registers .....                                                                  | 8         | <b>11</b>  | <b>Legal information .....</b>                                     | <b>50</b> |
| 4.2.2    | OTP hardware implementation .....                                                                | 8         |            |                                                                    |           |
| 4.3      | Kit featured components .....                                                                    | 9         |            |                                                                    |           |
| 4.3.1    | FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO .....                      | 11        |            |                                                                    |           |
| 4.3.1.1  | General description .....                                                                        | 11        |            |                                                                    |           |
| 4.3.1.2  | Features .....                                                                                   | 11        |            |                                                                    |           |
| 4.3.2    | Indicators .....                                                                                 | 12        |            |                                                                    |           |
| 4.3.3    | Connectors .....                                                                                 | 13        |            |                                                                    |           |
| 4.3.3.1  | VBAT connector (J1) .....                                                                        | 13        |            |                                                                    |           |
| 4.3.3.2  | Output power supply connectors .....                                                             | 14        |            |                                                                    |           |
| 4.3.3.3  | Debug connector (J29) .....                                                                      | 14        |            |                                                                    |           |
| 4.3.3.4  | Program connector (J30) .....                                                                    | 15        |            |                                                                    |           |
| 4.3.4    | Test points .....                                                                                | 15        |            |                                                                    |           |
| 4.3.5    | Jumpers .....                                                                                    | 17        |            |                                                                    |           |
| 4.3.6    | Switches .....                                                                                   | 18        |            |                                                                    |           |
| 4.4      | Schematic, board layout and bill of materials ...                                                | 19        |            |                                                                    |           |
| <b>5</b> | <b>Installing and configuring software and tools .....</b>                                       | <b>19</b> |            |                                                                    |           |
| 5.1      | Installing the Java JRE .....                                                                    | 19        |            |                                                                    |           |
| 5.2      | Installing Windows 7 FlexGUI driver .....                                                        | 19        |            |                                                                    |           |
| 5.3      | Installing FlexGUI software package .....                                                        | 27        |            |                                                                    |           |
| <b>6</b> | <b>Configuring the hardware for startup .....</b>                                                | <b>28</b> |            |                                                                    |           |
| <b>7</b> | <b>Using the KITFS85AEEVM evaluation board ...</b>                                               | <b>29</b> |            |                                                                    |           |
| 7.1      | Generating the OTP configuration file .....                                                      | 29        |            |                                                                    |           |
| 7.2      | Working in OTP emulation mode .....                                                              | 31        |            |                                                                    |           |
| 7.2.1    | Example script: Closing initialization phase, disabling FCCU monitoring and releasing FS0B ..... | 32        |            |                                                                    |           |
| 7.3      | Programming the device with an OTP configuration .....                                           | 33        |            |                                                                    |           |
| <b>8</b> | <b>Using FlexGUI .....</b>                                                                       | <b>33</b> |            |                                                                    |           |
| 8.1      | Starting the FlexGUI application .....                                                           | 33        |            |                                                                    |           |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2020.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 30 January 2019

Document identifier: UM11193