Kintex-7 FPGA KC705 Evaluation Kit (Vivado Design Suite 2013.1)

Getting Started Guide

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XILINX®

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/13/2012	1.0	Initial Xilinx release.
01/25/2012	1.1	Changed document title. Added BIST section. Changed Platform Flash to BPI Linear Flash. Added a note after Figure 30. Updated photos in Figure 2, Figure 3, and Figure 31.
02/27/2012	1.1.1	Added a note to Hardware Test Setup Requirements.
07/10/2012	1.2	Added XPN number to title page. Updated Introduction and Hardware Test Setup Requirements. Added Kit Contents, AMS Bring-up with the AMS101 Evaluation Card, and AMS Bring-up with the AMS101 Evaluation Card. Added Appendix B, Warranty. Removed "Modifying the Kintex-7 FPGA Base TRD" section.
12/20/12	2.0	The document was updated for Vivado™ Design Suite 2012.4. Agile Mixed Signal is now Analog Mixed Signal. The USB stick is removed from the kit and instead, design files are accessible from the Docs & Designs tab at www.xilinx.com/kc705. Removing the USB stick affected many sections including these: • Kit Contents, page 7 • Hardware Test Setup Requirements, page 9 • AMS Bring-up with the AMS101 Evaluation Card, page 13 • Step 4 in Install the Linux Driver, page 22. The first bullet under Introduction, page 7 removed "transceivers by using the LogiCORE™ IP Integrated Bit Error Ratio (IBERT) core". Under KC705 Evaluation Board Setup, page 10, "cord and brick" changed to "12V power adapter." Removed the *Transceiver Bring-up Using Integrated Bit Error Ratio Test* section on page 14. Requirements to Get Started, page 14 installation method **a** and step 3 changed. The use of the ChipScope™ tool is eliminated. Step 2 of Evaluating AMS, page 15 changed. Below Figure 9, this sentence was deleted: AMS Evaluator source code is not provided. CD-ROM was replaced with DVD-ROM. Appendix A, Additional Resources was reorganized.
04/16/2013	3.0	Added third, fourth, and fifth bullets in AMS Bring-up with the AMS101 Evaluation Card, page 13. Updated step 2 and step 3 in Requirements to Get Started, page 14. Updated step 2 in Evaluating AMS, page 15. Added eighth bullet in Hardware Test Setup Requirements, page 18.

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Getting Started with the Kintex-7 FPGA KC705 Evaluation Kit (Vivado Design Suite 2013.1)

Introduction

The Kintex™-7 FPGA KC705 evaluation kit provides a comprehensive, high-performance development and demonstration platform using the Kintex-7 FPGA family for high-bandwidth and high-performance applications in multiple market segments. The kit enables designing with DDR3, I/O expansion through FMC, and common serial standards, such as PCI Express®, XAUI, and proprietary serial standards through the SMA interface. See the *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) and the KC705 support website at www.xilinx.com/kc705.

The built-in self-test (BIST) and Kintex-7 FPGA Base Targeted Reference Design (TRD) are developed on this kit.

This Getting Started Guide is divided into two sections:

- Basic Hardware Bring-up: Enables hands-on operation of all the features in the BIST as well as evaluation of Analog Mixed Signal (AMS) using the AMS101 evaluation card.
- Advanced Operation: Enables hands-on operation with the base TRD, which features PCIe, DDR3 memory, and AXI—all supported through a custom evaluation graphical user interface (GUI).

Kit Contents

The Kintex-7 FPGA KC705 evaluation kit includes:

- KC705 base board, including the XC7K325T-2FFG900CES FPGA.
- AMS101 evaluation card, enabling evaluation of the AMS technology built into all 7 series FPGAs.
- Software and licenses:
  - Vivado™ Design Suite Installation DVD.
  - Printed entitlement voucher: Provides entitlement of the Vivado Design Suite Logic Edition device-locked to the XC7K325T-2FFG900 FPGA. Follow the printed instructions on the voucher to redeem your software entitlement.
  - Fedora 16 Live DVD to support the Base Targeted Reference Design.

- Designs:
  - Targeted Reference Design: Robust sub-system including PCIe Gen2 x4, Northwest Logic DMA, multi-port virtual FIFO, AXI, and DDR3 memory controller.
  - Additional Reference Designs: Numerous additional reference designs available online and linked from the KC705 product page www.xilinx.com/kc705.
- Documentation:
  - *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883—this guide, included in the box)
  - *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) (online on product page)
  - *KC705 Reference Design User Guide* (UG845) (online on product page)
  - *Kintex-7 FPGA KC705 Base Targeted Reference Design User Guide (Vivado Design Suite 2012.4)* (UG882) (online on product page)
  - Board design files including schematics, Gerber files, and BOM (online on product page)
- Cables and power supply:
  - Universal 12V power adapter and cords
  - Two USB cables (1x USB Type-A/Mini-B and 1x USB Type-A/Micro-B) for download and debug
  - Ethernet crossover cable
- HDMI cable

Basic Hardware Bring-up Using the BIST

The built-in self-test (BIST) tests many of the features offered by the Kintex-7 FPGA KC705 evaluation kit. The test is stored in the nonvolatile BPI Linear Flash memory, and configures the FPGA when the mode and upper flash address pins on the board are set for Master BPI.

Figure 1 provides an overview of the board features used by the BIST.

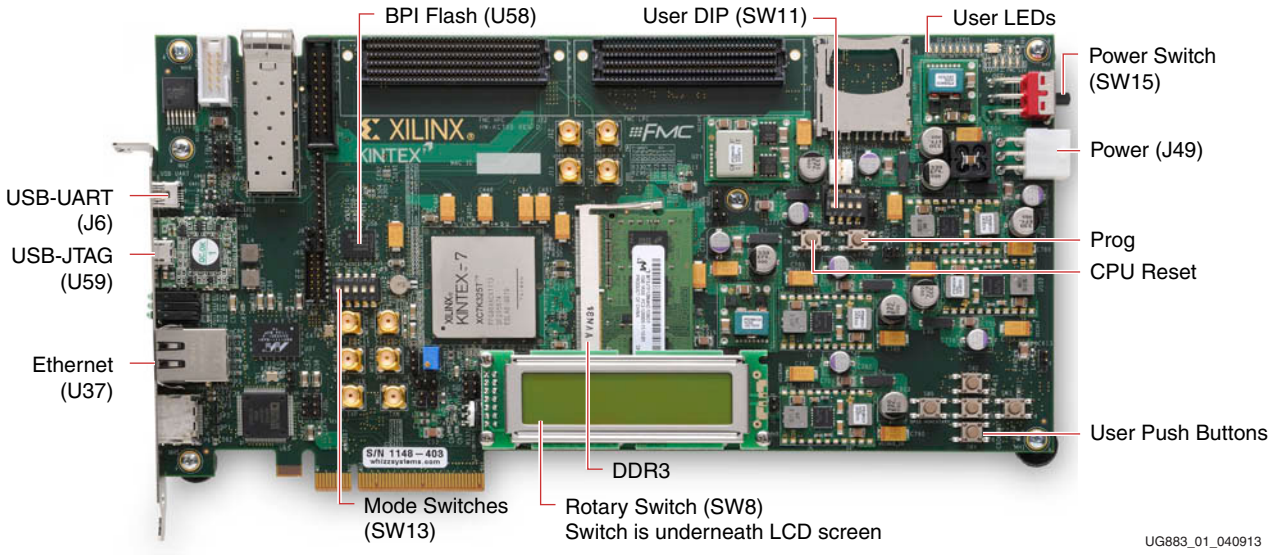


Figure 1: **KC705 Board Features Used by the BIST**

Note: For a diagram of all the features on the KC705, see *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810).

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900CES device
- USB-to-Mini-B cable (for UART)
- AC power adapter (12 VDC)
- Terminal program [Ref 3]

  Note: The Tera Term Pro program is used for illustrative purposes. Other programs can be used.
- USB-UART drivers from SiLabs [Ref 4]

Hardware Test Board Setup Requirements

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

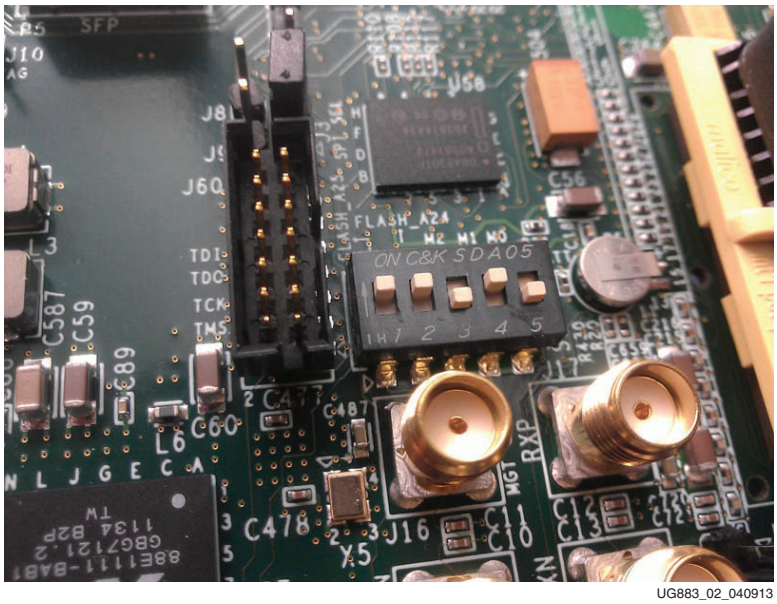
KC705 Evaluation Board Setup

1. Set the jumpers and switches on the KC705 board as follows:
   - The mode switches (SW13) are set for Master BPI mode 010.
   - The upper flash address switches (SW13) are set to 11.
2. Verify the switch and jumper settings are set as shown in Table 1 and Figure 2.

Note: For this application, the board should be set up as a stand-alone system, with power coming from the 12V power adapter included with the KC705 evaluation kit.

Table 1: **Switch & Jumper Settings**

Switch	Setting	
SW15	Board Power slide-switch	
	..	Off
SW11	User GPIO DIP switch	
	4	Off
	3	Off
	2	Off
	1	Off
SW13	Configuration Mode switch	
	5	Off
	4	On
	3	Off
	2	On
	1	On



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Figure 2: **BIST Switch and Jumper Settings**

Hardware Bring-Up

This section details the steps for hardware bring-up:

1. With the board switched off, plug a USB-to-Mini-B cable into the UART port of the KC705 board and your PC (see Figure 3).

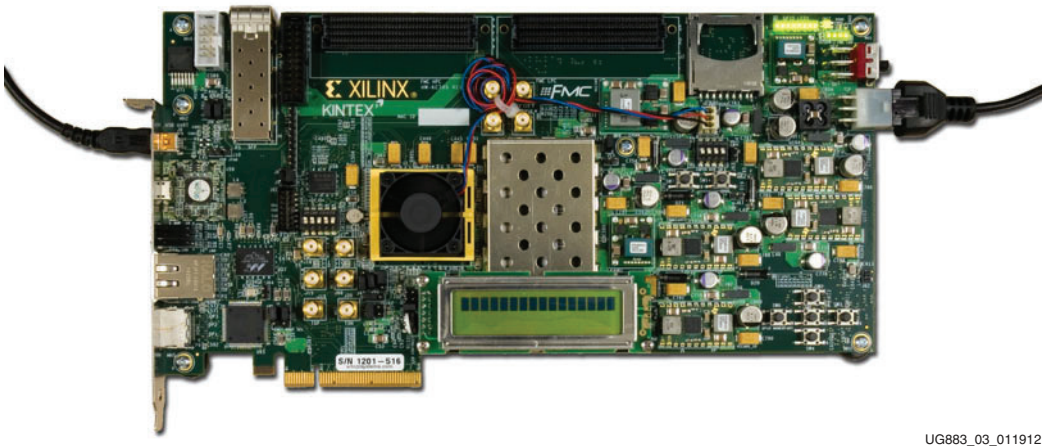


Figure 3: **KC705 with the UART and Power Cable Attached**

2. Install the power cable.
3. Switch the KC705 board power to ON.

Install the UART Driver

1. Run the downloaded executable UART-USB driver file listed in Hardware Test Setup Requirements, page 9. This enables UART-USB communications with a host PC (see Figure 4).

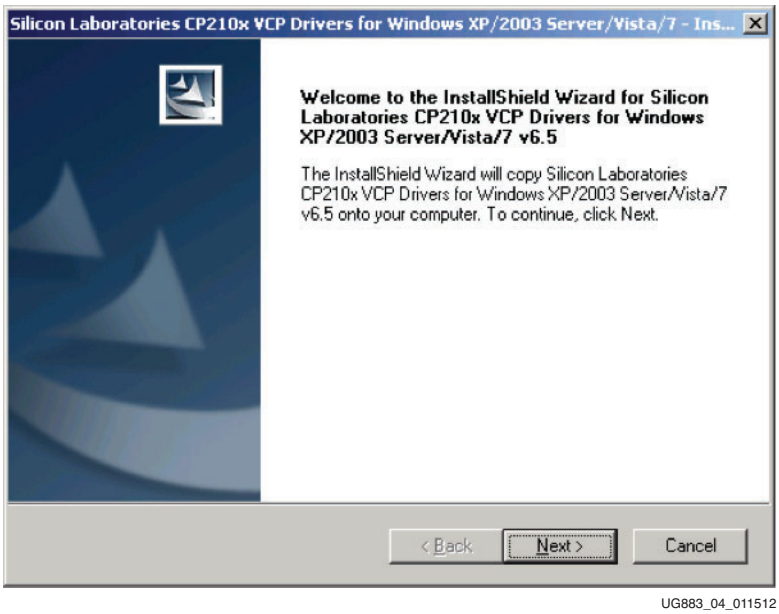


Figure 4: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known port in the Device Manager as follows:
   - Right-click **My Computer** and select **Properties**.
   - Select the **Hardware** tab, then click the **Device Manager** button.
   - Find and right-click the Silicon Labs device in the list. Then select **Properties**.
   - Click the **Port Settings** tab and the **Advanced...** button.
   - Select an open COM port between COM1 and COM4.

Figure 5 shows the steps needed to set the USB-UART port.

Note: Steps and diagrams refer to use with a Windows host PC with the Windows XP or Windows 7 operating system.

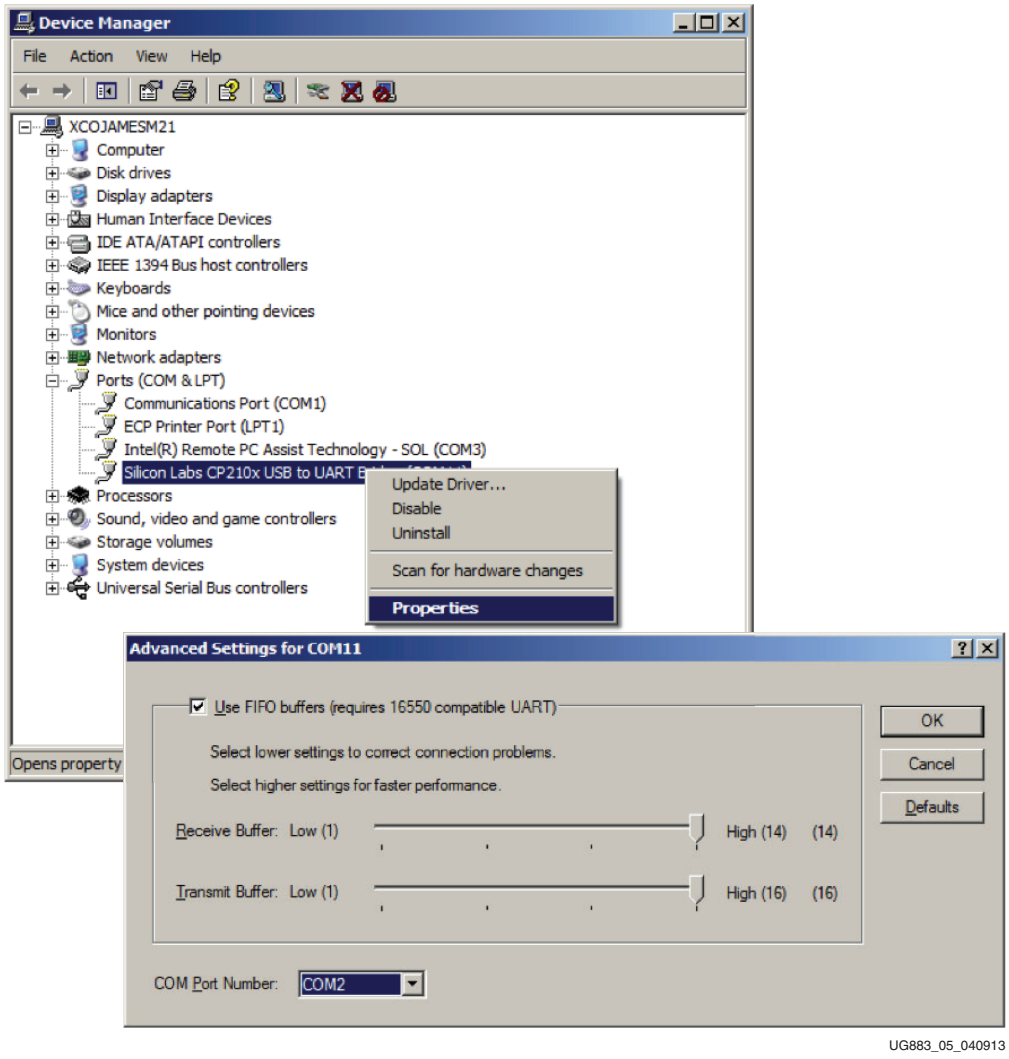


Figure 5: **Port Selection on the Device Manager Screen**

Run the BIST Application

1. Start the installed terminal program.
2. Press PROG (SW14) on the KC705 board, and view the BIST output on the terminal window (see Figure 6).

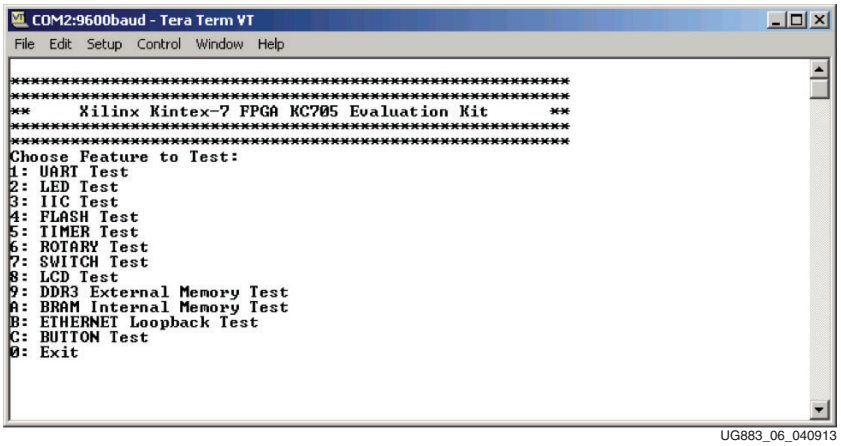


Figure 6: **BIST Main Menu**

3. Select the relevant tests to run, and observe the results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the KC705 support website at http://www.xilinx.com/kc705 under the Docs & Designs tab.

AMS Bring-up with the AMS101 Evaluation Card

The Xilinx® 7 series FPGAs each feature a 1 MSPS, 12-bit, analog-to-digital converter built into the FPGA for everything from simple analog monitoring to more signal processing intensive tasks like linearization, calibration, oversampling and filtering. The Kintex-7 FPGA KC705 evaluation kit includes the hardware and software to evaluate this feature and determine its usefulness in the user's end system.

For evaluation of Xilinx Analog Mixed Signal (AMS) capability, the following items from your kit are needed:

- Access to XADC header in your FPGA base board
- AMS101 evaluation card (Figure 7)
- FPGA design and software files downloaded from the Docs & Designs tab at www.xilinx.com/kc705
- USB/UART drivers from Silicon Labs
- AMS Evaluator tool

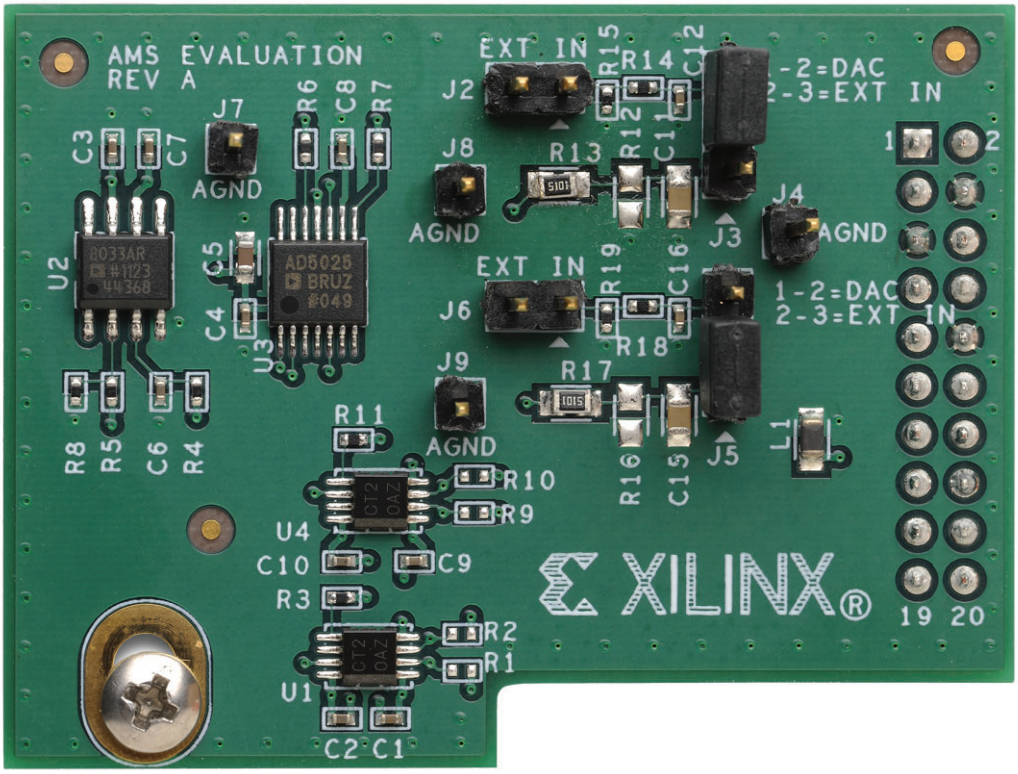


Figure 7: **AMS101 Evaluation Card**

Requirements to Get Started

1. Open the USB/UART as described in Install the UART Driver, page 11.
2. The AMS101 evaluation card requires a Windows host PC to install the AMS Evaluator tool which uses National Instruments' LabView run-time engine. Install the AMS Evaluator tool by unzipping the AMS Evaluator installer files https://secure.xilinx.com/webreg/clickthrough.do?cid=199651&license=RefDesLicense&filename=ams101_gui_installer_v1_1.zip located in the Targeted Reference Designs section in the Docs & Designs tab at www.xilinx.com/kc705. After opening the zip file folder, click the setup.exe file to begin the installation. When loading the National Instruments LabView runtime engine, Click OK to accept the license agreement. Running the setup program loads the AMS101 Evaluator tool with the red Xilinx logo on the desktop.
3. Download the AMS Targeted Reference Design files from the Docs & Designs tab **`Kintex-7 FPGA KC705 Evaluation Kit - (7 Series FPGA AMS Targeted Reference Design User Guide (Vivado Design Suite 2012.4 and ISE Design Suite 14.4))`** section at www.xilinx.com/kc705. Unzip the `xadc_eval_design_kc705_V1_0.zip` files. Open the `ready_to_test` folder. Save the `xadc_eval_design.bit` bitstream.

Evaluating AMS

1. Connect and power the hardware:
   a. Plug the AMS101 evaluation card into the XADC header on your FPGA base board.

      Note: Ensure the notch on the XADC header lines up correctly with the AMS101 evaluation card (see Figure 8).

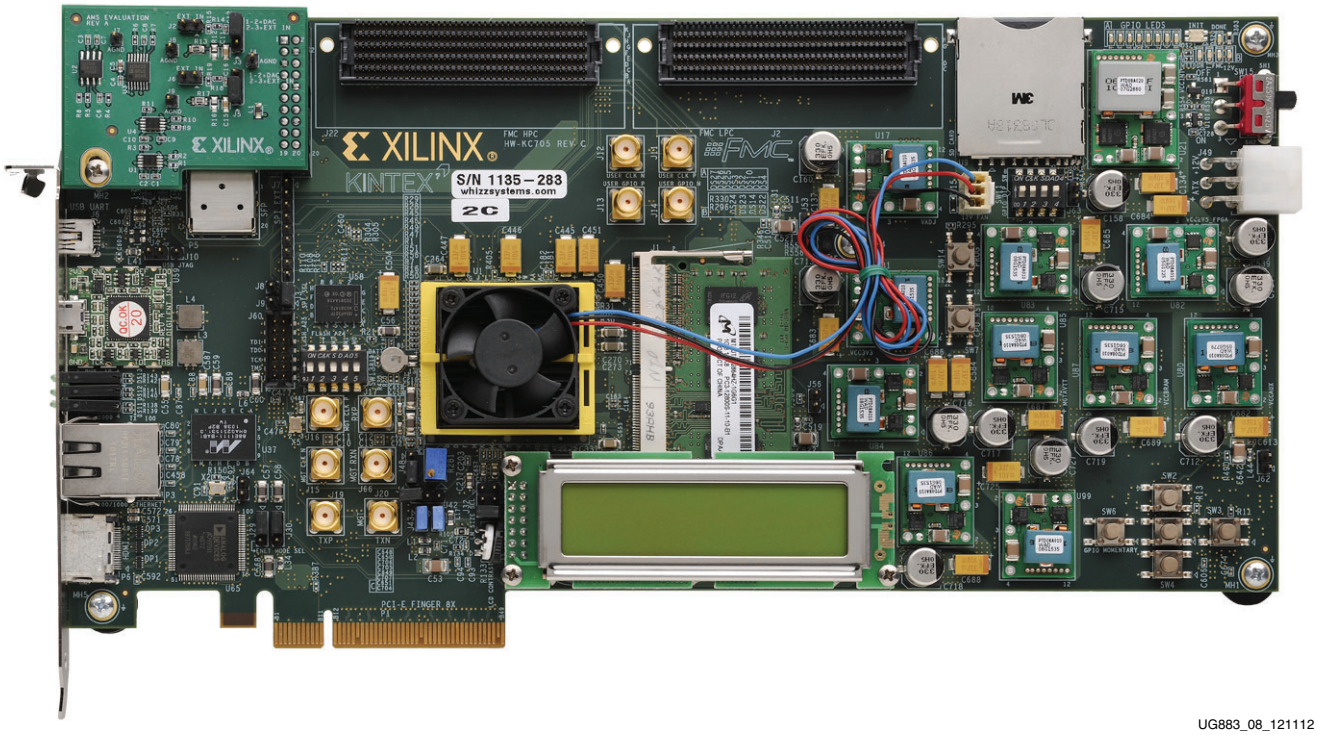


Figure 8: **KC705 Base Board with AMS101 Evaluation Card Plugged into XADC Header**

   b. Power up the FPGA base board
2. Download the design to the FPGA. Installation of ISE Programming tools or Lab Tools is required for downloading the bitstream to the FPGA.

   Refer to the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) at http://www.xilinx.com/support/documentation/dt_vivado.htm to obtain information on downloading the design to the FPGA.

   a. Open the `xadc_eval_design.bit` file from the AMS Targeted Reference Design files.
3. Run the AMS101 Evaluator LabVIEW GUI executable from your desktop. After loading the AMS Evaluator installer files, a red `X` with the AMS Evaluator program should reside on your desktop.

Note: The AMS bitstream can also be loaded with ChipScope analyzer.

The AMS101 Evaluator GUI is shown in Figure 9.

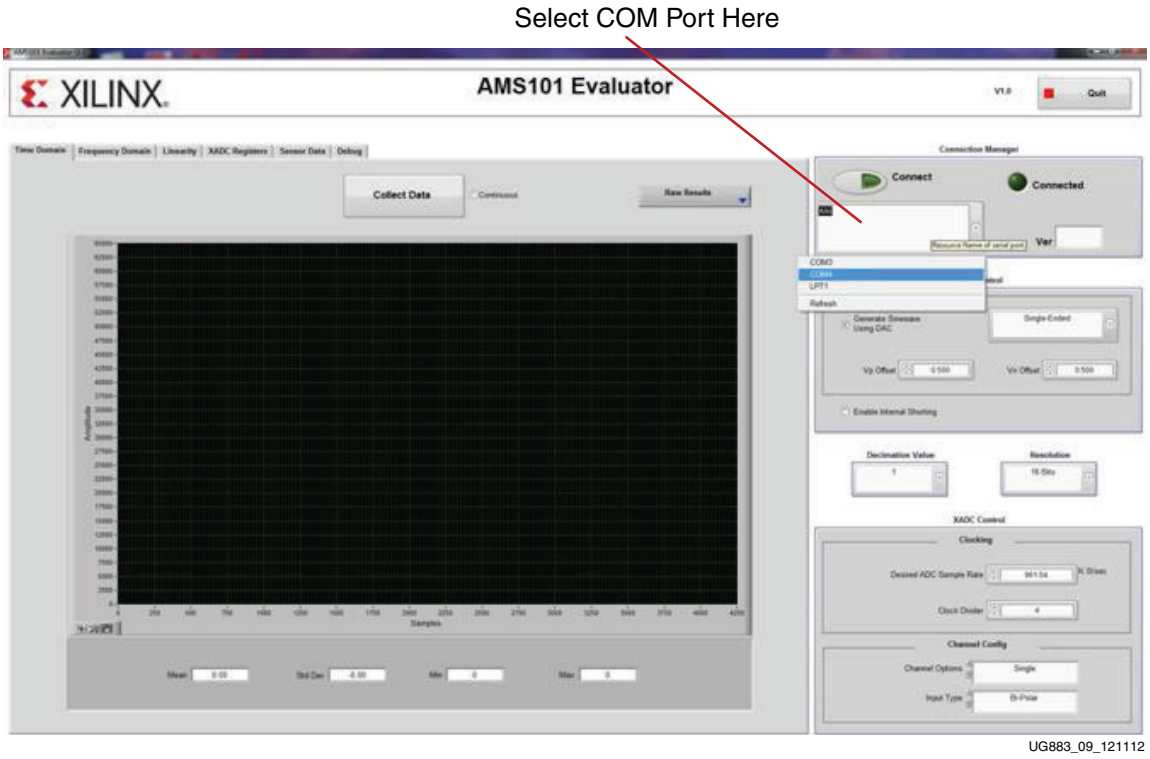


Figure 9: **AMS101 Evaluator GUI**

The AMS Evaluator Tool allows designers to quickly evaluate the analog signals in the time domain, frequency domain, display linearity, verify the XADC register settings, and measure the internal temperature sensor and supply voltages.

For a more extensive explanation of the AMS101 evaluation card and the applicable files, refer to *AMS101 Evaluation Platform User Guide* (UG886).

Advanced Bring-up Using the Base Targeted Reference Design

The primary components of the Kintex-7 FPGA Base TRD are:

- Integrated Endpoint block for PCI Express (PCIe). See *7 Series FPGAs Integrated Block for PCI Express User Guide* (UG477).
- Northwest Logic Packet DMA [Ref 5]
- Multiport Virtual FIFO

The TRD system can sustain up to 10 Gb/s throughput end to end.

Figure 10 provides an overview of the TRD.

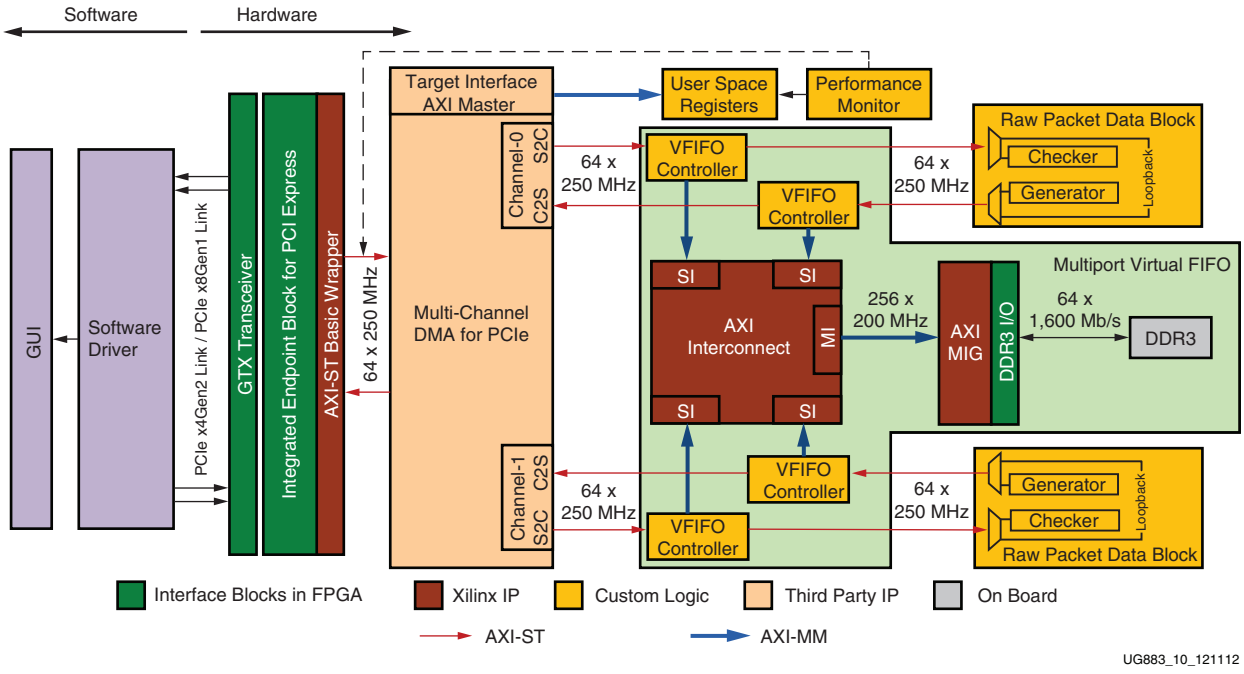


Figure 10: **Kintex-7 FPGA Base TRD Block Diagram**

Note: In Figure 10 the arrows indicate AXI interface directions (from master to slave). They do not indicate data flow directions.

Components

The Kintex-7 FPGA Base TRD features these components:

- Kintex-7 FPGA integrated Endpoint block for PCI Express:
  - Configured with 4 lanes at a 5 Gb/s link rate (Gen2) or 8 lanes at a 2.5 Gb/s link rate (Gen1) for PCI Express v2.0
  - Provides a user interface compliant with AXI4-Stream interface protocol
  - Performance monitor tracks the integrated block's AXI4-Stream interface for PCIe transactions
- Bus Mastering Scatter-Gather Packet DMA from Northwest Logic, a multichannel DMA:
  - Supports full-duplex operation with independent transmit and receive paths

    - Provides an AXI4-Stream interface on the back end
    - Monitors the performance of data transfers in receive and transmit directions
    - Provides an AXI4 memory-mapped target interface to access user-defined registers

  Note: The Northwest Logic Packet DMA shipped with the Base TRD is an evaluation version and expires after 12 hours of run time. To get the full version, contact Northwest Logic [Ref 7].
- Multiport Virtual FIFO:
  - DDR3 SDRAM SODIMM (64-bit @ 1600 Mb/s; 800 MHz) is used for buffering packets. The memory controller delivered through the memory interface generator (MIG) tool interfaces to the DDR3 memory.
  - AXI Interconnect IP along with the memory controller supports multiple ports on the memory.
  - The Packetized Virtual FIFO controller controls addressing of the DDR3 memory for each port, allowing DDR3 to be used as Virtual Packet FIFO.
- Software driver for a 32-bit Linux platform:
  - Configures the hardware design parameters
  - Generates and consumes traffic
  - Provides a GUI to report status and performance statistics

The Kintex-7 FPGA integrated Endpoint block for PCI Express and the Packet DMA are responsible for data transfers from host system to Endpoint card (S2C) and Endpoint card to host system (C2S). Data to and from the host is stored in a Virtual FIFO built around the DDR3 memory. This Multiport Virtual FIFO abstraction layer around the DDR3 memory allows the user to move traffic efficiently without the need to manage addressing and arbitration on the memory interface. It also provides more depth than storage implemented using Block RAMs.

The integrated Endpoint block for PCI Express, Packet DMA, and Multiport Virtual FIFO form the base system. The base system can bridge the host to any user application running on the other end. The raw data packet module is a dummy application that generates and consumes packets. It can be replaced by any user specific protocol like Aurora or XAUI.

The software driver runs on the host system. It generates raw data traffic for transmit operations in the S2C direction. It also consumes the data looped back or generated at the application end in the C2S direction.

Hardware Test Setup Requirements

These are the prerequisites for testing the design in hardware:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900C device
- Design files provided as a zipped collection under the Docs & Designs tab at www.xilinx.com/kc705 include:
  - Design source files
  - Device driver files
  - Board design files
  - Documentation
- Vivado Design Suite
- ISE Programming tools or LabTools

- Micro USB cable
- 4-pin to 6-pin PCIe adapter cable
- Fedora 16 Live DVD [Ref 6]
- PC with PCIe v2.0 slot. For a complete list of machines tested, and all known issues, refer to the Kintex-7 FPGA Base Targeted Reference Design Release Notes and Known Issues Master Answer Record (http://www.xilinx.com/support/answers/45679.htm). This PC could also have Fedora Core 16 Linux OS installed on it.

TRD Demonstration Setup

This section describes hardware setup and use of the application GUI to help the user get started quickly with the design in hardware. It provides a step-by-step explanation of hardware bring-up, and describes using the application GUI.

When following the demonstration setup steps for the Kintex-7 FPGA Base TRD, if the behavior is not as described, refer to the known issues at www.xilinx.com/support/answers/45679.htm.

Board Setup

This section describes how to set up the KC705 Evaluation board required to demonstrate the TRD.

1. Set the KC705 Jumpers and Switches: Verify that the KC705 Evaluation board jumpers and switches are set as shown in Table 2 and Figure 11.

Table 2: **Switch and Jumper Settings**

Jumper	Function		Setting
J32	PCIe configuration width — 4 lane design		Jump 3-4
Switch	**Function or Type**		**Setting**
SW15	Board power slide-switch		Off
SW11	User GPIO DIP switch		
	4		Off
	3		Off
	2		Off
	1		Off
S13	DIP switch SW13 positions 1 and 2 control the setting of address bits of the flash. DIP switch SW13 positions 3, 4, and 5 control which configuration mode.		
	5 (M0)	M2 =0 M1=1 M0=0 – Master BPI M2 =0 M1=0 M0=1 – Master SPI M2 =1 M1=0 M0=1 – JTAG	Off
	4 (M1)		On
	3 (M2)		Off
	2		Off
	1		Off

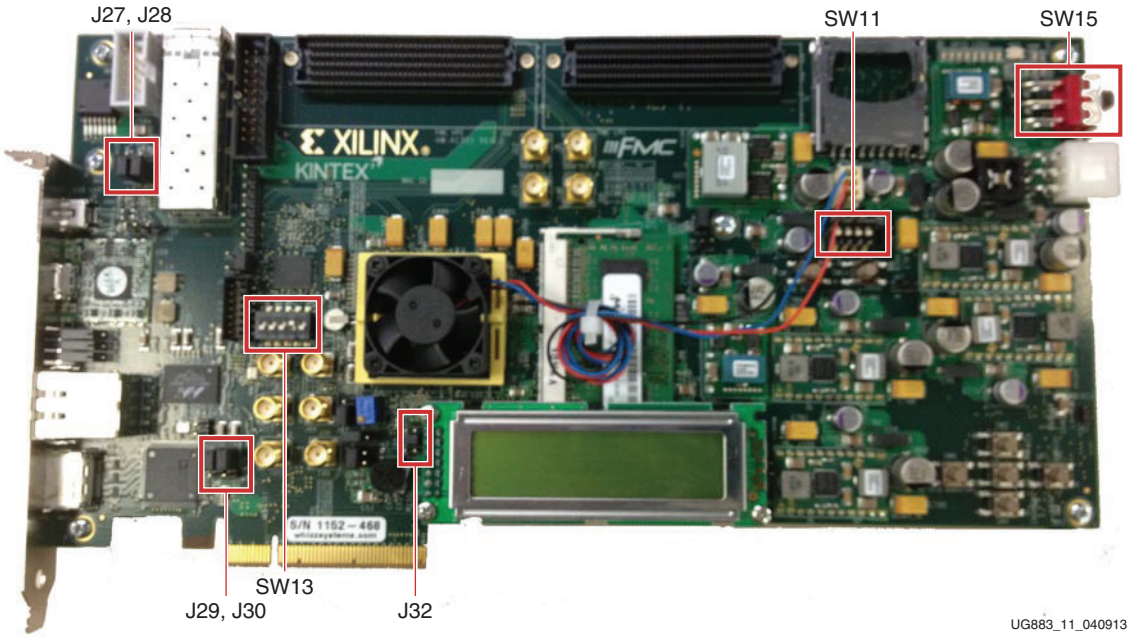


Figure 11: **Switch and Jumper Settings**

Hardware Bring-Up

This section presents steps for hardware bring-up.

1. With the host system switched off, insert the KC705 board in the PCIe slot through the PCI Express x8 or x16 edge connector (Figure 12).

   The TRD programmed on the KC705 board has a 4-lane PCIe v2.0 configuration, running at a 5 Gb/s link rate per lane. The PCI Express specification allows for a smaller lane width Endpoint to be installed into a larger lane width PCIe connector.

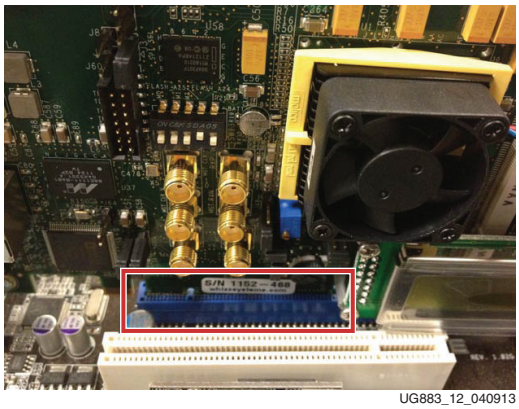


Figure 12: **KC705 Board Plugged into a PCIe x16 Slot**

2. Figure 13 shows the 12V power connection. Connect the 12V ATX power supply's available 4-pin connector to the board (J49) via a 4-pin to 6-pin PCIe adapter cable. Toggle the Power switch SW15 to the ON position.

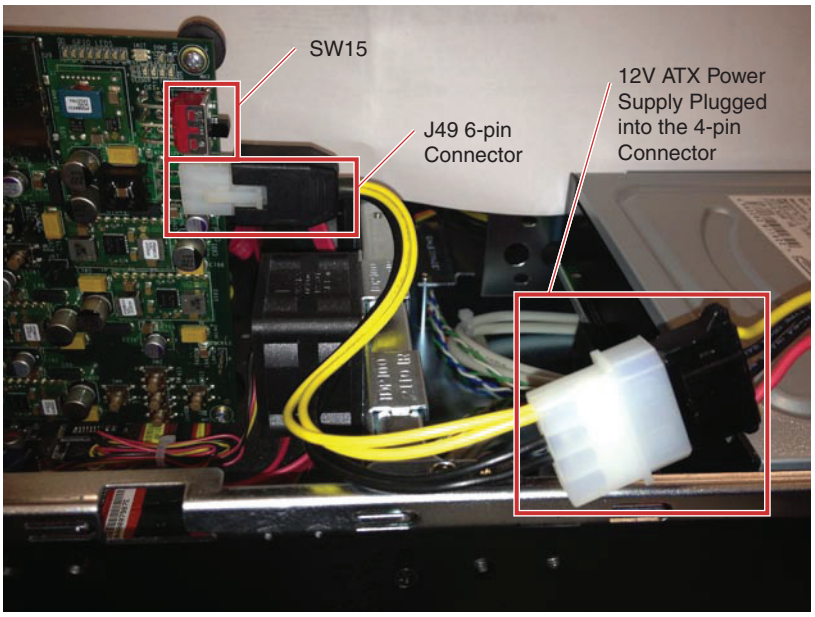


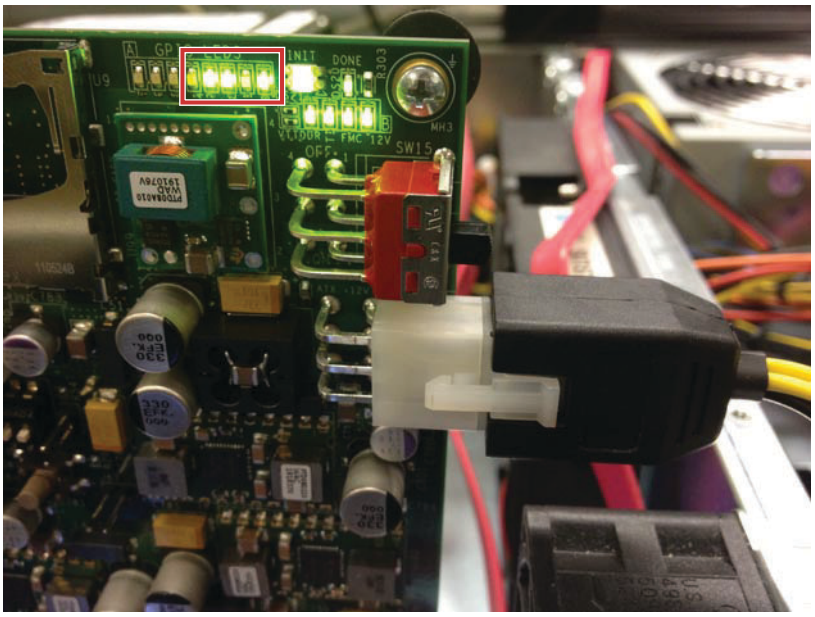
Figure 13: **Power Supply Connection**

3. Make sure the connections are tight, and then power on the PC system.

   Note: If the user wishes to boot Linux from the Fedora 16 Live DVD, place the DVD in the PC's DVD-ROM drive as soon as the PC system is powered on.

4. Verify the status of the design on the KC705 LEDs. The design provides status on the GPIO LEDs on the upper right of the KC705 board (Figure 14). After the PC system is powered on and the TRD has successfully configured, status LEDs, from right to left, should indicate:

- LED 0 — ON if the PCIe link is up
- LED 1 — Flashes if the PCIe user clock is present
- LED 2 — ON if lane width is what is expected, else it flashes (for a 4 lane design, the expected lane width is 4; for an 8 lane design, the expected lane width is 8)
- LED 3 — ON if memory calibration is done
- LED 4 to LED 7 — Not connected



UG883_14_121112

Figure 14: **Location of GPIO Status LEDs (Indicates TRD Status)**

Install the Linux Driver

1. If Fedora 16 is installed on the PC system's hard disk, boot as a root-privileged user, and skip to step 3, page 23.
2. To boot from the Fedora 16 Live DVD provided in the kit, place the DVD in the PC's DVD-ROM drive. The Fedora 16 Live Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. For more details, see Fedora Information, page 2. The PC boots from the DVD-ROM drive and logs into a liveuser account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: Users might have to adjust BIOS boot order settings to make sure that the DVD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the DEL or F2 key when the system is powered on. Set the boot order and save the changes. (The DEL or F2 key is used by most PC systems to enter the BIOS setup. Some PCs might have a different way to enter the BIOS setup.)

   The PC should boot from the DVD-ROM drive. The images in Figure 15 are seen on the monitor during boot up.

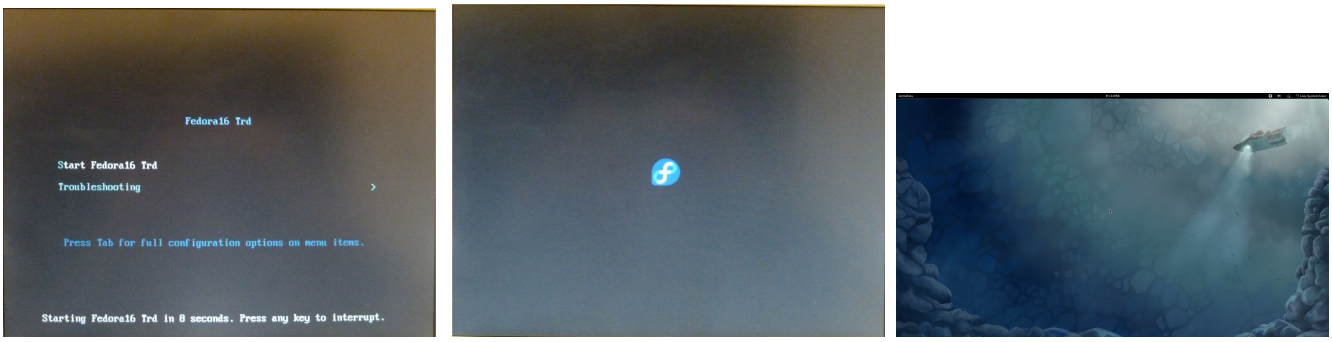


Figure 15: **Fedora 16 Live DVD Booting**

3. After Fedora 16 Core boots, open a terminal window (click **`Activities`**, click **`Application`**, scroll down, and click the **`Terminal`** icon). To find out if the PCIe Endpoint is detected, at the terminal command line, type

   ```
   $ lspci
   ```

   The lspci command displays the devices in the PCI and PCI Express buses of the PC. On the bus of the KC705 card slot is the message

   ```
   Communication controller: Xilinx Corporation Device 7042
   ```

   This message confirms that the design programmed into the KC705 board has been found by the BIOS and the Fedora 16 OS. The bus number varies depending on which PC motherboard and slot are used. Figure 16 shows a lspci output for an example system. Xilinx device 7042 has been found by the BIOS on bus number 2 (`02:00.0 - bus:dev.function`).

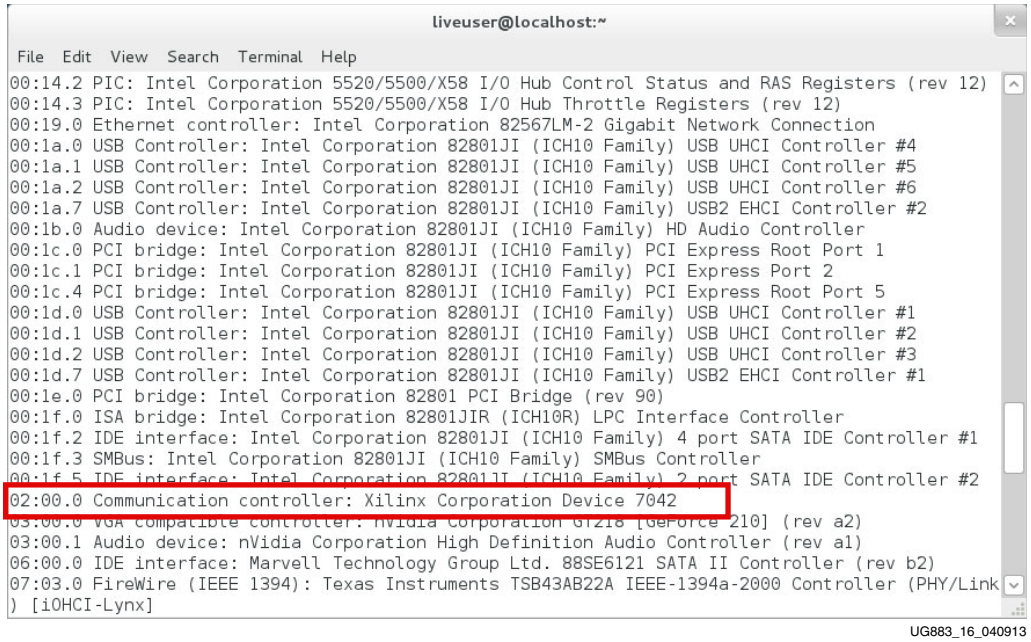


Figure 16: **PCI and PCI Express Bus Devices**

4. Download the reference design from the Docs & Designs tab at www.xilinx.com/kc705 and copy the `k7_pcie_dma_ddr3_base` folder into any directory.
5. To set up and run the TRD demonstration, the software driver should be installed on the PC system. Software driver installation involves:
   a. Building the kernel objects and the GUI
   b. Inserting the driver modules into the kernel.

   After the driver modules are loaded, the application GUI can be invoked. The user can set parameters through the GUI and run the TRD.

   When the user is done running the TRD, the application GUI can be closed and the drivers can be removed.

   A script is provided to execute all the above actions so that the user can quickly start the TRD.

   The `k7_trd_lin_quickstart` script is available in the `k7_pcie_dma_ddr3_base` folder. Right click the script, select **`properties`**, go to the **`permissions`** tab, check the box **`Allow executing file as program`**—this makes the script executable. Close the window.

   To run the script, double-click `k7_trd_lin_quickstart` in the `k7_pcie_dma_ddr3_base` folder (Figure 17). The window prompt in Figure 18 appears.

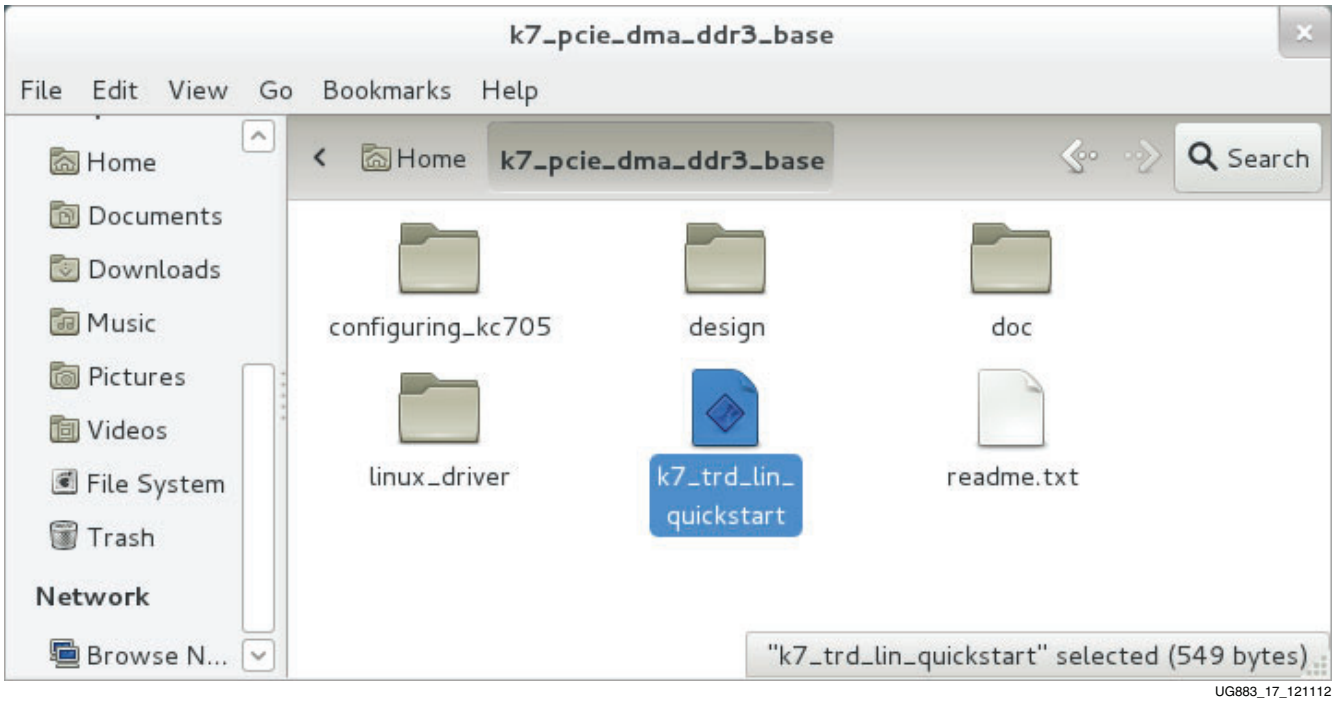


Figure 17: **Load Driver and Launch Application GUI**

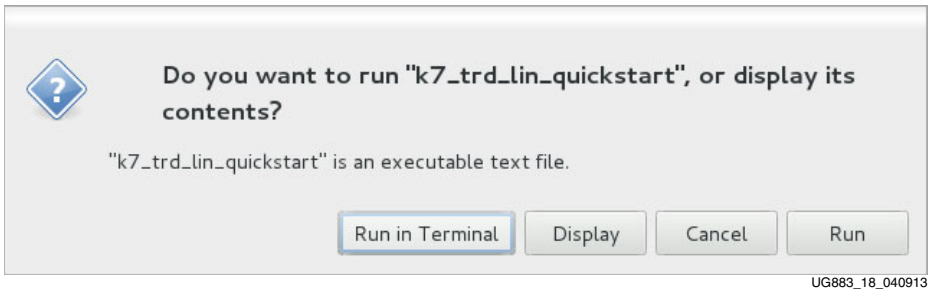


Figure 18: **Run in Terminal**

Click **`Run in Terminal`** to proceed. The application GUI is invoked.

Proceed to the next section, Using the Application GUI, to set design parameters and run the TRD.

Using the Application GUI

When the drivers are loaded and the Performance Monitor GUI is invoked, the user can configure the sending and receiving of data. The GUI allows the user to observe the collected statistics and other status information.

1. Click the **`System Status`** tab to verify the status of the KC705 board and the PCIe link (see Figure 19 and Table 3).

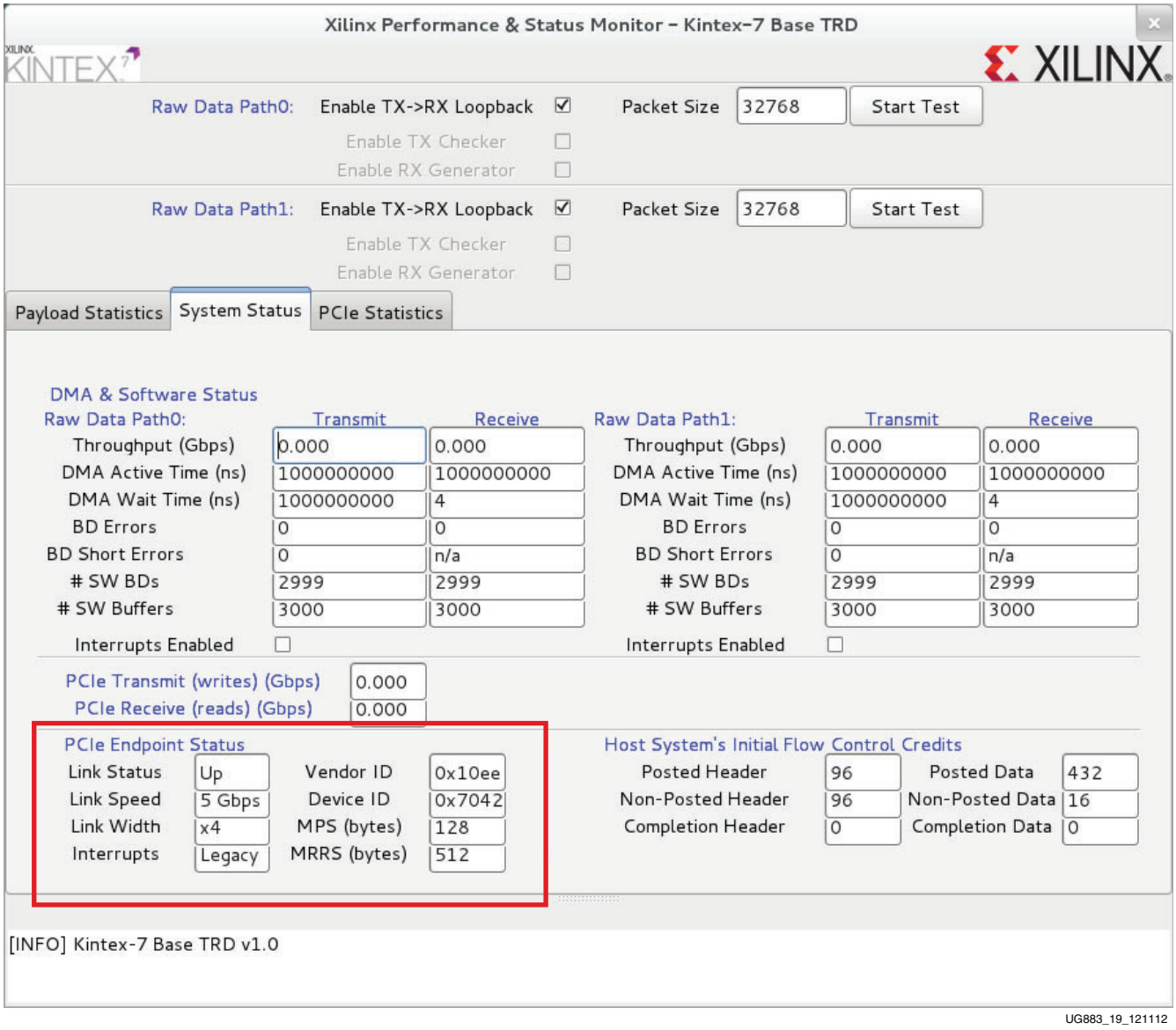


Figure 19: **Verify Board Status in the Performance Monitor**

Table 3: **KC705 Board Status Field Explanations**

Field	Status	Explanation
Link Status	Up	This confirms that the PCIe link is up and a PCIe connection is established between the Kintex-7 FPGA Endpoint for PCI Express and the PC motherboard chipset.
Link Speed	5.0 Gb/s	This confirms that the PCIe link is operating at line rate speed per PCI Express, v2.0.
Link Width	x4	This confirms that the PCIe link is trained as a x4 link.

2. To start data traffic on the two data paths:
   a. Click **`Start Test`** on `Raw Data Path0` as shown in Figure 20. This enables the driver to start generating the data for `Raw Data Path0`.
   b. Click **`Start Test`** on `Raw Data Path1` as shown in Figure 20. This enables the driver to start generating the data for `Raw Data Path1`.

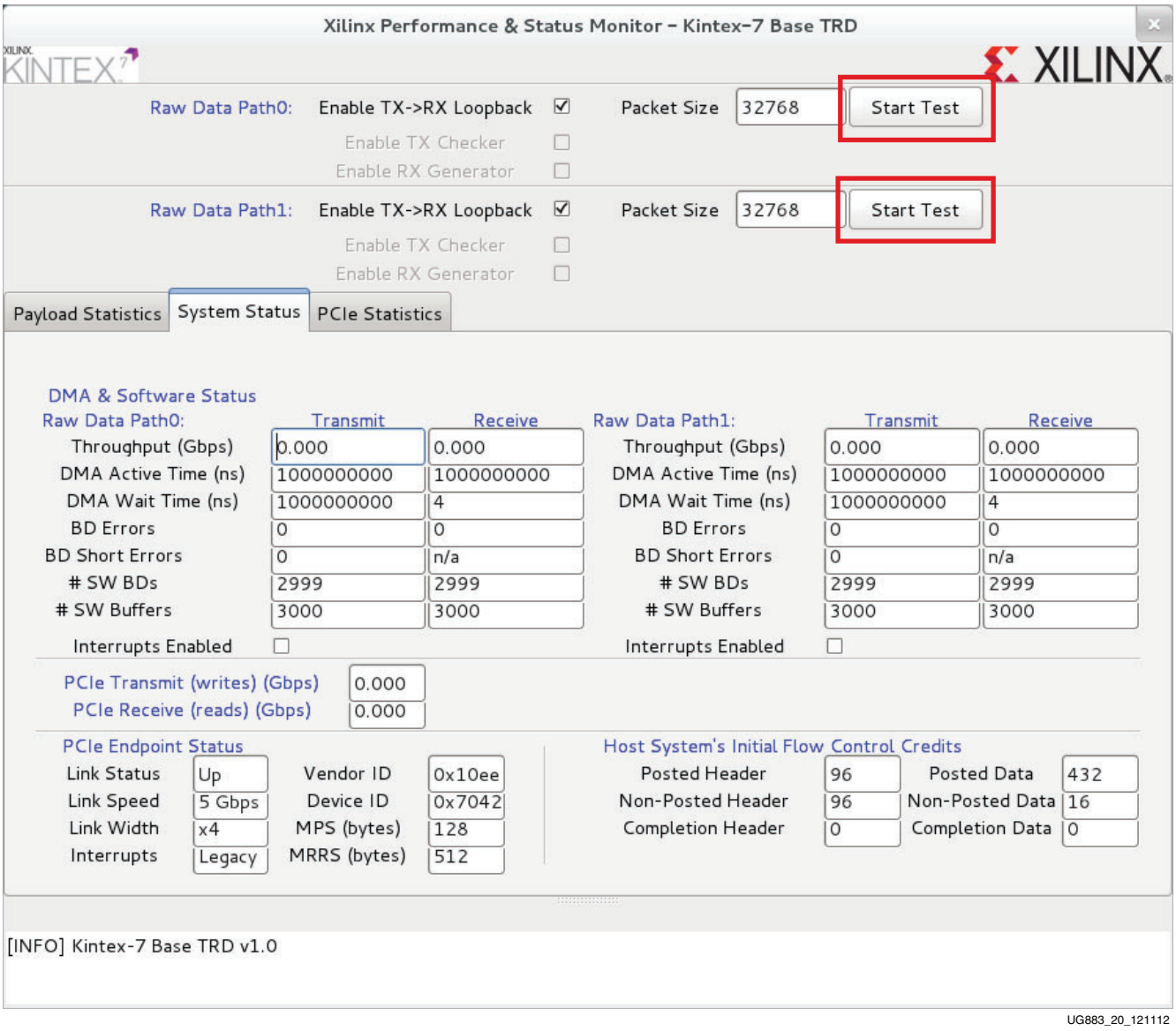


Figure 20: **Start Data Traffic from the Performance Monitor**

3. Verify TRD operations through the status information provided by the GUI (see Figure 21).
   a. Verify the PCIe throughput.
   b. Verify the DMA channel throughput for the `Raw Data Path0`.
   c. Verify the DMA channel throughput for the `Raw Data Path1`.
   d. Verify there are no buffer descriptor errors for error-free operation.

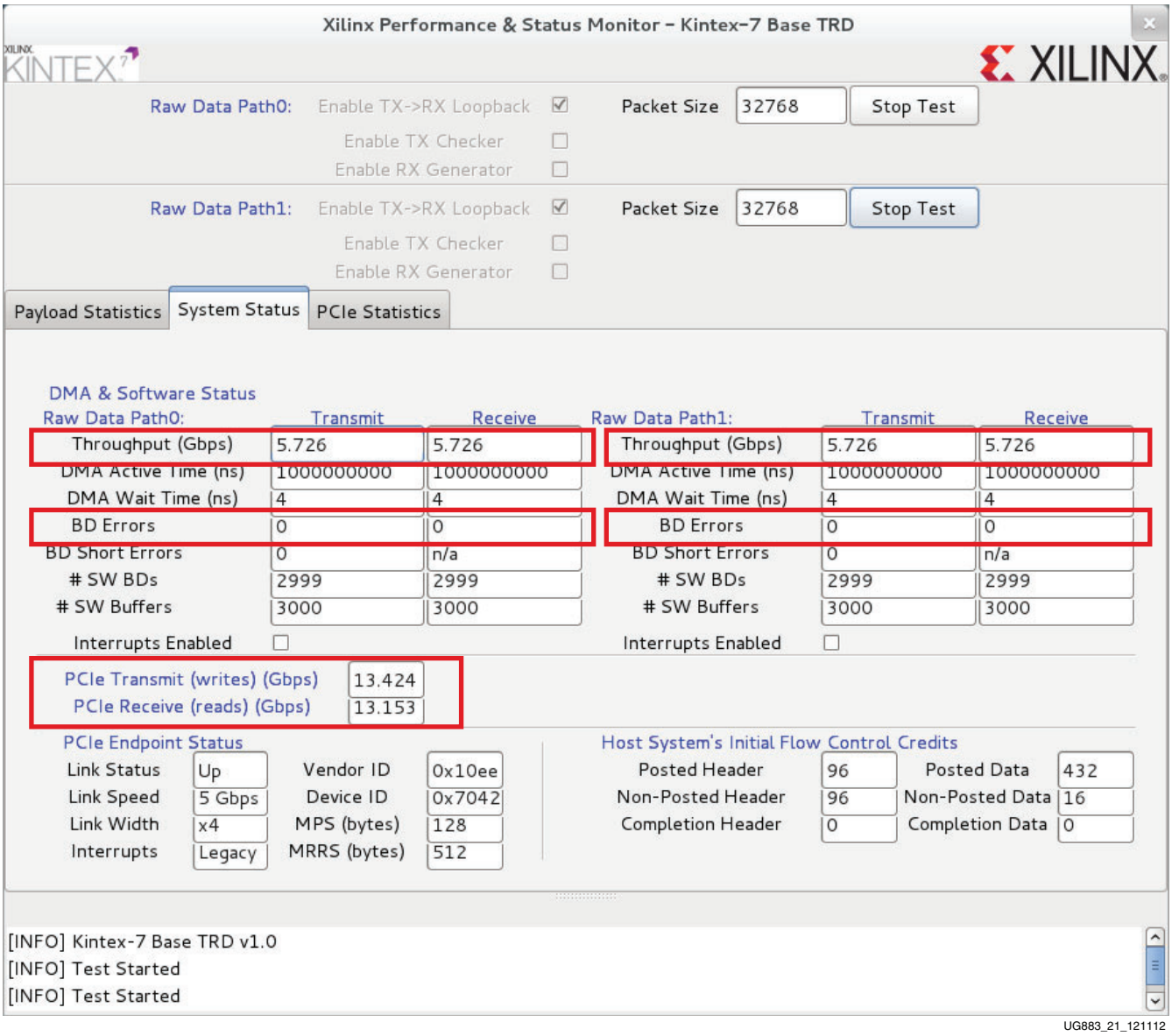


Figure 21: **Verify Error-Free Operation in the Performance Monitor**

The Kintex-7 FPGA PCIe-DMA TRD is now set up and running. Close the Application GUI to unload the software drivers and stop traffic flow.

Evaluating the Kintex-7 FPGA Base TRD

The Kintex-7 FPGA Base TRD provides a Performance and Status monitor application and GUI. The application enables customers to evaluate different system parameters. This section demonstrates performance variances for the PCI Express and DMA interfaces based on the parameters set.

To evaluate the Kintex-7 FPGA Base TRD:

1. Launch the Performance Monitor for the Kintex-7 FPGA Base TRD.
   a. Navigate to the `k7_pcie_dma_ddr3_base` folder.
   b. Double-click `k7_lin_trd_quickstart` (Figure 22)—make sure that the script has executable permission—to launch the Performance Monitor and Status GUI.

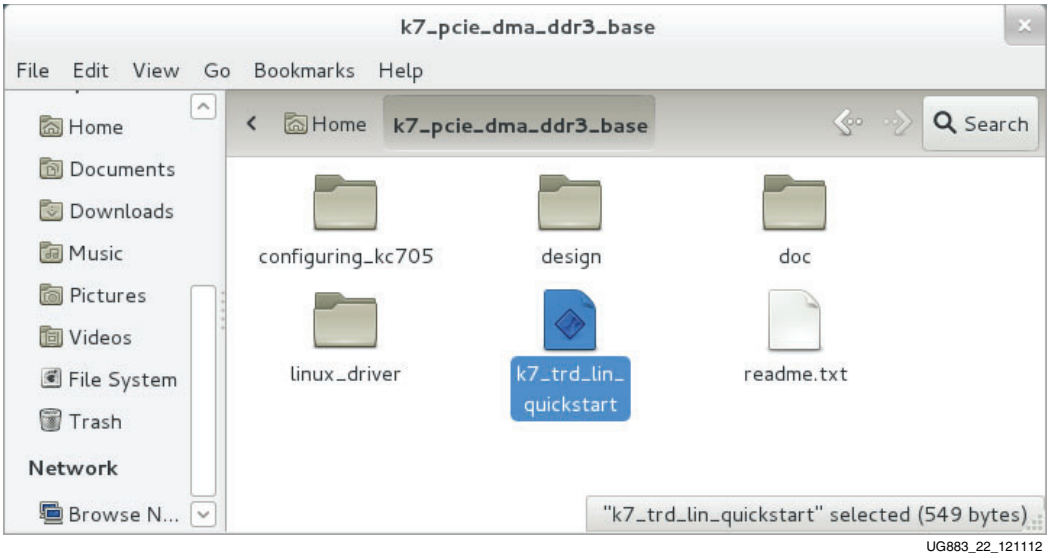


Figure 22: **Launch the Performance Monitor and Status GUI**

   c. A window prompt appears as shown in Figure 23. Click **Run in Terminal** to proceed.

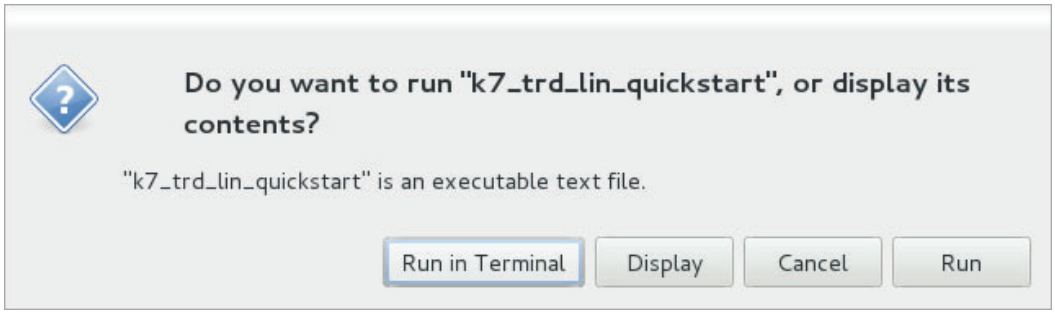


Figure 23: **Run k7_lin_trd_quickstart**

2. Set up the test parameters in the Performance Monitor.
   a. Two data paths are available: `Raw Data Path0` and `Raw Data Path1`. On each path, set the `Packet Size` to a value between 64 – 32,768 bytes.

3. Execute the test, and view payload statistics in the Performance and Status Monitor (see Figure 24).
   a. Click **`Start Test`** to start the performance test.
   b. Click the **`Payload Statistics`** tab to view data transfers on the DMA channels.
   c. Click **`Stop Test`** to stop data traffic.

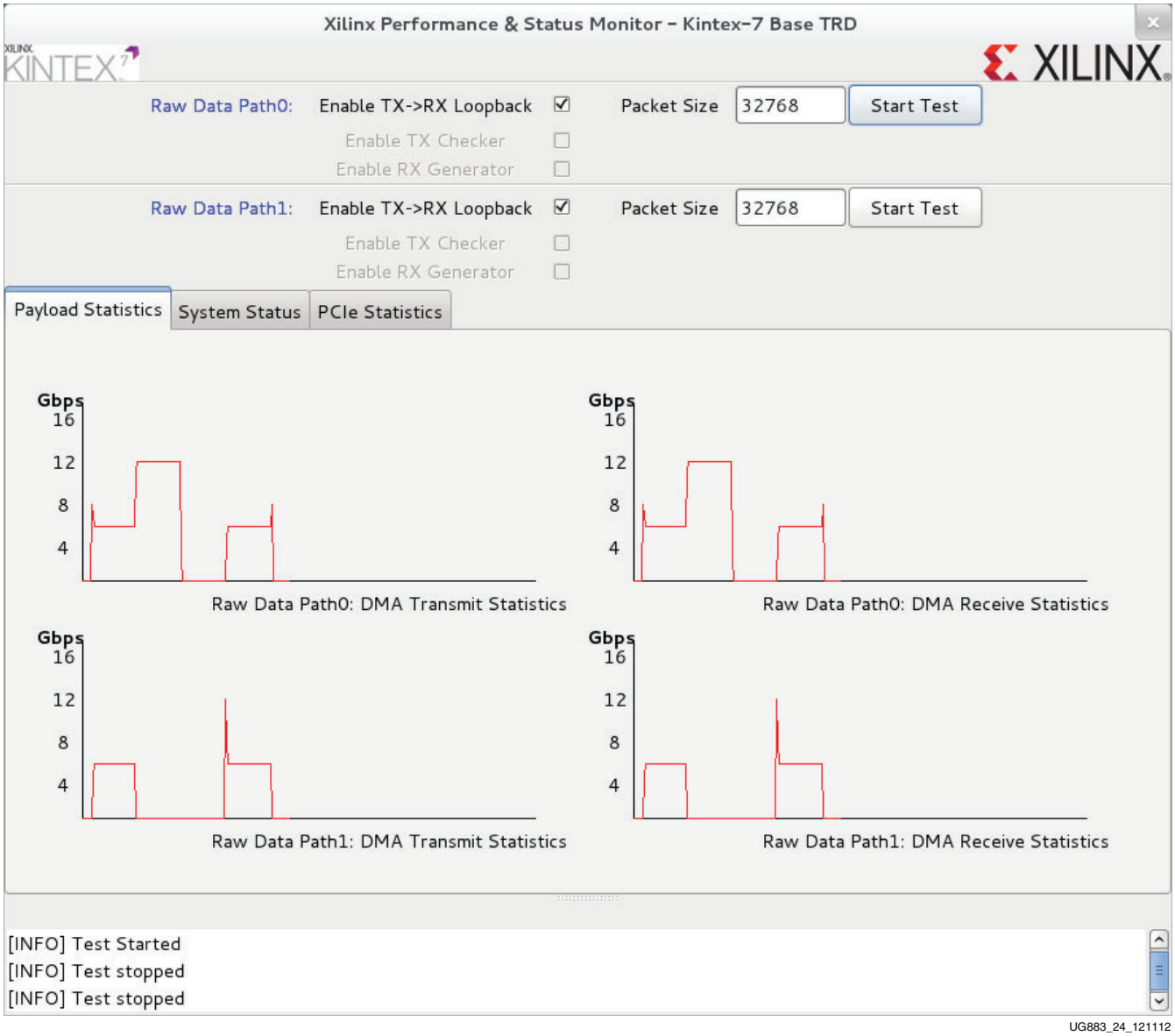


Figure 24: **Payload Statistics**

   d. Vary the Packet Size parameters for the Raw Data Paths (see Figure 25) and click **`Start Test`**. Then view the payload statistics to review data transfer rate on the DMA channels. With a decrease in packet size, the performance drops.

Note: Before changing packet size, click **`Stop Test`**, change the size, and then click **`Start Test`**.

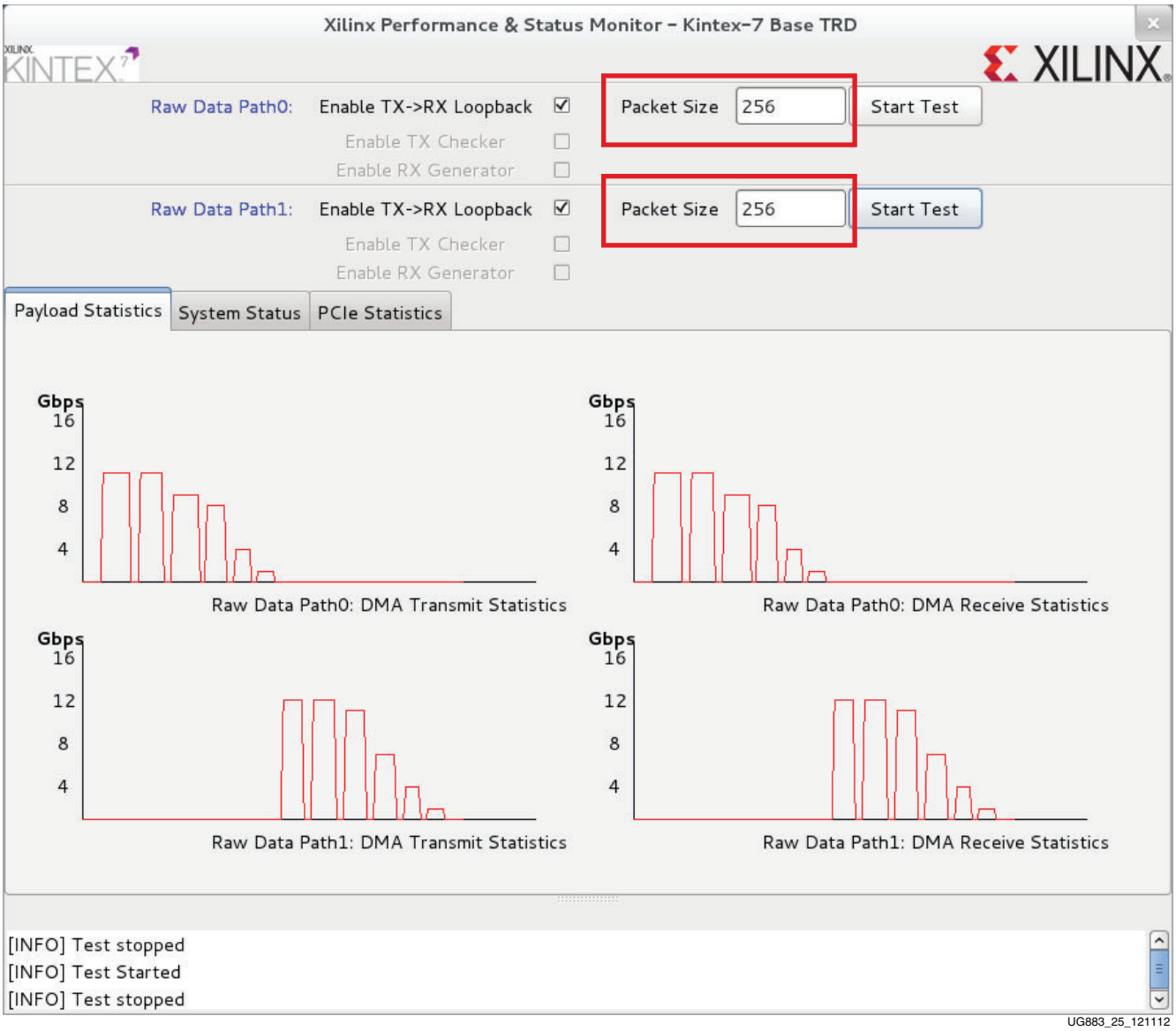


Figure 25: **Effect of Varying Packet Sizes on Performance**

Note: For packet sizes equal to 64 or 128 bytes, the throughput is reduced and might not be visible on the **`Payload Statistics`** tab. The exact values can be viewed on the **`System Status`** tab.

4. Click the **`PCIe Statistics`** tab to view data transfer numbers with varying packet sizes on the PCIe interface (Figure 26).

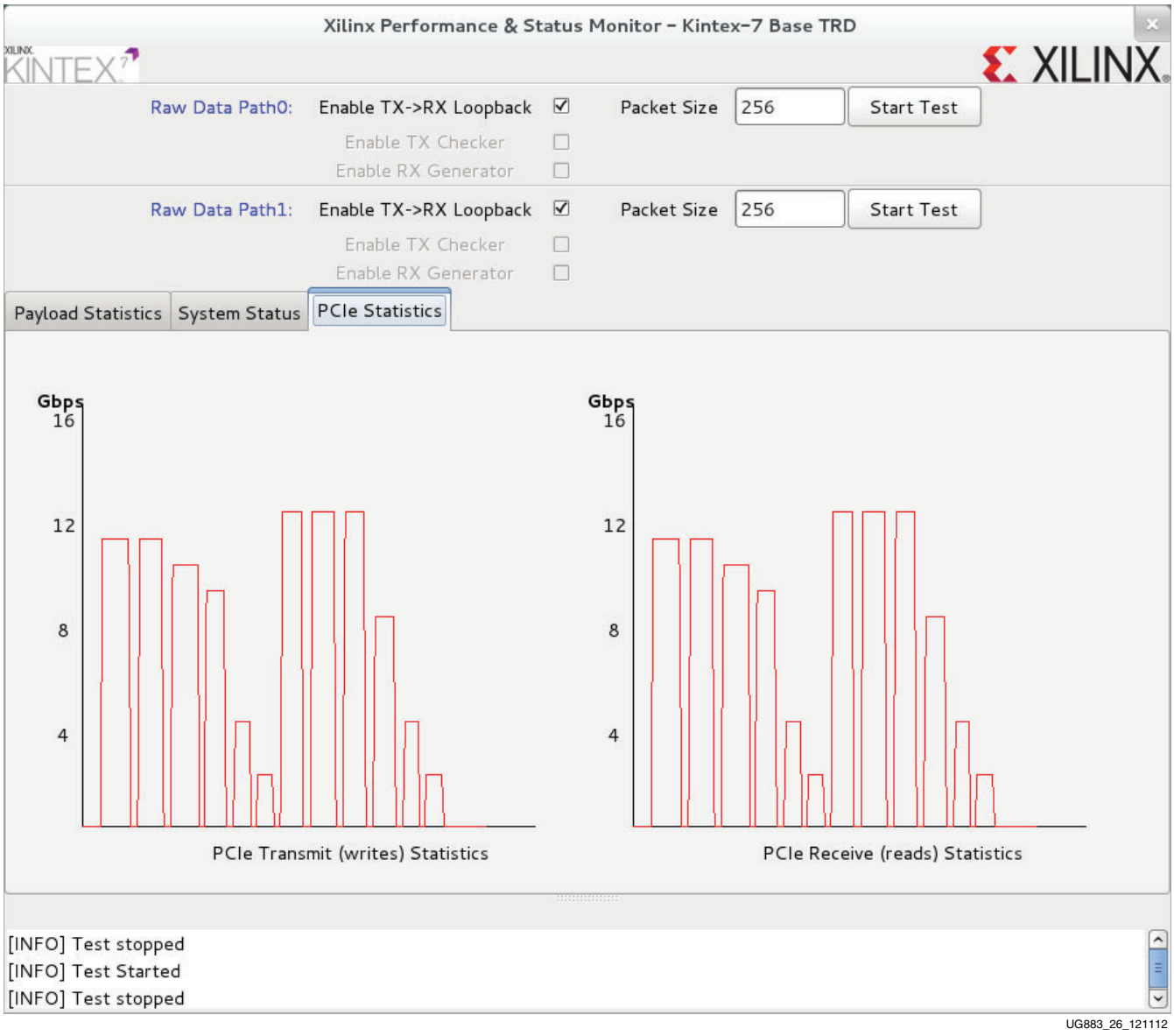


Figure 26: **PCIe Statistics in the Performance Monitor**

The system performance of the Kintex-7 FPGA Base TRD has now been evaluated using the pre-built demonstration design bit file.

Now that the Kintex-7 FPGA Base TRD demonstration has been set up and evaluated, the design can be modified. Before the design can be modified, make sure to install the Vivado Design Suite on a PC. It is not required that tools be installed on the PC system in which the KC705 evaluation board is plugged in by way of the PCIe edge connector.

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Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the KC705 board and its documentation is available on the following websites.

The Kintex-7 FPGA KC705 Evaluation Kit Product Page:

www.xilinx.com/kc705

The Kintex-7 FPGA KC705 Evaluation Kit Master Answer Record:

www.xilinx.com/support/answers/47787.htm

Design advisories by software release for the Kintex-7 FPGA KC705 Evaluation Kit:

www.xilinx.com/support/#nav=sd-nav-link-179661&tab=tab-bk

Kintex-7 FPGA Base Targeted Reference Design Release Notes and Known Issues Master Answer Record:

www.xilinx.com/support/answers/45679.htm

These documents provide supplemental material useful with this user guide:

UG810, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide*

UG845, *KC705 Reference Design User Guide*

UG798, *Xilinx Design Tools: Installation and Licensing Guide, Vivado Design Suite and ISE Design Suite*

UG908, *Vivado Design Suite User Guide: Programming and Debugging*

UG882, *Kintex-7 FPGA KC705 Base Targeted Reference Design User Guide (Vivado Design Suite 2012.4)*

UG886, *AMS101 Evaluation Card User Guide*

UG477, *7 Series FPGAs Integrated Block for PCI Express User Guide*

References

The following websites provide supplemental material useful with this guide:

1. LabVIEW 32-bit Run-Time Engine: http://joule.ni.com/nidu/cds/view/p/id/2534/lang/en
2. LabVIEW 64-bit Run-Time Engine: http://joule.ni.com/nidu/cds/view/p/id/2536/lang/en
3. Tera Term Pro program: http://hp.vector.co.jp/authors/VA002416/teraterm.html
4. Drivers on the Silicon Labs site: http://www.silabs.com/Support%20Documents/Software/CP210x_VCP_Win_XP_S2K3_Vista_7.exe
5. Northwest Logic DMA back end core: http://www.nwlogic.com/packetdma
6. Fedora project: http://fedoraproject.org

   Fedora is a Linux-based operating system used in the development of this TRD.
7. The GTK+ project API documentation: http://www.gtk.org/documentation.php

   GTK+ is a toolkit for creating graphical user interfaces (GUI).

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Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
(i) engineering samples or beta versions of Development Systems (which are provided "AS IS" without warranty); (ii) design defects or errors known as "errata";
(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

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