

# KAI-08050

## 3296 (H) x 2472 (V) Interline CCD Image Sensor

### Description

The KAI-08050 Image Sensor is an 8-megapixel CCD in a 4/3" optical format. Based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, the sensor features broad dynamic range, excellent imaging performance, and a flexible readout architecture that enables use of 1, 2, or 4 outputs. The sensor supports full resolution readout up to 16 frames per second, while a Region of Interest (ROI) mode supports partial readout of the sensor at even higher frame rates. A vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

The sensor shares common pin-out and electrical configurations with other devices based on the TRUESENSE 5.5 micron Interline Transfer Platform, allowing a single camera design to support multiple members of this sensor family.

**Table 1. GENERAL SPECIFICATIONS**

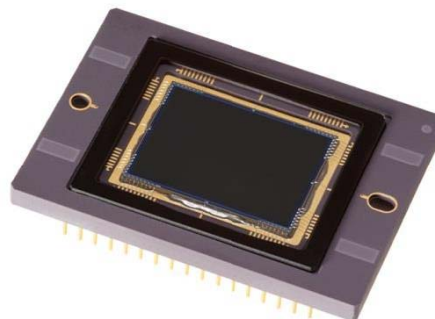
| Parameter                           | Typical Value                                                       |
|-------------------------------------|---------------------------------------------------------------------|
| Architecture                        | Interline CCD; Progressive Scan                                     |
| Total Number of Pixels              | 3364 (H) x 2520 (V)                                                 |
| Number of Effective Pixels          | 3320 (H) x 2496 (V)                                                 |
| Number of Active Pixels             | 3296 (H) x 2472 (V)                                                 |
| Pixel Size                          | 5.5 $\mu\text{m}$ (H) x 5.5 $\mu\text{m}$ (V)                       |
| Active Image Size                   | 18.13 mm (H) x 13.60 mm (V)<br>22.66 mm (diag), 4/3" optical format |
| Aspect Ratio                        | 4:3                                                                 |
| Number of Outputs                   | 1, 2, or 4                                                          |
| Charge Capacity                     | 20,000 electrons                                                    |
| Output Sensitivity                  | 34 $\mu\text{V}/\text{e}^-$                                         |
| Quantum Efficiency                  |                                                                     |
| Pan (-ABA, -PBA)                    | 46%                                                                 |
| R, G, B (-CBA, -PBA)                | 29%, 37%, 39%                                                       |
| Read Noise ( $f = 40 \text{ MHz}$ ) | 12 electrons rms                                                    |
| Dark Current                        |                                                                     |
| Photodiode                          | 7 electrons/s                                                       |
| VCCD                                | 100 electrons/s                                                     |
| Dark Current Doubling Temp.         |                                                                     |
| Photodiode                          | 7°C                                                                 |
| VCCD                                | 9°C                                                                 |
| Dynamic Range                       | 64 dB                                                               |
| Charge Transfer Efficiency          | 0.999999                                                            |
| Blooming Suppression                | > 300 X                                                             |
| Smear                               | -100 dB                                                             |
| Image Lag                           | < 10 electrons                                                      |
| Maximum Pixel Clock Speed           | 40 MHz                                                              |
| Maximum Frame Rates                 |                                                                     |
| Quad Output                         | 16 fps                                                              |
| Dual Output                         | 8 fps                                                               |
| Single Output                       | 4 fps                                                               |
| Package                             | 68 pin PGA                                                          |
| Cover Glass                         | AR coated, 2 Sides or Clear Glass                                   |

NOTE: All parameters are specified at  $T = 40^\circ\text{C}$  unless otherwise noted.



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)



**Figure 1. KAI-08050 CCD Image Sensor**

### Features

- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome Configuration
- Progressive Scan Readout
- Flexible Readout Architecture
- High Frame Rate
- High Sensitivity
- Low Noise Architecture
- Excellent Smear Performance
- Package Pin Reserved for Device Identification

### Applications

- Industrial Imaging
- Medical Imaging
- Security

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# KAI-08050

## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION**

| Part Number         | Description                                                                                                                                     | Marking Code                   |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| KAI-08050-AAA-JP-BA | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade                                                     | KAI-08050-AAA<br>Serial Number |
| KAI-08050-AAA-JP-AE | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Grade                                                  |                                |
| KAI-08050-ABA-JD-BA | Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade                           | KAI-08050-ABA<br>Serial Number |
| KAI-08050-ABA-JD-AE | Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade                        |                                |
| KAI-08050-ABA-JP-BA | Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade                                            |                                |
| KAI-08050-ABA-JP-AE | Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Grade                                         |                                |
| KAI-08050-CBA-JD-BA | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade               | KAI-08050-CBA<br>Serial Number |
| KAI-08050-CBA-JD-AE | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade            |                                |
| KAI-08050-CBA-JB-B2 | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2                                     |                                |
| KAI-08050-CBA-JB-AE | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Engineering Grade                           |                                |
| KAI-08050-PBA-JD-BA | Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade    | KAI-08050-PBA<br>Serial Number |
| KAI-08050-PBA-JD-AE | Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade |                                |

NOTE: Not recommended for new designs. Consider device KAI-08051.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).



### ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and

power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

### Bayer Color Filter Pattern

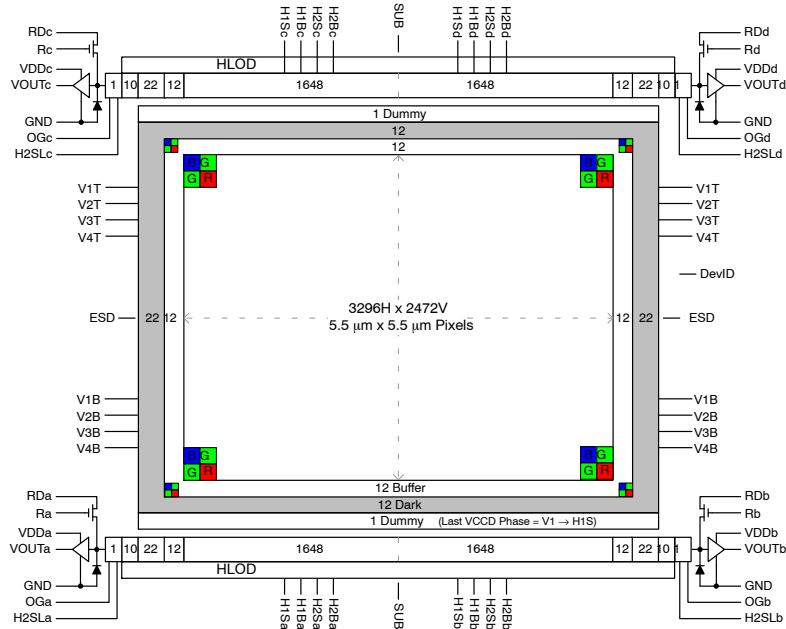


Figure 3. Bayer Color Filter Pattern

### TRUESENSE Sparse Color Filter Pattern

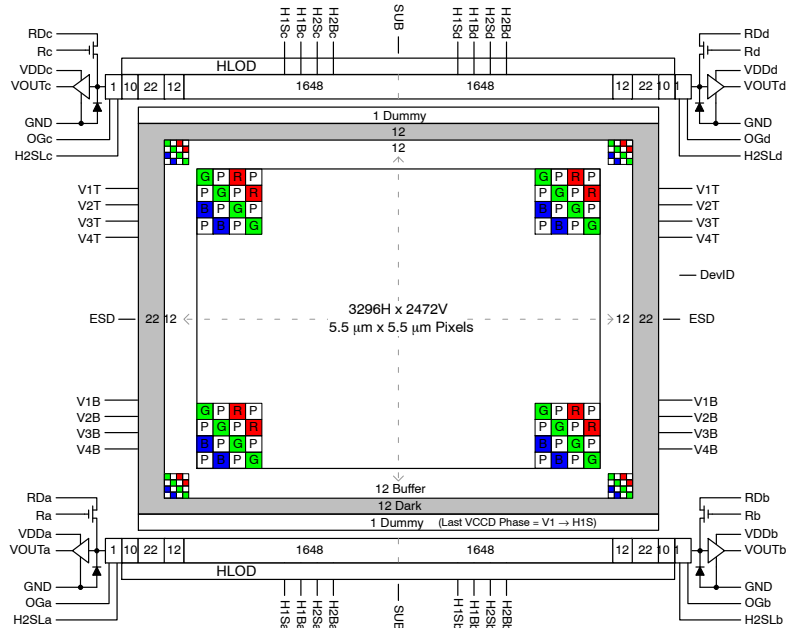


Figure 4. TRUESENSE Sparse Color Filter Pattern

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

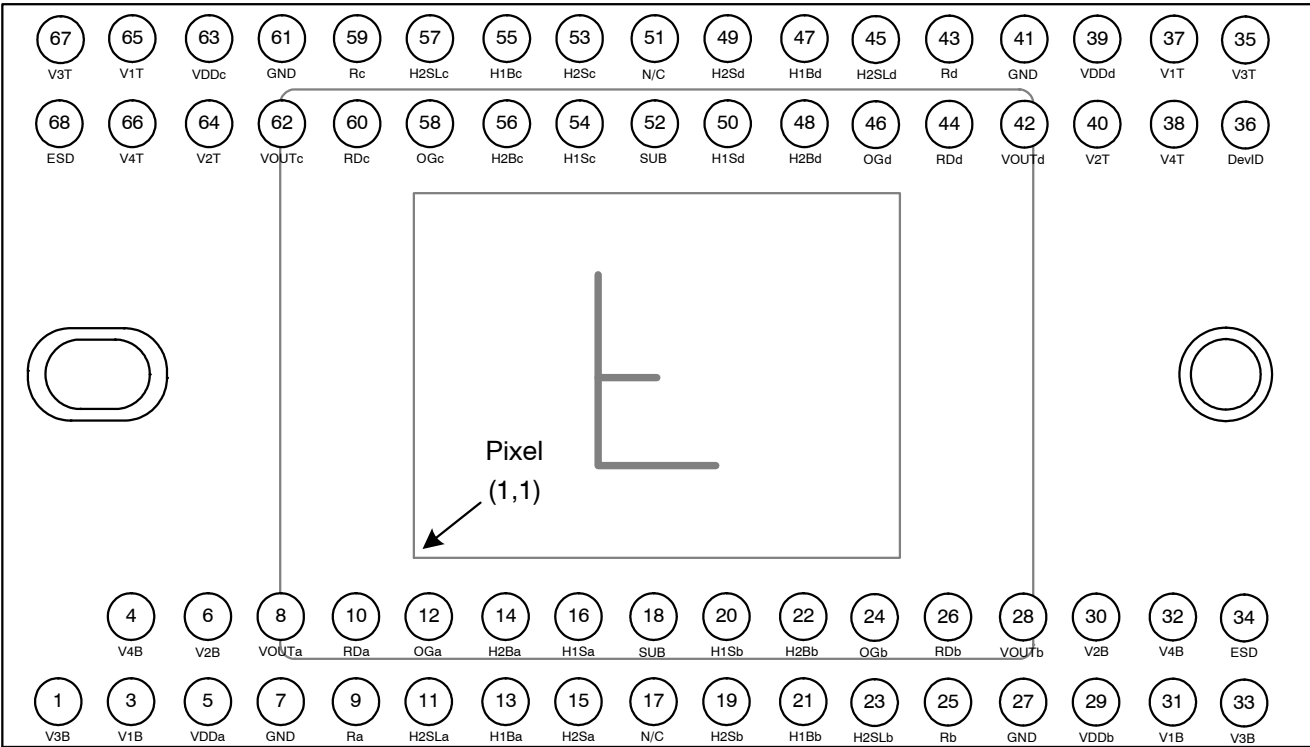


Figure 5. Package Pin Designations – Top View

Table 3. PIN DESCRIPTION

| Pin | Name  | Description                                                    |
|-----|-------|----------------------------------------------------------------|
| 1   | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 3   | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 4   | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 5   | VDDa  | Output Amplifier Supply, Quadrant a                            |
| 6   | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 7   | GND   | Ground                                                         |
| 8   | VOUTa | Video Output, Quadrant a                                       |
| 9   | Ra    | Reset Gate, Quadrant a                                         |
| 10  | RDa   | Reset Drain, Quadrant a                                        |
| 11  | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 12  | OGa   | Output Gate, Quadrant a                                        |
| 13  | H1Ba  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a             |
| 14  | H2Ba  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a             |
| 15  | H2Sa  | Horizontal CCD Clock, Phase 2, Storage, Quadrant a             |
| 16  | H1Sa  | Horizontal CCD Clock, Phase 1, Storage, Quadrant a             |
| 17  | N/C   | No Connect                                                     |
| 18  | SUB   | Substrate                                                      |
| 19  | H2Sb  | Horizontal CCD Clock, Phase 2, Storage, Quadrant b             |
| 20  | H1Sb  | Horizontal CCD Clock, Phase 1, Storage, Quadrant b             |
| 21  | H1Bb  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b             |
| 22  | H2Bb  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b             |
| 23  | H2SLb | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b |
| 24  | OGb   | Output Gate, Quadrant b                                        |
| 25  | Rb    | Reset Gate, Quadrant b                                         |
| 26  | RDb   | Reset Drain, Quadrant b                                        |
| 27  | GND   | Ground                                                         |
| 28  | VOUTb | Video Output, Quadrant b                                       |
| 29  | VDDb  | Output Amplifier Supply, Quadrant b                            |
| 30  | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 31  | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 32  | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 33  | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 34  | ESD   | ESD Protection Disable                                         |

| Pin | Name  | Description                                                    |
|-----|-------|----------------------------------------------------------------|
| 68  | ESD   | ESD Protection Disable                                         |
| 67  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 66  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 65  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 64  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 63  | VDDc  | Output Amplifier Supply, Quadrant c                            |
| 62  | VOUTc | Video Output, Quadrant c                                       |
| 61  | GND   | Ground                                                         |
| 60  | RDc   | Reset Drain, Quadrant c                                        |
| 59  | Rc    | Reset Gate, Quadrant c                                         |
| 58  | OGc   | Output Gate, Quadrant c                                        |
| 57  | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 56  | H2Bc  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c             |
| 55  | H1Bc  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c             |
| 54  | H1Sc  | Horizontal CCD Clock, Phase 1, Storage, Quadrant c             |
| 53  | H2Sc  | Horizontal CCD Clock, Phase 2, Storage, Quadrant c             |
| 52  | SUB   | Substrate                                                      |
| 51  | N/C   | No Connect                                                     |
| 50  | H1Sd  | Horizontal CCD Clock, Phase 1, Storage, Quadrant d             |
| 49  | H2Sd  | Horizontal CCD Clock, Phase 2, Storage, Quadrant d             |
| 48  | H2Bd  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d             |
| 47  | H1Bd  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d             |
| 46  | OGd   | Output Gate, Quadrant d                                        |
| 45  | H2SLd | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 44  | RDd   | Reset Drain, Quadrant d                                        |
| 43  | Rd    | Reset Gate, Quadrant d                                         |
| 42  | VOUTd | Video Output, Quadrant d                                       |
| 41  | GND   | Ground                                                         |
| 40  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 39  | VDDd  | Output Amplifier Supply, Quadrant d                            |
| 38  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 37  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 36  | DevID | Device Identification                                          |
| 35  | V3T   | Vertical CCD Clock, Phase 3, Top                               |

1. Liked named pins are internally connected and should have a common drive signal.
2. N/C pins (17, 51) should be left floating.

## IMAGING PERFORMANCE

**Table 4. TYPICAL OPERATION CONDITIONS**

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

| Description  | Condition                                       | Notes                                       |
|--------------|-------------------------------------------------|---------------------------------------------|
| Light Source | Continuous red, green and blue LED illumination | For monochrome sensor, only green LED used. |
| Operation    | Nominal operating voltages and timing           |                                             |

**Table 5. SPECIFICATIONS**  
**All Configurations**

| Description                                          | Symbol              | Min.     | Nom.     | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------------------------|---------------------|----------|----------|------|-------|---------------|----------------------------|-------|
| Dark Field Global Non-Uniformity                     | DSNU                | –        | –        | 2    | mVpp  | Die           | 27, 40                     |       |
| Bright Field Global Non-Uniformity                   |                     | –        | 2        | 5    | %rms  | Die           | 27, 40                     | 1     |
| Bright Field Global Peak to Peak Non-Uniformity      | PRNU                | –        | 5        | 15   | %pp   | Die           | 27, 40                     | 1     |
| Bright Field Center Non-Uniformity                   |                     | –        | 1        | 2    | %rms  | Die           | 27, 40                     | 1     |
| Maximum Photoresponse Nonlinearity                   | NL                  | –        | 2        | –    | %     | Design        |                            | 2     |
| Maximum Gain Difference Between Outputs              | $\Delta G$          | –        | 10       | –    | %     | Design        |                            | 2     |
| Maximum Signal Error due to Nonlinearity Differences | $\Delta NL$         | –        | 1        | –    | %     | Design        |                            | 2     |
| Horizontal CCD Charge Capacity                       | HNe                 | –        | 55       | –    | ke–   | Design        |                            |       |
| Vertical CCD Charge Capacity                         | VNe                 | –        | 40       | –    | ke–   | Design        |                            |       |
| Photodiode Charge Capacity                           | PNe                 | –        | 20       | –    | ke–   | Die           | 27, 40                     | 3     |
| Horizontal CCD Charge Transfer Efficiency            | HCTE                | 0.999995 | 0.999999 | –    |       | Die           |                            |       |
| Vertical CCD Charge Transfer Efficiency              | VCTE                | 0.999995 | 0.999999 | –    |       | Die           |                            |       |
| Photodiode Dark Current                              | l <sub>pd</sub>     | –        | 7        | 70   | e/p/s | Die           | 40                         |       |
| Vertical CCD Dark Current                            | l <sub>vd</sub>     | –        | 100      | 300  | e/p/s | Die           | 40                         |       |
| Image Lag                                            | Lag                 | –        | –        | 10   | e–    | Design        |                            |       |
| Antiblooming Factor                                  | X <sub>ab</sub>     | 300      | –        | –    |       | Design        |                            |       |
| Vertical Smear                                       | S <sub>mr</sub>     | –        | –100     | –    | dB    | Design        |                            |       |
| Read Noise                                           | n <sub>e–T</sub>    | –        | 12       | –    | e–rms | Design        |                            | 4     |
| Dynamic Range                                        | DR                  | –        | 64       | –    | dB    | Design        |                            | 4, 5  |
| Output Amplifier DC Offset                           | V <sub>odc</sub>    | –        | 9.4      | –    | V     | Die           | 27, 40                     |       |
| Output Amplifier Bandwidth                           | f <sub>–3db</sub>   | –        | 250      | –    | MHz   | Die           |                            | 6     |
| Output Amplifier Impedance                           | R <sub>OUT</sub>    | –        | 127      | –    | Ω     | Die           | 27, 40                     |       |
| Output Amplifier Sensitivity                         | $\Delta V/\Delta N$ | –        | 34       | –    | μV/e– | Design        |                            |       |

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz
5. Uses 20LOG (PNe/ n<sub>e–T</sub>)
6. Assumes 5 pF load.

# KAI-08050

**Table 6. KAI-08050-ABA AND KAI-08050-PBA CONFIGURATIONS**

| Description                        | Symbol            | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|-------------------|------|------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | QE <sub>max</sub> | –    | 44   | –    | %     | Design        |                            |       |
| Peak Quantum Efficiency Wavelength | λQE               | –    | 480  | –    | nm    | Design        |                            | 7     |

7. Not recommended for new designs. Consider device KAI-08051.

**Table 7. KAI-08050-CBA AND KAI-08050-PBA GEN1 COLOR CONFIGURATIONS WITH MAR GLASS**

| Description                        |                      | Symbol            | Min. | Nom.              | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|------|-------------------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | –    | 39<br>37<br>29    | –    | %     | Design        |                            | 7     |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λQE               | –    | 470<br>540<br>620 | –    | nm    | Design        |                            | 7     |

**Table 8. KAI-08050-CBA GEN1 COLOR CONFIGURATION WITH CLEAR GLASS**

| Description                        |                      | Symbol            | Min. | Nom.              | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|------|-------------------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | –    | 36<br>34<br>27    | –    | %     | Design        |                            | 7     |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λQE               | –    | 470<br>540<br>620 | –    | nm    | Design        |                            | 7     |



## TYPICAL PERFORMANCE CURVES

### Quantum Efficiency

Monochrome, all configurations

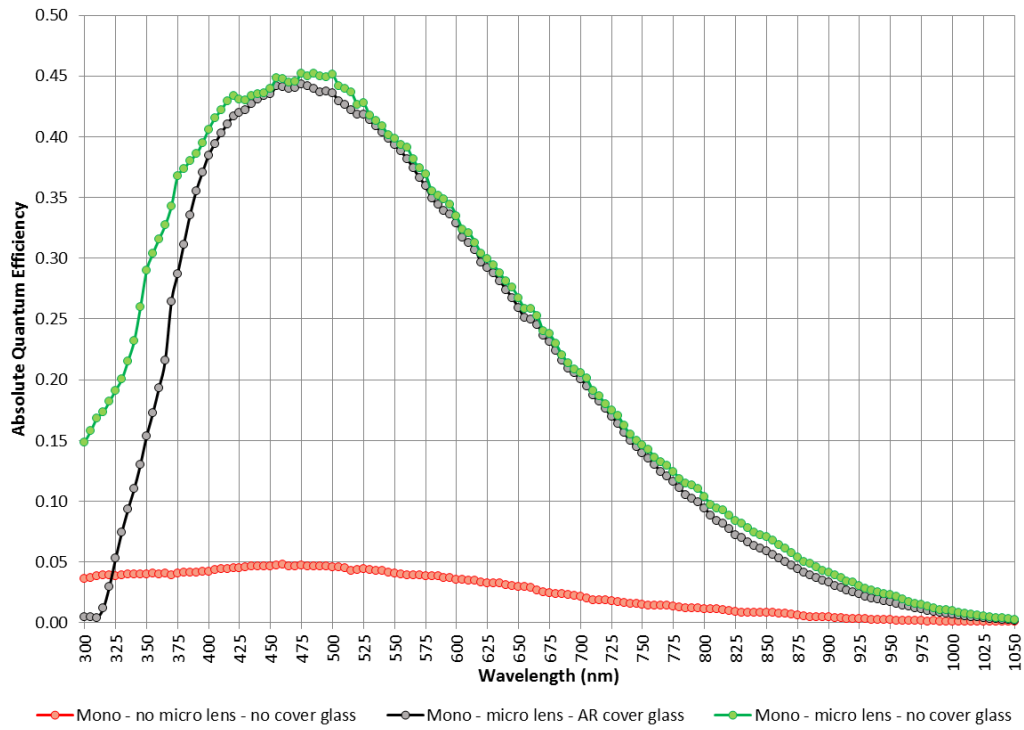


Figure 6. Monochrome Configurations – Quantum Efficiency

Color (Bayer RGB) with Microlens (Gen1 CFA)

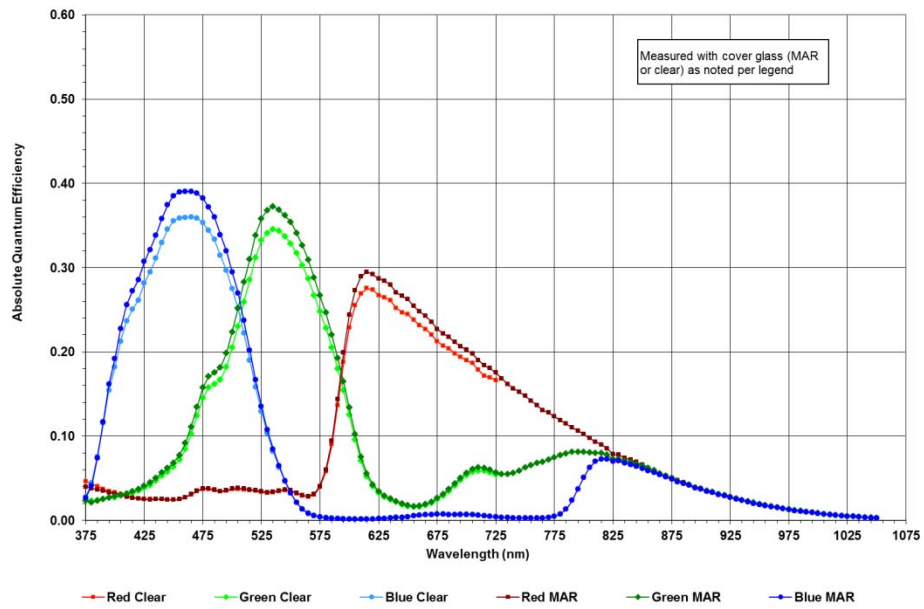


Figure 7. Color with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens (Gen1 CFA)

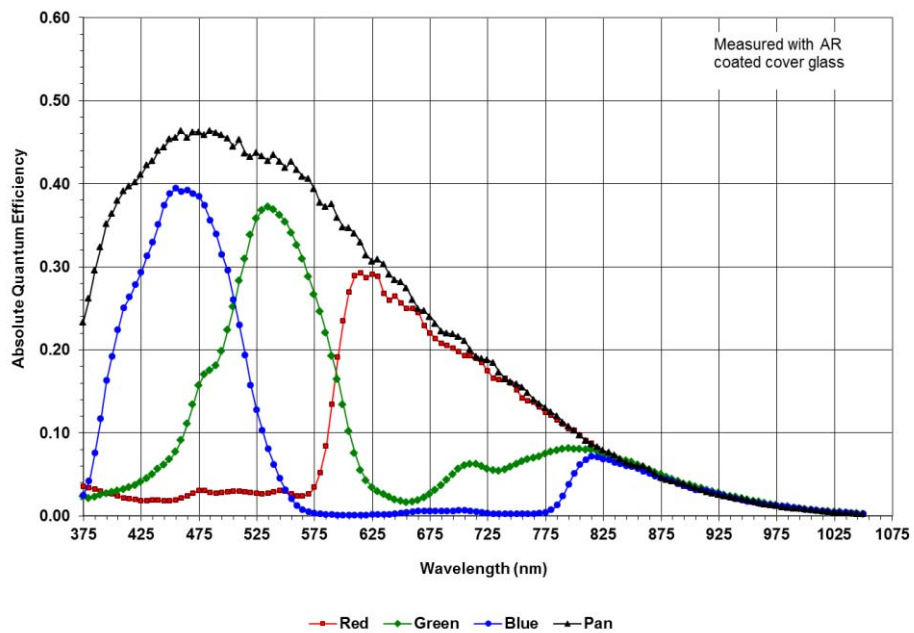


Figure 8. Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

### Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

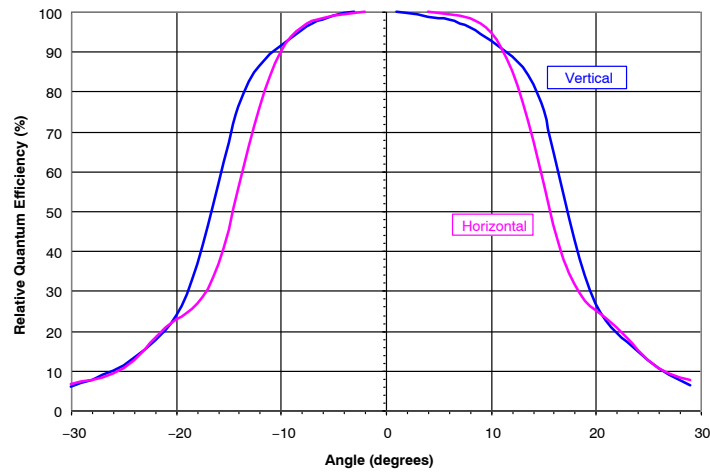


Figure 9. Monochrome with Microlens Angular Quantum Efficiency

### Dark Current versus Temperature

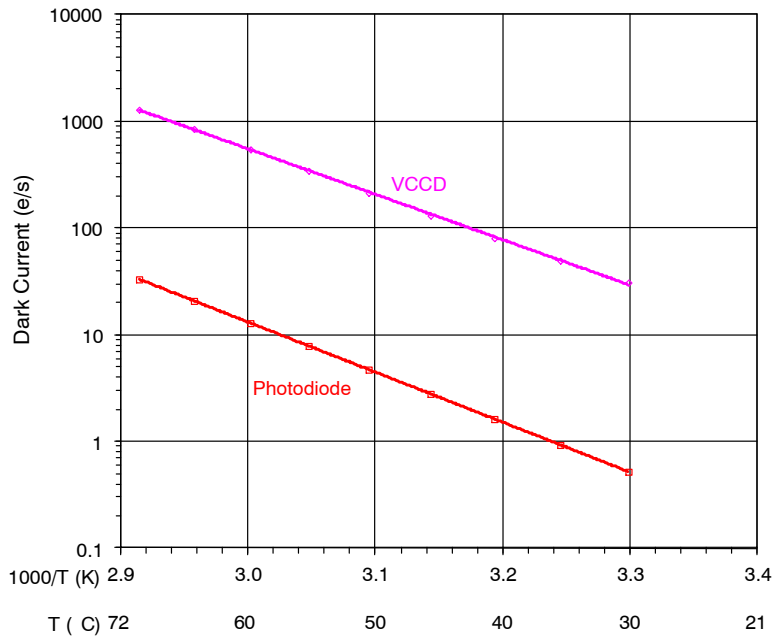


Figure 10. Dark Current versus Temperature

Power – Estimated

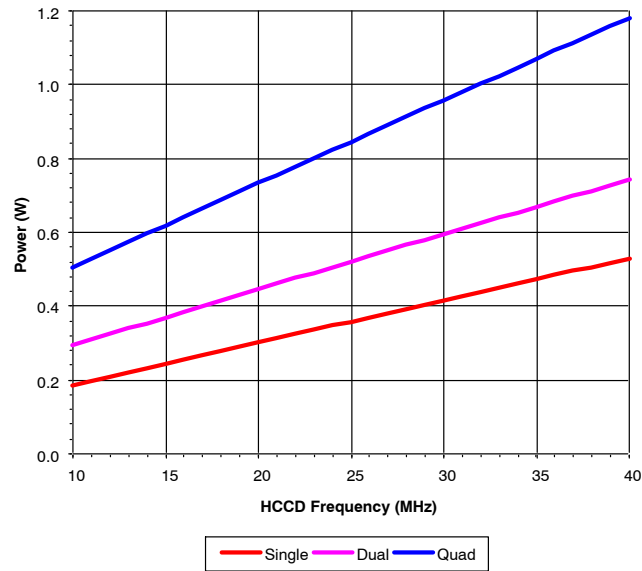


Figure 11. Power

Frame Rates

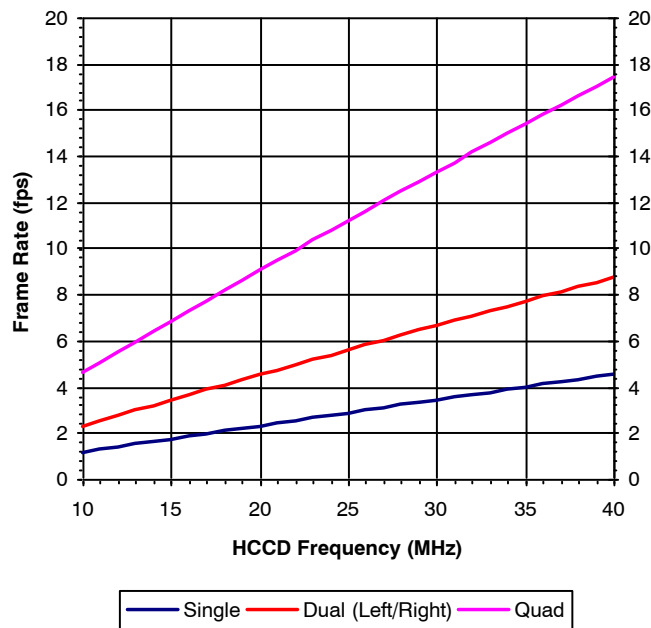


Figure 12. Frame Rates

## DEFECT DEFINITIONS

Table 9. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

| Description                 | Condition                                                             | Notes |
|-----------------------------|-----------------------------------------------------------------------|-------|
| Operational Mode            | Two outputs, using VOUTa and VOUTc, continuous readout                |       |
| HCCD Clock Frequency        | 10 MHz                                                                |       |
| Pixels Per Line             | 3520                                                                  | 1     |
| Lines Per Frame             | 1360                                                                  | 2     |
| Line Time                   | 354.9 $\mu$ sec                                                       |       |
| Frame Time                  | 482.7 msec                                                            |       |
| Photodiode Integration Time | Mode A: PD_Tint = Frame Time = 482.7 msec, no electronic shutter used |       |
|                             | Mode B: PD_Tint = 33 msec, electronic shutter used                    |       |
| VCCD Integration Time       | 447.2 msec                                                            | 3     |
| Temperature                 | 40°C                                                                  |       |
| Light Source                | Continuous red, green and blue LED illumination                       | 4     |
| Operation                   | Nominal operating voltages and timing                                 |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 1260 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

Table 10. DEFECT DEFINITIONS FOR TESTING AT 40°C

| Description                             | Definition                                                                                                      | Standard Grade | Grade 2 | Notes |
|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------|----------------|---------|-------|
| Major dark field defective bright pixel | PD_Tint = Mode A $\rightarrow$ Defect $\geq$ 166 mV<br>or<br>PD_Tint = Mode B $\rightarrow$ Defect $\geq$ 12 mV | 80             | 80      | 1     |
| Major bright field defective dark pixel | Defect $\geq$ 12%                                                                                               |                |         |       |
| Minor dark field defective bright pixel | PD_Tint = Mode A $\rightarrow$ Defect $\geq$ 86 mV<br>or<br>PD_Tint = Mode B $\rightarrow$ Defect $\geq$ 6 mV   | 800            | 800     |       |
| Cluster defect                          | A group of 2 to 10 contiguous major defective pixels, but no more than 3 adjacent defects horizontally.         | 15             | n/a     | 2     |
| Cluster defect (grade 2)                | A group of 2 to 10 contiguous major defective pixels                                                            | n/a            | 15      | 2     |
| Column defect                           | A group of more than 10 contiguous major defective pixels along a single column                                 | 0              | 0       | 2     |

1. For the color device (KAI-08050-CBA or KAI-08050-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

**Table 11. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C**

| Description                           | Condition                                                             | Notes |
|---------------------------------------|-----------------------------------------------------------------------|-------|
| Operational Mode                      | Two outputs, using VOUTa and VOUTc, continuous readout                |       |
| HCCD Clock Frequency                  | 20 MHz                                                                |       |
| Pixels Per Line                       | 3520                                                                  | 1     |
| Lines Per Frame                       | 1360                                                                  | 2     |
| Line Time                             | 177.8 $\mu$ sec                                                       |       |
| Frame Time                            | 241.8 msec                                                            |       |
| Photodiode Integration Time (PD_Tint) | Mode A: PD_Tint = Frame Time = 241.8 msec, no electronic shutter used |       |
|                                       | Mode B: PD_Tint = 33 msec, electronic shutter used                    |       |
| VCCD Integration Time                 | 224.0 msec                                                            | 3     |
| Temperature                           | 27°C                                                                  |       |
| Light Source                          | Continuous red, green and blue LED illumination                       | 4     |
| Operation                             | Nominal operating voltages and timing                                 |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 1260 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

**Table 12. DEFECT DEFINITIONS FOR TESTING AT 27°C**

| Description                             | Definition                                                                                                    | Standard Grade | Grade 2 | Notes |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------|----------------|---------|-------|
| Major dark field defective bright pixel | PD_Tint = Mode A $\rightarrow$ Defect $\geq$ 26 mV<br>or<br>PD_Tint = Mode B $\rightarrow$ Defect $\geq$ 4 mV | 80             | 80      | 1     |
| Major bright field defective dark pixel | Defect $\geq$ 12%                                                                                             |                |         |       |
| Cluster defect                          | A group of 2 to 10 contiguous major defective pixels, but no more than 3 adjacent defects horizontally.       | 15             | n/a     | 2     |
| Cluster defect (grade 2)                | A group of 2 to 10 contiguous major defective pixels                                                          | n/a            | 15      | 2     |
| Column defect                           | A group of more than 10 contiguous major defective pixels along a single column                               | 0              | 0       | 2     |

1. For the color device (KAI-08050-CBA or KAI-08050-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point

defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 13: Regions of interest for the location of pixel 1,1.

## TEST DEFINITIONS

### Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (3320, 2496)  
 Active Area ROI: Pixel (13, 13) to Pixel (3308, 2484)  
 Center ROI: Pixel (1611, 1199) to Pixel (1710, 1298)  
 Only the Active Area ROI pixels are used for performance and defect tests.

### Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions.

See Figure 13 for a pictorial representation of the regions of interest.

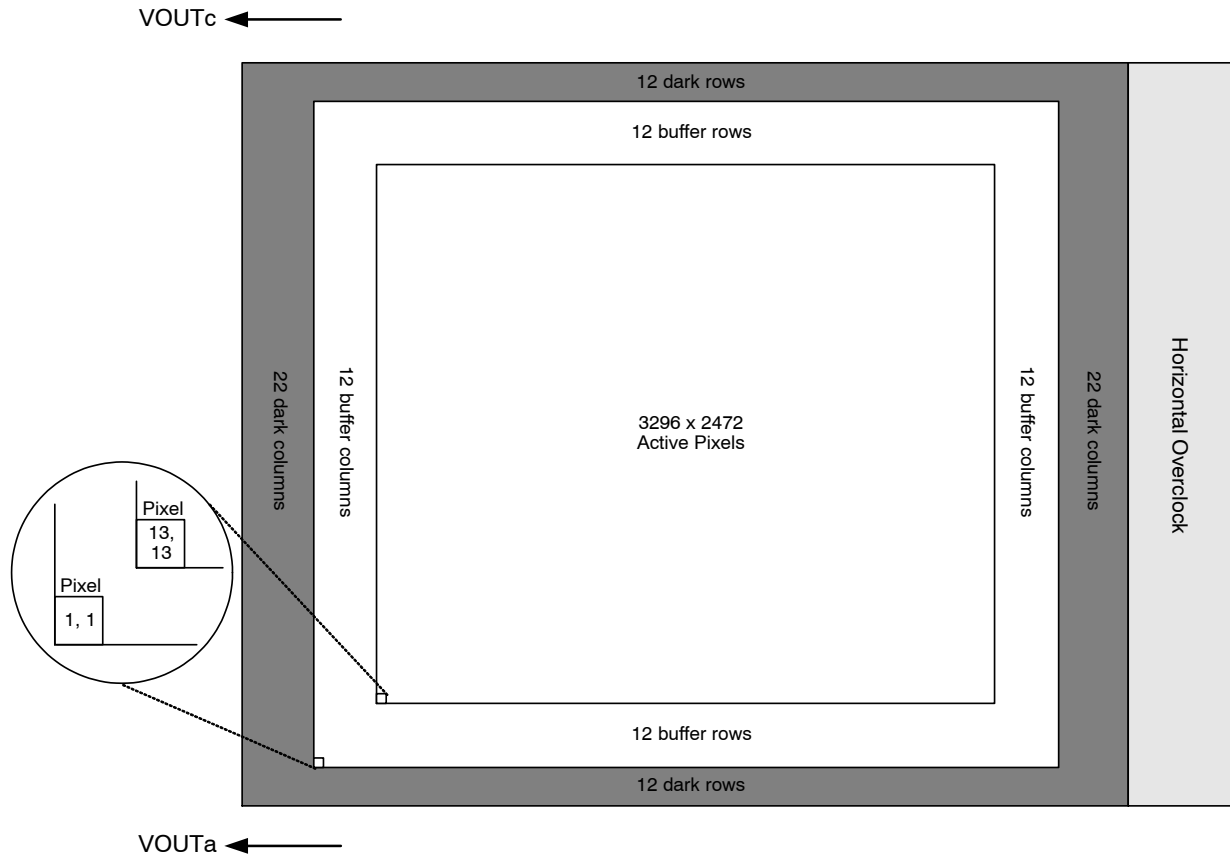


Figure 13. Regions of Interest

## Tests

### *Dark Field Global Non-Uniformity*

This test is performed under dark field conditions. The sensor is partitioned into 768 sub regions of interest, each of which is 103 by 103 pixels in size. The average signal level of each of the 768 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overlock average in counts) \* mV per count

Where i = 1 to 768. During this calculation on the 768 sub regions of interest, the maximum and minimum signal levels

$$\text{GlobalNon-Uniformity} = 100 \times \left( \frac{\text{ActiveAreaStandardDeviation}}{\text{ActiveAreaSignal}} \right)$$

Units: %rms.

Active Area Signal = Active Area Average – Dark Column Average

### *Global Peak to Peak Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The sensor is partitioned into 768 sub regions of interest, each of which is 103 by 103

$$\text{GlobalNon-Uniformity} = 100 \times \frac{\text{MaximumSignal} - \text{MinimumSignal}}{\text{ActiveAreaSignal}}$$

Units: %pp

### *Center Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed

$$\text{Center ROI Uniformity} = 100 \times \left( \frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms.

Center ROI Signal = Center ROI Average – Dark Column Average

### *Dark Field Defect Test*

This test is performed under dark field conditions. The sensor is partitioned into 768 sub regions of interest, each of which is 103 by 103 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

### *Bright Field Defect Test*

This test is performed with the imager illuminated to a level such that the output is at approximately 476 mV. Prior

are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

### *Dark Field Global Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Global non-uniformity is defined as

pixels in size. The average signal level of each of the 768 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overlock average in counts) \* mV per count

Where i = 1 to 768. During this calculation on the 768 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal \* threshold  
Bright defect threshold = Active Area Signal \* threshold

The sensor is then partitioned into 768 sub regions of interest, each of which is 103 by 103 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.



Example for major bright field defective pixels:

- Average value of all active pixels is found to be 476 mV
- Dark defect threshold:  $476 \text{ mV} * 12 \% = 57 \text{ mV}$
- Bright defect threshold:  $476 \text{ mV} * 12 \% = 57 \text{ mV}$
- Region of interest #1 selected. This region of interest is pixels 13, 13 to pixels 115, 115.
  - ◆ Median of this region of interest is found to be 470 mV.
- ◆ Any pixel in this region of interest that is  $\geq (470 + 57 \text{ mV}) 527 \text{ mV}$  in intensity will be marked defective.
- ◆ Any pixel in this region of interest that is  $\leq (470 - 57 \text{ mV}) 413 \text{ mV}$  in intensity will be marked defective.
- All remaining 768 sub regions of interest are analyzed for defective pixels in the same manner.

## OPERATION

**Table 13. ABSOLUTE MAXIMUM RATINGS**

| Description           | Symbol    | Minimum | Maximum | Units | Notes |
|-----------------------|-----------|---------|---------|-------|-------|
| Operating Temperature | $T_{OP}$  | -50     | +70     | °C    | 1     |
| Humidity              | RH        | +5      | +90     | %     | 2     |
| Output Bias Current   | $I_{out}$ |         | 60      | mA    | 3     |
| Off-chip Load         | CL        |         | 10      | pF    |       |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- $T = 25^{\circ}\text{C}$ . Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

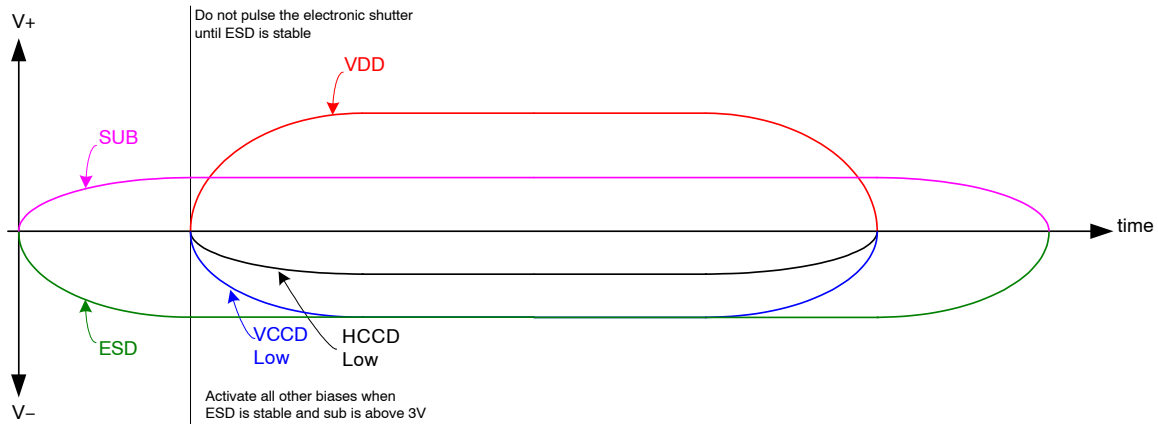
**Table 14. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND**

| Description                                                                                                        | Minimum   | Maximum    | Units | Notes |
|--------------------------------------------------------------------------------------------------------------------|-----------|------------|-------|-------|
| $VDD_{\alpha}$ , $VOUT_{\alpha}$                                                                                   | -0.4      | 17.5       | V     | 1     |
| $RD_{\alpha}$                                                                                                      | -0.4      | 15.5       | V     | 1     |
| $V1B$ , $V1T$                                                                                                      | ESD - 0.4 | ESD + 24.0 | V     |       |
| $V2B$ , $V2T$ , $V3B$ , $V3T$ , $V4B$ , $V4T$                                                                      | ESD - 0.4 | ESD + 14.0 | V     |       |
| $H1S_{\alpha}$ , $H1B_{\alpha}$ , $H2S_{\alpha}$ , $H2B_{\alpha}$ , $H2SL_{\alpha}$ , $R_{\alpha}$ , $OG_{\alpha}$ | ESD - 0.4 | ESD + 14.0 | V     | 1     |
| ESD                                                                                                                | -10.0     | 0.0        | V     |       |
| SUB                                                                                                                | -0.4      | 40.0       | V     | 2     |

- $\alpha$  denotes a, b, c or d
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

### Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.



**Figure 14. Power-Up and Power-Down Sequence**

Notes:

- Activate all other biases when ESD is stable and SUB is above 3 V
- Do not pulse the electronic shutter until ESD is stable
- VDD cannot be +15 V when SUB is 0 V
- The image sensor can be protected from an accidental improper ESD voltage by current

limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.

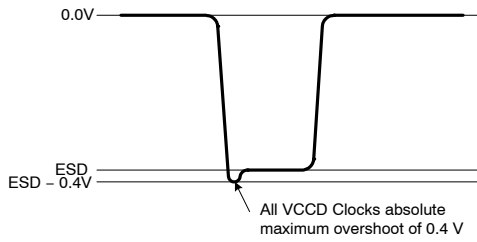


Figure 15.

Example of external diode protection for SUB, VDD and ESD.  $\alpha$  denotes a, b, c or d

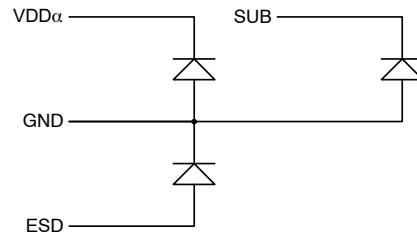


Figure 16.

Table 15. DC BIAS OPERATING CONDITIONS

| Description             | Pins         | Symbol           | Minimum | Nominal | Maximum          | Units | Maximum DC Current | Notes   |
|-------------------------|--------------|------------------|---------|---------|------------------|-------|--------------------|---------|
| Reset Drain             | RD $\alpha$  | RD               | +11.8   | +12.0   | +12.2            | V     | 10 $\mu$ A         | 1       |
| Output Gate             | OG $\alpha$  | OG               | -2.2    | -2.0    | -1.8             | V     | 10 $\mu$ A         | 1       |
| Output Amplifier Supply | VDD $\alpha$ | VDD              | +14.5   | +15.0   | +15.5            | V     | 11.0 mA            | 1,2     |
| Ground                  | GND          | GND              | 0.0     | 0.0     | 0.0              | V     | -1.0 mA            |         |
| Substrate               | SUB          | VSUB             | +5.0    | VAB     | VDD              | V     | 50 $\mu$ A         | 3, 8    |
| ESD Protection Disable  | ESD          | ESD              | -9.2    | -9.0    | V <sub>x_L</sub> | V     | 50 $\mu$ A         | 6, 7, 9 |
| Output Bias Current     | VOU $\alpha$ | I <sub>out</sub> | -3.0    | -7.0    | -10.0            | mA    |                    | 1, 4, 5 |

1.  $\alpha$  denotes a, b, c or d
2. The maximum DC current is for one output. I<sub>dd</sub> = I<sub>out</sub> + I<sub>ss</sub>. See Figure 17.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power-Up and Power-Down Sequence section.
7. ESD maximum value must be less than or equal to V1\_L + 0.4 V and V2\_L + 0.4 V
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
9. Where V<sub>x\_L</sub> is the level set for V1\_L, V2\_L, V3\_L, or V4\_L in the application.

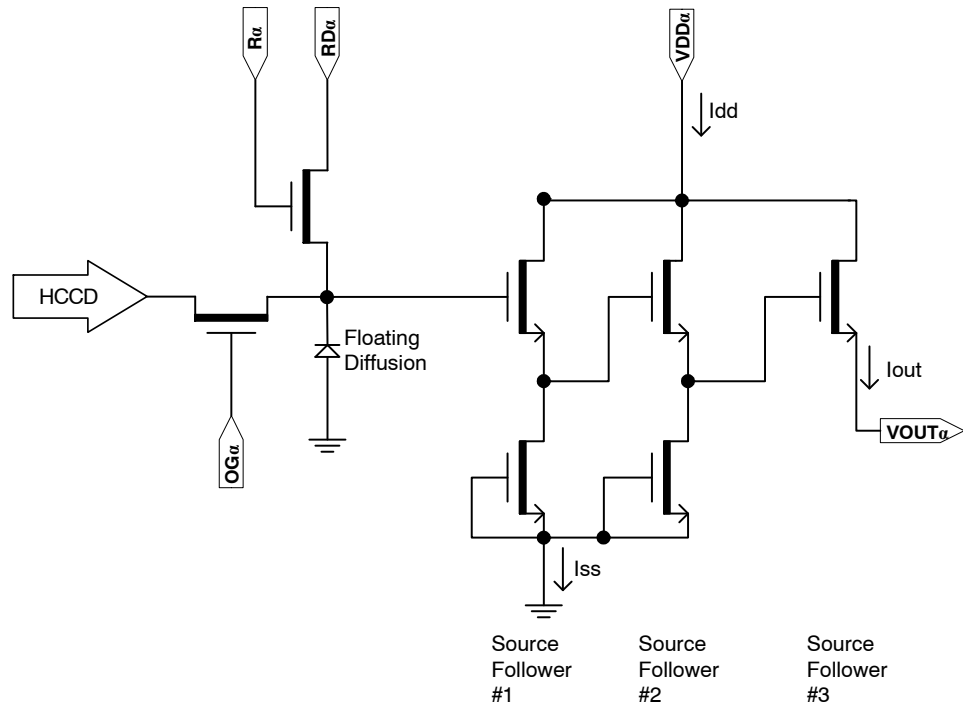


Figure 17. Output Amplifier

## AC Operating Conditions

Table 16. CLOCK LEVELS

| Description                                   | Pins <sup>1</sup> | Symbol           | Level     | Minimum  | Nominal | Maximum  | Units | Capacitance <sup>2</sup> |
|-----------------------------------------------|-------------------|------------------|-----------|----------|---------|----------|-------|--------------------------|
| Vertical CCD Clock, Phase 1                   | V1B, V1T          | V1_L             | Low       | -8.2     | -8      | -7.8     | V     | 43 nF (6)                |
|                                               |                   | V1_M             | Mid       | -0.2     | 0       | 0.2      |       |                          |
|                                               |                   | V1_H             | High      | 11.5     | 12      | 12.5     |       |                          |
| Vertical CCD Clock, Phase 2                   | V2B, V2T          | V2_L             | Low       | -8.2     | -8      | -7.8     | V     | 43 nF (6)                |
|                                               |                   | V2_H             | High      | -0.2     | 0       | 0.2      |       |                          |
| Vertical CCD Clock, Phase 3                   | V3B, V3T          | V3_L             | Low       | -8.2     | -8      | -7.8     | V     | 43 nF (6)                |
|                                               |                   | V3_H             | High      | -0.2     | 0       | 0.2      |       |                          |
| Vertical CCD Clock, Phase 4                   | V4B, V4T          | V4_L             | Low       | -8.2     | -8      | -7.8     | V     | 43 nF (6)                |
|                                               |                   | V4_H             | High      | -0.2     | 0       | 0.2      |       |                          |
| Horizontal CCD Clock, Phase 1 Storage         | H1S $\alpha$      | H1S_L            | Low       | -5.2 (7) | -4      | -3.8     | V     | 280 pF (6)               |
|                                               |                   | H1S_A            | Amplitude | 3.8      | 4       | +5.2 (7) |       |                          |
| Horizontal CCD Clock, Phase 1 Barrier         | H1B $\alpha$      | H1B_L            | Low       | -5.2 (7) | -4      | -3.8     | V     | 190 pF (6)               |
|                                               |                   | H1B_A            | Amplitude | 3.8      | 4       | +5.2 (7) |       |                          |
| Horizontal CCD Clock, Phase 2 Storage         | H2S $\alpha$      | H2S_L            | Low       | -5.2 (7) | -4      | -3.8     | V     | 280 pF (6)               |
|                                               |                   | H2S_A            | Amplitude | 3.8      | 4       | +5.2 (7) |       |                          |
| Horizontal CCD Clock, Phase 2 Barrier         | H2B $\alpha$      | H2B_L            | Low       | -5.2 (7) | -4      | -3.8     | V     | 190 pF (6)               |
|                                               |                   | H2B_A            | Amplitude | 3.8      | 4       | +5.2 (7) |       |                          |
| Horizontal CCD Clock, Last Phase <sup>3</sup> | H2SL $\alpha$     | H2SL_L           | Low       | -5.2     | -5      | -4.8     | V     | 20 pF (6)                |
|                                               |                   | H2SL_A           | Amplitude | 4.8      | 5       | 5.2      |       |                          |
| Reset Gate                                    | R $\alpha$        | R_L <sup>4</sup> | Low       | -3.5     | -2      | -1.5     | V     | 16 pF (6)                |
|                                               |                   | R_H              | High      | 2.5      | 3       | 4        |       |                          |
| Electronic Shutter <sup>5</sup>               | SUB               | VES              | High      | 29       | 30      | 40       | V     | 3 nF (6)                 |

1.  $\alpha$  denotes a, b, c or d

2. Capacitance is total for all like named pins

3. Use separate clock driver for improved speed performance.

4. Reset low should be set to -3 volts for signal levels greater than 40,000 electrons.

5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

6. Capacitance values are estimated

7. If the minimum horizontal clock low level is used (-5.2 V), then the maximum horizontal clock amplitude should be used (5.2 V amplitude) to create a -5.2 V to 0.0 V clock. If a 5 volt clock driver is used, the horizontal low level should be set to -5.0 V and the high level should be a set to 0.0 V.

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

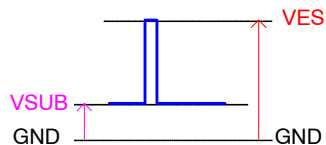


Figure 18.

**Device Identification**

The device identification pin (DevID) may be used to determine which Truesense Imaging 5.5 micron pixel interline CCD sensor is being used.

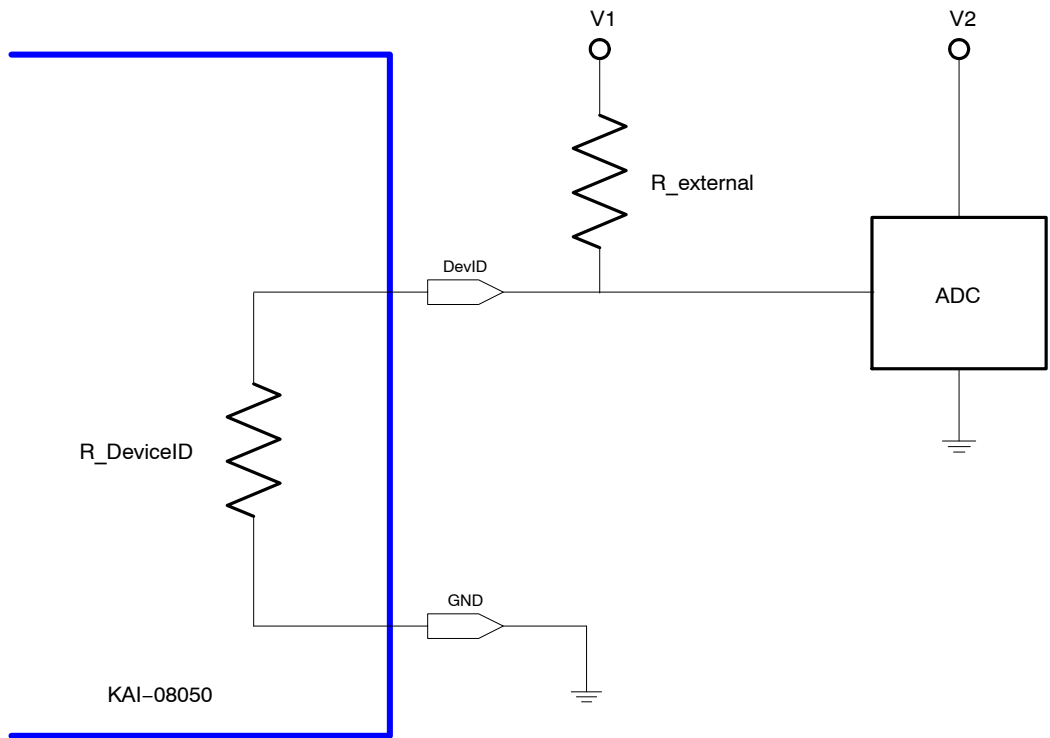
**Table 17. DEVICE IDENTIFICATION**

| Description           | Pins  | Symbol | Minimum | Nominal | Maximum | Units    | Maximum DC Current | Notes   |
|-----------------------|-------|--------|---------|---------|---------|----------|--------------------|---------|
| Device Identification | DevID | DevID  | 8,000   | 10,000  | 12,000  | $\Omega$ | 50 $\mu$ A         | 1, 2, 3 |

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. Values specified are for 40°C.

*Recommended Circuit*

Note that V1 must be a different value than V2.



**Figure 19. Device Identification Recommended Circuit**

## TIMING

Table 18. REQUIREMENTS AND CHARACTERISTICS

| Description            | Symbol           | Minimum | Nominal | Maximum | Units   | Notes               |
|------------------------|------------------|---------|---------|---------|---------|---------------------|
| Photodiode Transfer    | $t_{pd}$         | 1.0     | –       | –       | $\mu s$ |                     |
| VCCD Leading Pedestal  | $t_{3p}$         | 4.0     | –       | –       | $\mu s$ |                     |
| VCCD Trailing Pedestal | $t_{3d}$         | 4.0     | –       | –       | $\mu s$ |                     |
| VCCD Transfer Delay    | $t_d$            | 1.0     | –       | –       | $\mu s$ |                     |
| VCCD Transfer          | $t_v$            | 2.0     | –       | –       | $\mu s$ |                     |
| VCCD Clock Cross-over  | $v_{VCR}$        | 75      |         | 100     | %       |                     |
| VCCD Rise, Fall Times  | $t_{VR}, t_{VF}$ | 5       | –       | 10      | %       | 2, 3                |
| HCCD Delay             | $t_{hs}$         | 0.2     | –       | –       | $\mu s$ |                     |
| HCCD Transfer          | $t_e$            | 25.0    | –       | –       | ns      |                     |
| Shutter Transfer       | $t_{sub}$        | 1.0     | –       | –       | $\mu s$ |                     |
| Shutter Delay          | $t_{hd}$         | 1.0     | –       | –       | $\mu s$ |                     |
| Reset Pulse            | $t_r$            | 2.5     | –       | –       | ns      |                     |
| Reset – Video Delay    | $t_{rv}$         | –       | 2.2     | –       | ns      |                     |
| H2SL – Video Delay     | $t_{hv}$         | –       | 3.1     | –       | ns      |                     |
| Line Time              | $t_{line}$       | 45.5    | –       | –       | $\mu s$ | Dual HCCD Readout   |
|                        |                  | 87.6    | –       | –       |         | Single HCCD Readout |
| Frame Time             | $t_{frame}$      | 57.4    | –       | –       | ms      | Quad HCCD Readout   |
|                        |                  | 114.8   | –       | –       |         | Dual HCCD Readout   |
|                        |                  | 220.7   | –       | –       |         | Single HCCD Readout |

1. Refer to timing diagrams as shown in Figures 20, 21, 22, 23 and 24.
2. Refer to Figure 24: VCCD Clock Edge Alignment
3. Relative to the pulse width

**Timing Diagrams**

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1–P7) as shown in the table below. The patterns are defined in Figure 20 and

Figure 21. Contact ON Semiconductor Application Engineering for other readout modes.

**Table 19.**

| Device Pin        | Quad Readout | Dual Readout<br>VOUTa, VOUTb        | Dual Readout<br>VOUTa, VOUTc        | Single Readout<br>VOUTa             |
|-------------------|--------------|-------------------------------------|-------------------------------------|-------------------------------------|
| V1T               | P1T          | P1B                                 | P1T                                 | P1B                                 |
| V2T               | P2T          | P4B                                 | P2T                                 | P4B                                 |
| V3T               | P3T          | P3B                                 | P3T                                 | P3B                                 |
| V4T               | P4T          | P2B                                 | P4T                                 | P2B                                 |
| V1B               | P1B          |                                     |                                     |                                     |
| V2B               | P2B          |                                     |                                     |                                     |
| V3B               | P3B          |                                     |                                     |                                     |
| V4B               | P4B          |                                     |                                     |                                     |
| H1Sa              | P5           |                                     |                                     |                                     |
| H1Ba              |              |                                     |                                     |                                     |
| H2Sa2             | P6           |                                     |                                     |                                     |
| H2Ba              |              |                                     |                                     |                                     |
| Ra                | P7           |                                     |                                     |                                     |
| H1Sb              | P5           |                                     | P5                                  |                                     |
| H1Bb              |              |                                     | P6                                  |                                     |
| H2Sb <sup>2</sup> | P6           |                                     | P6                                  |                                     |
| H2Bb              |              |                                     | P5                                  |                                     |
| Rb                | P7           |                                     | P7 <sup>1</sup> or Off <sup>3</sup> | P7 <sup>1</sup> or Off <sup>3</sup> |
| H1Sc              | P5           | P5 <sup>1</sup> or Off <sup>3</sup> | P5                                  | P5 <sup>1</sup> or Off <sup>3</sup> |
| H1Bc              |              |                                     |                                     |                                     |
| H2Sc <sup>2</sup> | P6           | P6 <sup>1</sup> or Off <sup>3</sup> | P6                                  | P6 <sup>1</sup> or Off <sup>3</sup> |
| H2Bc              |              |                                     |                                     |                                     |
| Rc                | P7           | P7 <sup>1</sup> or Off <sup>3</sup> | P7                                  | P7 <sup>1</sup> or Off <sup>3</sup> |
| H1Sd              | P5           | P5 <sup>1</sup> or Off <sup>3</sup> | P5                                  | P5 <sup>1</sup> or Off <sup>3</sup> |
| H1Bd              |              |                                     | P6                                  |                                     |
| H2Sd <sup>2</sup> | P6           | P6 <sup>1</sup> or Off <sup>3</sup> | P6                                  | P6 <sup>1</sup> or Off <sup>3</sup> |
| H2Bd              |              |                                     | P5                                  |                                     |
| Rd                | P7           | P7 <sup>1</sup> or Off <sup>3</sup> | P7 <sup>1</sup> or Off <sup>3</sup> | P7 <sup>1</sup> or Off <sup>3</sup> |

|                         |      |      |      |      |
|-------------------------|------|------|------|------|
| # Lines/Frame (Minimum) | 1260 | 2520 | 1260 | 2520 |
| # Pixels/Line (Minimum) | 1693 |      | 3386 |      |

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = +5 V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.



### Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 632 or 1264 minimum counts required. It is important to note that, in

general, the rising edge of a vertical clock (patterns P1–P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3<sup>rd</sup> level) state to the mid-state when P4 transitions from the low state to the high state.

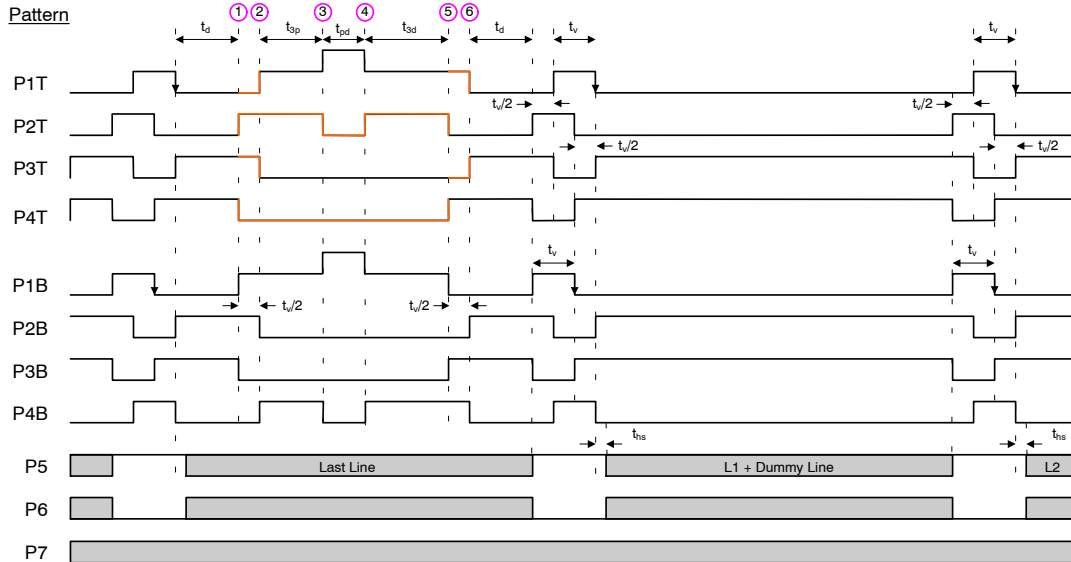


Figure 20. Photodiode Transfer Timing

### Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependent on

readout mode – either 853 or 1706 minimum counts required.

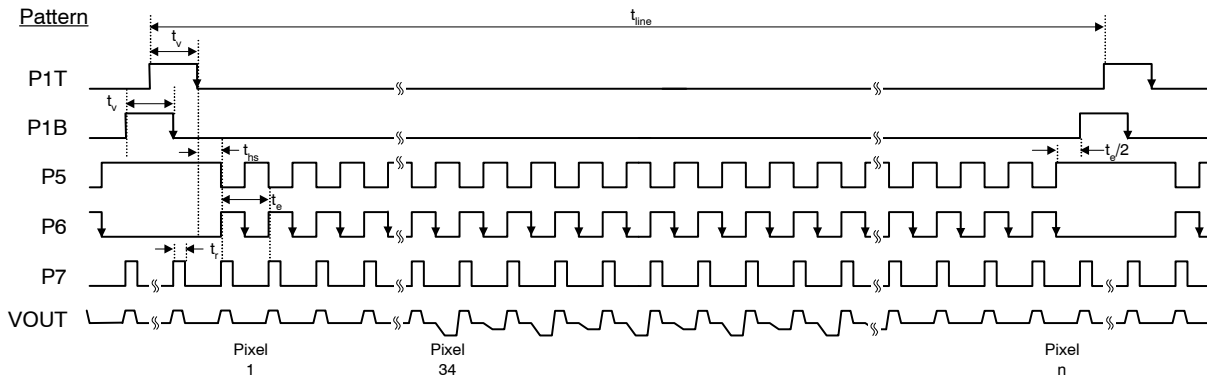


Figure 21. Line and Pixel Timing

## Pixel Timing Detail

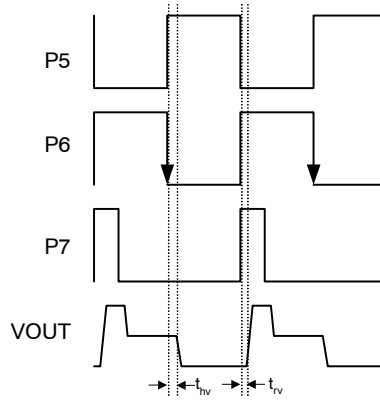


Figure 22. Pixel Timing Detail

## Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below.

The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

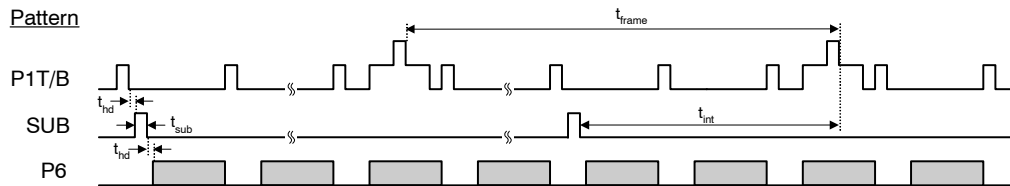


Figure 23. Frame/Electronic Shutter Timing

## VCCD Clock Edge Alignment

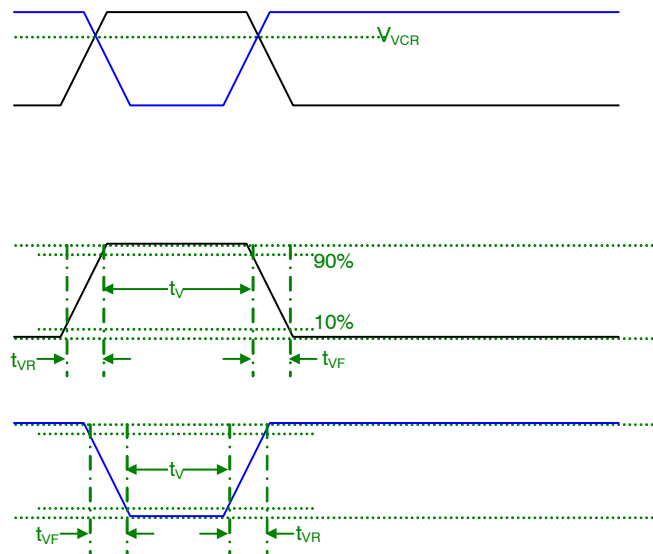


Figure 24. VCCD Clock Edge Alignment

## Line and Pixel Timing – Vertical Binning by 2

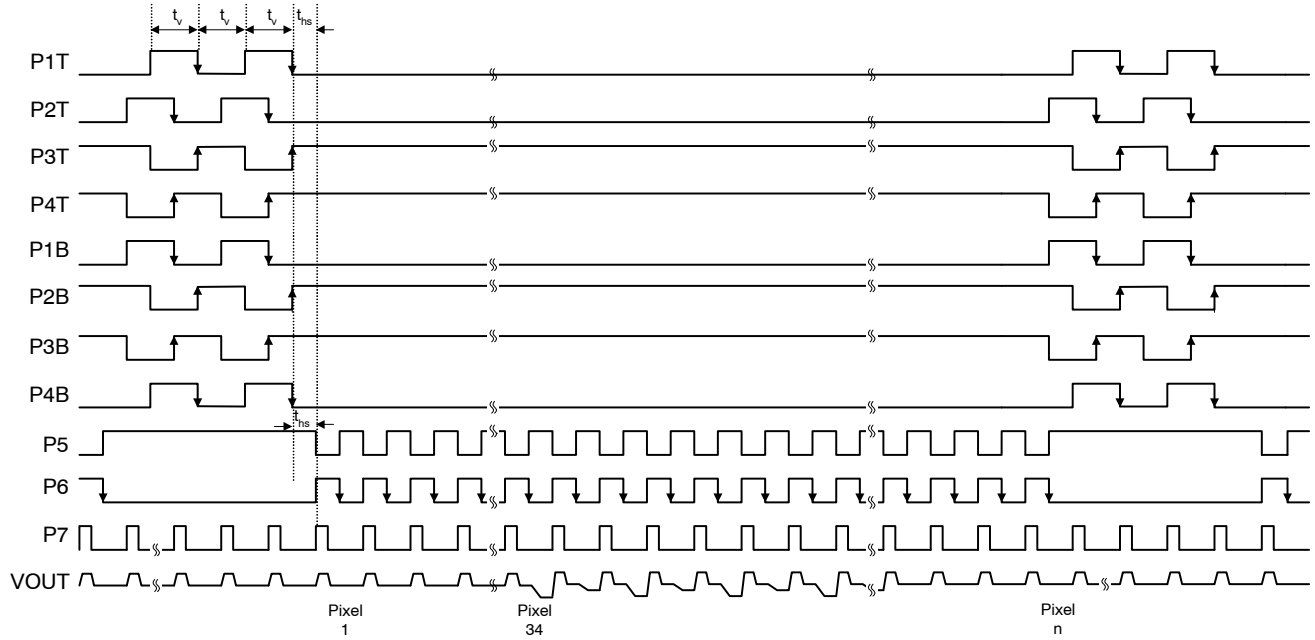


Figure 25. Line and Pixel Timing – Vertical Binning by 2

## STORAGE AND HANDLING

Table 20. STORAGE CONDITIONS

| Description         | Symbol          | Minimum | Maximum | Units | Notes |
|---------------------|-----------------|---------|---------|-------|-------|
| Storage Temperature | T <sub>ST</sub> | -55     | +80     | °C    | 1     |
| Humidity            | RH              | 5       | 90      | %     | 2     |

1. Long term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

## MECHANICAL INFORMATION

## Completed Assembly

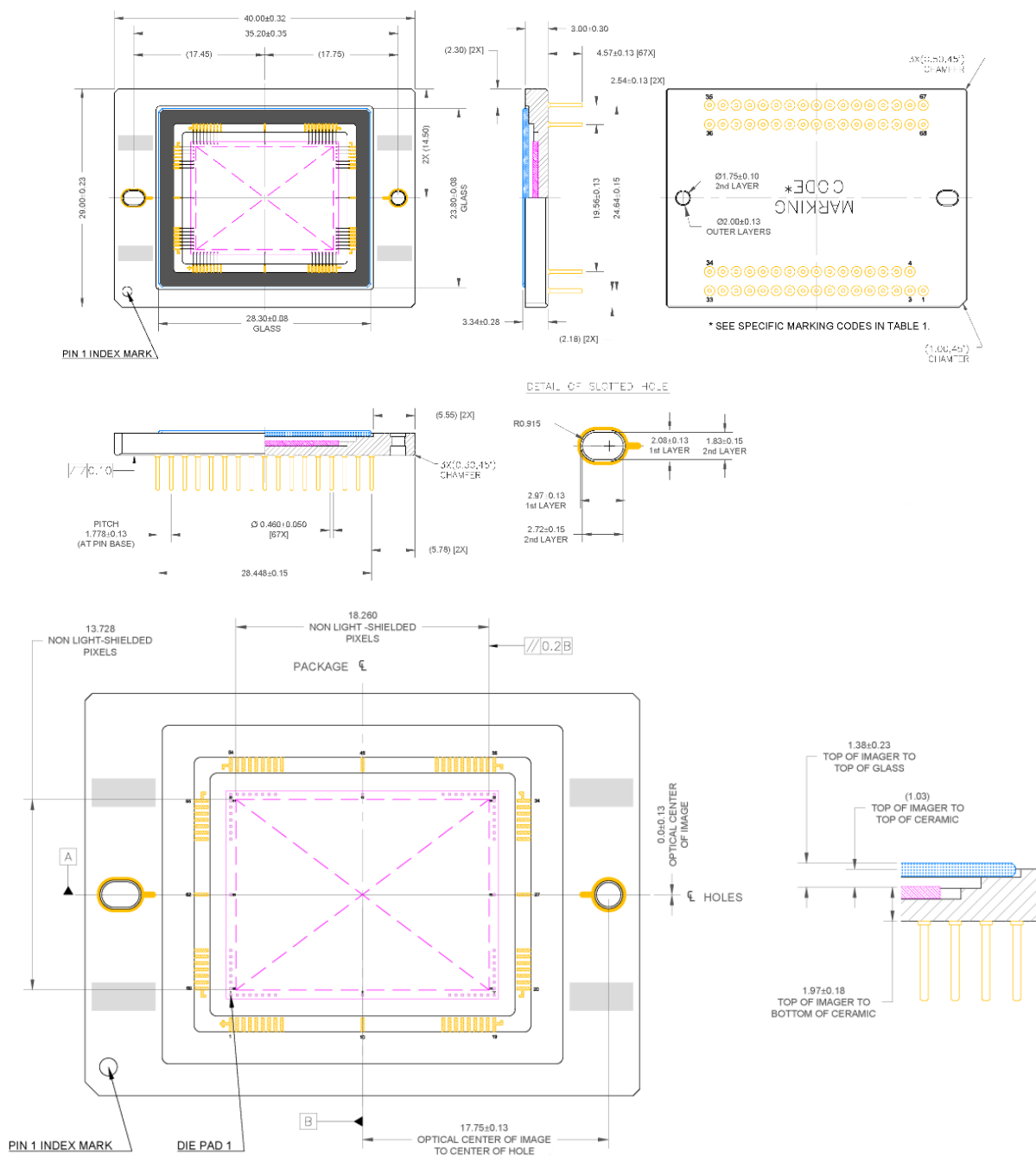


Figure 26. Completed Assembly

## Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through guide holes.
3. The center of the active image is nominally at the center of the package.
4. Die rotation  $< 0.5$  degrees
5. Internal traces may be exposed on sides of package. Do not allow metal to contact sides of ceramic package.
6. Recommended mounting screws: 1.6 X 0.35 mm (ISO Standard); 0 – 80 (Unified Fine Thread Standard)
7. Units: millimeters

# MAR Cover Glass

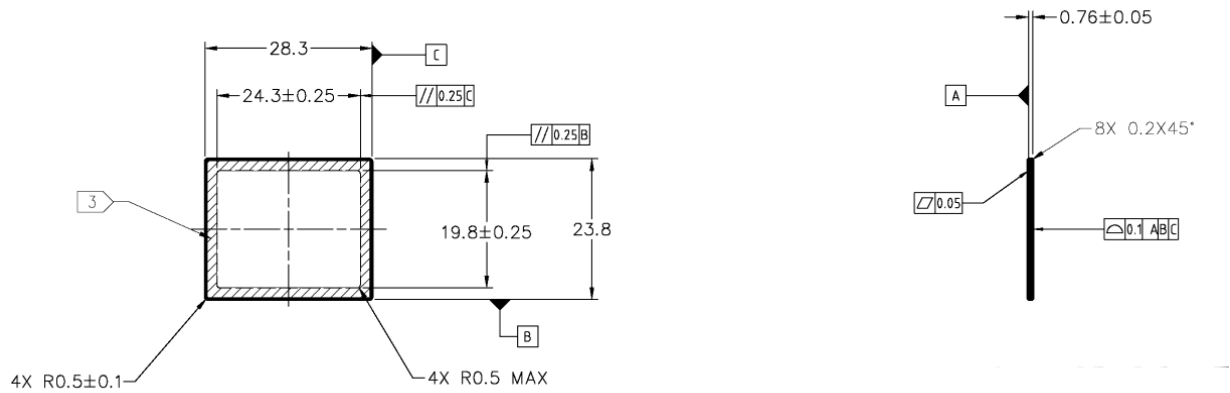


Figure 27. MAR Cover Glass

## Notes:

1. Dust/Scratch count – 12 micron maximum
2. Units: mm

# Clear Cover Glass

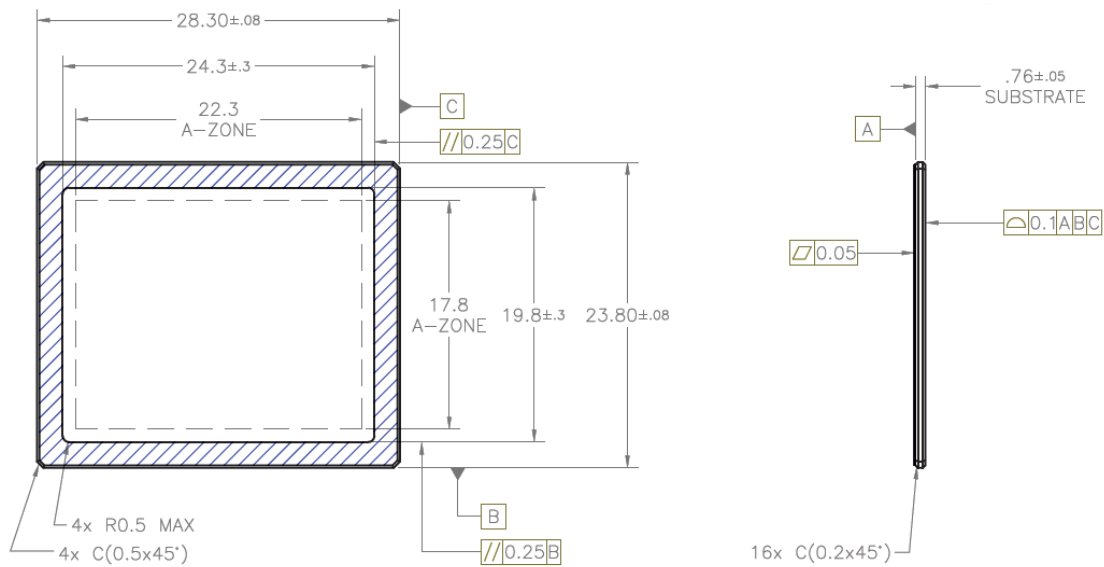


Figure 28. Clear Cover Glass

## Notes:

1. Dust/Scratch count – 10 micron maximum
2. Units: mm

# Cover Glass Transmission

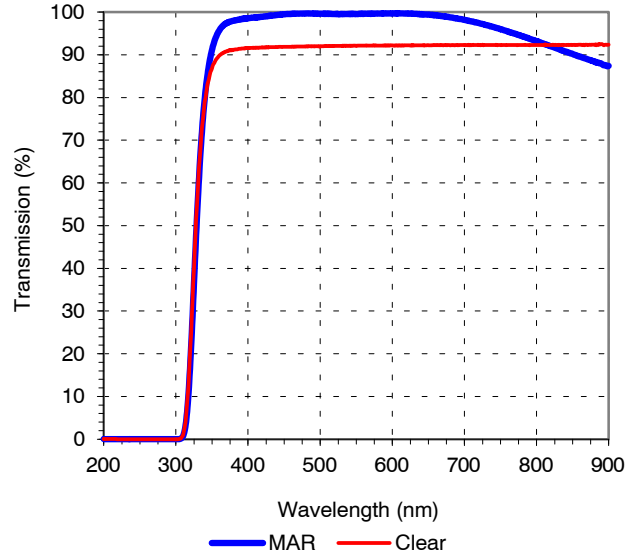


Figure 29. Cover Glass Transmission

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative