EVBUM2263/D

KAI-0340 Image Sensor Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code described in this document is intended for use in the KSC−1000 Timing Board. The code is developed specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit	PN 4H0472
Timing Generator Board	PN 3F5054 (AD9840A 40 MHz)
KAI−0340 CCD Imager Board	PN 3E8422
Framegrabber Board	National Instruments PCI−1424

ALTERA CODE FEATURES/FUNCTIONS

The Altera Programmable Logic Device (PLD) serves as a state machine, which performs a variety of functions. Three basic functions are required, common to all CCD image sensor configurations: serial input steering, AFE default programming, and KSC−1000 default programming. In addition, certain other functions specific to the KAI−0340 Image Sensor are implemented.

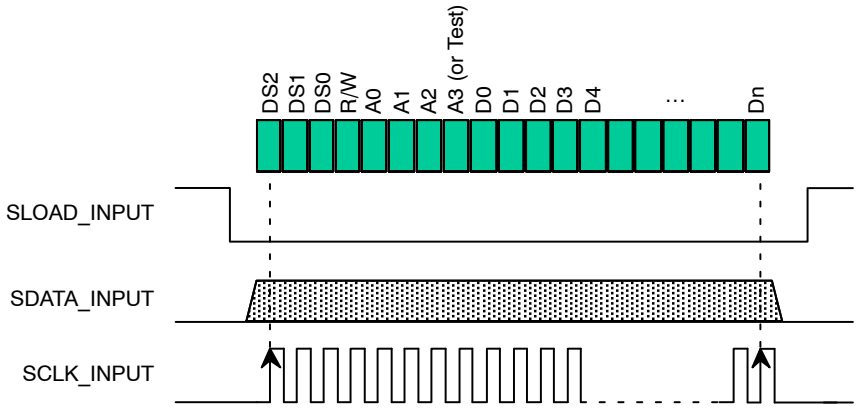


Figure 1. Serial Input Timing

Serial Input Steering

The 3-wire serial interface enters the Timing Board through the DIO Interface connector, and is routed to the PLD. The Altera PLD decodes the addressing of the serial input, and steers the datastream to the correct device. The serial input must be formatted so that the Altera PLD can correctly decode and steer the data to the correct device.

This feature can be used to dynamically change the operating conditions of the AFE or KSC−1000 chips by reprogramming the appropriate registers. Reprogramming these registers through the serial interface will have no effect on the default settings that are automatically programmed into these devices on power-up or board reset.

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Table 2. SERIAL INPUT DEVICE SELECT

Device Select DS[2..0]	Serial Device
000	PLD
001	AFE1
010	AFE2
011	KSC−1000
100	(Not Used)
101	(Not Used)
110	(Not Used)
111	(Not Used)

The first 3 bits in the datastream are the Device Select bits DS[2..0], sent MSB first, as shown in Figure 1. The Device Select bits are decoded as shown in Table 2.

The next bit in the datastream is the Read/Write bit (R/$\overline{W}$). Only writing is supported; therefore this bit is always LOW.

The definition of next four bits in the datastream depends on the device being addressed with the Device Select bits. For the KSC−1000 device, they are Register address bits A[0..3], LSB first. For the AD9845A or AD9840A AFE, they are Register Address bits A[0..2], LSB first, followed by a Test bit which is always set LOW.

The remaining bits in the bitstream are Data bits, LSB first, with as many bits as are required to fill the appropriate register.

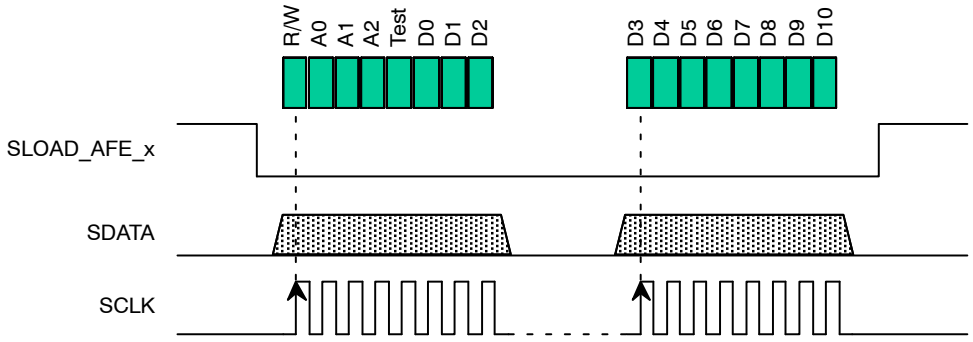


Figure 2. KSC−1000 Initialization Timing

AFE Default Initialization

Upon power up, or when the BOARD_RESET button is pressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via the 3-wire serial interface. See Table 12 for details. The AD9840A AFE must be reprogrammed on power-up, as it does not retain register settings when power is removed.

The data for each AFE register is formatted into two bytes of data, as shown in Figure 2. The Read/Write bit is always low, and the Address bits specify the register being programmed, as shown in Table 12. Each byte is read into an 8-bit shift register, and is shifted out as a serial stream of eight bits. Each register in the AFE is programmed in this fashion until the entire AFE is programmed.

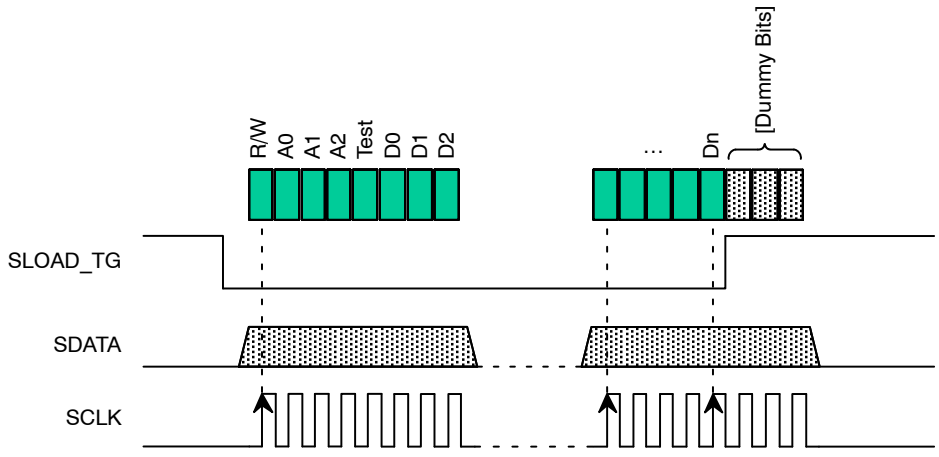


Figure 3. KSC−1000 Initialization Timing

KSC−1000 Default Initialization

Upon power-up, or when the BOARD_RESET button is pressed, the Altera PLD programs the registers of the KSC−1000 chip on the AFE Timing Generator Board to their default settings via the 3-wire serial interface. The default settings are selected by the user through the PLD inputs SW[7..0] and DIO[15..0] (See Table 14 through Table 26 for details). The KSC−1000 must be reprogrammed on power-up, as it does not retain register settings when power is removed.

The data for each KSC−1000 register is formatted into bytes of data, as shown in Figure 3. The Read/Write bit is always low, and the Address bits specify the register being programmed, as shown in Table 3. Each byte is read into an 8-bit shift register, and is shifted out of the PLD as a serial stream of eight bits. The last byte of data sent to a particular register may need to be padded with extra “dummy” bits; the SLOAD_TG signal is brought HIGH at the appropriate time so that the correct number of bits are streamed into each register, and the extra bits are ignored. Each register in the KSC−1000 is programmed in this fashion until the entire device is programmed.

Table 3. KSC−1000 REGISTERS

Register Address	Register Description	Data Bits
0	Frame Table Pointer	3
1	General Setup	202
2	General Control	2
3	INTG_STRT Setup	30
4	INTG_STRT Line	13
5	Signal Polarity	25
6	Offset	78
7	Width	65
8	Frame Table Access	(Variable)
9	Line Table Access	(Variable)

Select Timing Mode

PLD inputs SW[2..0] are used to select one of the supported timing modes: Full Field Single Output, Full Field Dual Output, and Center Rows and Columns Single Output. When making a change to the switch settings, the user must press the BOARD_RESET button (S1) on the Timing Board for the change to take effect.

Electronic Shutter Modes

In the Full Field Timing Modes (Modes 0 and 1), PLD inputs SW[7..6] may be used to select one of the supported Electronic Shutter modes: Full Field integration, 3/4 Field integration, 1/2 Field integration, and 1/4 Field integration. See Table 23 for timing details. When making a change to the switch settings, the user must press the BOARD_RESET button (S1) on the Timing Board for the change to take effect.

Center Fast Dump Gate Control

The Altera PLD has several outputs (PLD[2..0]) which are connected to the Imager Board, and are available for auxiliary clocking and control not provided by the KSC−1000.

The KAI−0340 Imager Board provides separate Fast Dump clocks, whose outputs are named FD_CCD and FDC_CCD, to the CCD. Certain imaging modes require the activation of the FD_CCD clock separately from the FDC_CCD clock, in order to clock out only the center columns of the image area. The PLD2 output from the Altera PLD controls the FDC_CCD clock, while the V6 clock of the KSC−1000 chip controls the FD_CCD clock.

Integration Clock

The Altera PLD uses the System Clock and an internal counter to generate a 1.0 ms-period clock. This clock is used to generate an internal delay after power-up or Board Reset. It may also be used to control precise integration times for the image sensor.

ALTERA CODE I/O

Inputs

The Altera PLD takes as its inputs user selectable switches SW[7..0] on the Timing Board, remote digital inputs DIO[15..0] and a 3-wire serial interface through Timing Board connector J7, Timing Board signals, and various outputs from the KSC−1000 Timing Generator. The KSC−1000 outputs may be monitored by the PLD to control auxiliary timing functions, but are not used for KAI−0340 operation. The remote digital inputs DIO[15..0] are optional, and are not used for KAI−0340 operation.

Table 4. ALTERA INPUTS

Symbol	Description
POWER_ON_DELAY	The Rising Edge of This Signal Clears and Re-initializes the PLD
SYSTEM_CLK	80 MHz Clock, 2X the Desired Pixel Clock Rate
PIXCLK	NI1424 40 MHz Pixel Rate Clock from the KSC1000TG (Not Used)
SW[2..0]	Timing Mode (See Table 9 for Details) Mode SW[2..0] Description 0 000 1ch, Full Image 1 001 2ch, Full Image 2 010 (Not Supported) 3 011 (Not Supported) 4 100 (Not Supported) 5 101 (Not Supported) 6 110 1ch, Center Rows, Center Columns 7 111 (Not Supported)
SW[5..3]	(Not Used for KAI−0340 Operation)
SW[7..6]	Electronic Shutter Pulse Location (Modes 0/1 Only) SW[7..6] Line Description 00 500 FULL FRAME INTEGRATION (NO SHUTTER) 01 122 3/4 FRAME INTEGRATION 10 244 1/2 FRAME INTEGRATION 11 366 1/4 FRAME INTEGRATION
DIO[15..0]	(Not Used for KAI−0340 Operation)
SLOAD_INPUT	3-wire Serial Interface LOAD Signal Input
SDATA_INPUT	3-wire Serial Interface DATA Signal Input
SCLOCK_INPUT	3-wire Serial Interface CLOCK Signal Input
LINE_VALID	(Not Ysed for KAI−0340 Operation)
FRAME_VALID	(Not Used for KAI−0340 Operation)
AUX_SHUT	(Not Used for KAI−0340 Operation)
INTG_START	(Not Used for KAI−0340 Operation)

Outputs

Table 5. ALTERA OUTPUTS

Symbol	Description
PLD_OUT0	KAI−0340 Vdeo MUX Control (ON Semiconductor Test Use Only)
PLD_OUT1	(Not Used for KAI−0340 Operation)
PLD_OUT2	Center Fast Dump Gate
GIO[2..0]	(Not Used for KAI−0340 Operation)
SLOAD_AFE_1	Serial Load Enable, Ch1 AD9840A AFE
SLOAD_AFE_2	Serial Load Enable, Ch2 AD9840A AFE
SLOAD_TG	Serial Load Enable, KSC−1000
SDATA	3-wire Serial Interface DATA Signal Output
SCLOCK	3-wire Serial Interface CLOCK Signal Output
INTEGRATE	High During CCD Integration Time
HD_TG	(Not Used for KAI−0340 Operation)
VD_TG	(Not Used for KAI−0340 Operation)
ARSTZ	(Not Used for KAI−0340 Operation)

KAI−0340 TIMING CONDITIONS

System Timing Conditions

Table 6. SYSTEM TIMING

Description	Symbol	Time	Notes
System Clock Period	T_{sys}	12.5 ns	80 MHz System Clock
Unit Integration Time	U_{int}	1 ms	Generated by PLD
Power Stable Delay	T_{pwr}	30 ms	Typical
Default Serial Load Time	T_{sload}	112.5 μs	Typical
Integration Time	T_{int}		Operating Mode Dependent

CCD Timing Conditions

Table 7. CCD TIMING

Description	Symbol	Time	Pixel Counts	Notes
H1, H2, RESET Period	T_{pix}	25.0 ns	1	40 MHz Clocking of H1, H1L, H2, RESET
VCCD Delay	T_{VD}	25.0 ns	1	Delay after Hclks Stop
VCCD Transfer Time	T_{VCCD}	500.0 ns	20	V2 Rising Edge to V2 Falling Edge
HCCD Delay	T_{HD}	425.0 ns	17	Delay before Hclks Resume
Vertical Transfer Period	V_{period}	950.0 ns	38	$V_{period} = T_{VD} + T_{VCCD} + T_{HD}$
VCCD Pedestal Time	T_{3P}	15.0 μs	600	
Photodiode Transfer Time	T_{V3rd}	525.0 ns	21	V2 3rd Level
Photodiode Delay	T_{3D}	5.0 μs	200	
Photodiode Frame Delay	T_{3FD}	15.0 μs	600	
Shutter Pulse Setup	T_{EL}	25.0 ns	1	
Shutter Pulse Time	T_S	1.0 μs	40	
Shutter Pulse Delay	T_{SD}	1.0 μs	40	

PCI−1424 Timing Conditions

Table 8. PCI−1424 TIMING

Description	Symbol	Time	Pixel Counts	Notes
PIX Period	T_{PIX}	25 ns	1	40 MHz Clocking of DATACLK Sync Signal
FRAME Time − Mode 0	T_{FRAME}	9.68 ms	387309	$T_{FRAME} = T_{PIX} * ((V_{period} + PIX_X) * PIX_Y + VCCD_{period})$
FRAME Time − Mode 1	T_{FRAME}	5.27 ms	210733	$T_{FRAME} = T_{PIX} * ((V_{period} + PIX_X) * PIX_Y + VCCD_{period})$
FRAME Time − Mode 6	T_{FRAME}	1.23 ms	49133	$T_{FRAME} = T_{PIX} * ((V_{period} + PIX_X) * PIX_Y + VCCD_{period})$

MODES OF OPERATION

The following modes of operation are available to the user:

Timing Modes

The Timing Modes labeled as Modes 0 through 7 in Table 9 are selected by setting the SW[2..0] inputs to the appropriate level (See Table 9). These modes correspond to the Timing Modes as described in the KAI−0340 Device Specification (See References). Each switch has a unique function, and the combinations of these switch settings implement the eight different Timing Modes. For each supported Timing Mode, a unique combination of default values is programmed in the KSC−1000 registers. The BOARD_RESET switch must be pressed after changing the switch settings to initiate reprogramming the KSC−1000.

At this time, not all possible Timing Modes are supported by the KAI−0340 Evaluation Board timing.

Single/Dual Outputs (SW0)

The KAI−0340 device features a split horizontal register and two output amplifiers. Setting the SW0 switch to the LOW position causes all of the CCD pixels to be clocked out the CCD's left output amplifier. Setting the SW0 switch to the HIGH position causes each half of the horizontal register to be clocked out in opposite directions, nearly doubling the frame rate. See the KAI−0340 Device Specification (References) for details.

Center Columns (SW1)

Setting the SW1 switch to the HIGH position activates the Fast Dump Clock to the outer columns. This causes the charge in the outer vertical registers to be dumped before it reaches the horizontal register. In this way, only the center columns are read out.

Center Rows (SW2)

Setting the SW2 switch to the HIGH position changes the V2 Diode transfer clock timing such that only charge in the center rows is transferred to the vertical registers. In this way, only the center rows are read out.

Table 9. TIMING MODE SWITCH SETTINGS

TIMING MODE	SW2	SW1	SW0	OPERATION MODE
0	LOW	LOW	LOW	Single Output, Full Image (740 × 496)
1	LOW	LOW	HIGH	Dual Output, Full Image (384 × 496 × 2 Outputs)
2	LOW	HIGH	LOW	(Not Supported)
3	LOW	HIGH	HIGH	(Not Supported)
4	HIGH	LOW	LOW	(Not Supported)
5	HIGH	LOW	HIGH	(Not Supported)
6	HIGH	HIGH	LOW	Single Output, Center Rows, Center Columns (246 × 168)
7	HIGH	HIGH	HIGH	(Not Supported)

Electronic Shutter Modes

In Timing Modes 0 and 1, integration times less than one frame time can be achieved by electronic shuttering of the device. In Electronic Shutter Mode, the integration time can be set from 1x to 1/4x frame time via the configuration switches SW[7..6] (See Table 10 and Table 11). The BOARD_RESET switch must be pressed after changing the switch settings to initiate reprogramming the KSC−1000.

The line location of the shutter pulse is controlled by the Integrate Start Pulse Line Number entry in Register 4 of the KSC−1000. The Integrate Start Pulse Line Number Altera PLD default value is 500, which is greater than the number of lines in the full image, so no pulse is asserted. Through the Serial Interface, the user may program this register with any chosen value, and is not limited to the switch-selectable defaults.

Table 10. MODE 0 ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE SW[7..6]	VES LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0	500	1	9.51	Default – No Shutter Pulse
1	122	0.75	7.14	
2	244	0.5	4.76	
3	366	0.25	2.39	

Table 11. MODE 1 ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE SW[7..6]	VES LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0	500	1	5.16	Default – No Shutter Pulse
1	122	0.75	3.88	
2	244	0.5	2.59	
3	366	0.25	1.3	

Black Clamp Mode

One of the features of the AD9840A AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. At this time, the location of these pulses is fixed in the default Timing Modes, but can be adjusted dynamically through the 3-wire serial interface. The default settings are shown in Table 21.

POWER-ON/BOARD RESET INITIALIZATION

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the AFE registers, and will then load the KSC−1000 frame tables, line tables, and registers. Upon completion, the KSC−1000 will be ready to proceed according to its programmed configuration. In the background, the Altera PLD monitors the activity of the KSC−1000, and the 3-wire Serial Interface

AFE Register Default Settings

On power-up or board reset, the AFE registers are programmed to the default levels shown in Table 12. See the AD9840A specifications sheet (References) for details.

Table 12. DEFAULT AD9840A AFE REGISTER PROGRAMMING

Register Address	Description	Value (decimal)	Notes
0	Operation	128	
1	VGA Gain	177	Corresponds to a VGA Stage Gain of 4.4 dB
2	Clamp	24	The Output of the AD9840A will be Clamped to Code 96 during the CLPOB Period
3	Control	8	CDS Gain Enabled
4	CDS Gain	43	Corresponds to a CDS Stage Gain of 0.0 dB

KSC−1000 Timing Generator Default Settings

On power-up or board reset, The KSC−1000 is programmed to the default settings as detailed in Table 14 through Table 26. See the KSC−1000 Device Specification (References) for details.

Register 2: General Control

Register 2 controls the Power Management and Operation state of the KSC−1000. The Low Power Mode is not used on the KAI−0340, so this bit is always LOW. The Memory Table Mode bit is used to halt execution of the KSC−1000 timing sequences and to enable programming of the registers. The KSC−1000 Initialization sequence begins with setting the Memory Table Mode bit in Register 2 to Program Mode, and ends by setting the bit to Execution Mode. See the KSC−1000 Device Specification (References) for more details.

Table 13. REGISTER 2 SETTINGS

Register Entry	Program Mode	Execution Mode
Low Power Enable	0	0
Memory Table Mode	0	1

Frame Tables

Two Frame Tables are written by default to the KSC−1000 Frame Table registers. Frame Table 0 is used for Timing Modes 0 and 1 (all rows clocked out), while Frame Table 1 used for Timing Mode 6 (only center rows are clocked out).

Table 14. FRAME TABLE 0 DEFAULT SETTING

Bit Location	Frame Table Data	FT0 Entry				
		0	1	2	3	4
0	Check and Increment Line Counter	0	1	1	1	0
1	Clear Line Counter	1	0	0	0	0
2	Force INTG_STRT	0	0	0	0	0
3:04	Horizontal Binning Factor	0	0	0	0	0
5	HCLK_V Enable	0	0	0	0	0
6	LINE_VALID Enable	0	1	1	1	0
7	FRAME_VALID Enable	0	1	1	1	0
8	Video Amplifier Enable	0	0	0	0	0
9	AFE Clock Enable	1	1	1	1	1
10	CLPDM2 Enable	0	0	0	1	0
11	CLPDM1 Enable	0	0	0	0	0
12	CLPOB2 Enable	0	0	0	1	0
13	CLPOB1 Enable	0	0	0	0	0
14	PBLK Enable	0	1	1	1	1
15	Pblk_Idle_Val	1	1	1	1	1
16	Flag	0	0	0	0	0
17:29	Count	1	1	2	493	0
30:32:00	Address 2:0	0	1	1	1	0
33	Address 3	0	0	0	0	0
–	Mnemonic	ELT 0	ELT 1	ELT 1	ELT 1	JMPFT 0

Table 15. FRAME TABLE 1 DEFAULT SETTING

Bit Location	Frame Table Data	FT1 Entry				
		0	1	2	3	4
0	Check and Increment Line Counter	0	1	1	1	0
1	Clear Line Counter	1	0	0	0	0
2	Force INTG_STRT	0	0	0	0	0
3:04	Horizontal Binning Factor[0..1]	0	0	0	0	0
5	HCLK_V Enable	0	0	0	0	0
6	LINE_VALID Enable	0	1	1	1	0
7	FRAME_VALID Enable	0	1	1	1	0
8	Video Amplifier Enable	0	0	0	0	0
9	AFE Clock Enable	1	1	1	1	1
10	CLPDM2 Enable	0	0	1	0	0
11	CLPDM1 Enable	0	0	0	0	0
12	CLPOB2 Enable	0	0	1	0	0
13	CLPOB1 Enable	0	0	0	0	0
14	PBLK Enable	0	1	1	1	1
15	Pblk_Idle_Val	1	1	1	1	1
16	Flag	0	0	0	0	0
17:29	Count[0..12]	1	1	163	4	0
30:32:00	Address[0..2]	2	3	1	3	1
33	Address[3]	0	0	0	0	0
–	Mnemonic	ELT 2	ELT 3	ELT 1	ELT 3	JMPFT 1

Line Tables

For Timing Modes 0−3, there are four Line Tables which correspond to Timing Sequences A, B, C, and D as described in the KAI−0340 Device Specification (See References).

For Timing Modes 4−7, the Line Tables are Identical except that the V6 register entry (used for FDG) is 1 for each Line Table Entry except the last.

Table 16. LINE TABLE 0 DEFAULT SETTING

KAI−0340 Signal	Line Table Data Name	LT0 Entry								
		0	1	2	3	4	5	6	7	Notes
	Count[0..12]	1	600	6	14	1	200	600	0	
	HCLK_H Enable	0	0	0	0	0	0	0	0	
FDG	V6	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	1
	V5	0	0	0	0	0	0	0	0	
V1	V4	0	0	0	1	0	0	0	0	
V2	V3	0	1	1	1	1	1	0	0	
VCLK_ENABLE	V2	0	0	0	0	0	0	0	0	
V3RD	V1	0	0	1	1	1	0	0	0	

Table 17. LINE TABLE 1 DEFAULT SETTING

KAI−0340 Signal	Line Table Data Name	LT1 Entry							
		0	1	2	3	4	5	6	Notes
	Count[0..12]	1	5	12	2	1	17	0	
	HCLK_H Enable	0	0	0	0	0	1	0	
FDG	V6	0/1	0/1	0/1	0/1	0/1	0/1	0	1
	V5	0	0	0	0	0	0	0	
V1	V4	0	0	1	0	0	0	0	
V2	V3	0	1	1	1	0	0	0	
VCLK_ENABLE	V2	0	0	0	0	0	0	0	
V3RD	V1	0	0	0	0	0	0	0	

Table 18. LINE TABLE 2 DEFAULT SETTING

KAI−0340 Signal	Line Table Data Name	LT2 Entry							
		0	1	2	3	4	5	6	Notes
	Count[0..12]	1	600	6	14	1	200	600	
	HCLK_H Enable	0	0	0	0	0	0	0	
FDG	V6	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1
	V5	0	0	0	0	0	0	0	
V1	V4	0	0	0	1	0	0	0	
V2	V3	0	1	1	1	1	1	0	
VCLK_ENABLE	V2	1	1	1	1	1	1	1	
V3RD	V1	0	0	1	1	1	0	0	

Table 19. LINE TABLE 3 DEFAULT SETTING

KAI−0340 Signal	Line Table Data Name	LT3 Entry							
		0	1	2	3	4	5	6	Notes
	Count[0..12]	1	3	12	1	1	17	0	
	HCLK_H Enable	0	0	0	0	0	1	0	
FDG	V6	0/1	0/1	0/1	0/1	0/1	0/1	0	1
	V5	0	0	0	0	0	0	0	
V1	V4	0	0	0	0	0	0	0	
V2	V3	0	0	0	0	0	0	0	
VCLK_ENABLE	V2	0	0	0	0	0	0	0	
V3RD	V1	0	0	0	0	0	0	0	

NOTE: For Timing Modes 4−7, V6 (FDG) is “1” for each entry, except the final one.

Register 0: Frame Table Pointer

Register 0 contains the Frame Table Pointer, which instructs the KSC−1000 to perform the timing sequence defined in that table. Frame Table 0 is used for Timing Modes 0 and 1, while Frame Table 1 used for Timing Mode 6.

Table 20. REGISTER 0 DEFAULT SETTING

Register Entry	Timing Mode 0	Timing Mode 1	Timing Mode 6
Frame Table Address	0	0	1

Register 1: General Setup

Table 21. REGISTER 1 DEFAULT SETTINGS

Register Entry	Timing Mode 0	Timing Mode 1	Timing Mode 6
Pixels Per Line[0..12]	740	360	246
Line Valid Pixel Start[0..12]	0	0	0
Line Valid Pixel Quadrature Start[0..12]	0	0	0
Line Valid Pixel End[0..12]	708	366	244
CLPOB1_Pix_Start[0..12]	40	40	40
CLPOB1_Pix_End[0..12]	680	362	239
CLPOB2_Pix_Start[0..12]	14	20	14
CLPOB2_Pix_End[0..12]	34	34	34
CLPDM1_Pix_Start[0..12]	40	40	40
CLPDM1_Pix_End[0..12]	680	362	230
CLPDM2_Pix_Start[0..12]	14	20	14
CLPDM2_Pix_End[0..12]	34	34	34
PBLK_Pix_Start[0..12]	708	366	244
PBLK_Pix_End[0..12]	0	0	0
RG_Enable	1	1	1
H6_Enable	0	0	0
H4_Enable	1	1	1
H5_ Enable	0	0	0
SH2_Enable	1	1	1
SH4_Enable	1	1	1
DATACLK1_Enable	1	1	1
DATACLK2_Enable	1	1	1
PIXCLK_Enable	1	1	1
H3_Enable	1	1	1
H1_Enable	1	1	1
H2_Enable	1	1	1
SH1_Enable	1	1	1
SH3_Enable	1	1	1
H6 24 mA Output Enable	0	0	0
H4 24 mA Output Enable	0	0	0
H5 24 mA Output Enable	0	0	0
RG 24 mA Output Enable	0	0	0
SH2 24 mA Output Enable	0	0	0
SH4 24 mA Output Enable	0	0	0
DATACLK1 24 mA Output Enable	0	0	0
DATACLK2 24 mA Output Enable	0	0	0
H3 24 mA Output Enable	0	0	0
H1 24 mA Output Enable	0	0	0
H2 24 mA Output Enable	0	0	0
SH1 24 mA Output Enable	0	0	0
SH3 24 mA Output Enable	0	0	0
DLL Frequency Range Select	10	10	10

Register 3: INTG_START Setup

Table 22. REGISTER 3 DEFAULT SETTING

Register Entry	Data
Electronic Shutter Setup Clocks[0..9]	1
Electronic Shutter Pulse Width[0..9]	40
Electronic Shutter Hold Clocks [0..9]	40

Register 4: INTG_START Line

Table 23. REGISTER 4 DEFAULT SETTING

SW[7..6]	Frame Integration	Integrate Start Pulse Line Number[0..12]
00	1	500
01	3/4	122
10	1/2	244
11	1/4	366

Register 5: Signal Polarity

The H1 and H2 KSC−1000 signals are connected to the H2B and H1B signals, respectively, on the KAI−0340 Imager Board (See Table 27). For Dual channel operation, the polarity of these signals is reversed, as shown in Table 24. This is the only change necessary in Register 5 for the various Timing Modes.

Table 24. REGISTER 5 DEFAULT SETTING

Register Entry	Single Output	Dual Output
H6_IDLE_VAL	0	0
H3_IDLE_VAL	1	1
H4_IDLE_VAL	0	0
H1_IDLE_VAL	1	0
H5_IDLE_VAL	0	0
H2_IDLE_VAL	0	1
RG_IDLE_VAL	1	1
SH2_IDLE_VAL	1	1
SH1_IDLE_VAL	1	1
SH4_IDLE_VAL	1	1
SH3_IDLE_VAL	1	1
DATACLK1_IDLE_VAL	0	0
DATACLK2_IDLE_VAL	0	0
CLPOB_IDLE_VAL	1	1
CLPDM_IDLE_VAL	1	1
AMP_ENABLE_IDLE_VAL	0	0
FRAME_VALID_IDLE_VAL	0	0
LINE_VALID_IDLE_VAL	0	0
INTEGRATE_START_IDLE_VAL	1	1
V1_IDLE_VAL	1	1
V2_IDLE_VAL	1	1
V3_IDLE_VAL	1	1
V4_IDLE_VAL	0	0
V5_IDLE_VAL	0	0
V6_IDLE_VAL	1	1

Register 6: Pixel-Rate Signal Offset

Table 25. REGISTER 6 DEFAULT SETTING

Register Entry	Single Output	Dual Output	KAI−0340 Signal Name
H6_OFFSET[0..5]	0	0	(Not Used)
H3_OFFSET[0..5]	37	37	H1A
H4_OFFSET[0..5]	32	32	H2A
H1_OFFSET[0..5]	37	32	H2B
H5_OFFSET[0..5]	0	0	(Not Used)
H2_OFFSET[0..5]	38	38	H1B
RG_OFFSET[0..5]	7	7	RESET
SH2_OFFSET[0..5]	4	4	SHP1
SH1_OFFSET[0..5]	5	5	SHP2
SH4_OFFSET[0..5]	32	32	SHD1
SH3_OFFSET[0..5]	27	27	SHD2
DATACLK1_OFFSET[0..5]	54	54	ADCLK (to AFEs)
DATACLK2_OFFSET[0..5]	48	48	DATACLK (to Framegrabber)

Register 7: Pixel-Rate Signal Width

Table 26. REGISTER 7 DEFAULT SETTING

Register Entry	Single Output	Dual Output	KAI−0340 Signal Name
H6_OFFSET[0..5]	0	0	(Not Used)
H3_OFFSET[0..5]	37	37	H1A
H4_OFFSET[0..5]	32	32	H2A
H1_OFFSET[0..5]	37	32	H2B
H5_OFFSET[0..5]	0	0	(Not Used)
H2_OFFSET[0..5]	38	38	H1B
RG_OFFSET[0..5]	7	7	RESET
SH2_OFFSET[0..5]	4	4	SHP1
SH1_OFFSET[0..5]	5	5	SHP2
SH4_OFFSET[0..5]	32	32	SHD1
SH3_OFFSET[0..5]	27	27	SHD2
DATACLK1_OFFSET[0..5]	54	54	ADCLK (to AFEs)
DATACLK2_OFFSET[0..5]	48	48	DATACLK (to Framegrabber)

KAI−0340 TIMING

Line Table 0 (Sequence A)

Line Table 0 corresponds to Sequence A in the KAI−0340 device specification (See References). This is the Frame Transfer timing sequence that transfers charge from all the photodiodes to the vertical register.

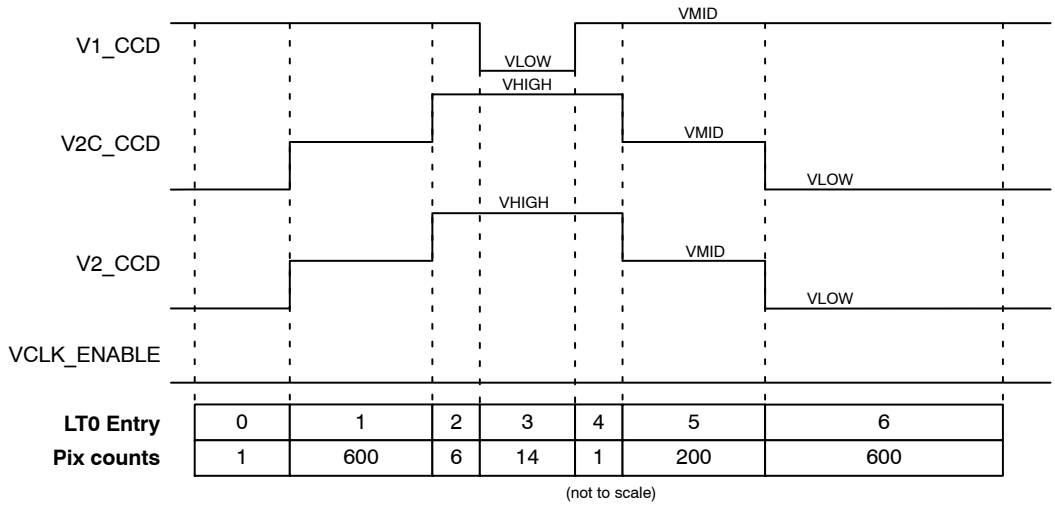


Figure 4. Line Table 0 Default Timing

Line Table 1 (Sequence B)

Line Table 1 corresponds to Sequence B in the KAI−0340 device specification (See References). This is the Line Transfer timing sequence that transfers one entire row charge toward the Horizontal register.

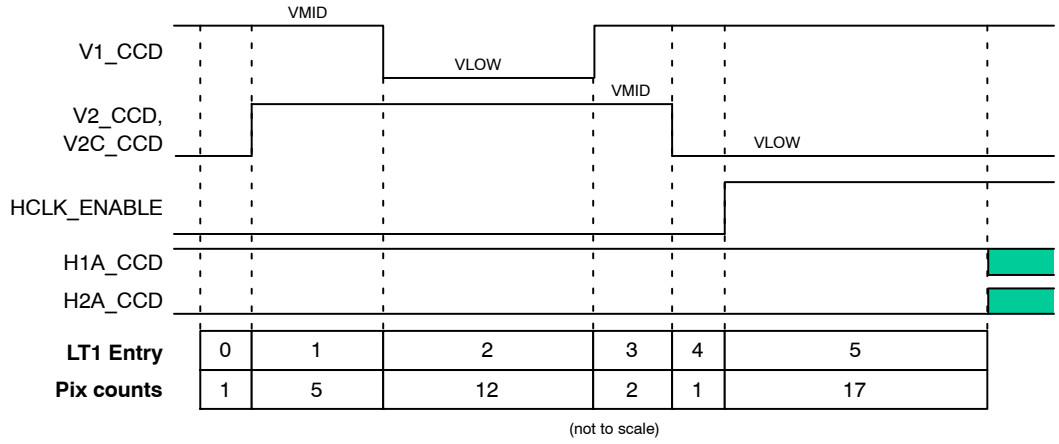


Figure 5. Line Table 1 Default Timing

Line Table 2 (Sequence C)

Line Table 2 corresponds to Sequence C in the KAI−0340 device specification (See References). This is the Frame Transfer timing sequence that transfers charge from the photodiodes in the center rows of the CCD to the vertical register. Note that V2_CCD, which clocks the outer rows of the imager, is not driven to the VHIGH level; therefore charge in the outer rows is not transferred from photodiode to vertical register.

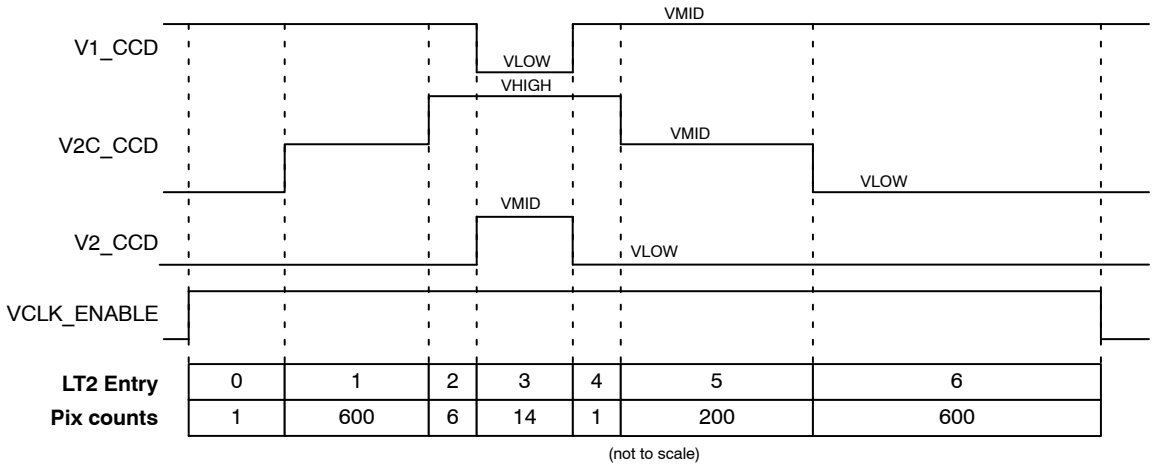


Figure 6. Line Table 2 Default Timing

Line Table 3 (Sequence D)

Line Table 3 corresponds to Sequence D in the KAI−0340 device specification (See References). This is the Line Transfer timing sequence during which the Vertical clocks are inactive; no charge is transferred into the Horizontal register, thereby creating a “dummy” or overclocked line.

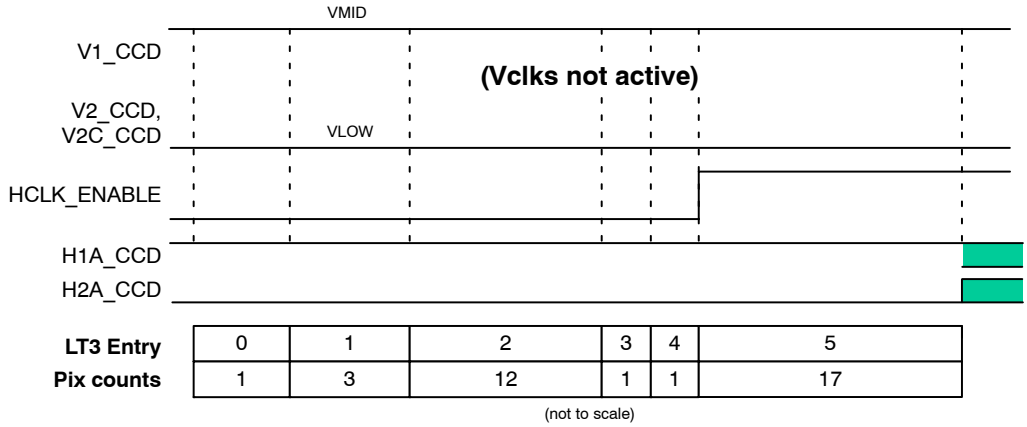
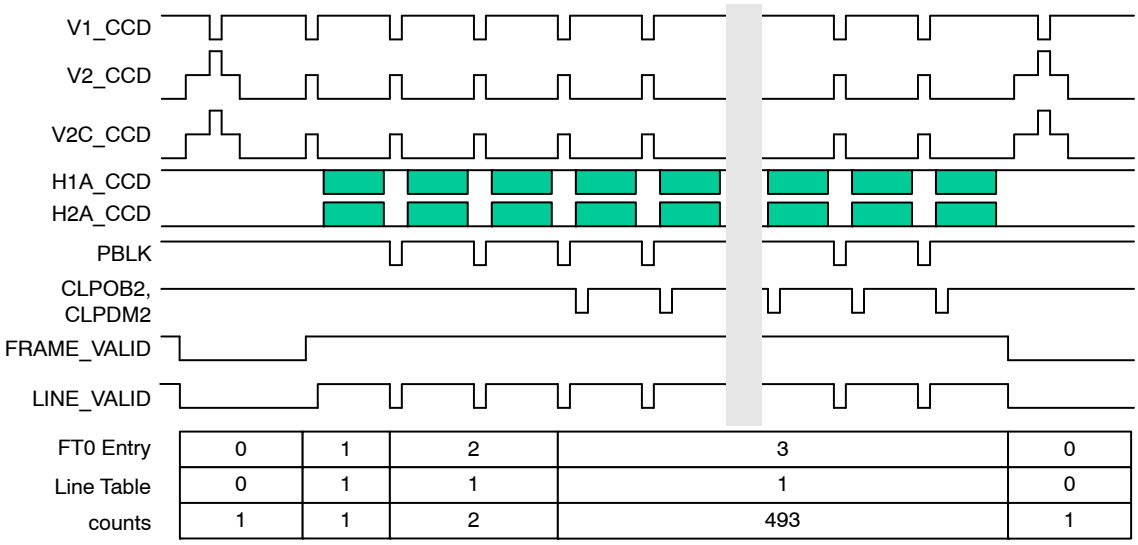


Figure 7. Line Table 3 Default Timing

Frame Table 0 Sequence

Frame Table 0 contains the timing sequence used to read out all rows of the CCD.

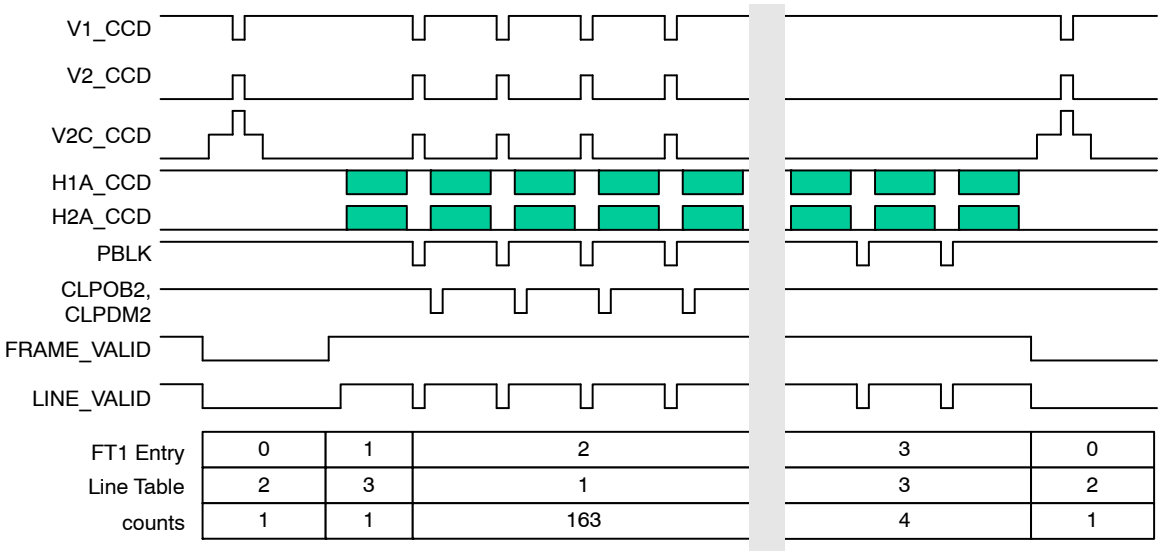


FT0 Entry	0	1	2	3	0
Line Table	0	1	1	1	0
counts	1	1	2	493	1

Figure 8. Frame Table 0 Default Timing

Frame Table 1 Sequence

Frame Table 1 contains the timing sequence used to read out only the center rows of the CCD. It contains one "dummy" line at the beginning of the frame, and four "dummy" lines at the end of the frame.



FT1 Entry	0	1	2	3	0
Line Table	2	3	1	3	2
counts	1	1	163	4	1

Figure 9. Frame Table 1 Default Timing

Electronic Shutter Timing

The electronic shutter timing is controlled by the values in Register 3 and Register 4. The setup, width, and hold times are determined by the values in Register 3, while the Line number on which the Electronic Shutter occurs is controlled by the Integrate Start Pulse Line Number value in Register 4. The shutter sequence is inserted before the specified line, so that line time is extended accordingly.

If the Integrate Start Pulse Line Number value in Register 4 is set to 0, the Electronic Shutter will occur immediately following the Diode Transfer sequence, before the first line is read out. If the Integrate Start Pulse Line Number value is greater than the number of vertical lines in the Frame Table, there will be no Electronic Shutter. This is the method used to disable the Electronic Shutter.

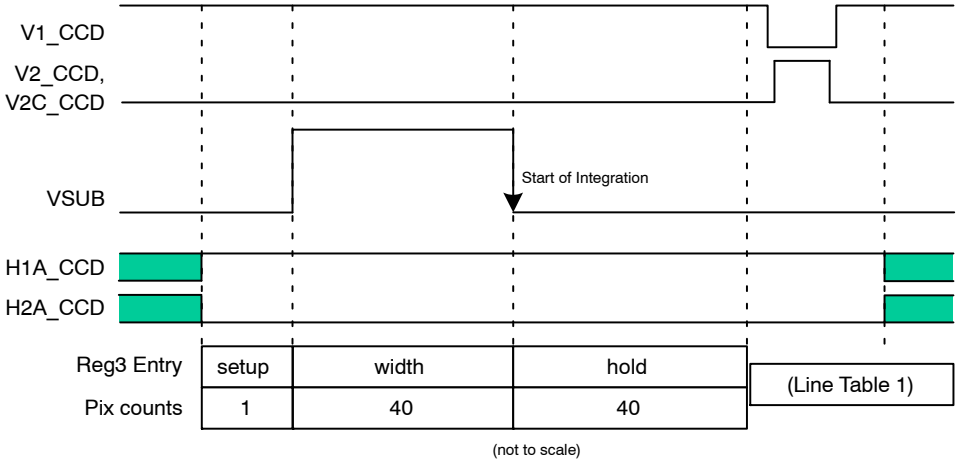


Figure 10. Electronic Shutter Timing

Horizontal Timing

Figure 11 depicts the basic theoretical relationship between the pixel-rate clocks to the CCD, the Video output of the CCD, and the pixel-rate clocks to the AFE.

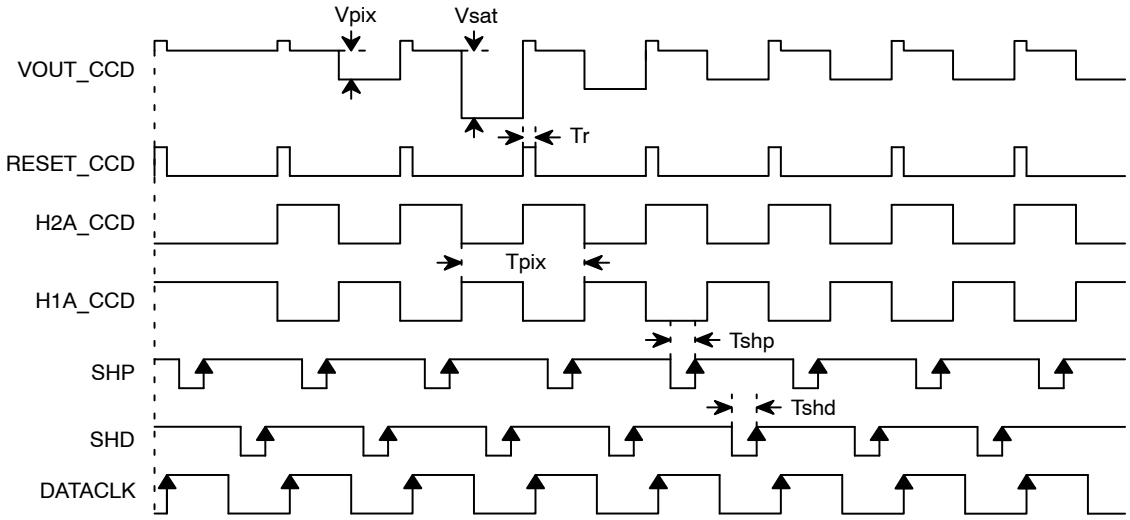


Figure 11. Horizontal Timing

BOARD INTERFACE CONNECTOR SIGNAL MAP

For reference, the board interface timing signals from the 3F5054 Timing Board to the 3E8422 Imager Board are shown in Table 27. Note that the power connections are not shown here.

Table 27. TIMING BOARD/IMAGER BOARD SIGNAL MAP

KSC−1000 Timing Board			KAI−0340 Imager Board		
KSC−1000 Signal Name	**LVDS Interface Signal Name (±)**	**3F5054J6 Pins**	**3E8422J1 Pins**	**LVDS Interface Signal Name (±)**	**Imager Board Signal Name**
V5	TIMING_OUT0	1/2	1/2	(NC)	
INTG_START	TIMING_OUT1	5/6	5/6	IMAGER_IN11	VES
V6	TIMING_OUT2	9/10	9/10	IMAGER_IN10	FDG
V1	TIMING_OUT3	13/14	13/14	IMAGER_IN9	V3RD
V2	TIMING_OUT4	17/18	17/18	IMAGER_IN8	VCLK_ENABLE
V3	TIMING_OUT5	21/22	21/22	IMAGER_IN7	V2
V4	TIMING_OUT6	25/26	25/26	IMAGER_IN6	V1
RG	TIMING_OUT7	29/30	29/30	IMAGER_IN5	RESET
H1	TIMING_OUT8	33/34	33/34	IMAGER_IN4	H2B
H4	TIMING_OUT9	37/38	37/38	IMAGER_IN3	H2A
H2	TIMING_OUT10	41/42	41/42	IMAGER_IN2	H1B
H3	TIMING_OUT11	45/46	45/46	IMAGER_IN1	H1A
H6	TIMING_OUT12	51/52	51/52	(NC)	
H5	TIMING_OUT13	55/56	55/56	(NC)	
AMP_EN	TIMING_OUT14	59/60	59/60	IMAGER_IN0	AMP_ENABLE
SCLOCK	TIMING_OUT15	63/64	63/64	IMAGER_IN15	(Not Used)
SDATA	TIMING_OUT16	67/68	67/68	IMAGER_IN14	(Not Used)
PLD_OUT2	TIMING_OUT17	71/72	71/72	IMAGER_IN13	FDG_CENTER
PLD_OUT0	TIMING_OUT18	75/76	75/76	IMAGER_IN12	VIDEO_MUX
PLD_OUT1	TIMING_OUT19	79/80	79/80	(NC)	

VIDEO SIGNAL PATH

The entire video signal path through the Imager Board and Timing Board is represented in Figure 12. The individual blocks are discussed in the Imager Board User Manual and the Timing Board User Manual.

The gain for the entire signal path can be calculated by multiplying the gains of the individual stages.

$$0.96 \times 1.25 \times 0.5 \times 1.25 = 0.75 \qquad \text{(eq. 1)}$$

The gain of the hardware signal path is designed so that the Saturation output voltage of the KAI−0340 CCD will not overload the AFE input. The Saturation output voltage of the KAI−0340 is specified as 1200 mV (See References). The AFE default CDS gain is set at 1.0 (0.0 dB), and the default VGA gain is set at 1.66 (4.4 dB) to maximize the dynamic range of the AFE (See Table 12 and References).

At pixel rates greater than 20 MHz, the KAI−0340 device specification recommends that the saturation output be limited to 600 mV, by adjusting the substrate voltage (See References). This guarantees the linearity of the output amplifier response at the higher clock speed. Under these conditions, the dynamic range of the AFE will not be optimized, since the hardware gain and AFE programmed gain were designed to accommodate the 1200 mV Saturation output.

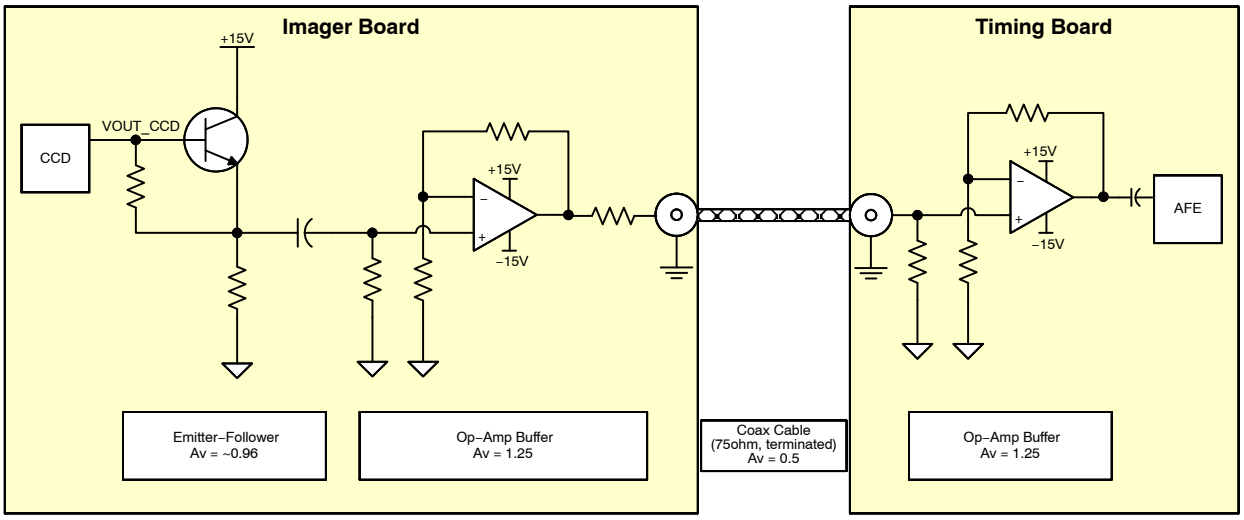


Figure 12. Video Signal Path Diagram

WARNINGS AND ADVISORIES

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a ON Semiconductor Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

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REFERENCES

[1] KAI−0340 Device Specification
[2] KAI−0340 Imager Board User Manual
[3] KAI−0340 Imager Board Schematic
[4] KSC−1000 Timing Generator Board User Manual
[5] KSC−1000 Timing Generator Board Schematic
[6] Analog Devices AD9840A Product Data Sheet (40 MHz operation)

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