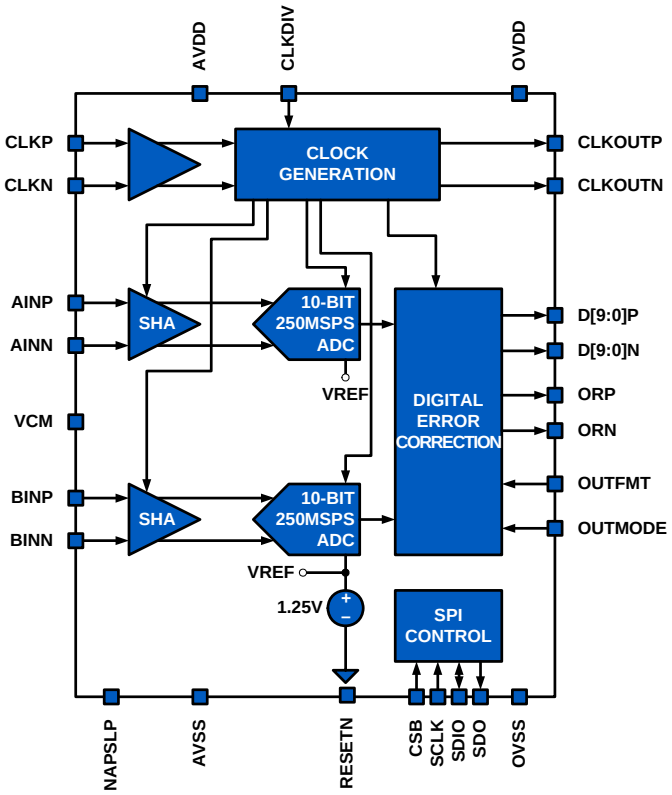
# Dual 10-Bit, 250/210/170/125MSPS A/D Converter

The KAD5610P is a family of low-power, high-performance, dual-channel 10-bit, analog-to-digital converters. Designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process, the family supports sampling rates of up to 250MSPS. The KAD5610P-25 is the fastest member of this pin-compatible family, which also features sample rates of 210MSPS (KAD5610P-21), 170MSPS (KAD5610P-17) and 125MSPS (KAD5610P-12).

A serial peripheral interface (SPI) port allows for extensive configurability, as well as fine control of gain, skew and offset matching between the two converter cores.

Digital output data is presented in selectable LVDS or CMOS formats. The KAD5610P is available in a 72-contact QFN package with an exposed paddle. Performance is specified over the full industrial temperature range (-40°C to +85°C).




## Features

- Programmable Gain, Offset and Skew control
- 1.3GHz Analog Input Bandwidth
- 60fs Clock Jitter
- Over-Range Indicator
- Selectable Clock Divider: ÷1, ÷2 or ÷4
- Clock Phase Selection
- Nap and Sleep Modes
- Two's Complement, Gray Code or Binary Data Format
- DDR LVDS-Compatible or LVCMOS Outputs
- Programmable Built-in Test Patterns
- Single-Supply 1.8V Operation

## Applications

- Power Amplifier Linearization
- Radar and Satellite Antenna Array Processing
- Broadband Communications
- High-Performance Data Acquisition
- Communications Test Equipment
- WiMAX and Microwave Receivers

## Key Specifications

- SNR = 60.7dBFS for $f_{IN}$ = 105MHz (-1dBFS)
- SFDR = 86.1dBc for $f_{IN}$ = 105MHz (-1dBFS)
- Power consumption
  - 411mW @ 250MSPS
  - 327mW @ 125MSPS

## Pin-Compatible Family

| MODEL | RESOLUTION | SPEED (MSPS) |
|---|---|---|
| KAD5612P-25 | 12 | 250 |
| KAD5612P-21 | 12 | 210 |
| KAD5612P-17 | 12 | 170 |
| KAD5612P-12 | 12 | 125 |
| KAD5610P-25 | 10 | 250 |
| KAD5610P-21 | 10 | 210 |
| KAD5610P-17 | 10 | 170 |
| KAD5610P-12 | 10 | 125 |



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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FemtoCharge is a trademark of Kenet Inc. Copyright Intersil Americas Inc. 2008. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

## Ordering Information

| PART NUMBER (Note) | PART MARKING | SPEED (MSPS) | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|---|
| KAD5610P-25Q72 | KAD5610P-25 Q72EP-I | 250 | -40 to +85 | 72 Ld QFN | L72.10X10D |
| KAD5610P-21Q72 | KAD5610P-21 Q72EP-I | 210 | -40 to +85 | 72 Ld QFN | L72.10X10D |
| KAD5610P-17Q72 | KAD5610P-17 Q72EP-I | 170 | -40 to +85 | 72 Ld QFN | L72.10X10D |
| KAD5610P-12Q72 | KAD5610P-12 Q72EP-I | 125 | -40 to +85 | 72 Ld QFN | L72.10X10D |

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Table of Contents


**Absolute Maximum Ratings** ..... **4**

**Thermal Information** ..... **4**

**Electrical Specifications** ..... **4**

**Digital Specifications** ..... **6**

**Timing Diagrams** ..... **6**

**Switching Specifications** ..... **7**

**Pinout/Package Information** ..... **8**

- Pin Descriptions ..... 8
- Pinout ..... 9

**Typical Performance Curves** ..... **10**

**Theory of Operation** ..... **13**

- Functional Description ..... 13
- Power-On Calibration ..... 13
- User-Initiated Reset ..... 14
- Analog Input ..... 14
- Clock Input ..... 15
- Jitter ..... 15
- Voltage Reference ..... 16
- Digital Outputs ..... 16
- Over-Range Indicator ..... 16
- Power Dissipation ..... 16
- Nap/Sleep ..... 16
- Data Format ..... 17

**Serial Peripheral Interface** ..... **19**

- SPI Physical Interface ..... 19
- SPI Configuration ..... 19
- Device Information ..... 20
- Indexed Device Configuration/Control ..... 20
- Global Device Configuration/Control ..... 21
- Device Test ..... 22
- SPI Memory Map ..... 23

**Equivalent Circuits** ..... **24**

**Layout Considerations** ..... **25**

- Split Ground and Power Planes ..... 25
- Clock Input Considerations ..... 25
- Exposed Paddle ..... 25
- Bypass and Filtering ..... 25
- LVDS Outputs ..... 25
- LVCMOS Outputs ..... 25
- Unused Inputs ..... 25

**Definitions** ..... **26**

**Revision History** ..... **26**

**Package Outline Drawing** ..... **27**

- L72.10x10D ..... 27

## Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS. . . . . -0.3V to 0.3V
Analog Inputs to AVSS. . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS. . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS. . . . . -0.4V to OVDD + 0.3V

## Thermal Information

| Thermal Resistance (Typical), Note 2 | $\theta_{JA}$ (°C/W) |
|---|---|
| 72 Ld QFN | 24 |

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

2. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

## Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, $T_A$ = -40°C to +85°C (typical specifications at +25°C), $A_{IN}$ = -1dBFS, $f_{SAMPLE}$ = Maximum Conversion Rate (per speed grade).

| PARAMETER | SYMBOL | CONDITIONS | KAD5610P-25 | | | KAD5610P-21 | | | KAD5610P-17 | | | KAD5610P-12 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DC SPECIFICATIONS** | | | | | | | | | | | | | | | |
| **Analog Input** | | | | | | | | | | | | | | | |
| Full-Scale Analog Input Range | $V_{FS}$ | Differential | 1.4 | 1.47 | 1.54 | 1.4 | 1.47 | 1.54 | 1.4 | 1.47 | 1.54 | 1.4 | 1.47 | 1.54 | $V_{P-P}$ |
| Input Resistance | $R_{IN}$ | Differential | | 1000 | | | 1000 | | | 1000 | | | 1000 | | Ω |
| Input Capacitance | $C_{IN}$ | Differential | | 1.8 | | | 1.8 | | | 1.8 | | | 1.8 | | pF |
| Full Scale Range Temp. Drift | $A_{VTC}$ | Full Temp | | 90 | | | 90 | | | 90 | | | 90 | | ppm/°C |
| Input Offset Voltage | $V_{OS}$ | | -10 | ±2 | 10 | -10 | ±2 | 10 | -10 | ±2 | 10 | -10 | ±2 | 10 | mV |
| Gain Error | $E_G$ | | | ±2 | | | ±0.6 | | | ±0.6 | | | ±0.6 | | % |
| Common-Mode Output Voltage | $V_{CM}$ | | 435 | 535 | 635 | 435 | 535 | 635 | 435 | 535 | 635 | 435 | 535 | 635 | mV |
| **Clock Inputs** | | | | | | | | | | | | | | | |
| Inputs Common Mode Voltage | | | | 0.9 | | | 0.9 | | | 0.9 | | | 0.9 | | V |
| CLKP,CLKN Input Swing | | | | 1.8 | | | 1.8 | | | 1.8 | | | 1.8 | | V |
| **Power Requirements** | | | | | | | | | | | | | | | |
| 1.8V Analog Supply Voltage | AVDD | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| 1.8V Digital Supply Voltage | OVDD | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| 1.8V Analog Supply Current | IAVDD | | | 170 | 177 | | 158 | 165 | | 142 | 152 | | 128 | 135 | mA |
| 1.8V Digital Supply Current (Note 3) | $I_{OVDD}$ | 3mA LVDS | | 58 | 65 | | 57 | 63 | | 55 | 62 | | 53 | 60 | mA |
| Power Supply Rejection Ratio | PSRR | 30MHz, 200m$V_{P-P}$ signal on AVDD | | -36 | | | -36 | | | -36 | | | -36 | | dB |
| **Power Dissipation** | | | | | | | | | | | | | | | |
| Normal Mode | PD | 3mA LVDS | | 411 | 438 | | 387 | 411 | | 357 | 387 | | 327 | 351 | mW |
| Nap Mode | PD | | | 148 | 163 | | 142 | 157 | | 136 | 151 | | 129 | 143 | mW |
| Sleep Mode | PD | | | 15 | 18 | | 14 | 17 | | 13 | 16 | | 12 | 15 | mW |

**Electrical Specifications** All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, $T_A$ = -40°C to +85°C (typical specifications at +25°C), $A_{IN}$ = -1dBFS, $f_{SAMPLE}$ = Maximum Conversion Rate (per speed grade). **(Continued)**

| PARAMETER | SYMBOL | CONDITIONS | KAD5610P-25 | | | KAD5610P-21 | | | KAD5610P-17 | | | KAD5610P-12 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **AC SPECIFICATIONS (Note 4)** | | | | | | | | | | | | | | | |
| Differential Nonlinearity | DNL | | -0.5 | ±0.12 | 0.5 | -0.5 | ±0.17 | 0.5 | -0.5 | ±0.17 | 0.5 | -0.5 | ±0.17 | 0.5 | LSB |
| Integral Nonlinearity | INL | | -0.75 | ±0.2 | 0.75 | -0.75 | ±0.3 | 0.75 | -0.75 | ±0.3 | 0.75 | -0.75 | ±0.3 | 0.75 | LSB |
| Minimum Conversion Rate (Note 5) | $f_S$ MIN | | | | 40 | | | 40 | | | 40 | | | 40 | MSPS |
| Maximum Conversion Rate | $f_S$ MAX | | 250 | | | 210 | | | 170 | | | 125 | | | MSPS |
| Signal-to-Noise Ratio (Note 4) | SNR | $f_{IN}$ = 10MHz | | 60.8 | | | 60.8 | | | 61.0 | | | 61.0 | | dBFS |
| | | $f_{IN}$ = 105MHz | 59.5 | 60.7 | | 60.0 | 60.9 | | 60.2 | 61.0 | | 60.2 | 61.0 | | dBFS |
| | | $f_{IN}$ = 190MHz | | 60.6 | | | 60.8 | | | 60.9 | | | 60.9 | | dBFS |
| | | $f_{IN}$ = 364MHz | | 60.5 | | | 60.6 | | | 60.7 | | | 60.7 | | dBFS |
| | | $f_{IN}$ = 695MHz | | 59.9 | | | 60.0 | | | 60.1 | | | 60.0 | | dBFS |
| | | $f_{IN}$ = 995MHz | | 59.1 | | | 59.2 | | | 59.3 | | | 59.2 | | dBFS |
| Signal-to-Noise and Distortion (Note 4) | SINAD | $f_{IN}$ = 10MHz | | 60.7 | | | 60.8 | | | 60.9 | | | 61.0 | | dBFS |
| | | $f_{IN}$ = 105MHz | 59.3 | 60.7 | | 59.9 | 60.9 | | 60.0 | 60.9 | | 60.0 | 61.0 | | dBFS |
| | | $f_{IN}$ = 190MHz | | 60.5 | | | 60.8 | | | 60.8 | | | 60.9 | | dBFS |
| | | $f_{IN}$ = 364MHz | | 60.4 | | | 60.5 | | | 60.6 | | | 60.4 | | dBFS |
| | | $f_{IN}$ = 695MHz | | 56.5 | | | 57.3 | | | 56.9 | | | 56.6 | | dBFS |
| | | $f_{IN}$ = 995MHz | | 49.8 | | | 46.9 | | | 47.7 | | | 49.1 | | dBFS |
| Effective Number of Bits (Note 4) | ENOB | $f_{IN}$ = 10MHz | | 9.8 | | | 9.8 | | | 9.8 | | | 9.8 | | Bits |
| | | $f_{IN}$ = 105MHz | 9.5 | 9.8 | | 9.6 | 9.8 | | 9.6 | 9.8 | | 9.6 | 9.8 | | Bits |
| | | $f_{IN}$ = 190MHz | | 9.8 | | | 9.8 | | | 9.8 | | | 9.8 | | Bits |
| | | $f_{IN}$ = 364MHz | | 9.7 | | | 9.8 | | | 9.8 | | | 9.7 | | Bits |
| | | $f_{IN}$ = 695MHz | | 9.1 | | | 9.2 | | | 9.2 | | | 9.1 | | Bits |
| | | $f_{IN}$ = 995MHz | | 8.0 | | | 7.5 | | | 7.6 | | | 7.9 | | Bits |
| Spurious-Free Dynamic Range (Note 4) | SFDR | $f_{IN}$ = 10MHz | | 83.0 | | | 82.0 | | | 78.0 | | | 79.0 | | dBc |
| | | $f_{IN}$ = 105MHz | 70.0 | 86.1 | | 70.0 | 86.6 | | 70.0 | 84.6 | | 70.0 | 85.8 | | dBc |
| | | $f_{IN}$ = 190MHz | | 78.0 | | | 80.1 | | | 81.0 | | | 81.2 | | dBc |
| | | $f_{IN}$ = 364MHz | | 76.2 | | | 77.1 | | | 77.9 | | | 72.1 | | dBc |
| | | $f_{IN}$ = 695MHz | | 60.8 | | | 61.9 | | | 61.0 | | | 61.1 | | dBc |
| | | $f_{IN}$ = 995MHz | | 50.2 | | | 47.2 | | | 47.9 | | | 49.4 | | dBc |
| Intermodulation Distortion (Note 4) | IMD | $f_{IN}$ = 70MHz | | -86.1 | | | -92.1 | | | -94.5 | | | -95.1 | | dBFS |
| | | $f_{IN}$ = 170MHz | | -96.9 | | | -87.1 | | | -91.6 | | | -85.7 | | dBFS |
| Channel-to-Channel Isolation | | $f_{IN}$ = 10MHz | | 90 | | | 90 | | | 90 | | | 90 | | dB |
| | | $f_{IN}$ = 124MHz | | 90 | | | 90 | | | 90 | | | 90 | | dB |
| Word Error Rate | WER | | | $10^{-12}$ | | | $10^{-12}$ | | | $10^{-12}$ | | | $10^{-12}$ | | |
| Full Power Bandwidth | FPBW | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | GHz |

NOTES:

3. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. $I_{OVDD}$ specifications apply for 10pF load on each digital output.
4. AC Specifications apply after internal calibration of the ADC is invoked at the given sample rate and temperature. Refer to “Power-On Calibration” on page 13 and “User-Initiated Reset” on page 14 for more details.
5. The DLL Range setting must be changed for low speed operation. See Table 15 on page 22 for more detail.

## Digital Specifications

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUTS** | | | | | | |
| Input Current High (SDIO,RESETN) | $I_{IH}$ | $V_{IN}$ = 1.8V | 0 | 1 | 10 | µA |
| Input Current Low (SDIO,RESETN) | $I_{IL}$ | $V_{IN}$ = 0V | -25 | -12 | -5 | µA |
| Input Voltage High (SDIO, RESETN) | $V_{IH}$ | | 1.17 | | | V |
| Input Voltage Low (SDIO, RESETN) | $V_{IL}$ | | | | .63 | V |
| Input Current High (OUTMODE, NAPSLP, CLKDIV, OUTFMT) (Note 6) | $I_{IH}$ | | 15 | 25 | 40 | µA |
| Input Current Low (OUTMODE, NAPSLP, CLKDIV, OUTFMT) | $I_{IL}$ | | -40 | 25 | -15 | µA |
| Input Capacitance | $C_{DI}$ | | | 3 | | pF |
| **LVDS OUTPUTS** | | | | | | |
| Differential Output Voltage | $V_T$ | 3mA Mode | | 620 | | $mV_{P-P}$ |
| Output Offset Voltage | $V_{OS}$ | 3mA Mode | 950 | 965 | 980 | mV |
| Output Rise Time | $t_R$ | | | 500 | | ps |
| Output Fall Time | $t_F$ | | | 500 | | ps |
| **CMOS OUTPUTS** | | | | | | |
| Voltage Output High | $V_{OH}$ | $I_{OH}$ = -500µA | OVDD - 0.3 | OVDD - 0.1 | | V |
| Voltage Output Low | $V_{OL}$ | $I_{OL}$ = 1mA | | 0.1 | 0.3 | V |
| Output Rise Time | $t_R$ | | | 1.8 | | ns |
| Output Fall Time | $t_F$ | | | 1.4 | | ns |

## *Timing Diagrams*

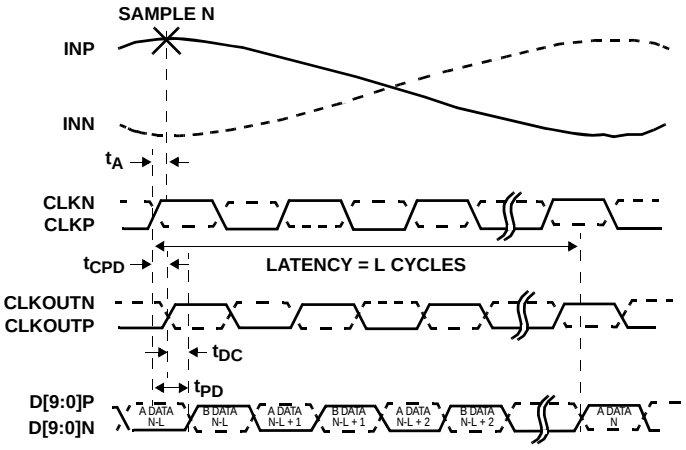



**FIGURE 1. LVDS TIMING DIAGRAM (DDR)**

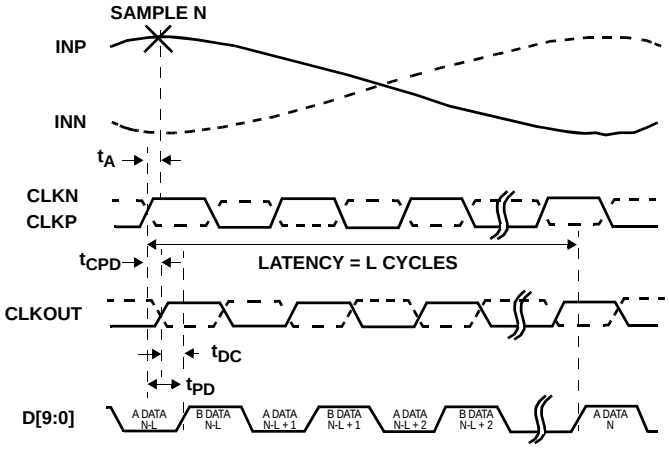



**FIGURE 2. CMOS TIMING DIAGRAM (DDR)**

## Switching Specifications

| PARAMETER | CONDITION | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ADC** | | | | | | |
| Aperture Delay | | $t_A$ | | 375 | | ps |
| RMS Aperture Jitter | | $j_A$ | | 60 | | fs |
| Output Clock to Data Propagation Delay, LVDS Mode (Note 7) | Rising Edge | $t_{DC}$ | -260 | -50 | 120 | ps |
| | Falling Edge | $t_{DC}$ | -160 | 10 | 230 | ps |
| Output Clock to Data Propagation Delay, CMOS Mode (Note 7) | Rising Edge | $t_{DC}$ | -220 | -10 | 200 | ps |
| | Falling Edge | $t_{DC}$ | -310 | -90 | 110 | ps |
| Latency (Pipeline Delay) | | L | | 7.5 | | cycles |
| Overvoltage Recovery | | $t_{OVR}$ | | 1 | | cycles |
| **SPI INTERFACE (Notes 8, 9)** | | | | | | |
| SCLK Period | Write Operation | $t_{CLK}$ | 64 | | | ns |
| | Read Operation | $t_{CLK}$ | 264 | | | ns |
| SCLK Duty Cycle ($t_{HI}/t_{CLK}$ or $t_{LO}/t_{CLK}$) | Read or Write | | 25 | 50 | 75 | % |
| SCLK↑ to CSB↓ Setup Time | Read or Write | $t_S$ | -4 | | | ns |
| SCLK↑ to CSB↑ Hold Time | Read or Write | $t_H$ | -12 | | | ns |
| SCLK↑ to Data Setup Time | Read or Write | $t_{DS}$ | -4 | | | ns |
| SCLK↑ to Data Hold Time | Read or Write | $t_{DH}$ | -12 | | | ns |

NOTES:

6. The Tri-Level Inputs internal switching thresholds are approximately .43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
7. The input clock to output clock delay is a function of sample rate, using the output clock to latch the data simplifies data capture for most applications. Contact factory for more info if needed.
8. SPI Interface timing is directly proportional to the ADC sample period ($t_S$). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates.
9. The SPI may operate asynchronously with respect to the ADC sample clock.

## Pinout/Package Information

### Pin Descriptions

| PIN # | LVDS [LVCMOS] NAME | LVDS [LVCMOS] FUNCTION |
|---|---|---|
| 1, 6, 19, 24, 71 | AVDD | 1.8V Analog Supply |
| 2-5, 17, 18, 28-35 | DNC | Do Not Connect |
| 7, 10-12, 72 | AVSS | Analog Ground |
| 8, 9 | BINP, BINN | B-Channel Analog Input Positive, Negative |
| 13, 14 | AINN, AINP | A-Channel Analog Input Negative, Positive |
| 15 | VCM | Common Mode Output |
| 16 | CLKDIV | Clock Divider Control |
| 20, 21 | CLKP, CLKN | Clock Input True, Complement |
| 22 | OUTMODE | Output Mode (LVDS, LVCMOS) |
| 23 | NAPSLP | Power Control (Nap, Sleep modes) |
| 25 | RESETN | Power On Reset (Active Low, See page 14) |
| 26, 45, 55, 65 | OVSS | Output Ground |
| 27, 36, 56 | OVDD | 1.8V Output Supply |
| 37, 38 | D0N, D0P [NC, D0] | LVDS Bit 0 (LSB) Output Complement, True [NC, LVCMOS Bit 0] |
| 39, 40 | D1N, D1P [NC, D1] | LVDS Bit 1 Output Complement, True [NC, LVCMOS Bit 1] |
| 41, 42 | D2N, D2P [NC, D2] | LVDS Bit 2 Output Complement, True [NC, LVCMOS Bit 2] |
| 43, 44 | D3N, D3P [NC, D3] | LVDS Bit 3 Output Complement, True [NC, LVCMOS Bit 3] |
| 46 | RLVDS | LVDS Bias Resistor (connect to OVSS with a 10kΩ, 1% resistor) |
| 47, 48 | CLKOUTN, CLKOUTP [NC, CLKOUT] | LVDS Clock Output Complement, True [NC, LVCMOS CLKOUT] |
| 49, 50 | D4N, D4P [NC, D4] | LVDS Bit 4 Output Complement, True [NC, LVCMOS Bit 4] |
| 51, 52 | D5N, D5P [NC, D5] | LVDS Bit 5 Output Complement, True [NC, LVCMOS Bit 5] |
| 53, 54 | D6N, D6P [NC, D6] | LVDS Bit 6 Output Complement, True [NC, LVCMOS Bit 6] |
| 57, 58 | D7N, D7P [NC, D7] | LVDS Bit 7 Output Complement, True [NC, LVCMOS Bit 7] |
| 59, 60 | D8N, D8P [NC, D8] | LVDS Bit 8 Output Complement, True [NC, LVCMOS Bit 8] |
| 61, 62 | D9N, D9P [NC, D9] | LVDS Bit 9 (MSB) Output Complement, True [NC, LVCMOS Bit 9] |
| 63, 64 | ORN, ORP [NC, OR] | LVDS Over Range Complement, True [NC, LVCMOS Over Range] |
| 66 | SDO | SPI Serial Data Output **(4.7kΩ pull-up to OVDD is required)** |
| 67 | CSB | SPI Chip Select (active low) |
| 68 | SCLK | SPI Clock |
| 69 | SDIO | SPI Serial Data Input/Output |
| 70 | OUTFMT | Output Data Format (Two's Comp., Gray Code, Offset Binary) |
| Exposed Paddle | AVSS | Analog Ground |

NOTE: LVCMOS Output Mode Functionality is shown in brackets (NC = No Connection).

## Pinout

**KAD5610P**
**(72 LD QFN)**
TOP VIEW

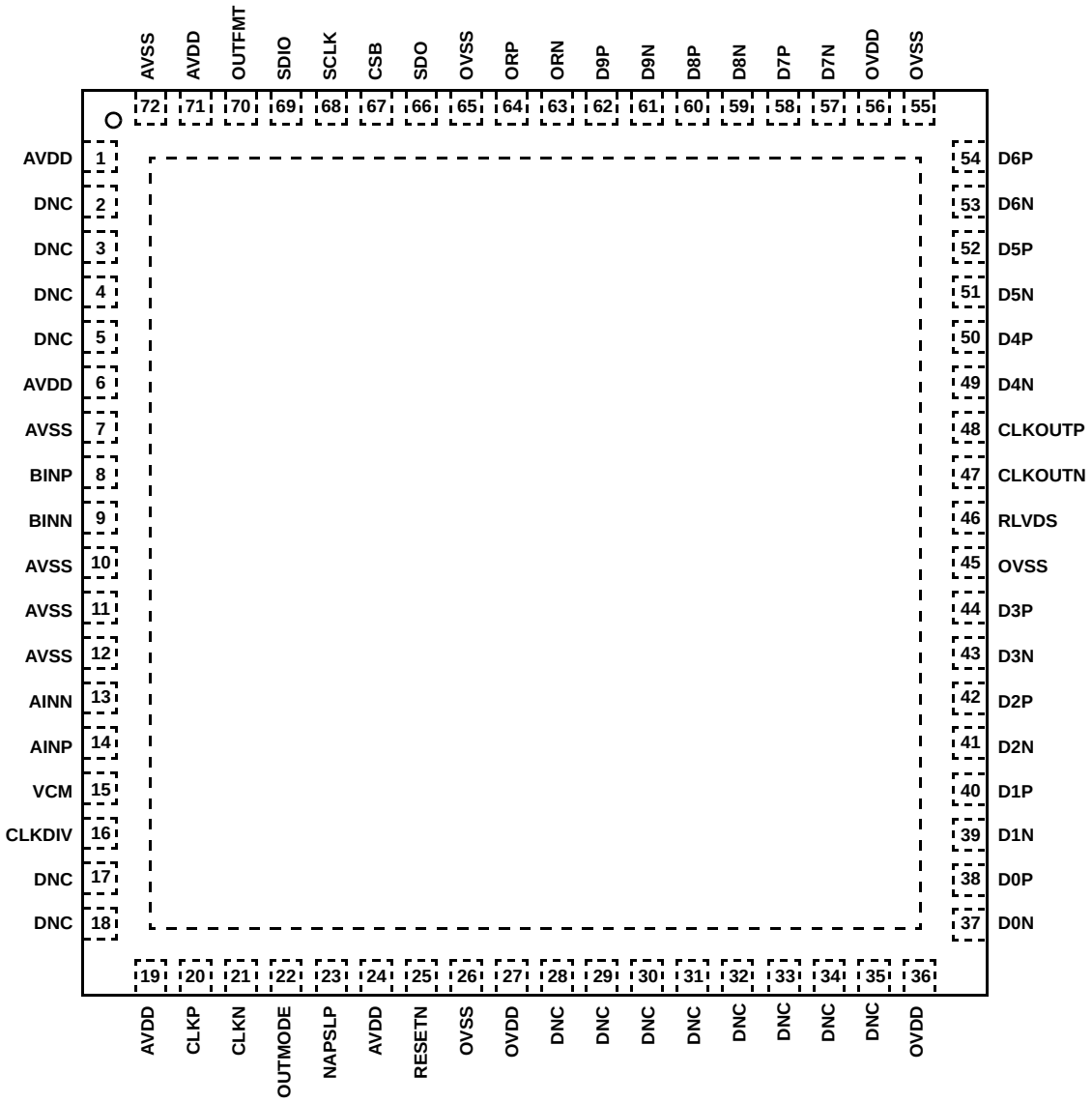



**FIGURE 3. PIN CONFIGURATION**

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = Maximum Conversion Rate (per speed grade).

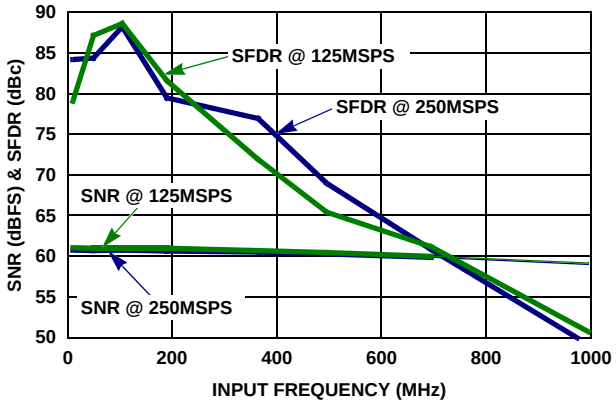



FIGURE 4. SNR AND SFDR vs $f_{IN}$

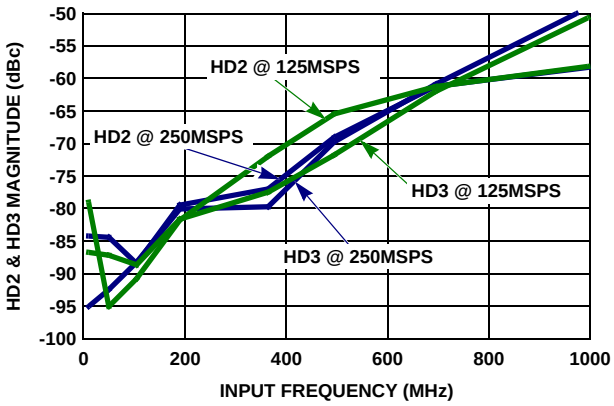



FIGURE 5. HD2 AND HD3 vs $f_{IN}$

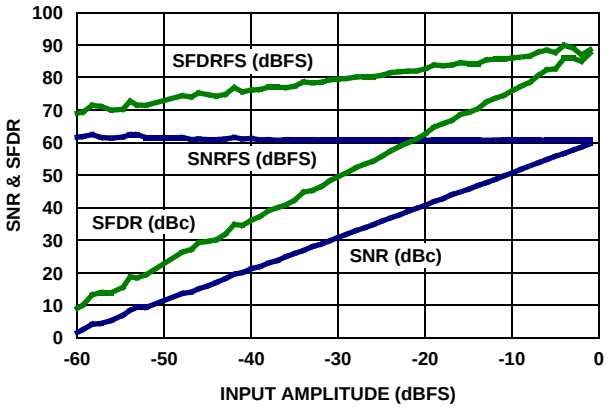



FIGURE 6. SNR AND SFDR vs $A_{IN}$

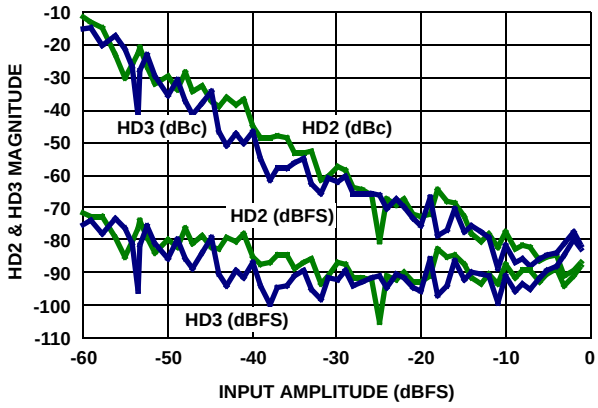



FIGURE 7. HD2 AND HD3 vs $A_{IN}$

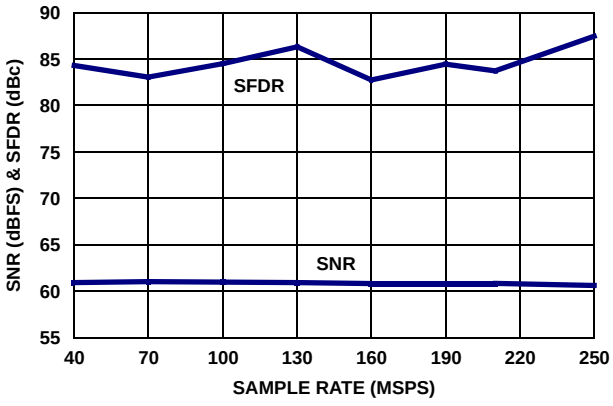



FIGURE 8. SNR AND SFDR vs $f_{SAMPLE}$

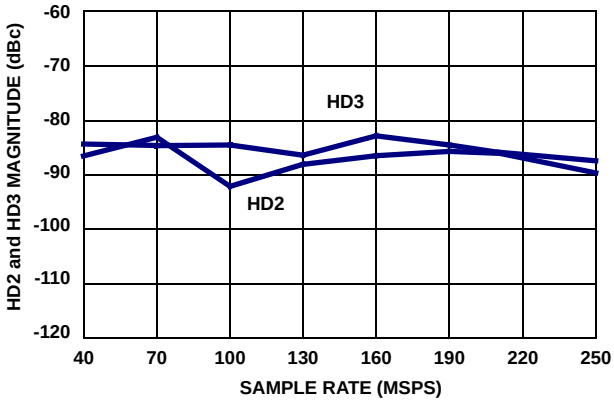



FIGURE 9. HD2 AND HD3 vs $f_{SAMPLE}$

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = Maximum Conversion Rate (per speed grade). **(Continued)**

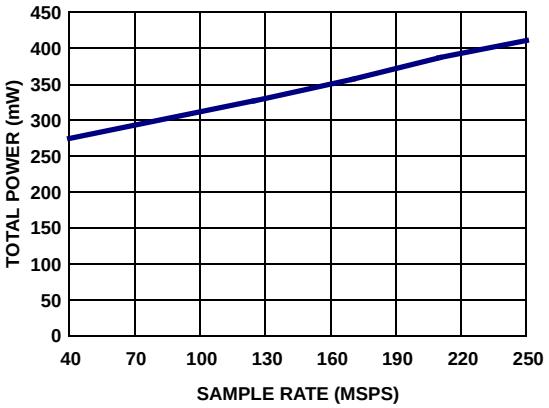



FIGURE 10. POWER vs $f_{SAMPLE}$ IN 3mA LVDS MODE

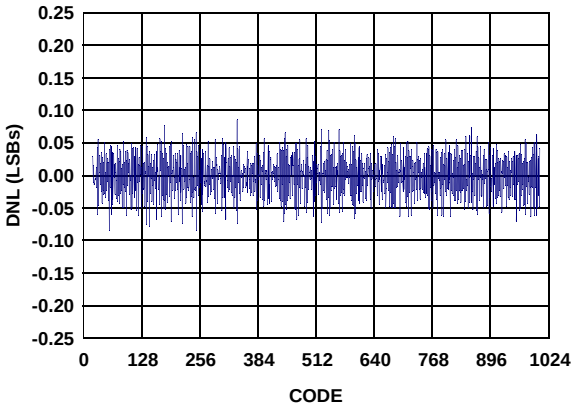



FIGURE 11. DIFFERENTIAL NONLINEARITY

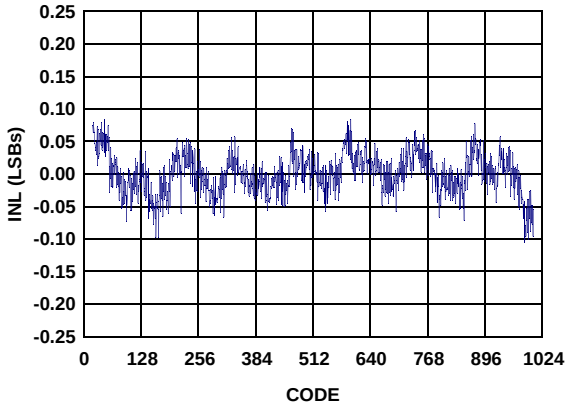



FIGURE 12. INTEGRAL NONLINEARITY

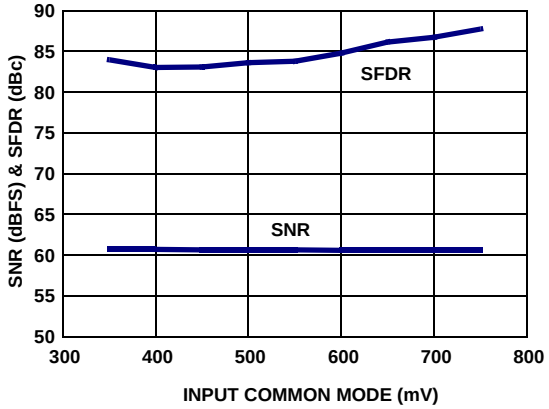



FIGURE 13. SNR AND SFDR vs VCM

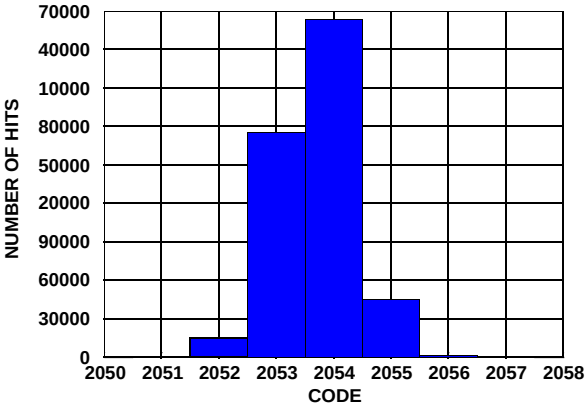



FIGURE 14. NOISE HISTOGRAM

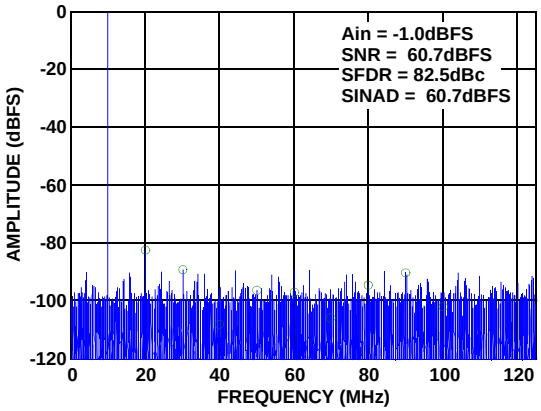



FIGURE 15. SINGLE-TONE SPECTRUM @ 10MHz

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = Maximum Conversion Rate (per speed grade). **(Continued)**

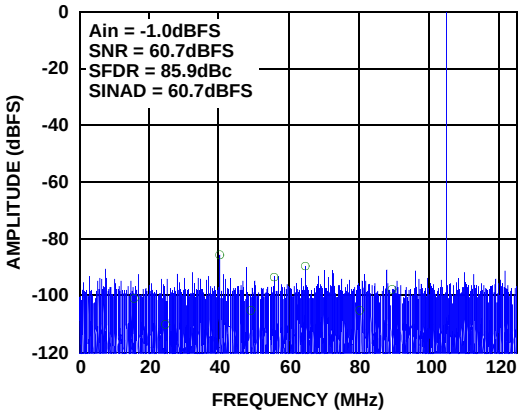



FIGURE 16. SINGLE-TONE SPECTRUM @ 105MHz

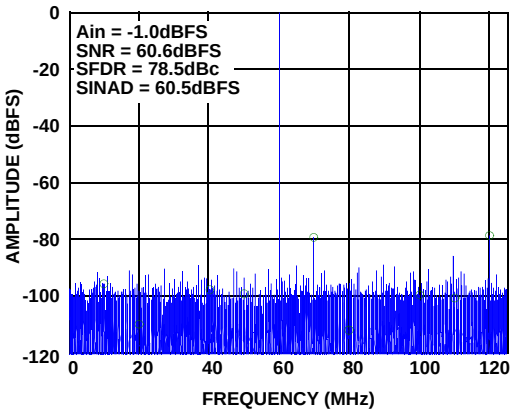



FIGURE 17. SINGLE-TONE SPECTRUM @ 190MHz

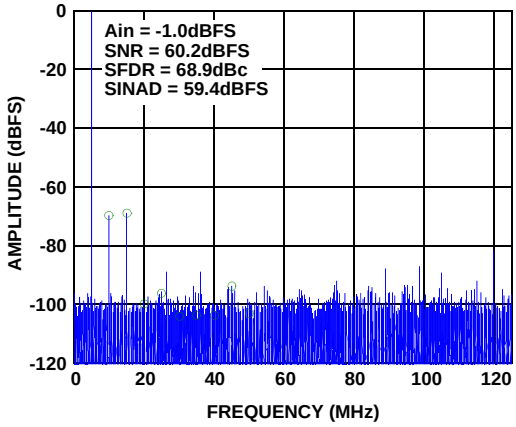



FIGURE 18. SINGLE-TONE SPECTRUM @ 495MHz

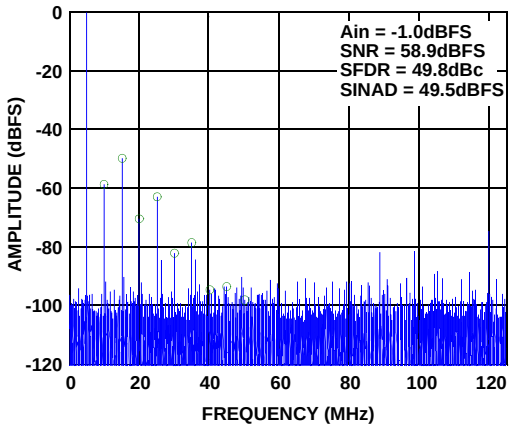



FIGURE 19. SINGLE-TONE SPECTRUM @ 995MHz

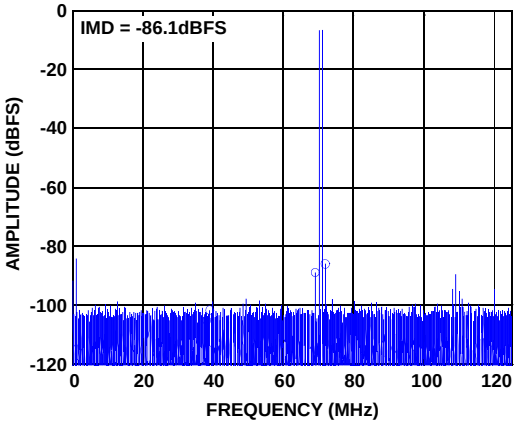



FIGURE 20. TWO-TONE SPECTRUM @ 70MHz

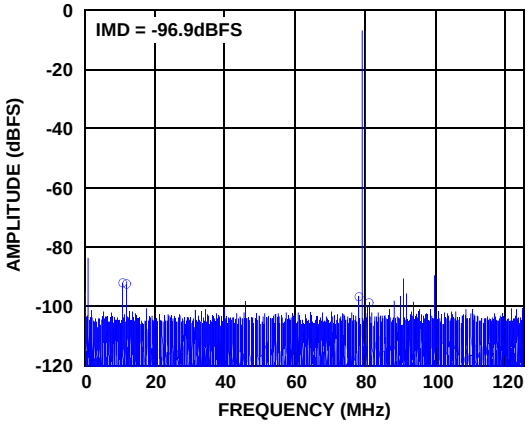



FIGURE 21. TWO-TONE SPECTRUM @ 170MHz

## Theory of Operation

### Functional Description

The KAD5610P is based upon a 10-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 22). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. The converter pipeline requires six samples to produce a result. Digital error correction is also applied, resulting in a total latency of seven and one half clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The device contains two A/D converter cores with carefully matched transfer characteristics. At start-up, each core performs a self-calibration to minimize gain and offset errors. The reset pin (RESETN) is initially set high at power-up and will remain in that state until the calibration is complete. The clock frequency should remain fixed during this time, and no SPI communications should be attempted. Recalibration can be initiated via the SPI port at any time after the initial self-calibration.

### Power-On Calibration

The ADC performs a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins (especially 3, 4 and 18) must not be pulled up or down
- SDO (pin 66) must be high
- RESETN (pin 25) must begin low
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

The SDO pin requires an external 4.7kΩ pull-up to OVDD. If the SDO pin is pulled low externally during power-up, calibration will not be executed properly.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is required, the RESETN pin should be connected to an open-drain driver with a drive strength of less than 0.5mA.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 23. The over-range output (OR) is set high once RESETN is pulled low, and remains in that state until calibration is complete. The OR output returns to normal operation at that time, so it is important that the analog input be within the converter's full-scale range to observe the transition. If the input is in an over-range condition the OR pin will stay high, and it will not be possible to detect the end of the calibration cycle.

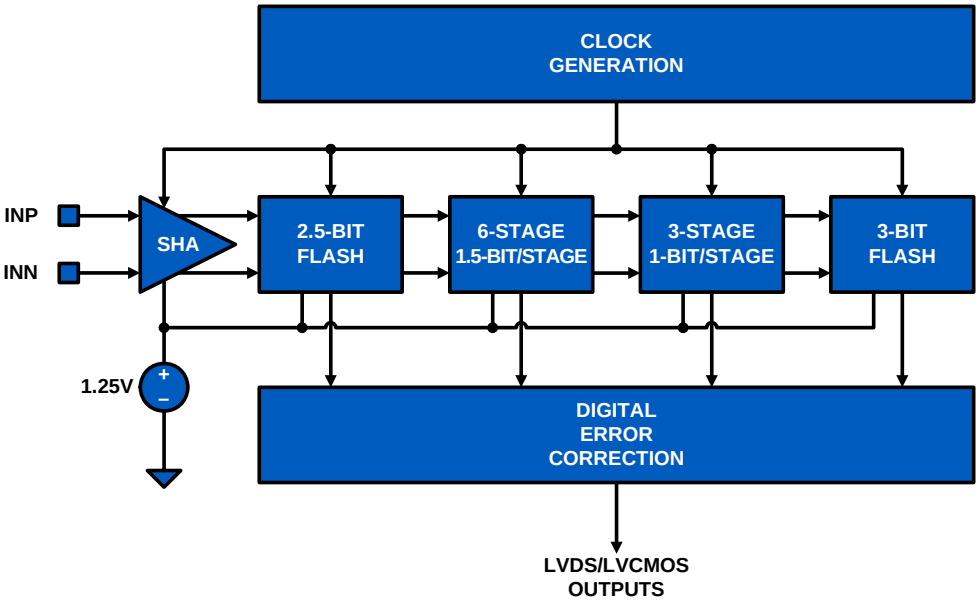



FIGURE 22. ADC CORE BLOCK DIAGRAM

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is deasserted. At 250MSPS the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

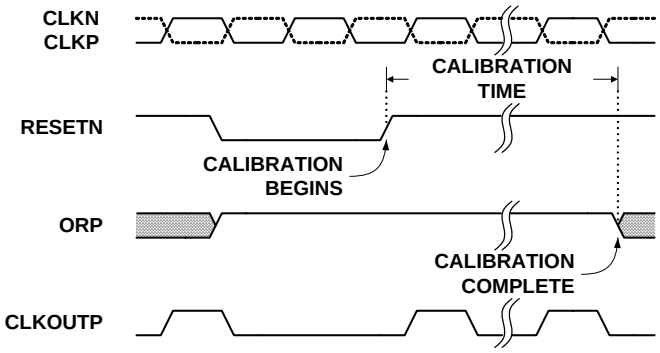



FIGURE 23. CALIBRATION TIMING

### User-Initiated Reset

Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength of less than 0.5mA is recommended, RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, the SDO, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the KAD5610P changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the ADC under the environmental conditions at which it will operate.

A supply voltage variation of less than 100mV will generally result in an SNR change of less than 0.1dBFS and SFDR change of less than 3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 75MSPS will typically result in an SNR change of less than 0.1dBFS and an SFDR change of less than 3dBc.

Figures 25 and 26 show the effect of temperature on SNR and SFDR performance without recalibration. In each plot the ADC is calibrated at +25°C and temperature is varied over the operating range without recalibrating. The average change in SNR/SFDR is shown, relative to the +25°C value.

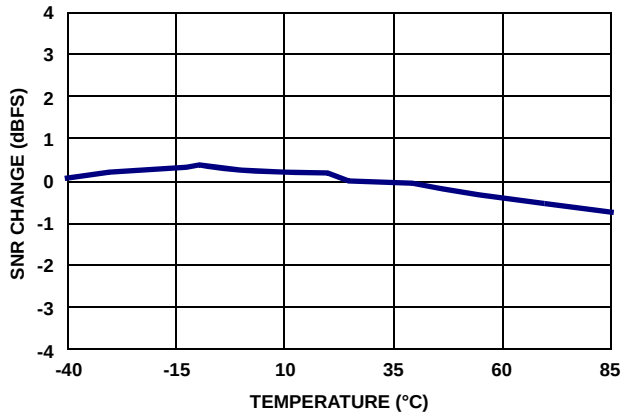



FIGURE 24. SNR PERFORMANCE vs TEMPERATURE AFTER +25°C CALIBRATION

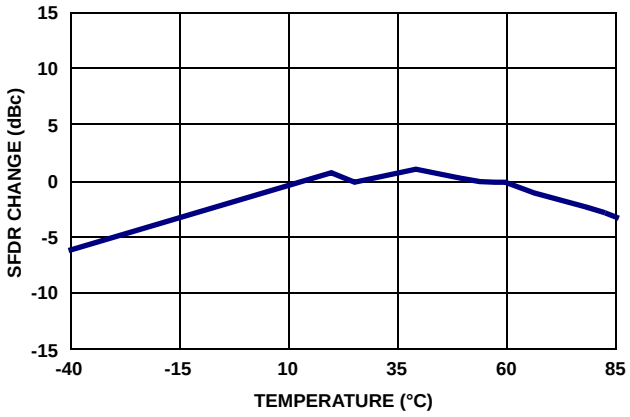



FIGURE 25. SFDR PERFORMANCE vs TEMPERATURE AFTER +25°C CALIBRATION

### Analog Input

Each ADC core contains a fully differential input (AINP/AINN, BINP/BINN) to the sample and hold amplifier (SHA). The ideal full-scale input voltage is 1.45V, centered at the VCM voltage of 0.535V as shown in Figure 26.

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 27 through 29.

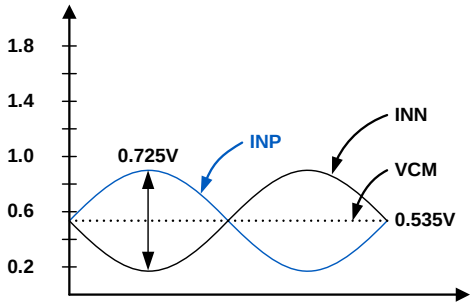



FIGURE 26. ANALOG INPUT RANGE

An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 27 and 28.

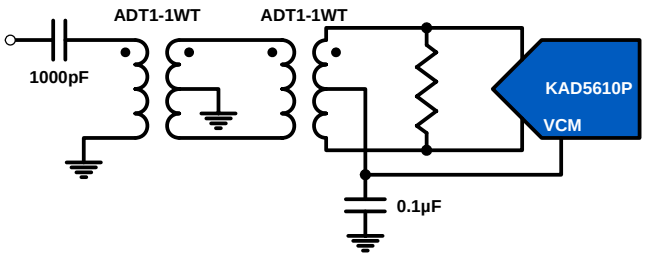



**FIGURE 27. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS**

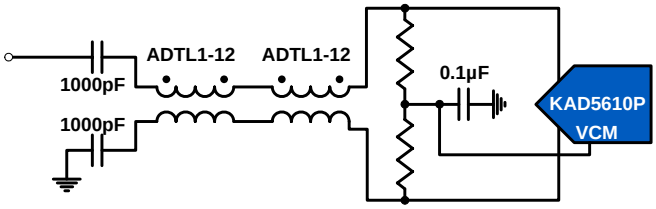



**FIGURE 28. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS**

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the KAD5610P is 1000Ω.

The SHA design uses a switched capacitor input stage (see Figure 41), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

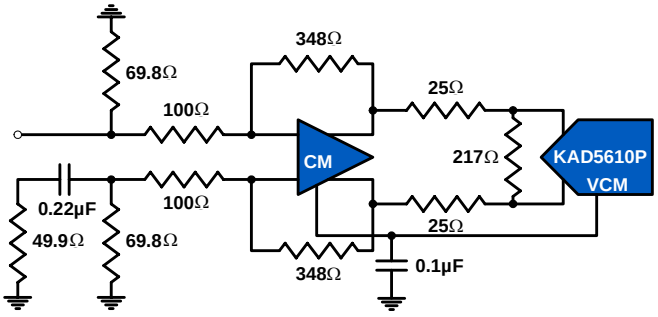



**FIGURE 29. DIFFERENTIAL AMPLIFIER INPUT**

A differential amplifier, as shown in Figure 29, can be used in applications that require DC-coupling. In this configuration the amplifier will typically dominate the achievable SNR and distortion performance.

## Clock Input

The clock input circuit is a differential pair (see Figure 42). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels.

The recommended drive circuit is shown in Figure 30. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

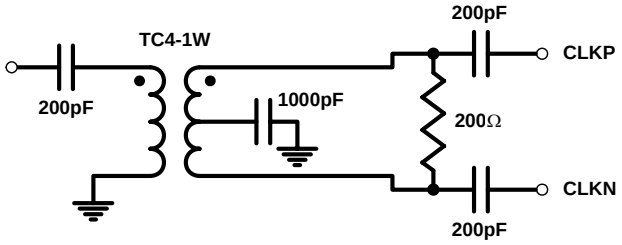



**FIGURE 30. RECOMMENDED CLOCK DRIVE**

A selectable 2x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs.

**TABLE 1. CLKDIV PIN SETTINGS**

| CLKDIV PIN | DIVIDE RATIO |
|---|---|
| AVSS | 2 |
| Float | 1 |
| AVDD | 4 |

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. Details on this are contained in “Serial Peripheral Interface” on page 19.

A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52ìs to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

## Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter ($t_J$) and SNR is shown in Equation 1 and is illustrated in Figure 31.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

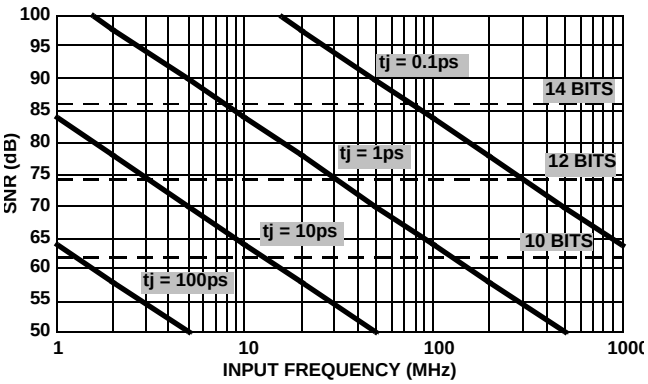



**FIGURE 31. SNR vs CLOCK JITTER**

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

### *Voltage Reference*

A temperature compensated voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

### *Digital Outputs*

Output data is available as a parallel bus in LVDS-compatible or CMOS modes. In either case, the data is presented in double data rate (DDR) format with the A and B channel data available on alternating clock edges. When CLKOUT is low channel A data is output, while on the high phase channel B data is presented. Figures 1 and 2 show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the ADC. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.

The output mode and LVDS drive current are selected via the OUTMODE pin as shown in Table 2.

**TABLE 2. OUTMODE PIN SETTINGS**

| OUTMODE PIN | MODE |
|---|---|
| AVSS | LVCMOS |
| Float | LVDS, 3mA |
| AVDD | LVDS, 2mA |

The output mode can also be controlled through the SPI port, which overrides the OUTMODE pin setting. Details on this are contained in “Serial Peripheral Interface” on page 19.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

### *Over-Range Indicator*

The over-range (OR) bit is asserted when the output code reaches positive full-scale (e.g. 0xFFF in offset binary mode). The output code does not wrap around during an over-range condition. The OR bit is updated at the sample rate.

### *Power Dissipation*

The power dissipated by the KAD5610P is primarily dependent on the sample rate and the output modes: LVDS vs. CMOS and DDR vs. SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

### *Nap/Sleep*

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation to less than 134mW and recovers to normal operation in approximately 1µs. Sleep mode reduces power dissipation to less than 14mW but requires 1ms to recover.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 250MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 3.

**TABLE 3. NAPSLP PIN SETTINGS**

| NAPSLP PIN | MODE |
|---|---|
| AVSS | Normal |
| Float | Sleep |
| AVDD | Nap |

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in “Serial Peripheral Interface” on page 19. This is an indexed function when controlled from the SPI, but a global function when driven from the pin.

### *Data Format*

Output data can be presented in three formats: two’s complement, Gray code and offset binary. The data format is selected via the OUTFMT pin as shown in Table 4.

**TABLE 4. OUTFMT PIN SETTINGS**

| OUTFMT PIN | MODE |
|---|---|
| AVSS | Offset Binary |
| Float | Two’s Complement |
| AVDD | Gray Code |

The data format can also be controlled through the SPI port, which overrides the OUTFMT pin setting. Details on this are contained in “Serial Peripheral Interface” on page 19.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two’s complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 32 shows this operation.

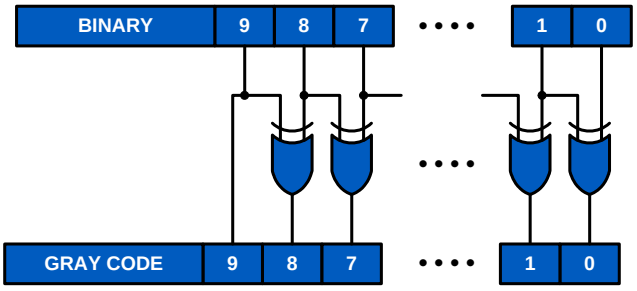



**FIGURE 32. BINARY TO GRAY CODE CONVERSION**

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 33.

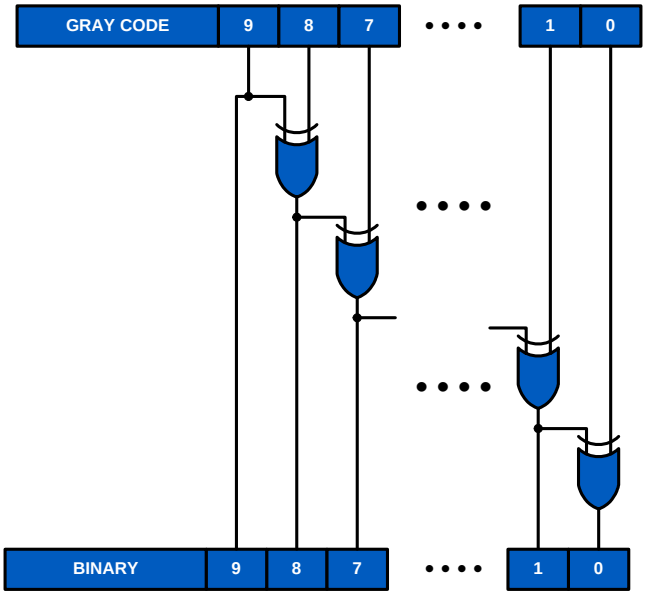



**FIGURE 33. GRAY CODE TO BINARY CONVERSION**

Mapping of the input voltage to the various data formats is shown in Table 5.

**TABLE 5. INPUT VOLTAGE TO OUTPUT CODE MAPPING**

| INPUT VOLTAGE | OFFSET BINARY | TWO’S COMPLEMENT | GRAY CODE |
|---|---|---|---|
| –Full Scale | 000 00 000 00 | 100 00 000 00 | 000 00 000 00 |
| –Full Scale + 1LSB | 000 00 000 01 | 100 00 000 01 | 000 00 000 01 |
| Mid–Scale | 100 00 000 00 | 000 00 000 00 | 110 00 000 00 |
| +Full Scale – 1LSB | 111 11 111 10 | 011 11 111 10 | 100 00 000 01 |
| +Full Scale | 111 11 111 11 | 011 11 111 11 | 100 00 000 00 |

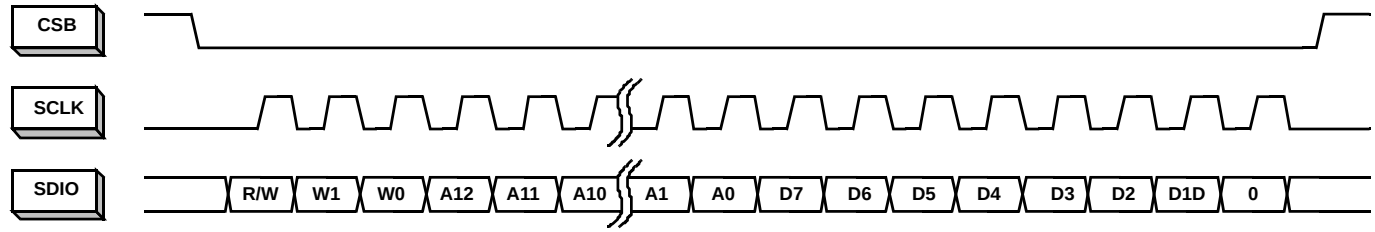



**FIGURE 34. MSB-FIRST ADDRESSING**

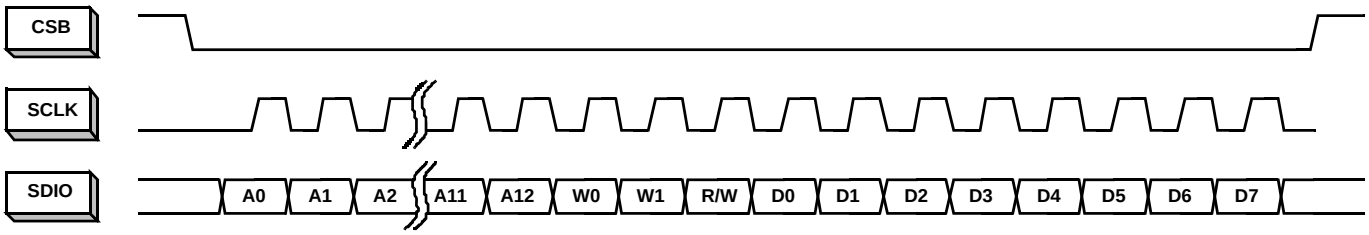



FIGURE 35. LSB-FIRST ADDRESSING

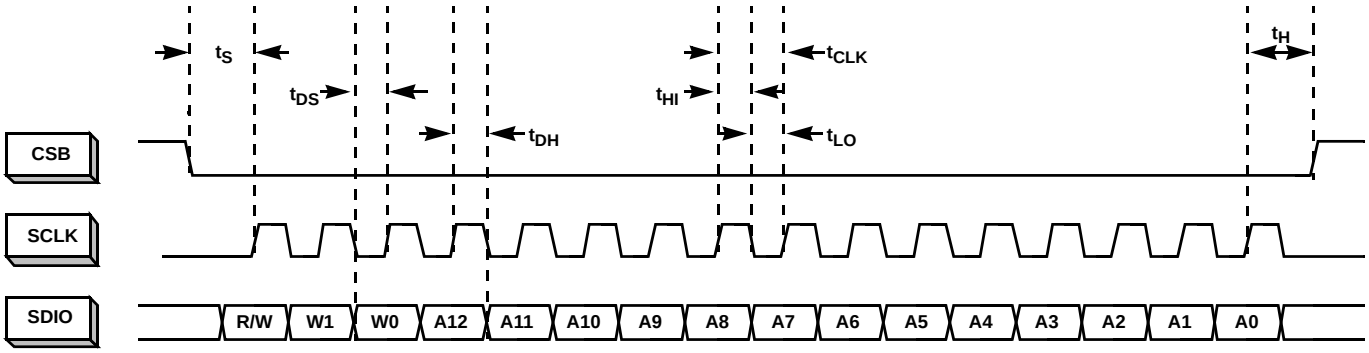



FIGURE 36. INSTRUCTION/ADDRESS PHASE

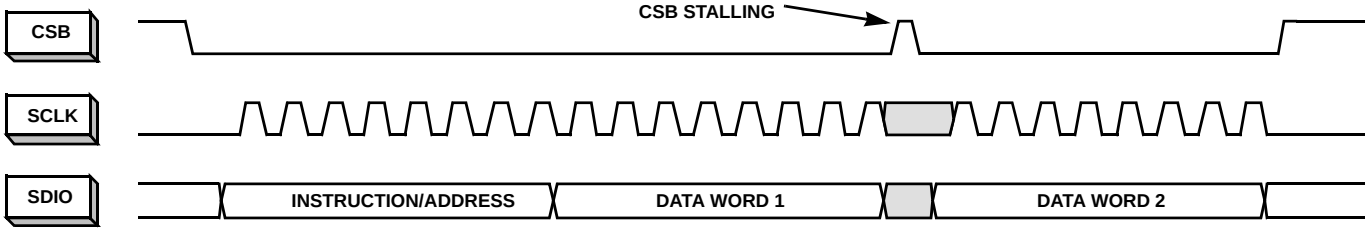



FIGURE 37. 2-BYTE TRANSFER

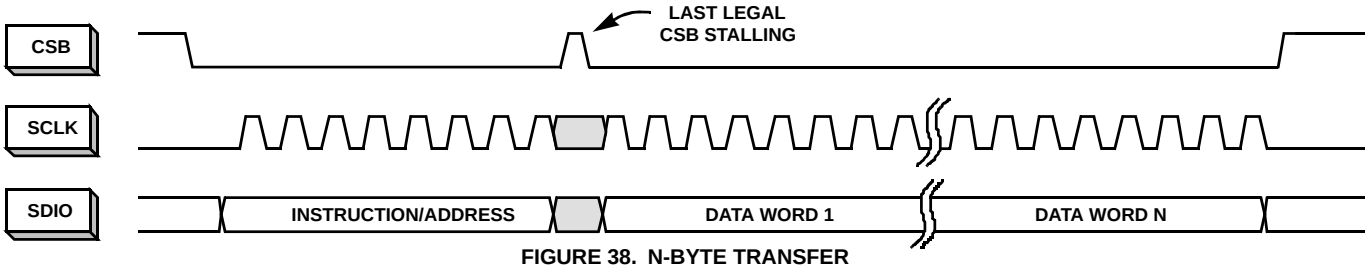



FIGURE 38. N-BYTE TRANSFER

## Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data input (SDI), and serial data input/output (SDIO). The maximum SCLK rate is equal to the ADC sample rate ($f_{SAMPLE}$) divided by 16 for write operations and $f_{SAMPLE}$ divided by 66 for reads. At $f_{SAMPLE}$ = 250MHz, maximum SCLK is 15.63MHz for writing and 3.79MHz for read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

### SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the KAD5610P functioning as a slave. Multiple slave devices can interface to a single master in four-wire mode only, since the SDIO output of an unaddressed device is asserted in three wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in four-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address command, SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 34 and 35 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 6). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 36, and timing values are given in "Switching Specifications" on page 7.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

**TABLE 6. BYTE TRANSFER SELECTION**

| [W1:W0] | BYTES TRANSFERRED |
|---|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 4 or more |

Figures 37 and 38 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

### SPI Configuration

**ADDRESS 0X00: CHIP_PORT_CONFIG**

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various microcontrollers.

**Bit 7** SDO Active

**Bit 6** LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

**Bit 5** Soft Reset

Setting this bit high resets all SPI registers to default values.

**Bit 4** Reserved

This bit should always be set high.

**Bits 3:0** These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

**ADDRESS 0X02: BURST_END**

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. In 3-wire SPI mode the burst is ended by pulling the CSB pin high. If the device is operated in 2-wire mode the CSB pin is not available. In that case, setting the

burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

**Bits 7:0** Burst End Address

This register value determines the ending address of the burst data.

### *Device Information*

**ADDRESS 0X08: CHIP_ID**

**ADDRESS 0X09: CHIP_VERSION**

The generic die identifier and a revision number, respectively, can be read from these two registers.

### *Indexed Device Configuration/Control*

**ADDRESS 0X10: DEVICE_INDEX_A**

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Intersil ADC products. Certain configuration commands (identified as Indexed in the SPI map) can be executed on a per-converter basis. This register determines which converter is being addressed for an Indexed command. It is important to note that only a single converter can be addressed at a time.

This register defaults to 00h, indicating that no ADC is addressed. Error code ‘AD’ is returned if any indexed register is read from without properly setting device_index_A.

**ADDRESS 0X20: OFFSET_COARSE**

**ADDRESS 0X21: OFFSET_FINE**

The input offset of each ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 7.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

**TABLE 7. OFFSET ADJUSTMENTS**

| PARAMETER | 0x20[7:0] COARSE OFFSET | 0x21[7:0] FINE OFFSET |
|---|---|---|
| Steps | 255 | 255 |
| –Full Scale (0x00) | -133LSB (-47mV) | -5LSB (-1.75mV) |
| Mid–Scale (0x80) | 0.0LSB (0.0mV) | 0.0LSB |
| +Full Scale (0xFF) | +133LSB (+47mV) | +5LSB (+1.75mV) |
| Nominal Step Size | 1.04LSB (0.37mV) | 0.04LSB (0.014mV) |

**ADDRESS 0X22: GAIN_COARSE**

**ADDRESS 0X23: GAIN_MEDIUM**

**ADDRESS 0X24: GAIN_FINE**

Gain of the ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of +/- 4.2%. ( ‘0011’ =~ -4.2% and ‘1100’ =~ +4.2% ) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 23h and 24h

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

**TABLE 8. COARSE GAIN ADJUSTMENT**

| 0x22[3:0] | NOMINAL COARSE GAIN ADJUST (%) |
|---|---|
| Bit3 | +2.8 |
| Bit2 | +1.4 |
| Bit1 | -2.8 |
| Bit0 | -1.4 |

**TABLE 9. MEDIUM AND FINE GAIN ADJUSTMENTS**

| PARAMETER | 0x23[7:0] MEDIUM GAIN | 0x24[7:0] FINE GAIN |
|---|---|---|
| Steps | 256 | 256 |
| –Full Scale (0x00) | -2% | -0.20% |
| Mid–Scale (0x80) | 0.00% | 0.00% |
| +Full Scale (0xFF) | +2% | +0.2% |
| Nominal Step Size | 0.016% | 0.0016% |

**ADDRESS 0X25: MODES**

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to “Nap/Sleep” on page 16). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

**TABLE 10. POWER-DOWN CONTROL**

| VALUE | 0x25[2:0] POWER-DOWN MODE |
|---|---|
| 000 | Pin Control |
| 001 | Normal Operation |
| 010 | Nap Mode |
| 100 | Sleep Mode |

## Global Device Configuration/Control

### ADDRESS 0X70: SKEW_DIFF

The value in the skew_diff register adjusts the timing skew between the two ADCs cores. The nominal range and resolution of this adjustment are given in Table 11. The default value of this register after power-up is 00h.

**TABLE 11. DIFFERENTIAL SKEW ADJUSTMENT**

| PARAMETER | 0X70[7:0] DIFFERENTIAL SKEW |
|---|---|
| Steps | 256 |
| –Full Scale (0x00) | -6.5ps |
| Mid–Scale (0x80) | 0.0ps |
| +Full Scale (0xFF) | +6.5ps |
| Nominal Step Size | 51fs |

### ADDRESS 0X71: PHASE_SLIP

When using the clock divider, it's not possible to determine the synchronization of the incoming and divided clock phases. This is particularly important when multiple ADCs are used in a time-interleaved system. The phase slip feature allows the rising edge of the divided clock to be advanced by one input clock cycle when in CLK/4 mode, as shown in Figure 39. Execution of a phase_slip command is accomplished by first writing a '0' to bit 0 at address 71h followed by writing a '1' to bit 0 at address 71h (32 sclk cycles).

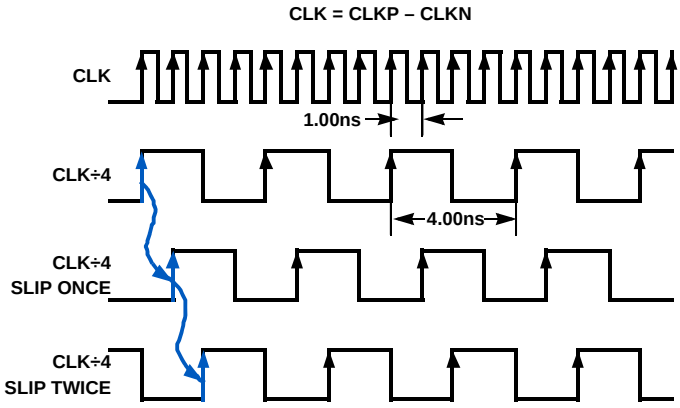



**FIGURE 39. PHASE SLIP: CLK÷4 MODE, $f_{CLOCK}$ = 1000MHz**

### ADDRESS 0X72: CLOCK_DIVIDE

The KAD5610P has a selectable clock divider that can be set to divide by four, two or one (no division). By default, the tri-level CLKDIV pin selects the divisor (refer to "Clock Input" on page 15). This functionality can be overridden and controlled through the SPI, as shown in Table 12. This register is not changed by a Soft Reset.

**TABLE 12. CLOCK DIVIDER SELECTION**

| VALUE | 0x72[2:0] CLOCK DIVIDER |
|---|---|
| 000 | Pin Control |
| 001 | Divide by 1 |
| 010 | Divide by 2 |
| 100 | Divide by 4 |

### ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The KAD5610P can present output data in two physical formats: LVDS or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (3mA) or low (2mA). By default, the tri-level OUTMODE pin selects the mode and drive level (refer to "Digital Outputs" on page 16). This functionality can be overridden and controlled through the SPI, as shown in Table 13.

Data can be coded in three possible formats: two's complement, Gray code or offset binary. By default, the tri-level OUTFMT pin selects the data format (refer to "Data Format" on page 17). This functionality can be overridden and controlled through the SPI, as shown in Table 14.

This register is not changed by a Soft Reset.

**TABLE 13. OUTPUT MODE CONTROL**

| VALUE | 0x93[7:5] OUTPUT MODE |
|---|---|
| 000 | Pin Control |
| 001 | LVDS 2mA |
| 010 | LVDS 3mA |
| 100 | LVCMOS |

**TABLE 14. OUTPUT FORMAT CONTROL**

| VALUE | 0x93[2:0] OUTPUT FORMAT |
|---|---|
| 000 | Pin Control |
| 001 | Two's Complement |
| 010 | Gray Code |
| 100 | Offset Binary |

### ADDRESS 0X74: OUTPUT_MODE_B

### ADDRESS 0X75: CONFIG_STATUS

**Bit 6** DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. Table 15 shows the allowable sample rate ranges for the slow and fast settings.

TABLE 15. DLL RANGES

| DLL RANGE | MIN | MAX | UNIT |
|---|---|---|---|
| Slow | 40 | 100 | MSPS |
| Fast | 80 | $f_S$ MAX | MSPS |

The output_mode_B and config_status registers are used in conjunction to select the frequency range of the DLL clock generator. The method of setting these options is different from the other registers.

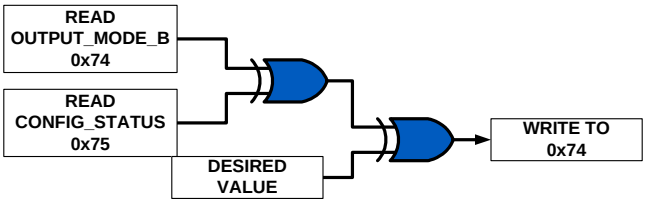



FIGURE 40. SETTING OUTPUT_MODE_B REGISTER

The procedure for setting output_mode_B is shown in Figure 40. Read the contents of output_mode_B and config_status and XOR them. Then XOR this result with the desired value for output_mode_B and write that XOR result to the register.

### *Device Test*

The KAD5610 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A static word can be placed on the output bus, or two different words can alternate. In the alternate mode, the values defined as Word 1 and Word 2 (as shown in Table 16) are set on the output bus on alternating clock phases. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

**ADDRESS 0XC0: TEST_IO**

**Bits 7:6** User Test Mode

These bits set the test mode to static (0x00) or alternate (0x01) mode. Other values are reserved.

The four LSBs in this register (Output Test Mode) determine the test pattern in combination with registers 0xC2 through 0xC5. Refer to Table 17.

TABLE 16. OUTPUT TEST MODES

| VALUE | 0xC0[3:0] OUTPUT TEST MODE | WORD 1 | WORD 2 |
|---|---|---|---|
| 0000 | Off | | |
| 0001 | Midscale | 0x8000 | N/A |
| 0010 | Positive Full-Scale | 0xFFFF | N/A |
| 0011 | Negative Full-Scale | 0x0000 | N/A |
| 0100 | Checkerboard | 0xAAAA | 0x5555 |
| 0101 | Reserved | N/A | N/A |
| 0110 | Reserved | N/A | N/A |
| 0111 | One/Zero | 0xFFFF | 0x0000 |
| 1000 | User Pattern | user_patt1 | user_patt2 |

**ADDRESS 0XC2: USER_PATT1_LSB**

**ADDRESS 0XC3: USER_PATT1_MSB**

These registers define the lower and upper eight bits, respectively, of the first user-defined test word.

**ADDRESS 0XC4: USER_PATT2_LSB**

**ADDRESS 0XC5: USER_PATT2_MSB**

These registers define the lower and upper eight bits, respectively, of the second user-defined test word.

## SPI Memory Map

**TABLE 17. SPI MEMORY MAP**

| | Addr (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value (Hex) | Indexed/ Global |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SPI Config | 00 | port_config | SDO Active | LSB First | Soft Reset | | | Mirror (bit5) | Mirror (bit6) | Mirror (bit7) | 00h | G |
| | 01 | Reserved | Reserved | | | | | | | | | |
| | 02 | burst_end | Burst end address [7:0] | | | | | | | | 00h | G |
| | 03-07 | Reserved | Reserved | | | | | | | | | |
| Info | 08 | chip_id | Chip ID # | | | | | | | | Read only | G |
| | 09 | chip_version | Chip Version # | | | | | | | | Read only | G |
| Indexed Device Config/Control | 10 | device_index_A | Reserved | | | | | | ADC01 | ADC00 | 00h | I |
| | 11-1F | Reserved | Reserved | | | | | | | | | |
| | 20 | offset_coarse | Coarse Offset | | | | | | | | cal. value | I |
| | 21 | offset_fine | Fine Offset | | | | | | | | cal. value | I |
| | 22 | gain_coarse | Reserved | | | | Coarse Gain | | | | cal. value | I |
| | 23 | gain_medium | Medium Gain | | | | | | | | cal. value | I |
| | 24 | gain_fine | Fine Gain | | | | | | | | cal. value | I |
| | 25 | modes | | | | | | **Power-Down Mode [2:0]**<br>000 = Pin Control<br>001 = Normal Operation<br>010 = Nap<br>100 = Sleep<br>other codes = Reserved | | | 00h<br>NOT affected by Soft Reset | I |
| | 26-5F | Reserved | Reserved | | | | | | | | | |
| | 60-6F | Reserved | Reserved | | | | | | | | | |
| Global DeviceConfig/Control | 70 | skew_diff | Differential Skew | | | | | | | | 80h | |
| | 71 | phase_slip | Reserved | | | | | | | Next Clock Edge | 00h | G |
| | 72 | clock_divide | | | | | | **Clock Divide [2:0]**<br>000=Pin Control<br>001=divide by 1<br>010=divide by 2<br>100=divide by 4<br>other codes=Reserved | | | 00h<br>NOT affected by Soft Reset | G |
| | 73 | output_mode_A | **Output Mode [2:0]**<br>000 = Pin Control<br>001 = LVDS 2mA<br>010 = LVDS 3mA<br>100 = LVCMOS<br>other codes = Reserved | | | | | **Output Format [2:0]**<br>000 = Pin Control<br>001 = Twos Complement<br>010 = Gray Code<br>100 = Offset Binary<br>other codes = Reserved | | | 00h<br>NOT affected by Soft Reset | G |
| | 74 | output_mode_B | | **DLL Range**<br>0 = fast<br>1 = slow | | | | | | | 00h<br>NOT affected by Soft Reset | G |
| | 75 | config_status | | XOR Result | | | | | | | Read Only | G |
| | 76-BF | Reserved | Reserved | | | | | | | | | |

TABLE 17. SPI MEMORY MAP

| | Addr (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value (Hex) | Indexed/ Global |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device Test | C0 | test_io | User Test Mode [1:0]<br>00 = Single<br>01 = Alternate<br>10 = Reserved<br>11 = Reserved | | | | Output Test Mode [3:0]<br>0 = Off<br>1 = Midscale Short<br>2 = +FS Short<br>3 = -FS Short<br>4 = Checker Board<br>5 = Reserved<br>6 = Reserved | | 7 = One/Zero Word Toggle<br>8 = User Input<br>9-15 = Reserved | | 00h | G |
| | C1 | Reserved | Reserved | | | | | | | | 00h | G |
| | C2 | user_patt 1_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | G |
| | C3 | user_patt1_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | G |
| | C4 | user_patt 2_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | G |
| | C5 | user_patt2_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | G |
| | C6-FF | Reserved | Reserved | | | | | | | | | |

## Equivalent Circuits

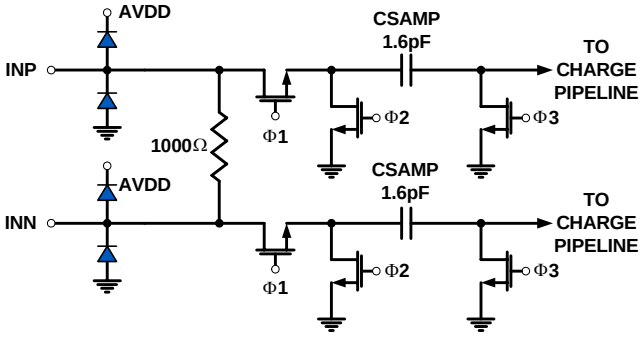



FIGURE 41. ANALOG INPUTS

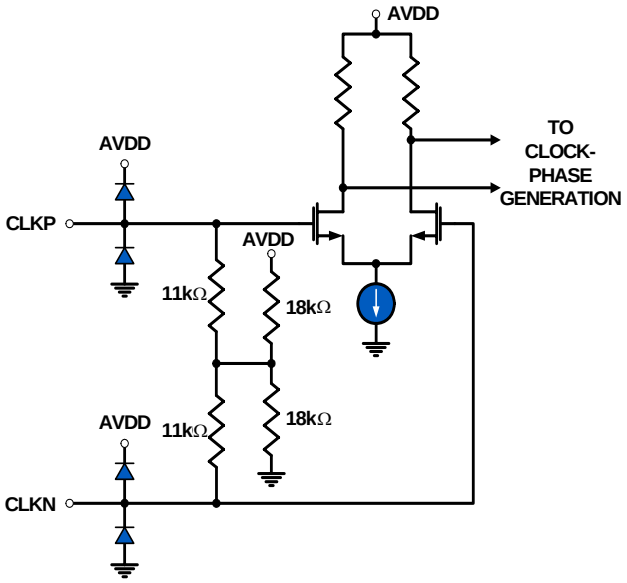



FIGURE 42. CLOCK INPUTS

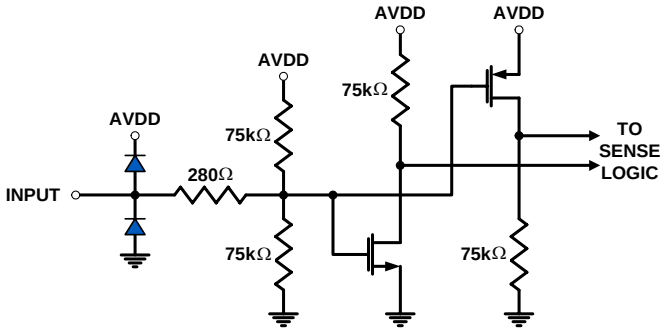



FIGURE 43. TRI-LEVEL DIGITAL INPUTS

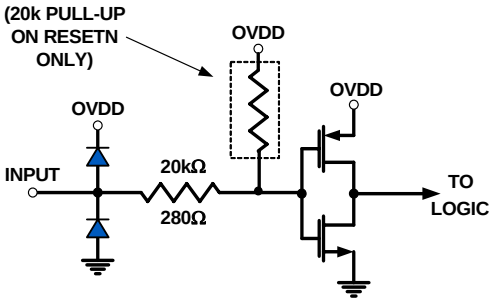



FIGURE 44. DIGITAL INPUTS

## Equivalent Circuits (Continued)

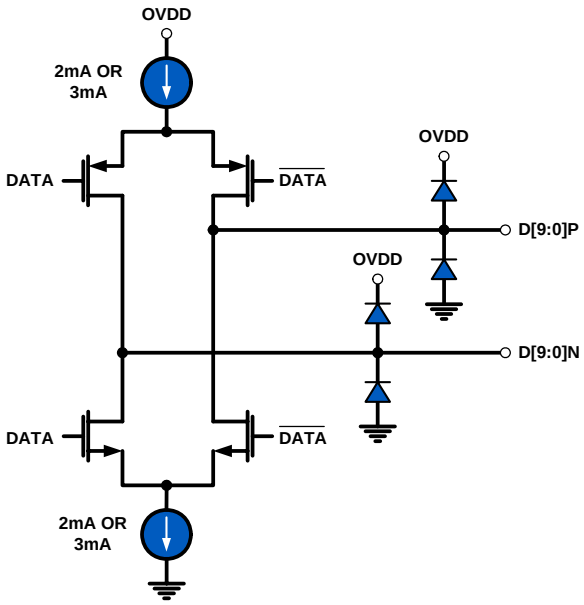



FIGURE 45. LVDS OUTPUTS

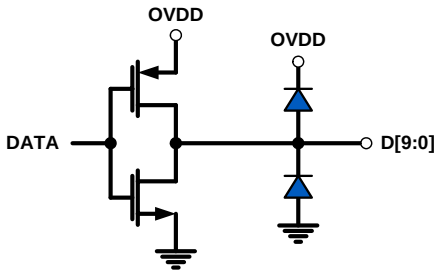



FIGURE 46. CMOS OUTPUTS

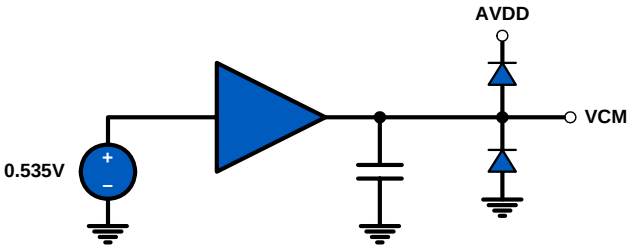



FIGURE 47. VCM_OUT OUTPUT

## Layout Considerations

### Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

### Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

### Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

### Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

### LVDS Outputs

Output traces and connections must be designed for 50Ω (100? differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power-plane breaks with signal traces.

### LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

### Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal ADC performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP, OUTMODE, OUTFMT, CLKDIV) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

## Definitions

**Analog Input Bandwidth** is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

**Aperture Delay or Sampling Delay** is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

**Aperture Jitter** is the RMS variation in aperture delay for a set of samples.

**Clock Duty Cycle** is the ratio of the time the clock wave is at logic high to the total time of one clock period.

**Differential Non-Linearity (DNL)** is the deviation of any code width from an ideal 1 LSB step.

**Effective Number of Bits (ENOB)** is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

**Gain Error** is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage less 2 LSB. It is typically expressed in percent.

**Integral Non-Linearity (INL)** is the maximum deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Least Significant Bit (LSB)** is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

**Missing Codes** are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

**Most Significant Bit (MSB)** is the bit that has the largest value or weight.

**Pipeline Delay** is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

**Power Supply Rejection Ratio (PSRR)** is the ratio of the observed magnitude of a spur in the ADC FFT, caused by an AC signal superimposed on the power supply voltage.

**Signal to Noise-and-Distortion (SINAD)** is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

**Signal-to-Noise Ratio** (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

NR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the converter's full-scale input power is used as the reference.

**Spurious-Free-Dynamic Range (SFDR)** is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

**Two-Tone SFDR** is the ratio of the RMS value of the lowest power input tone to the RMS value of the peak spurious component, which may or may not be an IMD product.

## Revision History

| DATE | REVISION | CHANGE |
|---|---|---|
| 8/6/08 | Rev 1 | Initial Release of Production Datasheet |
| 12/5/08 | FN6810.0 | Converted to intersil template. Assigned file number FN6810. Rev 0 - first release with new file number. Applied Intersil Standards. |
| 1/15/09 | FN6810.1 | P1; revised Key Specs<br>P1; changed RESET to RESETN in block diagram<br>P2; added Part Marking column to Order Info<br>P4; Moved Thermal Impedance under Thermal Info (used to be on p. 7). Added Theta JA Note 2.<br>P4-7; edits throughout the Specs table. Added Notes 8 and 9. Revised Notes 6 and 7.<br>P7; Removed ESD section<br>P10-12; revised Performance Curves throughout<br>P14; User Inititated Reset section; revised 2nd sentence of 1st paragraph<br>P19; Serial Peripheral Interface; revised 2nd to last sentence of 1st paragraph. SPI Physical Interface; revised 2nd and 3rd sentences of 4th paragraph<br>P20; added last 2 sentences to 1st paragraph of "ADDRESS 0X24: GAIN_FINE". Revised Table 8<br>P21; revised last 2 sentences of "ADDRESS 0X71: PHASE_SLIP". Removed Figure of "PHASE SLIP: CLK÷2 MODE, fCLOCK = 500MHz"<br>P24; revised Figure 44<br>P24; Table 17; revised Bits7:4, Addr C0<br>Throughout; formatted graphics to Intersil standards |

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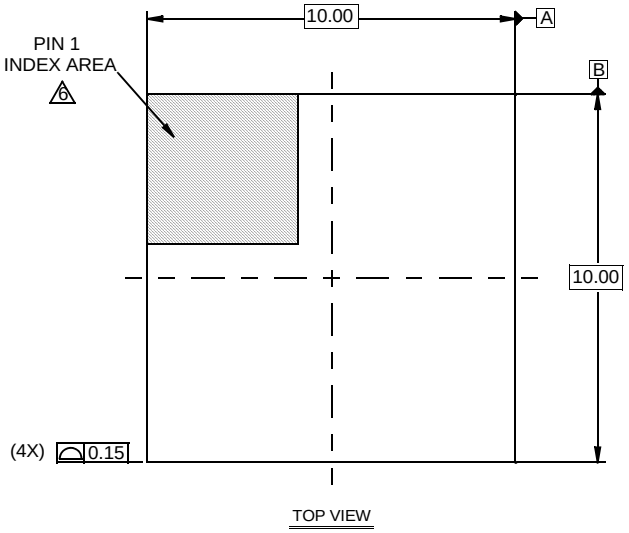
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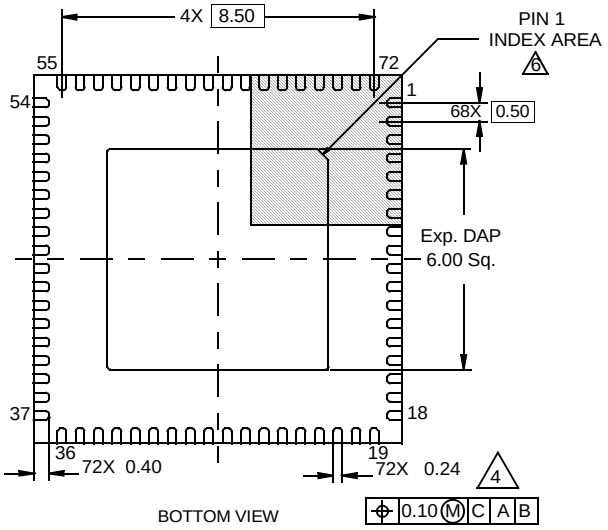
# Package Outline Drawing

## L72.10x10D

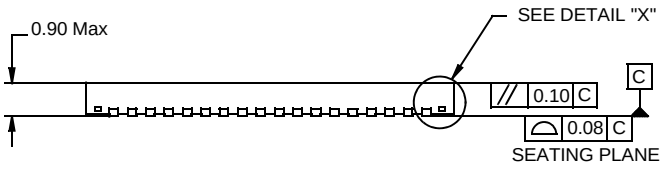
**72 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 1, 11/08**



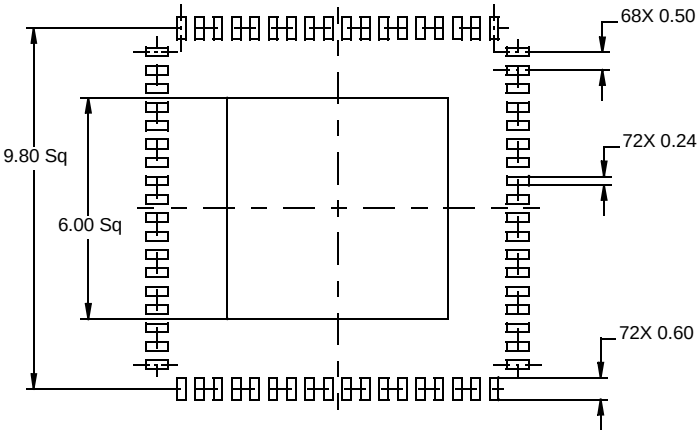

TOP VIEW



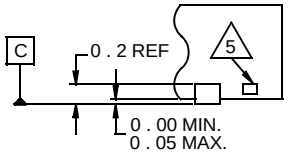

BOTTOM VIEW




SIDE VIEW




TYPICAL RECOMMENDED LAND PATTERN




DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.