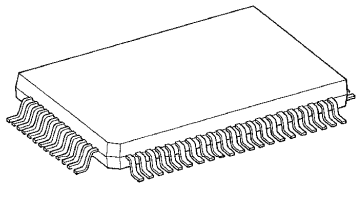
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# T6M19, JT6M19-AS

## T6M19, JT6M19-AS CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T6M19, JT6M19-AS is a 1 chip microcomputer for 10-digits + 2- digits electronic scientific calculation.
T6M19, JT6M19-AS is the complete single chip CMOS LSI for electronic calculator with 10 digit, 67 function, 3 expression and hexadecimal, octal and binary, statistic calculation, fractional number calculation, and logic operation with the following features.



QFP67-P-1420-0.80

Weight : 1.20g (Typ.)

### FEATURES

- Display 12 display digits plus 2 digits code at the right margin.
  - Scientific and engineering display.

    Mantissa 10 digits plus exponent 2 digits plus negative code 2 digits.
  - Other than above

    Mantissa 10 digits plus negative code 1 digit.
- 13 kinds of special display

| | | | |
|---|---|---|---|
| M | Memory | HEX | Hexadecimal mode |
| – | Mantissa and exponent Minus | SD | Statistic calculation mode |
| E | Error | DEG | Degree |
| INV | Inverse | RAD | Radian |
| HYP | Hyperbolic | GRAD | Gradian |
| BIN | Binary mode | ( ) | Parenthesis calculation |
| OCT | Octal mode | | |

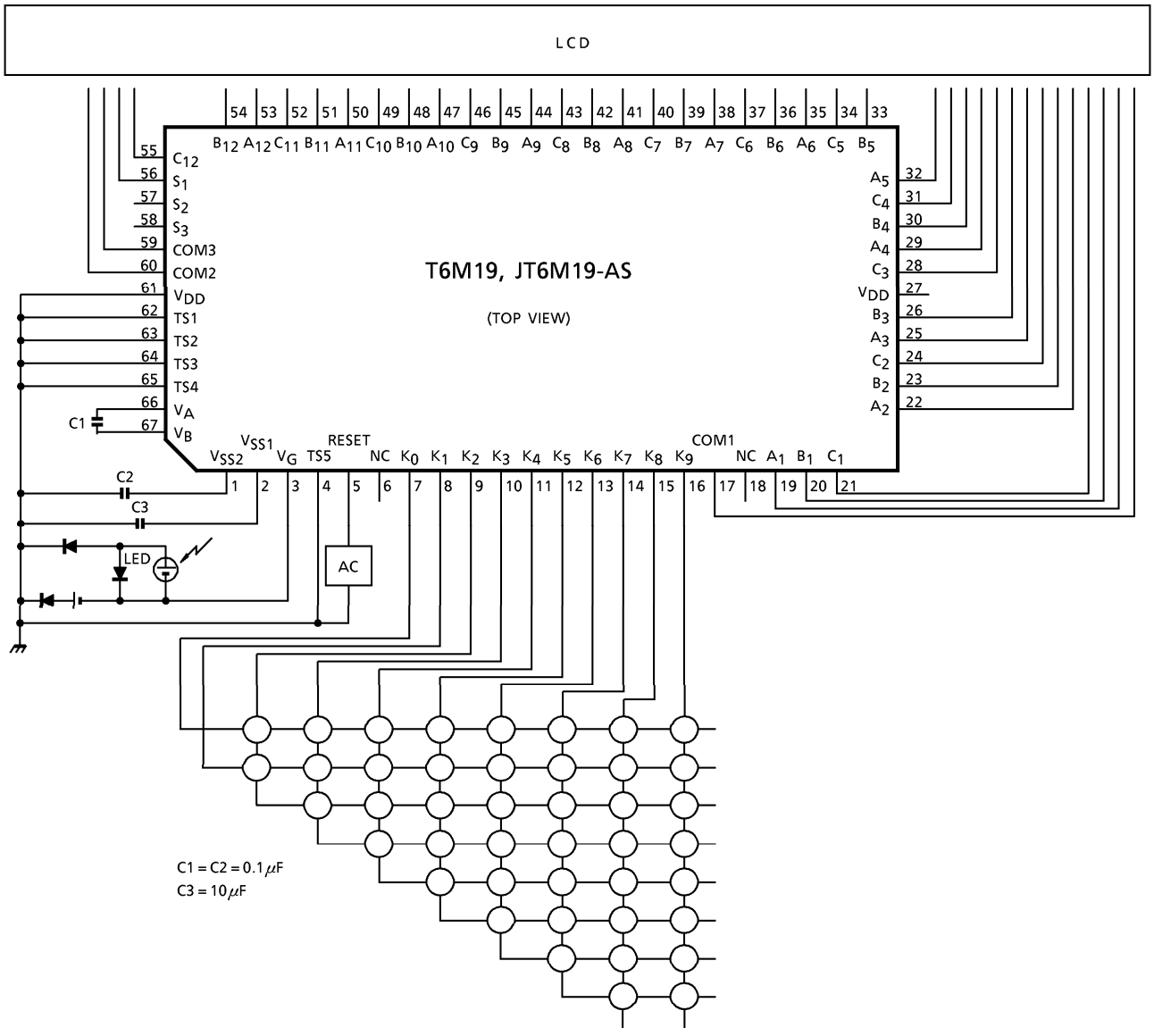
- The minus sign of the mantissa is floating minus.
- The arithmetic key operation in clouding $Y^x$ or $\sqrt[x]{Y}$ has same sequence as mathematical equation. 6 pending operations are allowed and ( ) are up to continuous 15 levels.
- Fractional number calculation.
- It is possible to convert mutually between decimal, binary, octal and hexadecimal, and the 4 operations in arithmetic in binary, octal and hexadecimal.
- One independent accumulating memory.
- It is possible to convert or fix the display number system by FLO (Floating) , SCI (Scientific) or ENG (Engineering) key.

980910EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

- It is possible to specify decimal part digits (0~9) by FIX key.
- Direct drive for FEM LCD (1 / 2 prebias, 1 / 3 duty) .
- Automatic power on clear.
- Low power consumption. $V_G$ = – 1.5V single power supply.
- The 67 pin flat package is used.
- Automatic power off (A time for about 10 min.) .

**SYSTEM BLOCK DIAGRAM**



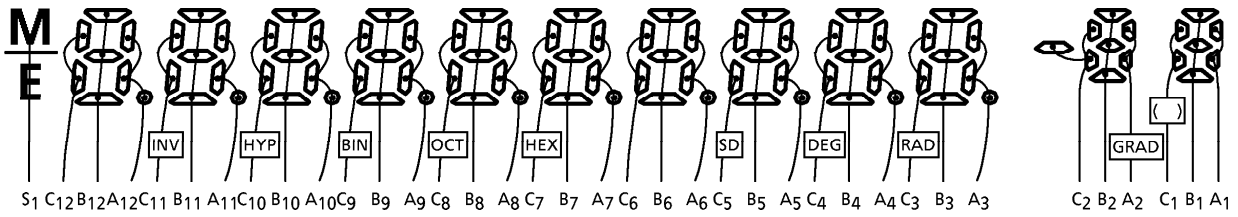

NOTE : Key resistance ≦ 5.0kΩ at $V_G$ = – 1.2V

980910EBA2'

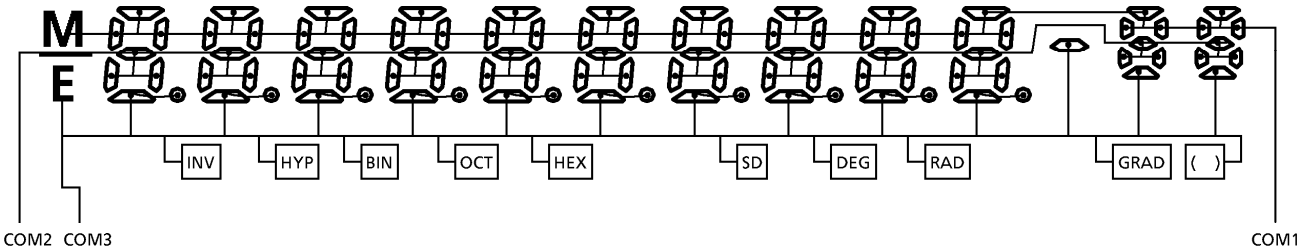

- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

## CONNECTION OF LCD

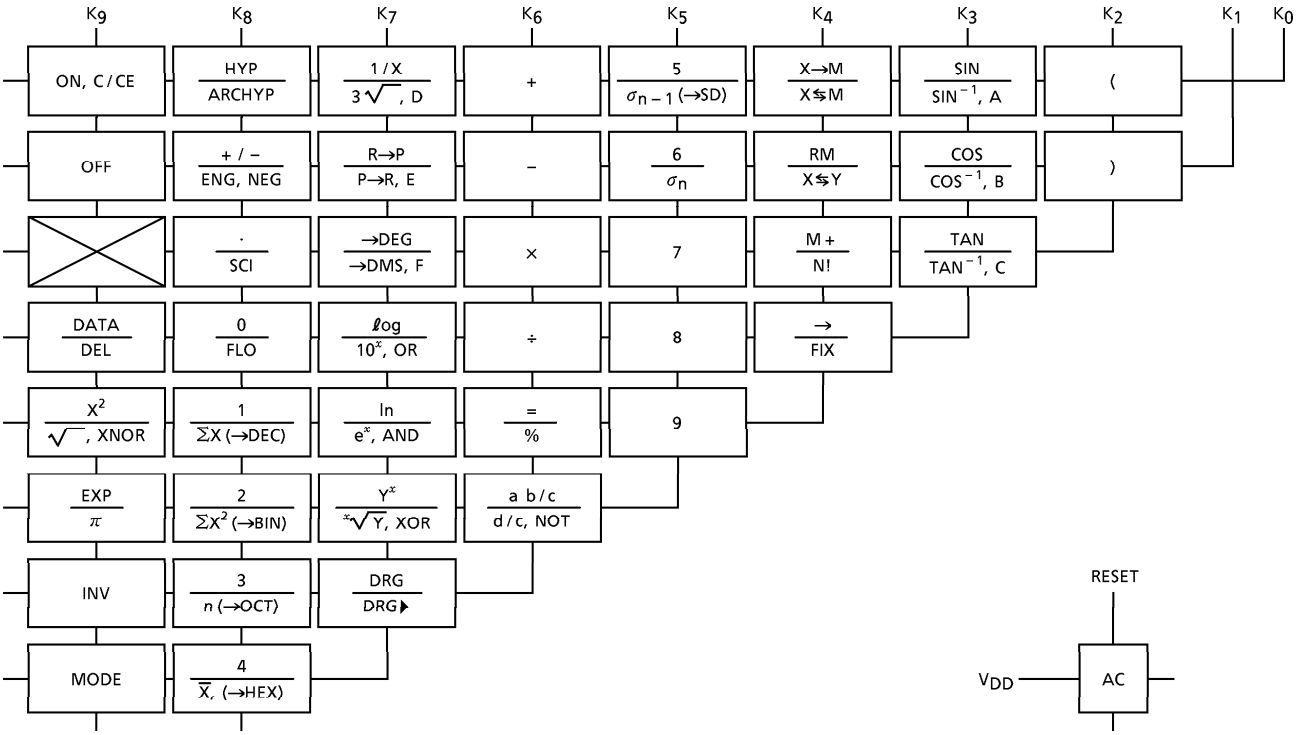
### SEGMENT



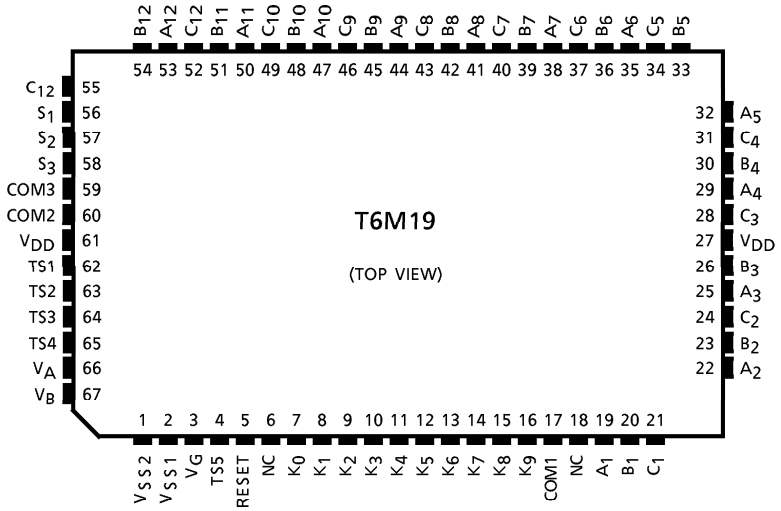

### COMMON




## KEY LAYOUT



**PIN LAYOUT**




**MAXIMUM RATINGS** (Ta = 25°C)

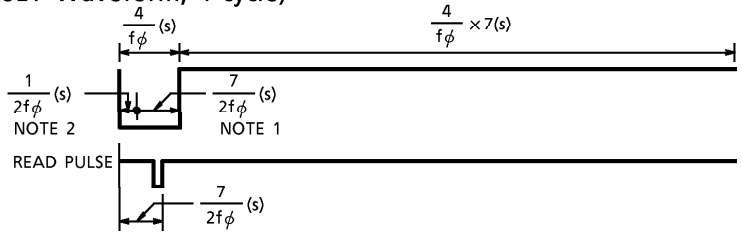
| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_G$ | +0.3~−2.2 | V |
| Input Voltage | $V_{IN}$ | +0.3~$V_G$−0.3 | V |
| Operating Temperature | $T_{opr}$ | 0~40 | °C |
| Storage Temperature | $T_{stg}$ | −55~125 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_G$ = −1.5V ± 0.2V, $V_{SS2}$ = −3.0 ± 0.4V, $V_{DD}$ = 0V, Ta = 25°C)

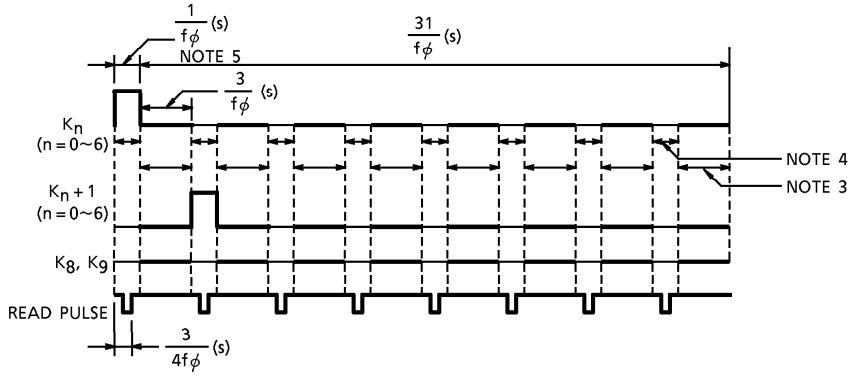
| PARAMETER | SYMBOL | TEST CIR-CUIT | PIN NAME | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_G$ | — | — | — | −1.2 | −1.5 | −2.0 | V |
| Supply Current (I) | $I_{DD}$ WAIT | — | — | $V_G$ = −1.5V, wait | — | 2.0 | 3.0 | μA |
| Supply Current (II) | $I_{DD}$ OP | — | — | $V_G$ = −1.2V, operate | — | 4.5 | 7.0 | μA |
| Supply Current (III) | $I_{DD}$ OFF | — | — | $V_G$ = −1.5V, off | — | — | 2.0 | μA |
| Oscillating Frequency (I) | fϕ WAIT | — | — | $V_G$ = −1.5V, wait | 5.4 | 9.0 | 12.6 | kHz |
| Oscillating Frequency (II) | fϕ OP | — | — | $V_G$ = −1.5V, operate | 14.4 | 24.0 | 33.6 | kHz |
| Frame Frequency | $f_F$ | — | — | $V_G$ = −1.5V, wait | 56.3 | 93.8 | 131.3 | Hz |
| "1" Input Voltage | $V_{IH}$ | — | $K_2$~$K_9$ RESET | — | $V_G$ +0.4 | — | $V_G$ | V |
| "0" Input Voltage | $V_{IL}$ | — | $K_2$~$K_9$ RESET | — | $V_{SS}$ | — | −0.4 | V |
| "1" Output Voltage | $V_{OH}$ (I) | — | SEGMENT COM1~3 | — | $V_{SS2}$ +0.2 | — | $V_{SS2}$ | V |

| PARAMETER | SYMBOL | TEST CIR-CUIT | PIN NAME | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| "0" Output Voltage | $V_{OL}$ (I) | — | SEGMENT COM1~3 | — | $V_{DD}$ | — | −0.2 | V |
| "M" Output Voltage | $V_{OH}$ | — | COM1~3 | — | $V_{SS1}$ +0.2 | — | $V_{SS1}$ −0.2 | V |
| "1" Output Voltage | $V_{OH}$ (II) | — | $K_0$~$K_9$ RESET | — | $V_{SS1}$ +0.2 | — | $V_{SS1}$ | V |
| "0" Output Voltage | $V_{OL}$ (II) | — | $K_0$~$K_9$ RESET | — | $V_{DD}$ | — | −0.2 | V |
| "1" Output Resistance | $R_{OH}$ | — | SEGMENT COM1~3 | $V_{OUT} = V_{SS2} + 0.5V$ | — | — | 70 | kΩ |
| "0" Output Resistance | $R_{OL}$ | — | SEGMENT COM1~3 | $V_{OUT} = -0.5V$ | — | — | 70 | kΩ |
| RESET Pull Up Resistance (I) | $R_{RESETH}$ (I) | — | RESET | $V_{OUT} = 0V$ (NOTE 1) | 156 | 260 | 364 | kΩ |
| RESET Pull Up Resistance (II) | $R_{RESETH}$ (II) | — | RESET | $V_{OUT} = 0V$ (NOTE 2) | 18 | 75 | 300 | kΩ |
| Key Pull Up Resistance (I) | $R_{KEYH}$ (I) | — | $K_0$~$K_9$ | $V_{OUT} = V_G + 0.5V$ (NOTE 3) | — | — | 500 | kΩ |
| Key Pull Up Resistance (II) | $R_{KEYH}$ | — | $K_0$~$K_9$ | $V_{OUT} = 0V$ (NOTE 4) | 60 | 300 | 1500 | kΩ |
| Key RESET Pull Down Resistance | $R_{KEYL}$ RESETL | — | $K_0$~$K_9$ RESET | $V_{OUT} = -0.5V$ (NOTE 5) | — | — | 25 | kΩ |

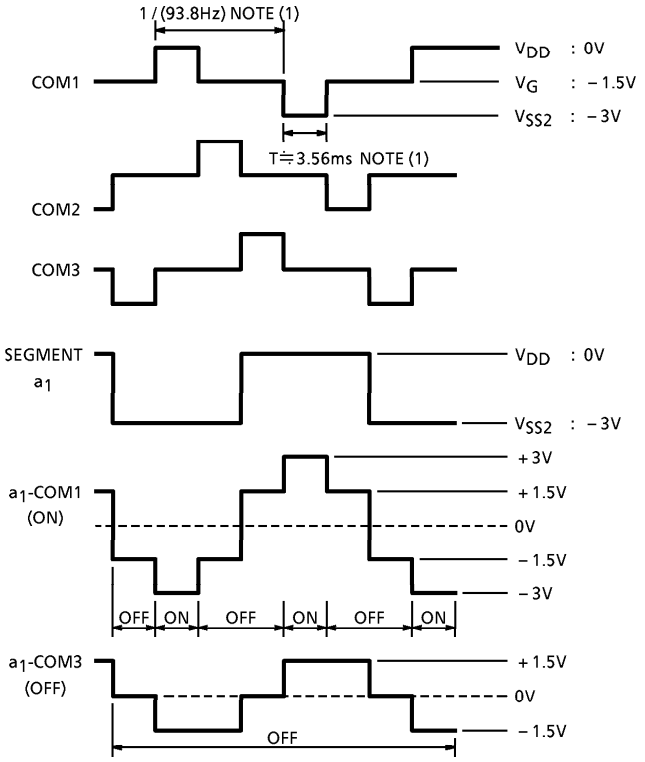
NOTE 1, 2, 5 (RESET Waveform, 1-cycle)




NOTE 3, 4, 5 (KEY Waveform, 1-cycle)



**WAVEFORMS FOR DISPLAY**



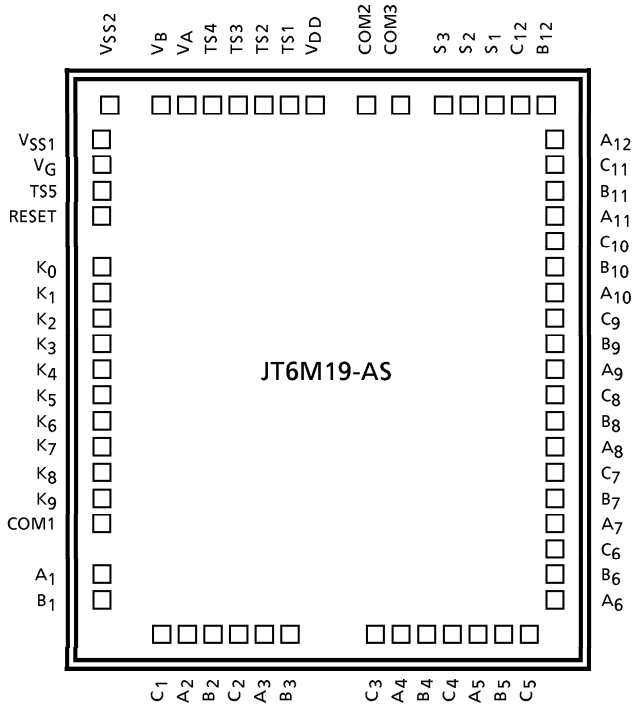

NOTE (1) $f_\phi$ WAIT = 9kHz

**PAD LOCATION TABLE** (μm)

| NAME | X POINT | Y POINT |
|---|---|---|
| $V_{SS2}$ | – 1783 | 2330 |
| $V_{SS1}$ | – 1894 | 2102 |
| $V_G$ | – 1894 | 1901 |
| TS5 | – 1894 | 1690 |
| RESET | – 1894 | 1469 |
| $K_0$ | – 1894 | 1070 |
| $K_1$ | – 1894 | 789 |
| $K_2$ | – 1894 | 547 |
| $K_3$ | – 1894 | 265 |
| $K_4$ | – 1894 | 23 |
| $K_5$ | – 1894 | – 259 |
| $K_6$ | – 1894 | – 501 |
| $K_7$ | – 1894 | – 782 |
| $K_8$ | – 1894 | – 1024 |
| $K_9$ | – 1894 | – 1306 |
| COM1 | – 1894 | – 1602 |
| $A_1$ | – 1894 | – 2023 |
| $B_1$ | – 1894 | – 2258 |
| $C_1$ | – 1513 | – 2330 |
| $A_2$ | – 1277 | – 2330 |
| $B_2$ | – 1042 | – 2330 |
| $C_2$ | – 806 | – 2330 |
| $A_3$ | – 571 | – 2330 |
| $B_3$ | – 336 | – 2330 |
| $C_3$ | 118 | – 2330 |
| $A_4$ | 353 | – 2330 |
| $B_4$ | 589 | – 2330 |
| $C_4$ | 824 | – 2330 |
| $A_5$ | 1059 | – 2330 |
| $B_5$ | 1295 | – 2330 |
| $C_5$ | 1530 | – 2330 |
| $A_6$ | 1894 | – 2234 |

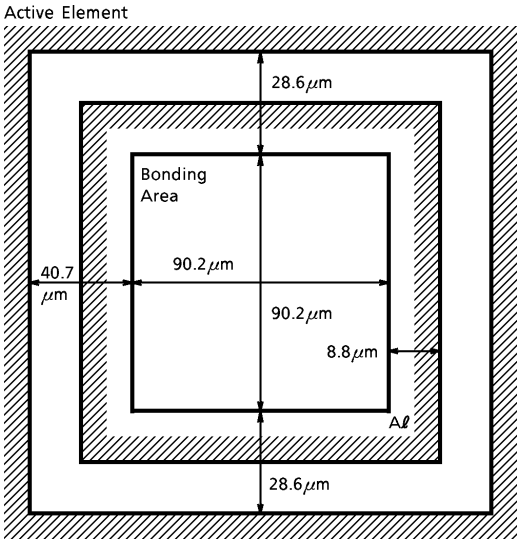
| NAME | X POINT | Y POINT |
|---|---|---|
| $B_6$ | 1894 | – 1937 |
| $C_6$ | 1894 | – 1709 |
| $A_7$ | 1894 | – 1482 |
| $B_7$ | 1894 | – 1254 |
| $C_7$ | 1894 | – 1026 |
| $A_8$ | 1894 | – 799 |
| $B_8$ | 1894 | – 571 |
| $C_8$ | 1894 | – 343 |
| $A_9$ | 1894 | – 116 |
| $B_9$ | 1894 | 112 |
| $C_9$ | 1894 | 332 |
| $A_{10}$ | 1894 | 557 |
| $B_{10}$ | 1894 | 784 |
| $C_{10}$ | 1894 | 1012 |
| $A_{11}$ | 1894 | 1240 |
| $B_{11}$ | 1894 | 1467 |
| $C_{11}$ | 1894 | 1695 |
| $A_{12}$ | 1894 | 1920 |
| $B_{12}$ | 1839 | 2330 |
| $C_{12}$ | 1606 | 2330 |
| $S_1$ | 1373 | 2330 |
| $S_2$ | 1140 | 2330 |
| $S_3$ | 902 | 2330 |
| COM3 | 565 | 2330 |
| COM2 | 295 | 2330 |
| $V_{DD}$ | – 51 | 2330 |
| TS1 | – 263 | 2330 |
| TS2 | – 484 | 2330 |
| TS3 | – 681 | 2330 |
| TS4 | – 888 | 2330 |
| $V_A$ | – 1124 | 2330 |
| $V_B$ | – 1371 | 2330 |

## CHIP LAYOUT




Chip size : 4.04 × 4.98 (mm)
Chip thickness : 450 ± 20 $\mu$m
Substrate : $V_{DD}$

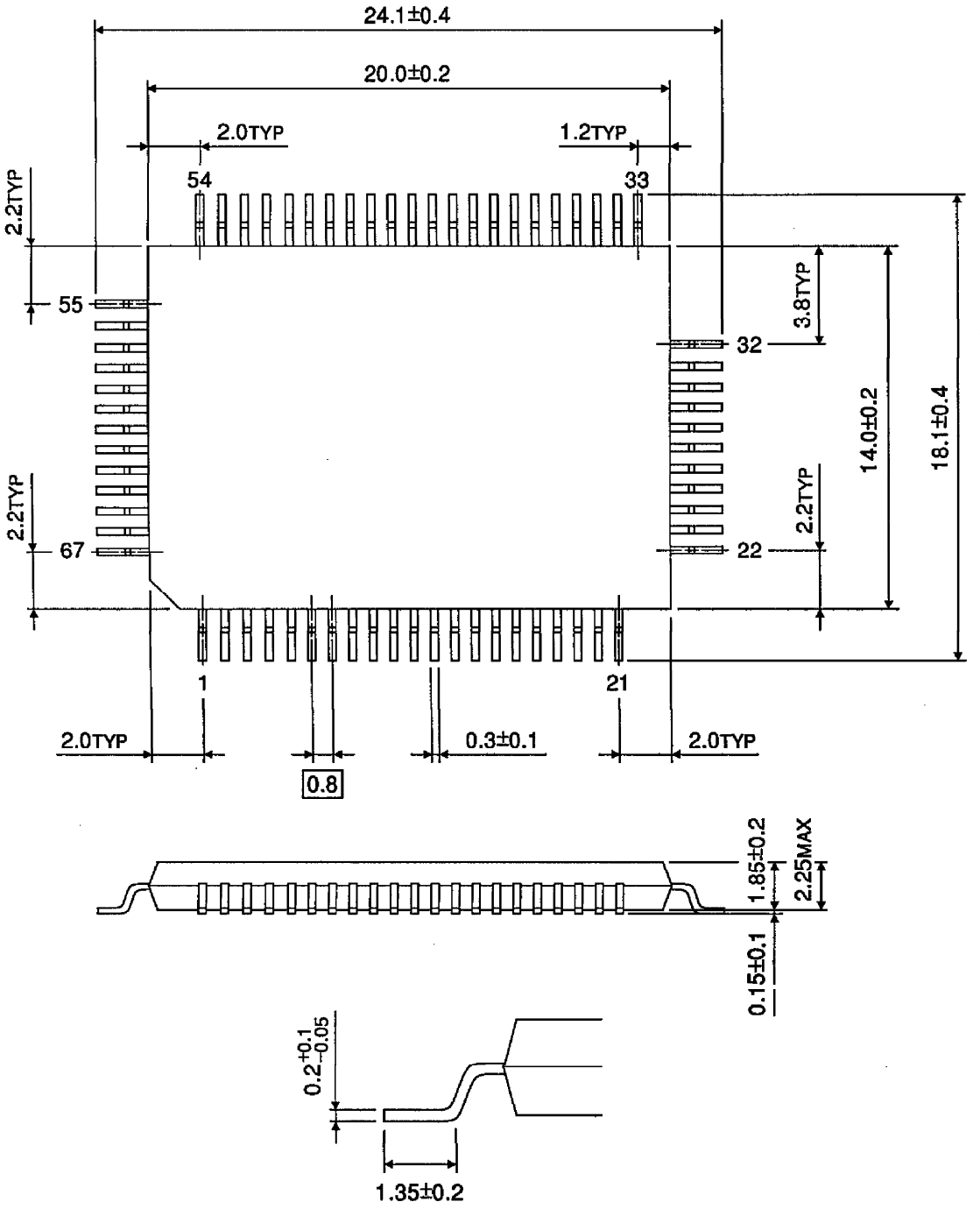
## PAD LAYOUT




PAD Pitch 201.3 $\mu$m

**OUTLINE DRAWING**

QFP67-P-1420-0.80 Unit : mm




Weight : 1.20g (Typ.)

**GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP**

1. Purpose

   This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

   This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

   When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

   1) Individual specification for the calculator LSI bare chip.
      (Both PURCHASER and VENDOR are confirmed by the special sheets.)
   2) General specifications for the calculator LSI bare chip.
   3) Other related specifications and standards.

4. Characteristics

   To be shown in the individual specification sheets.
   The individual specification shall consist of the following 4 items in principle.

   1) Rated specifications.
   2) Electrical characteristics.
   3) Pin configuration & mechanical dimensions.
   4) Others.

5. Inspection of product for delivery

   5.1 Inspection lot

   a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.

   b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level Ⅱ.

The acceptable quality level (AQL) shall be specified in following table :

| TEST ITEM | AQL (%) |
|---|---|
| Electrical | 2.5 |
| Visual | 4.0 |

5.3 Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.

b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

6.2 Inspection procedure

PURCHASER should do his incoming inspection according to the following procedure.

a) First : Visual inspection should be done.

b) Next : Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.
However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

a) Dice shall be placed in die tray with the top metalization facting up in order.

b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

| | |
|---|---|
| Date | |
| Name | |
| Lot No. | |
| Net | |
| **TOSHIBA**<br>MADE IN JAPAN | |

c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

9.1 Chips must be stored under proper conditions to insure that they are not subjected to a moist and / or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions :

A. Storage temperature, 40°C max.
B. Relative humidity, 50% max.
C. Clean, dust-free environment.

9.2 The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.

9.3 During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.

9.4 After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.
In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.

b) Operator should be properly grounded.

10.2 In-process handling

a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.

b) All external leads of the assemblies or subassemblies should be shorted together.

**VISUAL INSPECTION CRITERIA**

1. Visual inspection magnification shall be 40 × in principle.
2. Defects defined :

2.1 Thickness

See the technical data sheet.

2.2 Chip and crack

A die shall be rejected if :

a) Any crack of chip extends greater than 35$\mu$m in length into the inside of the scribble line. (see Fig.1)

2.3 Metallization

A die shall be rejected if :

a) More than 25% of the designed area of the metallization is missing at any bonding pad.

b) There is a short or break which affects electrical characteristics in any lead pattern. (see Fig.2)

2.4 Glass protection coat

A die shall be rejected if :

a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5 Attached foreign material

A die shall be rejected if :

a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.

b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6 Others

A die shall be rejected if :

a) There have no evident probed impression on the bonding pads.

b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.

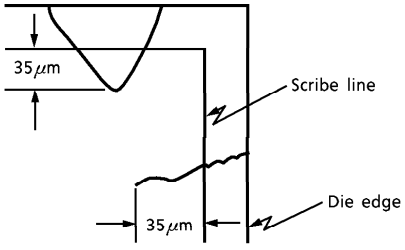



Fig.1

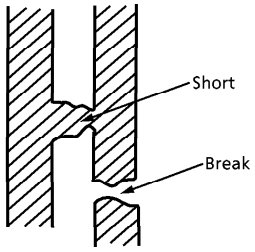



Fig.2 Lead pattern

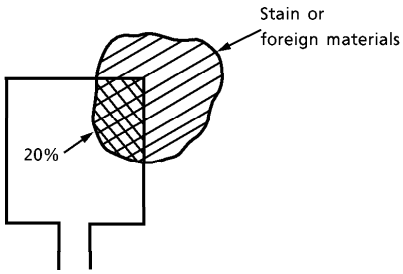
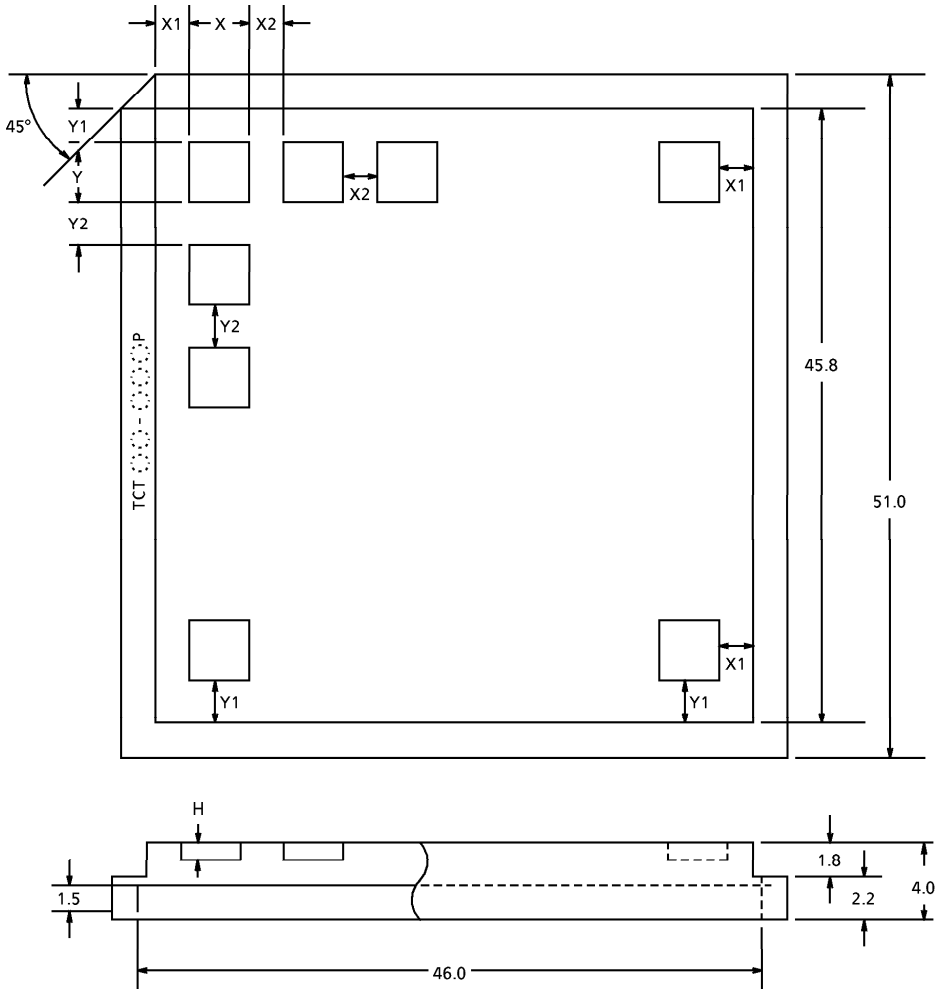



Fig.3

**OUTSIDE DIMENSIONS OF CHIP TRAY**



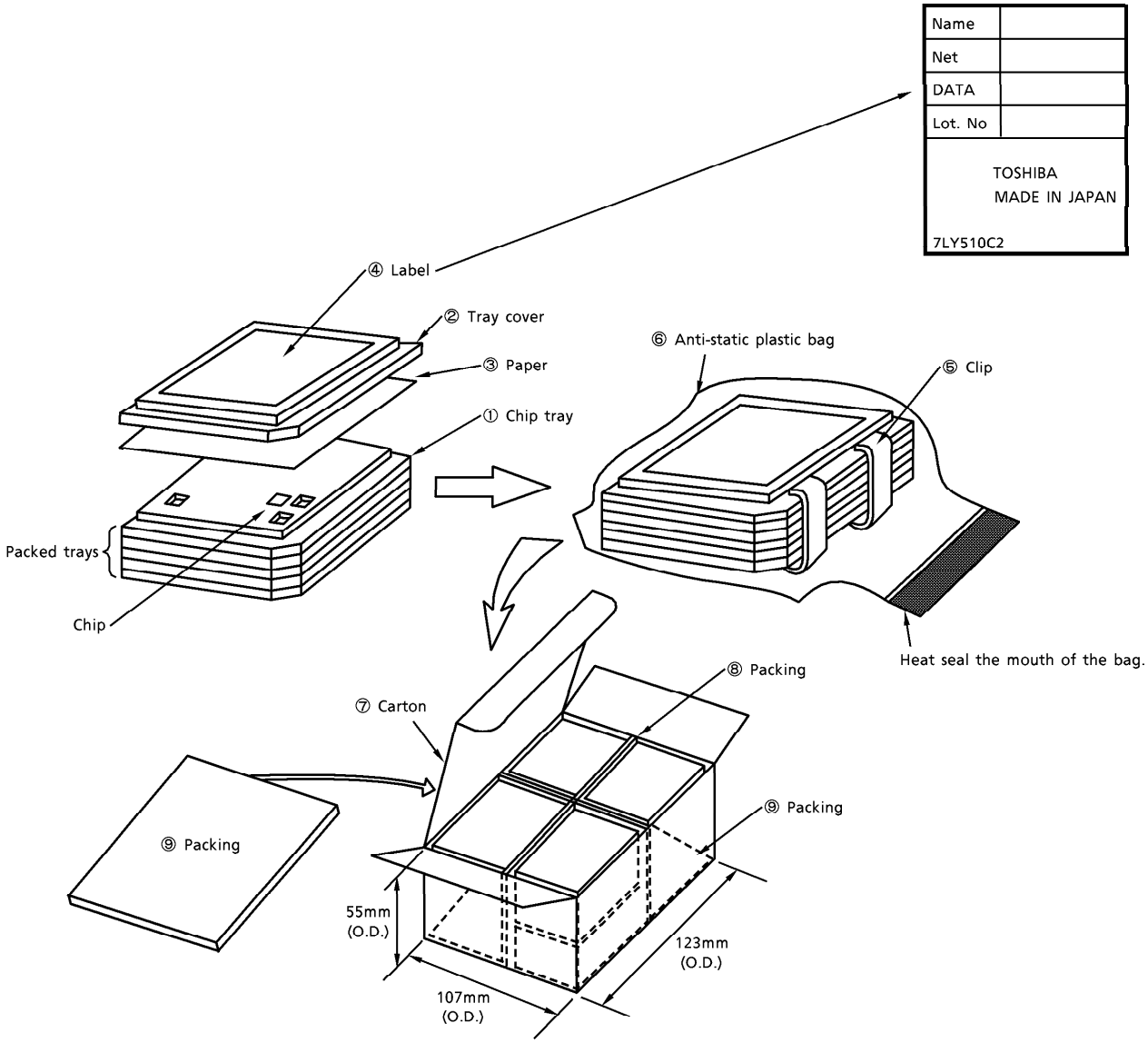

Unit : mm

| CHIP NAME | TRAY NAME | X | Y | (H) | No. OF POCKETS | X1 | X2 | Y1 | Y2 |
|---|---|---|---|---|---|---|---|---|---|
| JT6M19-AS | TCT53-060P | 5.30 | 5.30 | 0.60 | 7×7 (49) | 1.350 | 1.000 | 1.350 | 1.000 |

Tray material :

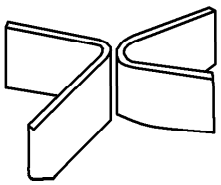
Carbon-containing polypropylene

## PACKING METHOD-1



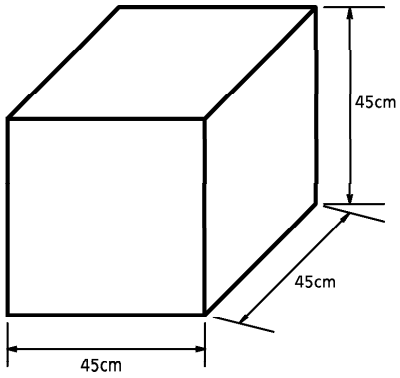

Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑧ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.



**PACKING METHOD-2**

Shipping box




- Inner box : Containing 20 boxes
- Weight : Approx. 15kg (including packing material)
- Material : Corrugated cardboard
- IC contents : 36×5×8×20=28.8kpcs.