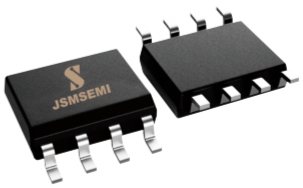
■ DESCRIPTION

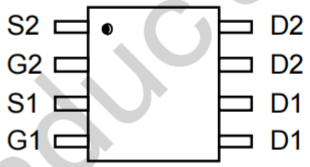
The APM9948KC-TRL is the N-Channel logic enhancement mode power field effect transistor, is produced using high cell density advanced trench technology.

This high density process is especially tailored to minimize on-state resistance.These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits.

■ PIN CONFIGURATION



Top View

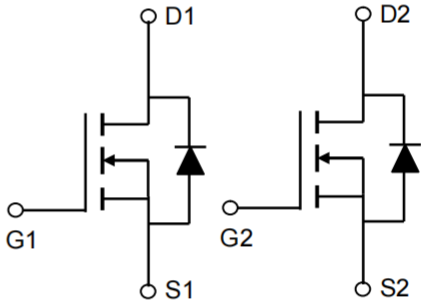


■ FEATURE

- ***60V/6.3A, $R_{DS(ON)}$=30mΩ (typ.)@VGS= 10V***
- ***60V/5.0A, $R_{DS(ON)}$=37mΩ (typ.)@VGS= 4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design

■ APPLICATIONS

- Power Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25℃	I_D	6.3	A
	T_A=70℃		5	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	62.5	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		73	110	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	31	40	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

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■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= 250uA	1.0	1.8	3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 48V, V_{GS}=0			1	uA
		V_{DS}= 48V, V_{GS}=0 T_J=55℃			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}= 10V, I_D= 6.3A		30	45	mΩ
		V_{GS}= 4.5V, I_D= 5.0A		37	55	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= 1.0A, V_{GS}=0V		0.8	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}= 30V V_{GS}= 10V I_D= 5.0A		15.6	16	nC
Q_{gs}	Gate-Source Charge			1.3		
Q_{gd}	Gate-Drain Charge			4.5		
C_{iss}	Input Capacitance	V_{DS}= 25V V_{GS}=0V f=1MHz		520		pF
C_{oss}	Output Capacitance			105		
C_{rss}	Reverse Transfer Capacitance			60		
$T_{d(on)}$	Turn-On Time	V_{DS}= 30V I_D= 1A V_{GEN}= 10V R_G=6Ω		8	16	nS
T_r				6	12	
$T_{d(off)}$	Turn-Off Time			25	46	
T_f				4	8	

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

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■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

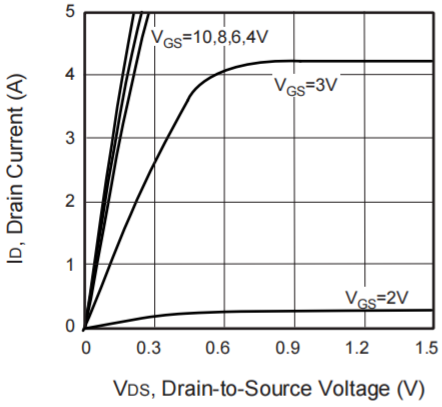

Figure 1. Output Characteristics

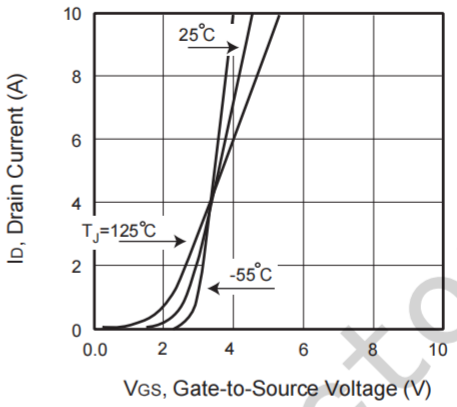

Figure 2. Transfer Characteristics

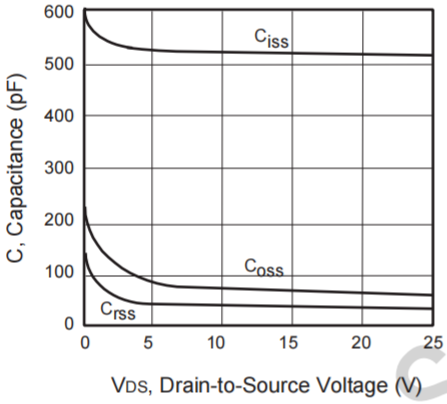

Figure 3. Capacitance

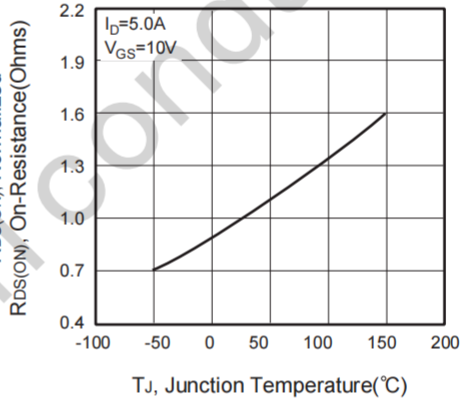

Figure 4. On-Resistance Variation with Temperature

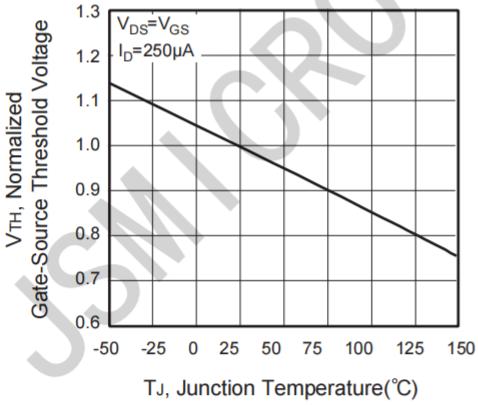

Figure 5. Gate Threshold Variation with Temperature

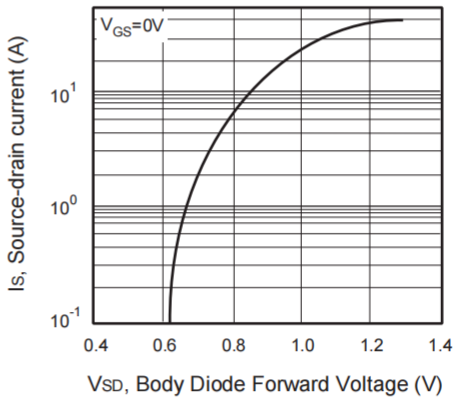

Figure 6. Body Diode Forward Voltage Variation with Source Current

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■ *TYPICAL CHARACTERISTICS (continuous)*

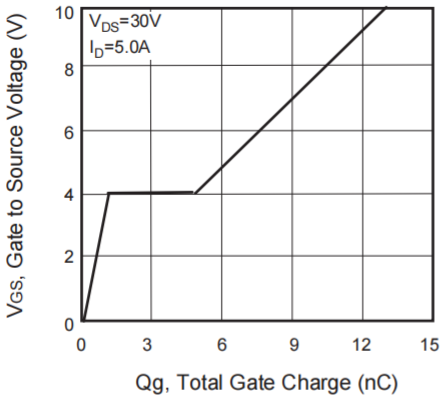

Figure 7. Gate Charge

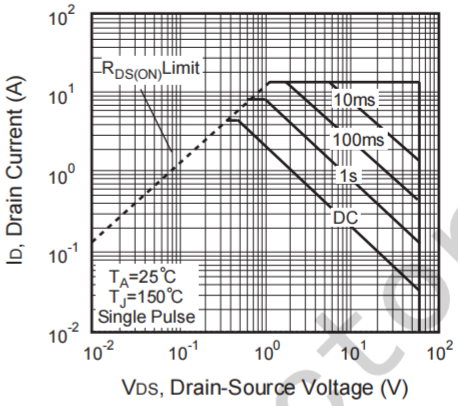

Figure 8. Maximum Safe Operating Area

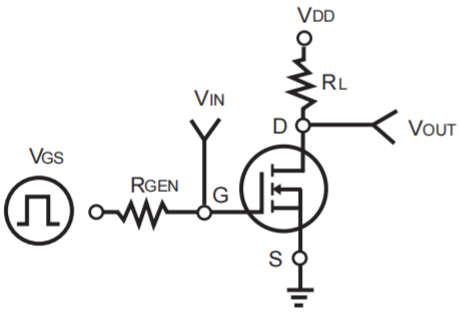

Figure 9. Switching Test Circuit

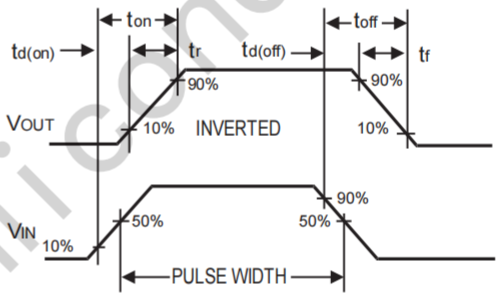

Figure 10. Switching Waveforms

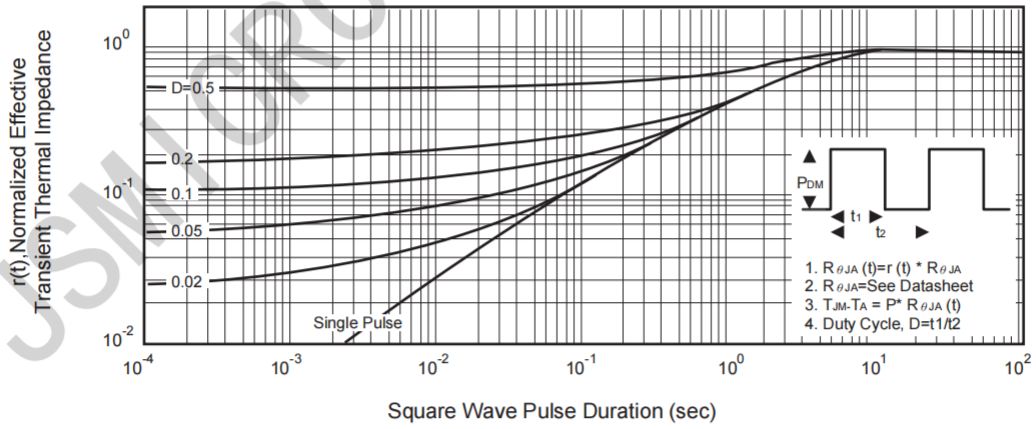

Figure 11. Normalized Thermal Transient Impedance Curve

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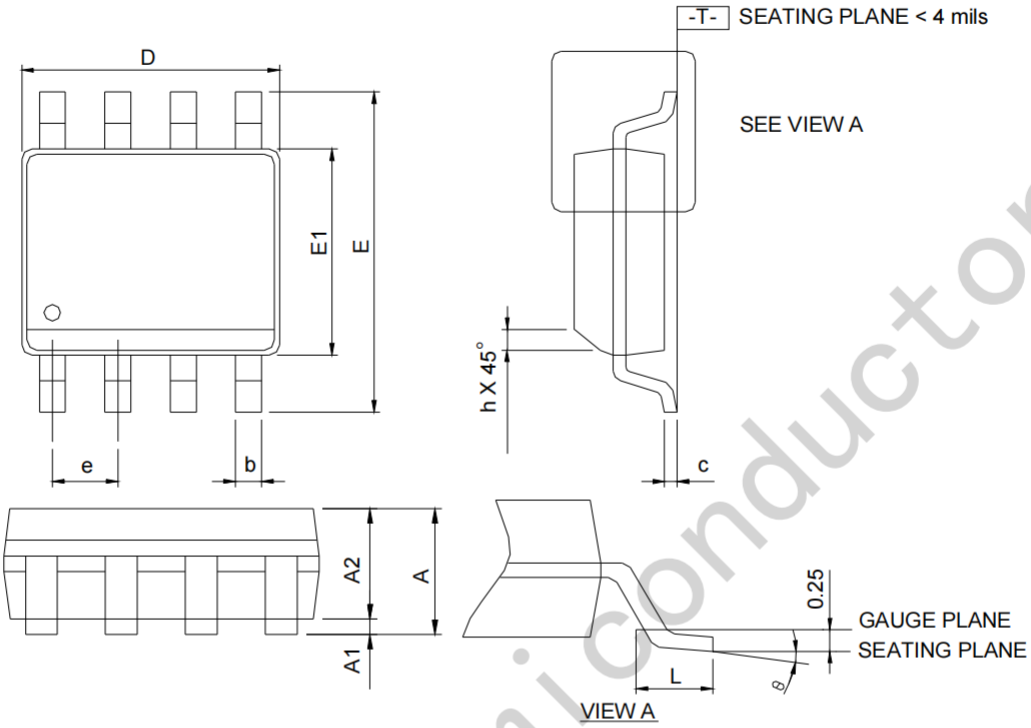
Package Information

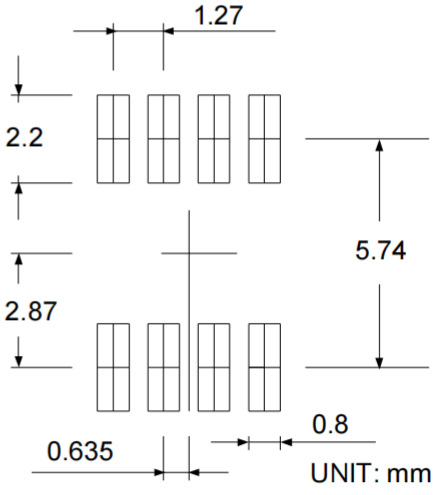
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN



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