Preliminary

IDG-2020 & IXZ-2020 Product Specification Revision 1.0

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1 Document Information

1.1 Revision History

Revision Date	Revision	Description
12/06/2011	1.0	Initial Release

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1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information for the Digital Still Camera & Digital Video Camera Optical Image Stabilization (OIS) two axis gyroscopes, IDG-2020™ and IXZ-2020™. Both devices are housed in small 3x3x0.90mm QFN package and are pin and function compatible.

Specifications are based upon design analysis and simulation results only. Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the IDG-2020 and IXZ-2020 Register Map and Register Descriptions document.

1.3 Product Overview

The IDG-2020 and IXZ-2020 are single-chip, digital output, 2 Axis MEMS gyroscope ICs which feature a 512-byte FIFO. In applications such as Electronic Image Stabilization, the gyro output is sampled at a fast rate, e.g.1 KHz, but is only needed at the video frame rate (ex: 30 fps). The FIFO can store the samples within a frame, lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. The FSYNC (Frame Sync) input allows precise timing to be achieved with Video Frame Sync at the host level for read out of the frame data.

The OIS gyros include specific features to enhance OIS performance including a narrow programmable full-scale range of ±31.25, ±62.5, ±125, and ±250 degrees/sec, fast sampling of the gyro output at up to 32KHz, low phase delay including fast 20MHz read out through SPI interface, very low Rate noise at 0.0075 dps/√Hz and extremely low power consumption at 2.7 mA for 2 axis operation. Factory-calibrated initial sensitivity reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% drift from -40°C to 85°C, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

By leveraging its patented and volume-proven Nasiri-Fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the gyro package size down to a footprint and thickness of 3x3x0.90mm (16-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

Sensor Axes for each device

Device	IDG-2020	IXZ-2020
Gyro Axes	X, Y	X, Z

1.4 Applications

- Optical Image Stabilization for Digital Still Camera and Video Cameras
- Electronic Image Stabilization for video jitter compensation

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2 Features

The IDG-2020 and IXZ-2020 MEMS gyroscopes include a wide range of features:

2.1 Sensors

- Monolithic angular rate sensor (gyros) integrated circuit
- Available in XY (IDG-2020) and XZ (IXZ-2020) versions.
- Digital-output temperature sensor
- External sync signal connected to the FSYNC pin supports image, video and GPS synchronization
- Factory calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000*g* shock tolerant

2.2 Digital Output

- Fast Mode (400kHz) I^2C serial interface
- 1 MHz SPI serial interface for full read/write capability
- 20 MHz SPI to read gyro sensor & temp sensor data.
- 16-bit ADCs for digitizing sensor outputs
- User-programmable full-scale-range of ±31.25°/sec, ±62.5°/sec, ±125°/sec and ±250°/sec

2.3 Data Processing

- The total data set obtained by the device includes gyroscope data, temperature data, and the one bit external sync signal connected to the FSYNC pin.
- FIFO allows burst read, reduces serial bus traffic and saves power on the system processor.
- FIFO can be accessed through both I^2C and SPI interfaces.
- Programmable interrupt
- Programmable low-pass filters

2.4 Clocking

- On-chip timing generator clock frequency ±1% drift over full temperature range

2.5 Power

- VDD supply voltage range of 1.71V to 3.6V
- Flexible VDDIO reference voltage allows for multiple I^2C and SPI interface voltage levels
- Power consumption for two axes active: 2.7mA
- Sleep mode: 5µA
- Each axis can be individually powered down

2.6 Package

- 3x3x0.90mm footprint and maximum thickness 16-pin QFN plastic package
- MEMS structure hermetically sealed at wafer level
- RoHS and Green compliant

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3 Electrical Characteristics

3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL=0		±31.25		º/s	
	FS_SEL=1		±62.5		º/s	
	FS_SEL=2		±125		º/s	
	FS_SEL=3		±250		º/s	
Sensitvity Scale Factor	FS_SEL=0		1048		LSB/(º/s)	
	FS_SEL=1		524		LSB/(º/s)	
	FS_SEL=2		262		LSB/(º/s)	
	FS_SEL=3		131		LSB/(º/s)	
Gyro ADC Word Length			16		bits	
Sensitivity Scale Factor Tolerance	25°C		±3		%	
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±0.025		%/ ºC	
Nonlinearity	Best fit straight line; 25°C		±0.1		%	
Cross-Axis Sensitivity			±2		%	
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±5		º/s	
ZRO Variation Over Temperature	-40°C to +85°C		±25		º/s	
Power-Supply Sensitivity (1-10Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	
Power-Supply Sensitivity (10 - 250Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	
Power-Supply Sensitivity (250Hz - 100kHz)	Sine wave, 100mVpp; VDD=2.2V		4		º/s	
Linear Acceleration Sensitivity	Static		0.1		º/s/*g*	
GYRO NOISE PERFORMANCE	**FS_SEL=0**					
Total RMS Noise	DLPFCFG=2 (100Hz)		0.075		º/s-rms	
Low-frequency RMS noise	Bandwidth 1Hz to10Hz		0.025		º/s-rms	
Rate Noise Spectral Density	At 10Hz		0.0075		º/s/√Hz	
GYRO MECHANICAL FREQUENCY		20			kHz	
GYRO START-UP TIME	DLPFCFG=0, from sleep mode					
ZRO Settling	to ±1º/s of Final		35	50	ms	
TEMPERATURE SENSOR						
Range			-40 to +85		ºC	
Sensitivity	Untrimmed		TBD		LSB/ºC	
Room-Temperature Offset	35°C		TBD		LSB	
Linearity			±0.2		°C	
TEMPERATURE RANGE						
Specified Temperature Range		-40		+85	ºC	

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3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
VDD POWER SUPPLY						
Operating Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	1		100	ms	
Normal Operating Current	Two Axes Active		2.7		mA	
Sleep Mode Current			5		µA	
VDDIO REFERENCE VOLTAGE (must be regulated)						
Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	1		100	ms	
Normal Operating Current	10pF load, 5MHz data rate. Does not include pull up resistor current draw as that is system dependent		300		µA	
START-UP TIME FOR REGISTER READ/WRITE			TBD	100	ms	
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, /CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 5		pF	
DIGITAL OUTPUT (INT, SDO)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ	0.9*VDDIO			V	
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	

Note: Power-Supply Ramp Rates are defined as the time it takes for the voltage to rise from 10% to 90% of the final value. VDD and VDDIO must be monotonic ramps.

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3.3 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A=25°C.

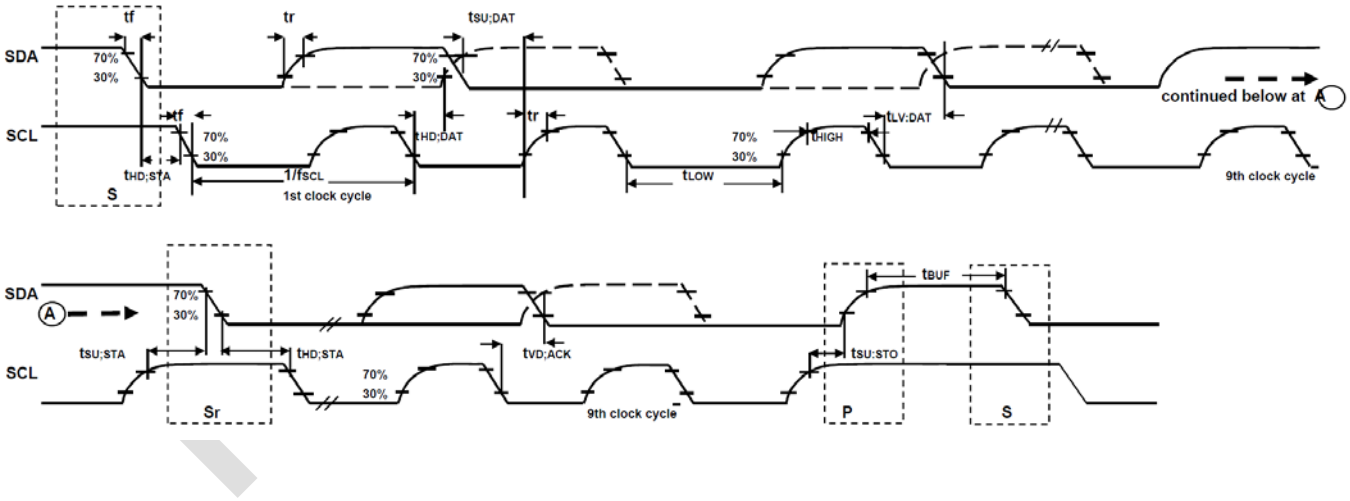
Parameters	Conditions	Min	Typical	Max	Units	Notes
I^2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage			-0.5V to 0.3*VDDIO		V	
V_{IH}, HIGH-Level Input Voltage			0.7*VDDIO to VDDIO + 0.5V		V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL1}, LOW-Level Output Voltage	3mA sink current		0 to 0.4		V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf		20+0.1C_b to 250		ns	
C_I, Capacitance for Each I/O pin			< 10		pF	
INTERNAL CLOCK SOURCE						
	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
Sample Rate	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-2		+2	%	
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	
Frequency Variation over Temperature	CLK_SEL=0,6		-10 to +10		%	
	CLK_SEL=1,2,3,4,5		±1		%	
PLL Settling Time	CLK_SEL=1,2,3,4,5		4		ms	

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3.4 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V±5%, 2.5V±5%, 3.0V±5%, or 3.3V±5%, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		0		400	kHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1 C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1 C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	



I²C Bus Timing Diagram

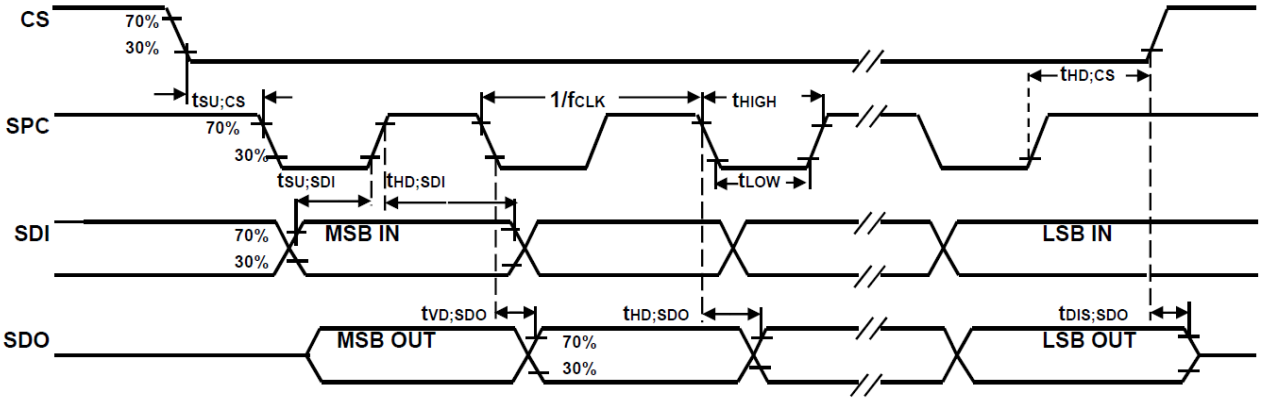
3.5 SPI Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.1V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units
SPI TIMING					
f_{SCLK}, SCLK Clock Frequency		0.9		1	MHz
t_{LOW}, SCLK Low Period		400			ns
t_{HIGH}, SCLK High Period		400			ns
$t_{SU.CS}$, CS Setup Time		8			ns
$t_{HD.CS}$, CS Hold Time		500			ns
$t_{SU.SDI}$, SDI Setup Time		11			ns
$t_{HD.SDI}$, SDI Hold Time		7			ns
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			100	ns
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	4			ns
$t_{DIS.SDO}$, SDO Output Disable Time				10	ns

Note:

1. Based on characterization of 5 parts over temperature as mounted on evaluation board or in sockets



SPI Bus Timing Diagram

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3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

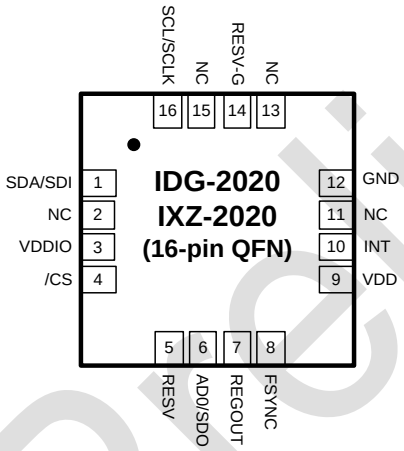
Parameter	Rating
Supply Voltage, VDD	-0.5V to +3.6V
VDDIO Input Voltage Level	-0.5V to 3.6V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC)	-0.5V to VDD
SCL, SDA, INT (SPI enable)	-0.5V to VDD
SCL, SDA, INT (SPI disable)	-0.5V to VDD
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2),125°C

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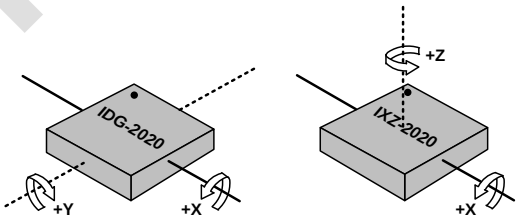
4 Applications Information

4.1 Pin Out and Signal Description

Pin Number 3x3x0.90mm	Pin Name	Pin Description
1	SDA/SDI	I^2C serial data (SDA); SPI serial data input (SDI)
3	VDDIO	Digital I/O supply voltage.
4	/CS	SPI chip select (0=SPI mode, 1= I^2C mode)
5	RESV	Reserved. Do not connect.
6	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
7	REGOUT	Regulator filter capacitor connection
8	FSYNC	Frame synchronization digital input. Connect to GND if not used.
9	VDD	Power supply voltage and Digital I/O supply voltage
10	INT	Interrupt digital output (totem pole or open-drain)
12	GND	Power supply ground
14	RESV-G	Reserved. Connect to Ground.
16	SCL/SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
2, 11, 13, 15	NC	Not internally connected. May be used for PCB trace routing.



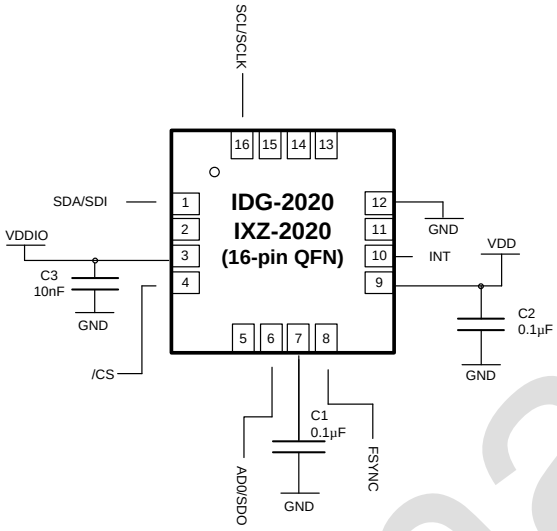
QFN Package (Top View)
16-pin, 3mm x 3mm x 0.90mm
Footprint and maximum thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

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4.2 Typical Operating Circuit



Typical Operating Circuit

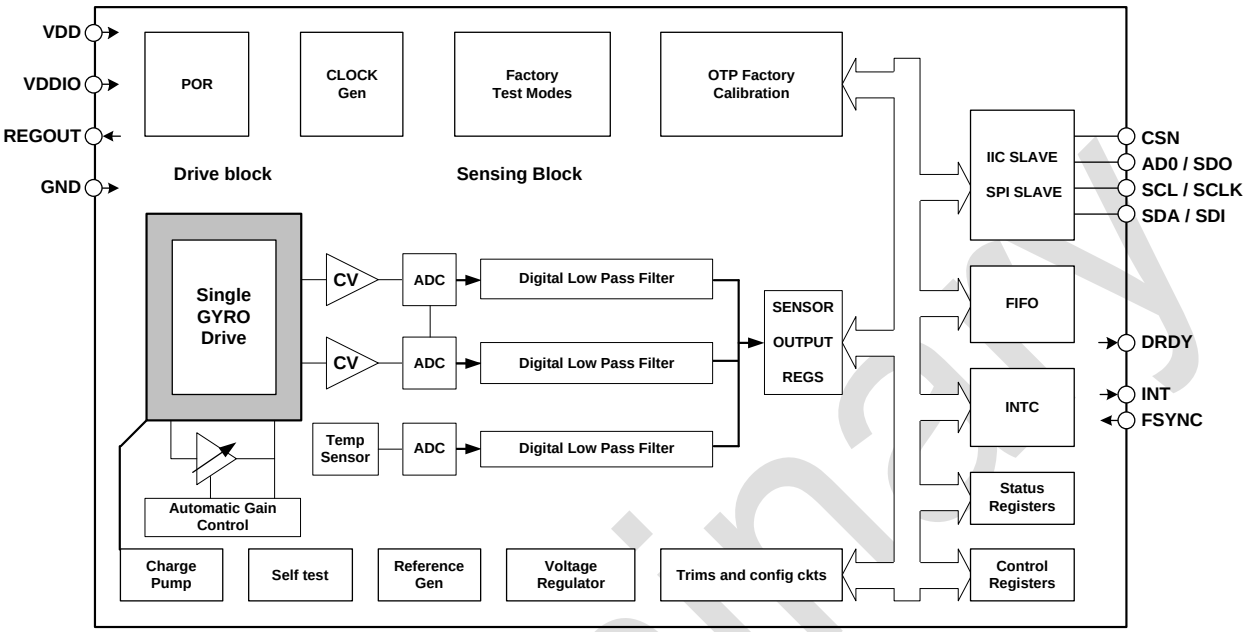
4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

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5 Functional Overview

5.1 Block Diagram



5.2 Overview

The IDG-2020 or IXZ-2020 is comprised of the following key blocks / functions:

- Two-axis MEMS rate gyroscope sensors with 16-bit ADCs and signal conditioning
- Available in two axis XY and XZ configurations
- I^2C and SPI serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO

5.3 Two-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The IDG-2020 or IXZ-2020 consists of a single structure vibratory MEMS rate gyroscope, which detects rotation about the X&Y or X&Z axes, respectively. When the gyro is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pick off. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The chip features a programmable full-scale range of the gyro sensors of ±31.25, ±62.5, ±125, and ±250 dps. The FSR range is optimized for image stabilization applications where the narrower range improves hand jitter detection accuracy via the 16 bit ADCs. User-selectable low-pass filters enable a wide range of cut-off frequencies. The ADC sample rate can be programmed to 32 kHz, 8 kHz, 1 kHz, 500 Hz, 333.3 Hz, 250 Hz, 200 Hz, 166.7 Hz, 142.9 Hz, or 125 Hz.

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5.4 I²C and SPI Serial Communications Interface

The IDG-2020 or IXZ-2020 has both I²C and SPI serial interfaces. The device always acts as a slave when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VDDIO pin. The LSB of the of the I²C slave address is set by the AD0 pin. The I²C and SPI protocols are described in more detail in Section 6.

5.5 Internal Clock Generation

The IDG-2020 or IXZ-2020 has a flexible clocking scheme, allowing for a variety of internal clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, various control circuits, and registers.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- PLL (gyroscope based clock)

In order for the gyroscope to perform to spec, the PLL must be selected as the clock source. When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscopes disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.

5.6 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

5.7 FIFO

The IDG-2020 or IXZ-2020 contains a 512-byte FIFO register that is accessible via the both the I²C and SPI Serial Interfaces. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, temperature readings and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

5.8 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources), (2) new data is available to be read (from the FIFO and Data registers), and (3) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

5.9 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the device's die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

5.10 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IDG-2020 or IXZ-2020. Its two inputs are unregulated VDD of 1.71V to 3.6V and a VDDIO logic reference supply voltage of 1.71V to 3.6V. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.

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6 Digital Interface

6.1 I²C Serial Interface

The internal registers and memory of the IDG-2020 or IXZ-2020 can be accessed using the I²C interface.

Serial Interface

Pin Number	Pin Name	Pin Description
3	VDDIO	Digital I/O supply voltage.
6	AD0 / SDO	I²C Slave Address LSB (AD0); SPI serial data output (SDO)
16	SCL / SCLK	I²C serial clock (SCL); SPI serial clock (SCLK)
1	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

6.1.1 I²C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IDG-2020 or IXZ-2020 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

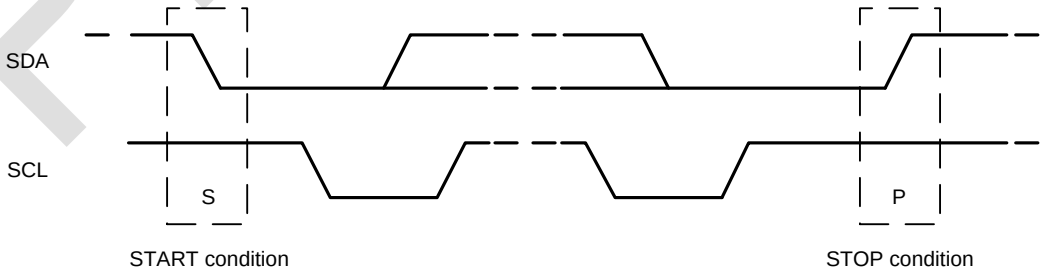
The slave address of the device is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two IDG-2020 or IXZ-2020 devices to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I²C address is stored in WHO_AM_I register.

I²C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.



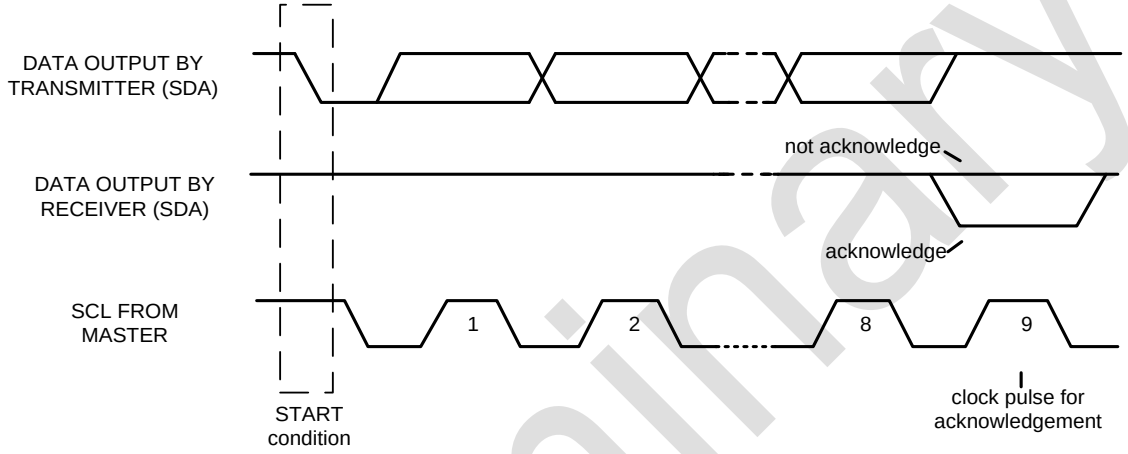
START and STOP Conditions

Preliminary

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

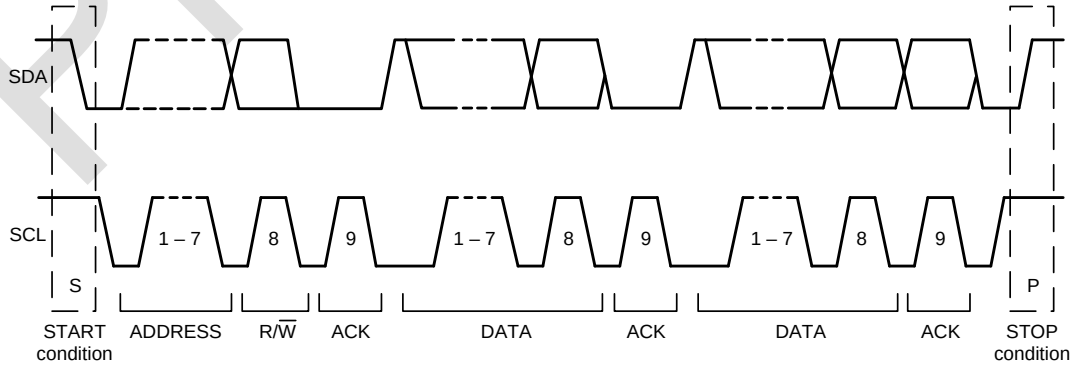
If a slave is busy and is unable to transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



Complete I²C Data Transfer

Preliminary

To write the internal IDG-2020 or IXZ-2020 registers, the master transmits the start condition (S), followed by the I^2C address and the write bit (0). At the 9th clock cycle (when the clock is high), the device acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the device acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the device automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal device registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the device, the master transmits a start signal followed by the slave address and read bit. As a result, the device sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	The internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

6.1.2 SPI interface

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. The IDG-2020 or IXZ-2020 always operates as a Slave device during standard Master-Slave SPI operation. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDO) and the Data Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (/CS) for each Slave device; /CS goes low at the start of transmission and goes back high at the end. The Serial Data Output (SDO) line, remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. SCLK frequency is 1MHz max for SPI in full read/write capability mode. When the SPI frequency is set to 20MHz, its operation is limited to reading sensor registers only.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

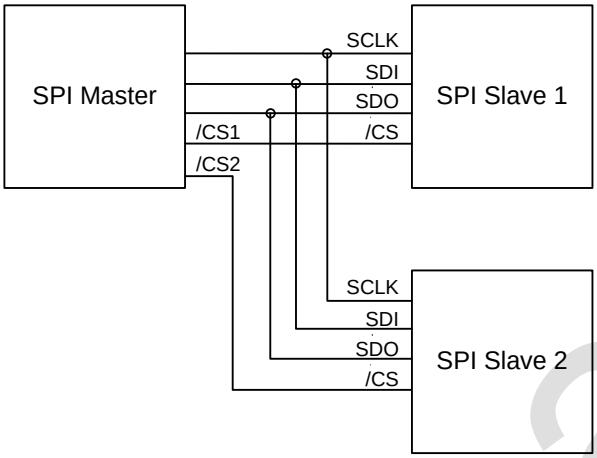
MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

Preliminary



Typical SPI Master / Slave Configuration

Each SPI slave requires its own Chip Select (/CS) line. SDO, SDI and SCLK lines are shared. Only one /CS line is active (low) at a time ensuring that only one slave is selected at a time. The /CS lines of other slaves are held high which causes their respective SDO pins to be high-Z.

Preliminary

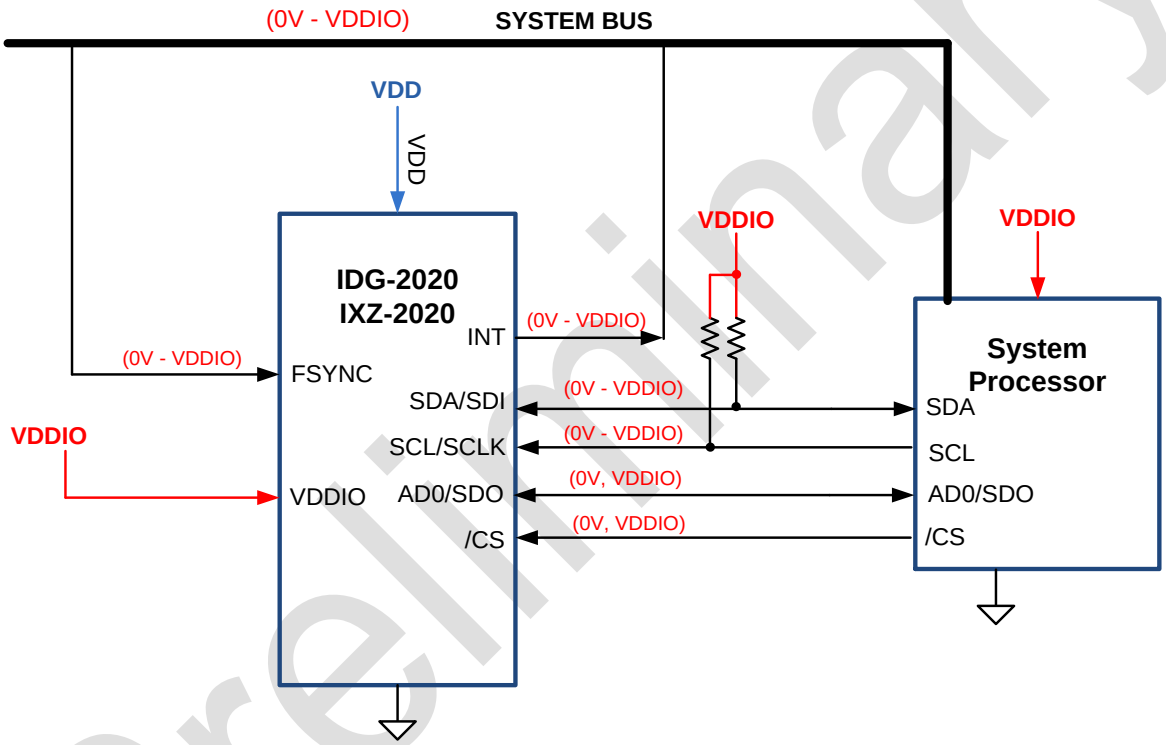
7 Serial Interface Considerations

7.1 Supported Interfaces

The IDG-2020 or IXZ-2020 supports I^2C and SPI communication.

7.2 Logic Levels

The I/O logic levels are set to VDDIO. VDDIO may be set to be equal to VDD or to another voltage, such that it is between 1.71 V and 3.6V at all times. Both I^2C and SPI communication support VDDIO.



Preliminary

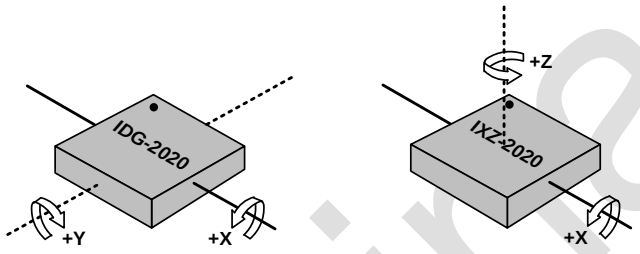
8 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits.

This preliminary datasheet only provides limited information with respect to IDG-2020 or IXZ-2020 Assembly. Additional information will be supplied in subsequent versions of the document.

8.1 Orientation of Axes

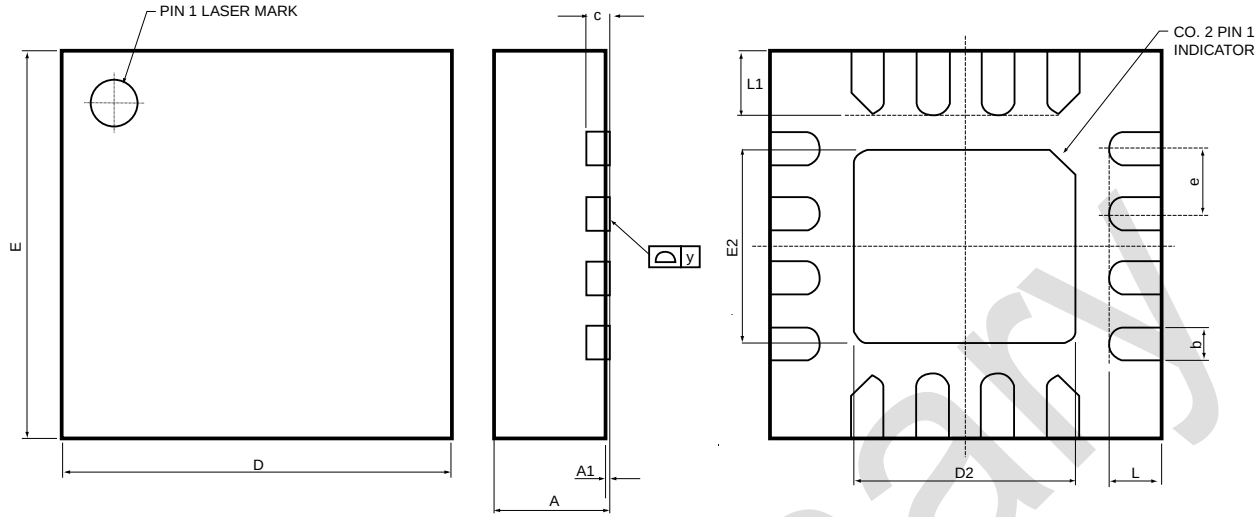
The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier in the figure.



Orientation of Axes of Sensitivity and Polarity of Rotation

Preliminary

8.2 Package Dimensions



Dimensions in Millimeters			
Dimension	**Min**	**Nom**	**Max**
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.127 ref	---
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.45	1.50	1.55
e	---	0.50	---
Legend	0.35	0.40	0.45
L1	0.45	0.50	0.55
y	0.000	---	0.075

8.2.1 Package Thickness Tolerance

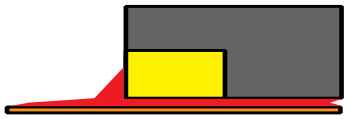
The table below shows the typical and maximum package thicknesses.

Typ	Max
0.90mm	0.95mm

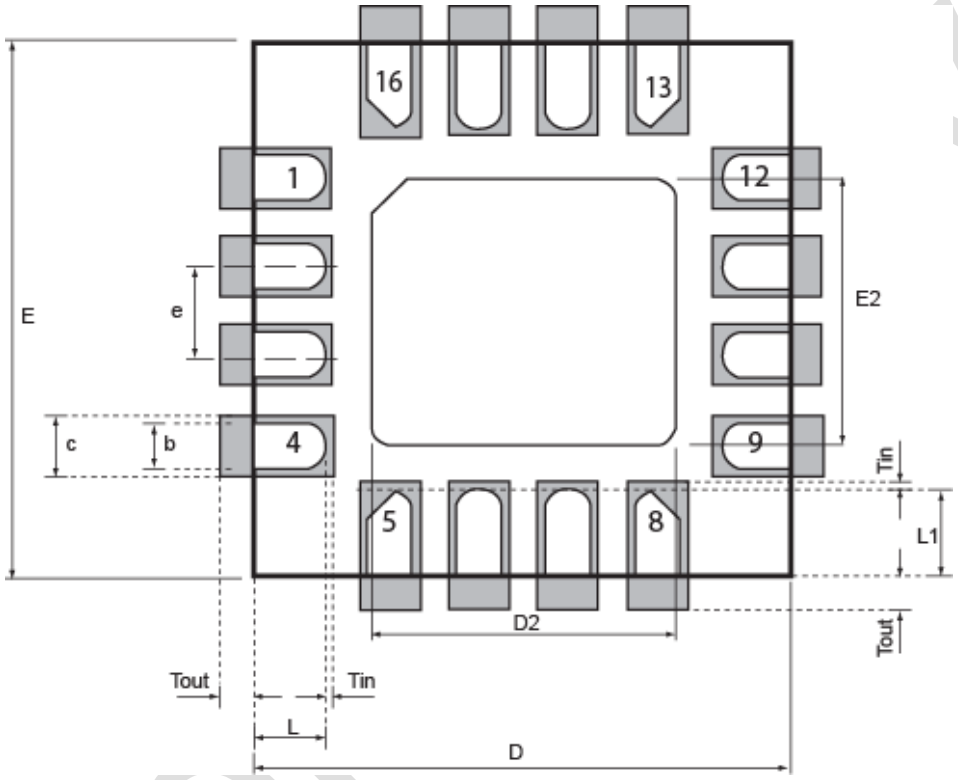
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8.3 PCB Design Guidelines

The Pad Diagram using a JEDEC type extension with solder rising on the outer edge is shown below. The Pad Dimensions Table shows pad sizing (mean dimensions) recommended for the product.



JEDEC type extension with solder rising on outer edge



	Dimensions in Millimeters	
Dimension	**Description**	**Nominal**
Nominal Package I/O Pad Dimensions		
e	Pad Pitch	0.50
b	Pad Width	0.25
L	Pad Length (1-4, 9-12)	0.40
L1	Pad Length (5-8, 13-16)	0.50
D	Package Width	3.00
E	Package Length	3.00
I/O Land Design Dimensions (Guidelines)		
D2	Epad Width	1.70
E2	Epad Height	1.50
c	Land Width	0.35
Tout	Outward Extension	0.20
Tin	Inward Extension	0.05

Note: Solder Screen Option shown for exposed pad with four 0.35 x 0.35 pads
Other options are (1) No solder on exposed pad, or (2) fully soldered exposed pad

PRELIMINARY

9 Reliability

9.1 Qualification Test Policy

InvenSense's products complete a Qualification Test Plan before being released to production. The Qualification Test Plan for the IDG-2020 or IXZ-2020 followed the JEDEC JESD47H.01 Standard, "Stress-Test-Driven Qualification of Integrated Circuits." The individual tests are described below.

9.2 Qualification Test Plan

Accelerated Life Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
High Temperature Operating Life (HTOL/LFR)	JEDEC JESD22-A108D, Dynamic, 3.63V biased, Tj>125°C [read-points 168, 500, 1000 hours]	3	77	(0/1)
Accelerated Moisture Resistance – Unbiased HAST(1)	JEDEC JESD22-A118A Condition A, 130°C, 85%RH, 33.3 psia., Unbiased, [read-point 96 hours]	3	77	(0/1)
High Temperature Storage Life (HTS)	JEDEC JESD22-A103D, Cond. A, 125°C, Unbiased [read-points 168, 500, 1000 hours]	3	77	(0/1)

Device Component Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
ESD-HBM	JEDEC JS-001-2010, (Class 2, 2000V)	1	3	(0/1)
ESD-MM	JEDEC JESD22-A115C, (200V)	1	3	(0/1)
Latch Up	JEDEC JESD78C Class 1, 25°C; Level A ±100mA	1	6	(0/1)
Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883H, method 2002.5, Cond. E, 10,000*g's*, 0.2ms, ±X, Y, Z – 6 directions, 5 times/direction	3	30	(0/1)
Vibration	JEDEC JESD22-B103B, Variable Frequency (random), Cond. B, 5-500Hz, X, Y, Z – 4 times/direction	1	5	(0/1)
Temperature Cycling (TC) (1)	JEDEC JESD22-A104D Condition G, [-40°C to +125°C], Soak Mode 2 [5'], 850 cycles	3	77	(0/1)

Board Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
Board Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883H, method 2002.5, Cond. E, 10000*g's*, 0.2ms, +-X, Y, Z – 6 directions, 5 times/direction	1	5	(0/1)

(1) Tests are preceded by MSL3 Preconditioning in accordance with JEDEC JESD22-A113F

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10 Environmental Compliance

The IDG-2020 and IXZ-2020 are RoHS and Green compliant.

The IDG-2020 and IXZ-2020 are in full environmental compliance as evidenced in report HS-Ixx-2020, Materials Declaration Data Sheet.

Environmental Declaration Disclaimer:
InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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