IXYS

Advance Technical Information

High Voltage XPT™ IGBT

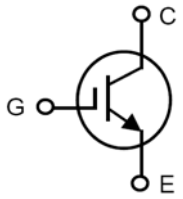
IXYF30N450

V_{CES} = 4500V

I_{C110} = 17A

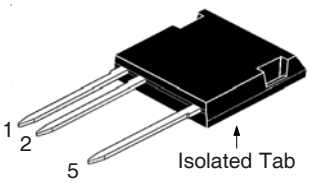
$V_{CE(sat)} \leq$ 3.9V

(Electrically Isolated Tab)



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	4500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	4500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	23	A
I_{C110}	T_C = 110°C	17	A
I_{CM}	T_C = 25°C, 1ms	190	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 15Ω	I_{CM} = 90	A
(RBSOA)	Clamped Inductive Load	3600	V
P_C	T_C = 25°C	230	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		5	g

ISOPLUS i4-Pak™



1 = Gate 5 = Collector
2 = Emitter

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	4500			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	Note 2, T_J = 100°C		100		μA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 30A, V_{GE} = 15V, Note 1		3.2	3.9	V
	T_J = 125°C		4.5		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

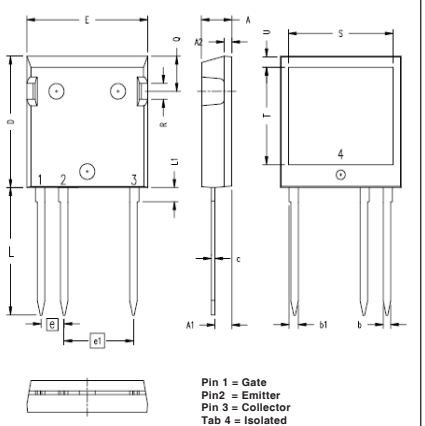
Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

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Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 30A, V_{CE} = 10V, Note 1	11	18	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1840	pF
C_{oes}			83	pF
C_{res}			35	pF
Q_g	I_C = 30A, V_{GE} = 15V, V_{CE} = 1000V		88	nC
Q_{ge}			11	nC
Q_{gc}			40	nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		38	ns
t_r	I_C = 30A, V_{GE} = 15V		318	ns
$t_{d(off)}$	V_{CE} = 960V, R_G = 15Ω		168	ns
t_f			1220	ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		42	ns
t_r	I_C = 30A, V_{GE} = 15V		590	ns
$t_{d(off)}$	V_{CE} = 960V, R_G = 15Ω		180	ns
t_f			1365	ns
R_{thJC}				0.54 °C/W
R_{thCS}			0.15	°C/W

ISOPLUS i4-Pak™ (HV) Outline



Pin 1 = Gate
Pin2 = Emitter
Pin 3 = Collector
Tab 4 = Isolated

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Notes:

1. Pulse test, t < 300µs, duty cycle, d < 2%.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25ºC

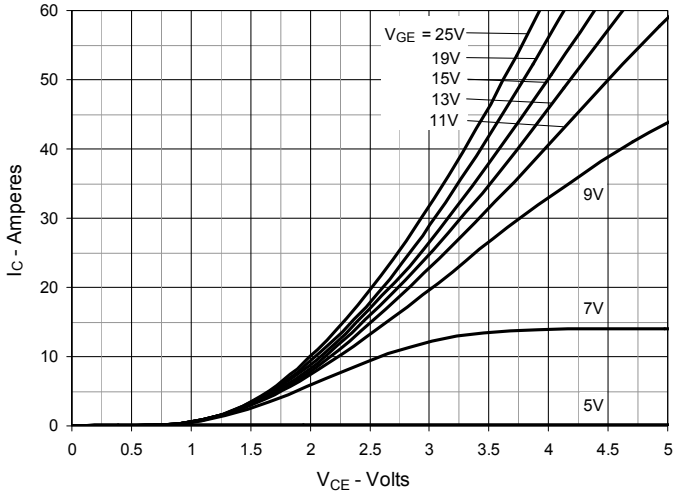


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

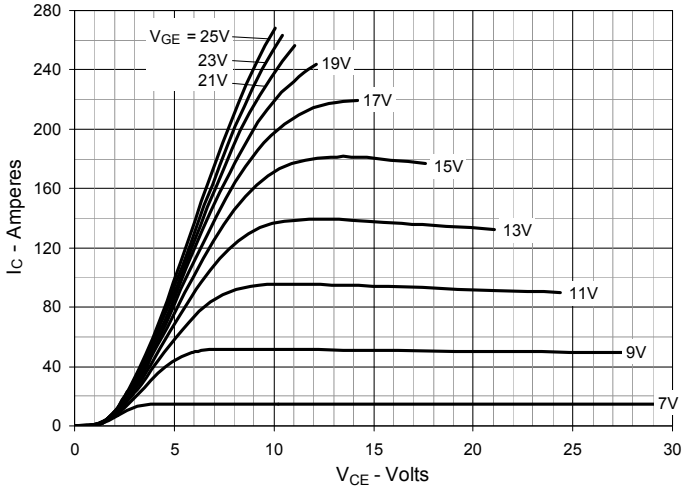


Fig. 3. Output Characteristics @ T_J = 125ºC

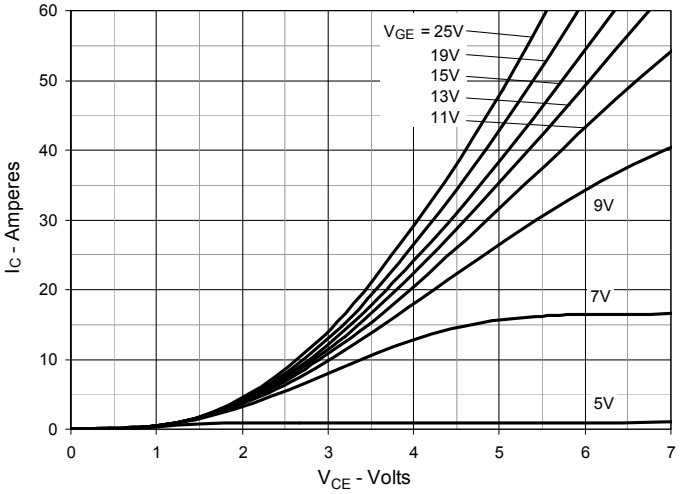


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

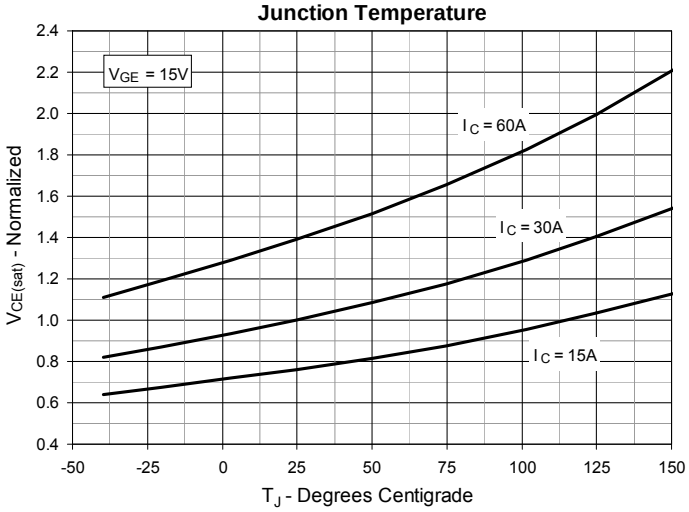


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

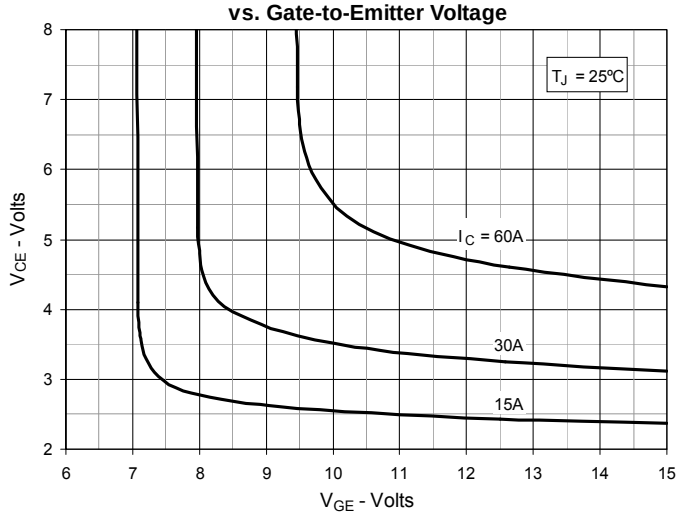
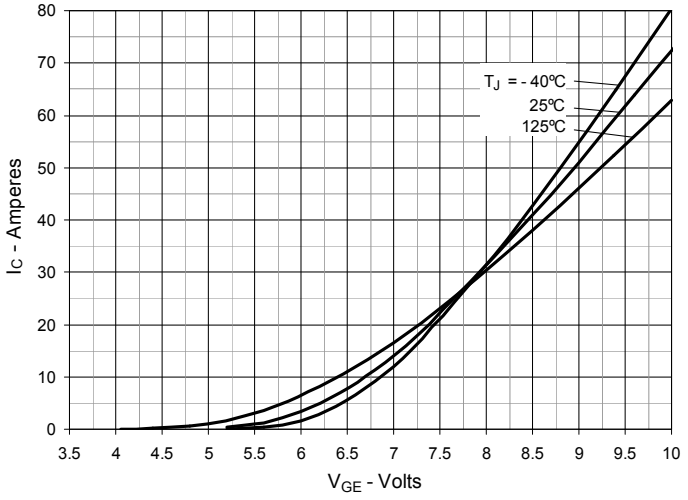


Fig. 6. Input Admittance



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Fig. 7. Transconductance

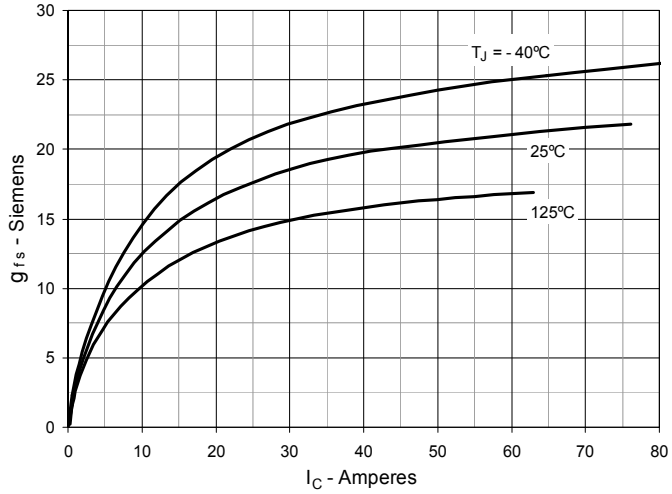


Fig. 8. Gate Charge

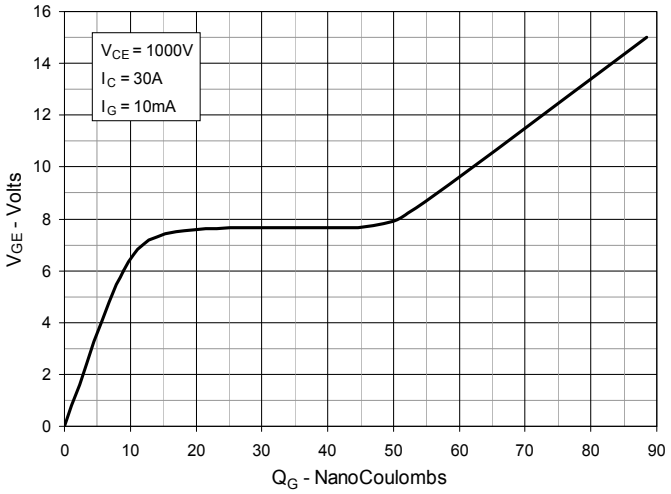


Fig. 9. Capacitance

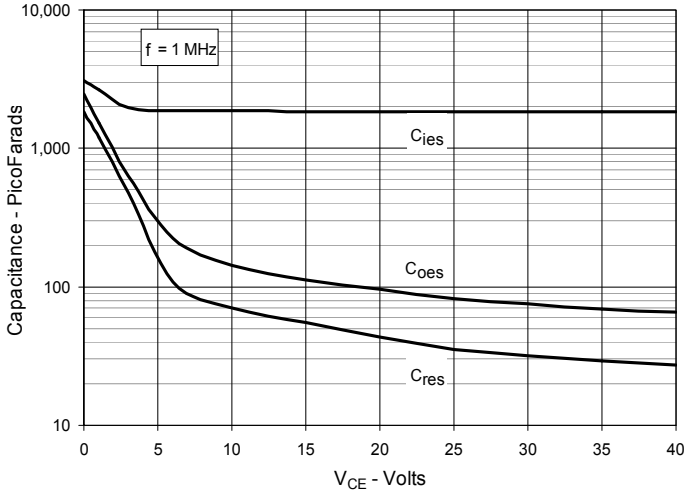


Fig. 10. Reverse-Bias Safe Operating Area

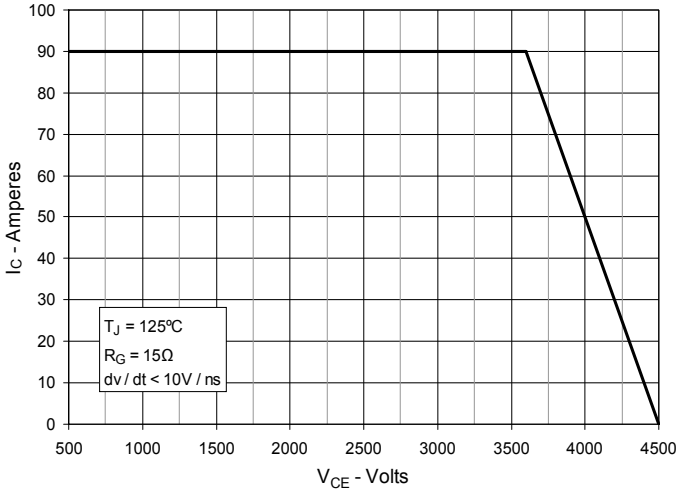
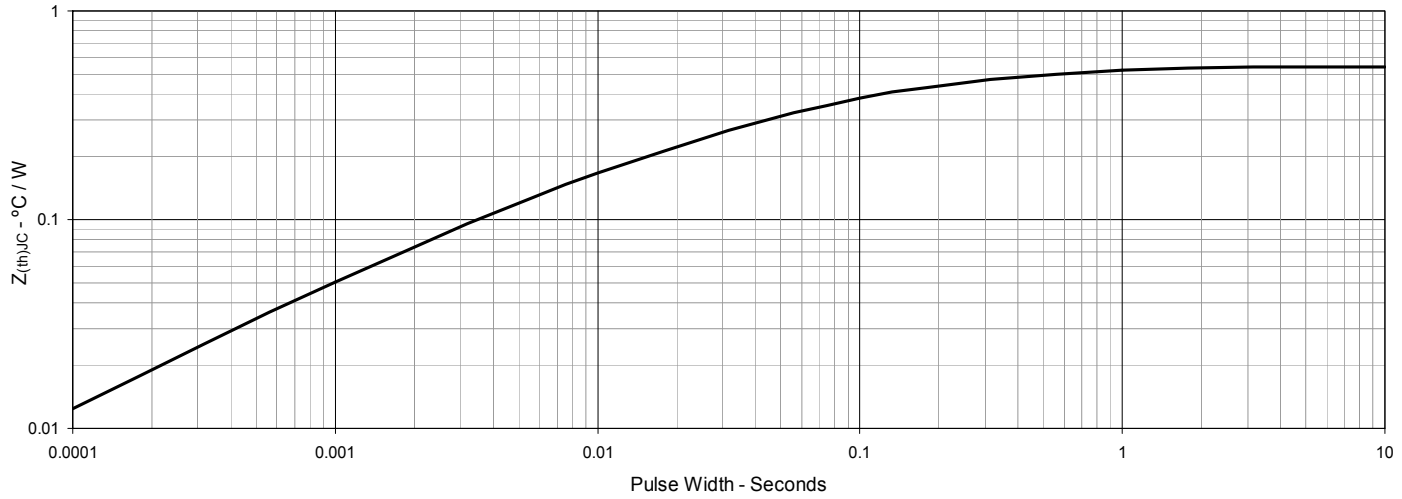


Fig. 11. Maximum Transient Thermal Impedance



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