IXYS

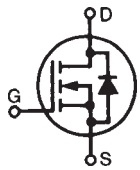
Standard Power MOSFET

IXTH 41N25

V_{DSS} = 250 V
$I_{D(cont)}$ = 41 A
$R_{DS(on)}$ = 72 mΩ

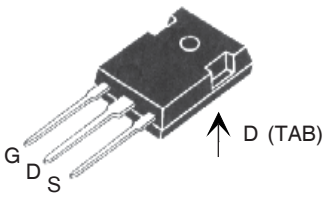
N-Channel Enhancement Mode

Preliminary Data Sheet



Symbol	Test conditions	Maximum ratings	
V_{DSS}	T_J = 25°C to 150°C	250	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1.0 MΩ	250	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C MOSFET chip capability	41	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	164	A
I_{AR}		41	A
E_{AR}	T_C = 25°C	30	mJ
E_{AS}	T_C = 25°C	1.0	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$ $T_J \le$ 150°C, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight	TO-264	6	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	250			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	2.0		4.0	V
I_{GSS}	V_{GS} = ±20 V DC, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V T_J = 125°C			25	μA
				250	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15A Pulse test, t ≤ 300 ms, duty cycle d ≤ 2%		60	72	mΩ

Features

- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- International standard package JEDEC TO-247 AD
- Fast switching times
- High commutating dv/dt rating

Applications

- Motor controls
- DC choppers
- Switched-mode and resonant-mode power supplies
- Uninterruptible Power Supplies (UPS)

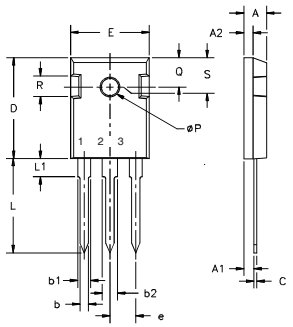
Advantages

- Easy to mount with one screw (isolated mounting screw hole)
- Space savings
- High power density

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Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	20	28		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3200		pF
C_{oss}			510		pF
C_{rss}			180		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25} R_G = 3.6 Ω (External)		19		ns
t_r			19		ns
$t_{d(off)}$			79		ns
t_f			17		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		110		nC
Q_{gs}			18		nC
Q_{gd}			48		nC
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

Source-Drain Diode **Ratings and Characteristics**

(T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	
I_S	V_{GS} = 0V			41	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			164	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 0.5 I_S, -di/dt = 100 A/µs, V_R = 100V		300		ns
Q_{rr}			3.0		µC

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:
4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

Fig. 1. Output Characteristics @ 25 Deg. C

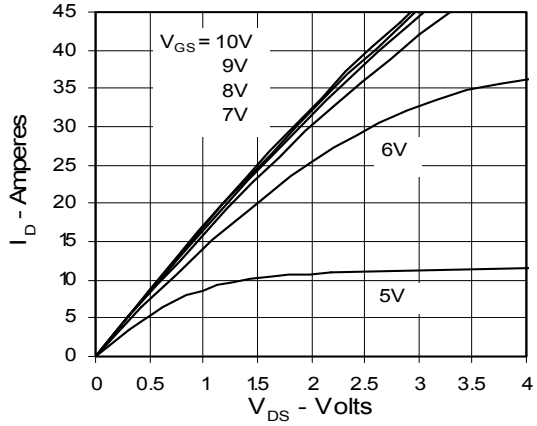


Fig. 2. Extended Output Characteristics @ 25 deg. C

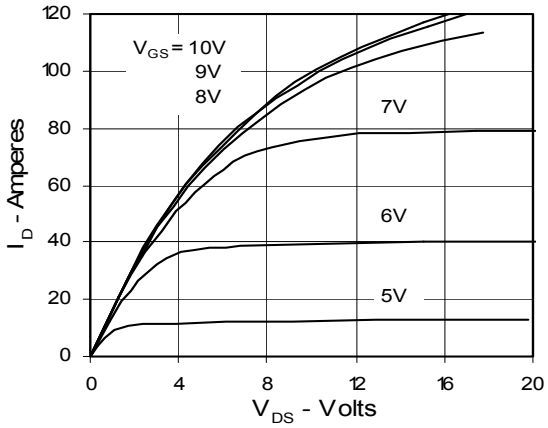


Fig. 3. Output Characteristics @ 125 Deg. C

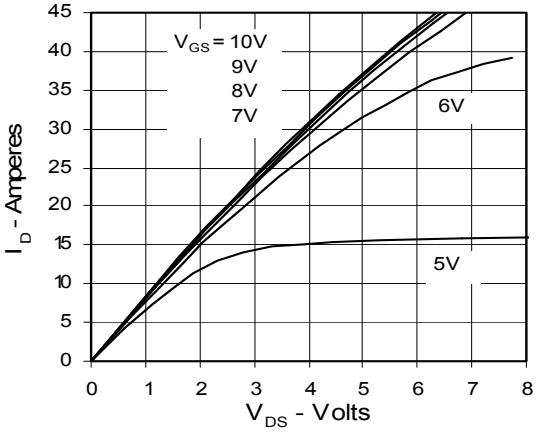


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

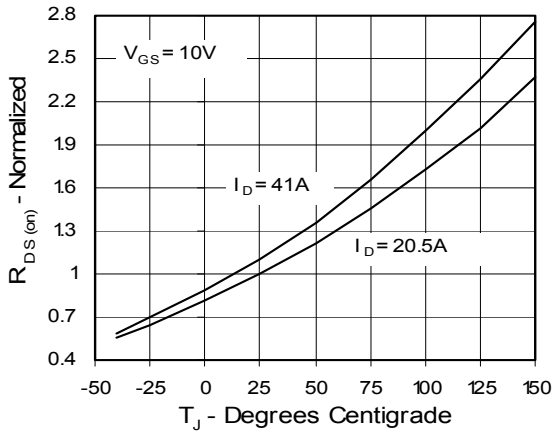


Fig. 5. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

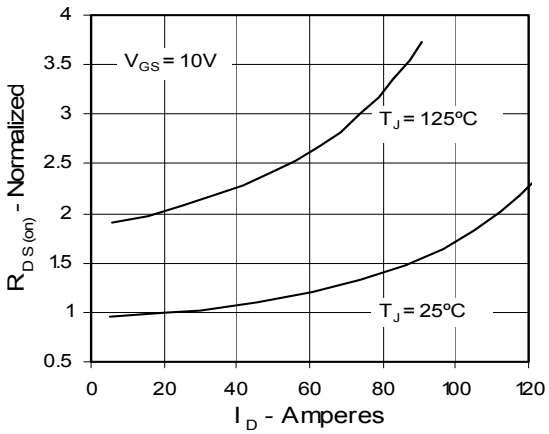
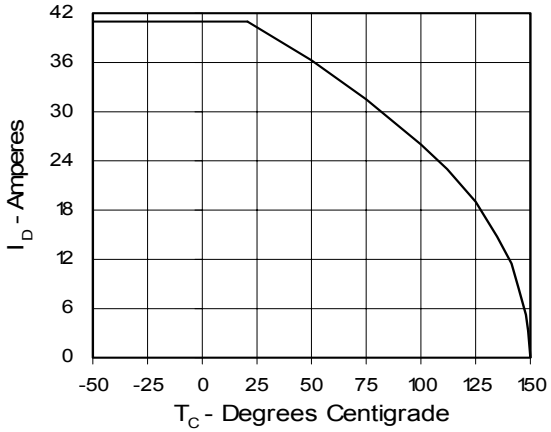


Fig. 6. Drain Current vs. Case Temperature



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Fig. 7. Input Admittance

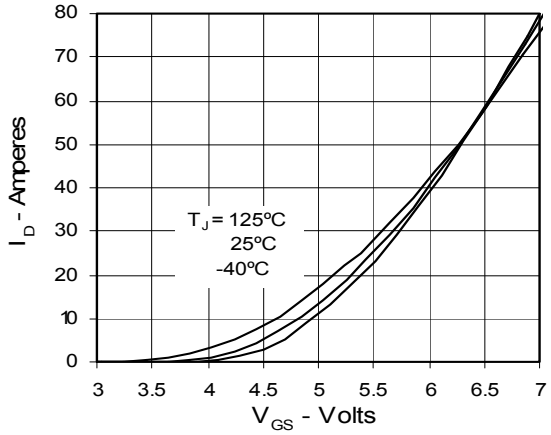


Fig. 8. Transconductance

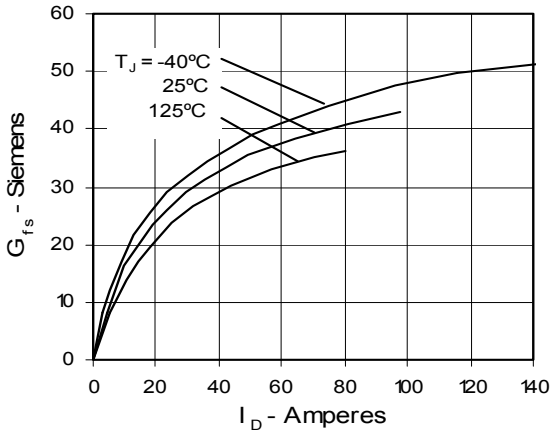


Fig. 9. Source Current vs. Source-To-Drain Voltage

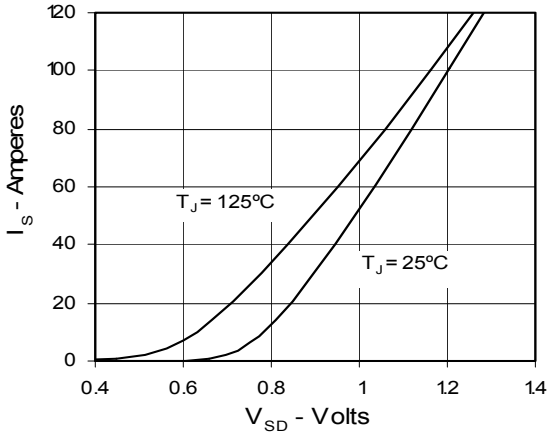


Fig. 10. Gate Charge

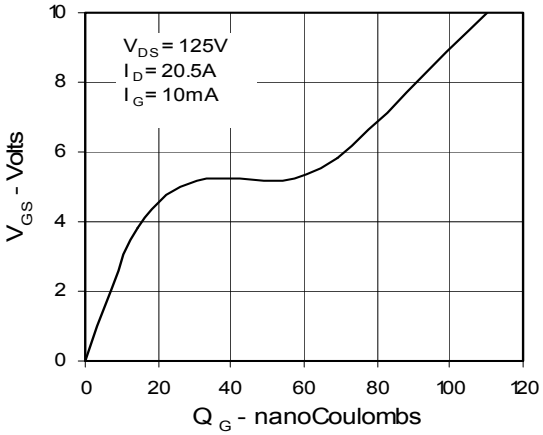


Fig. 11. Capacitance

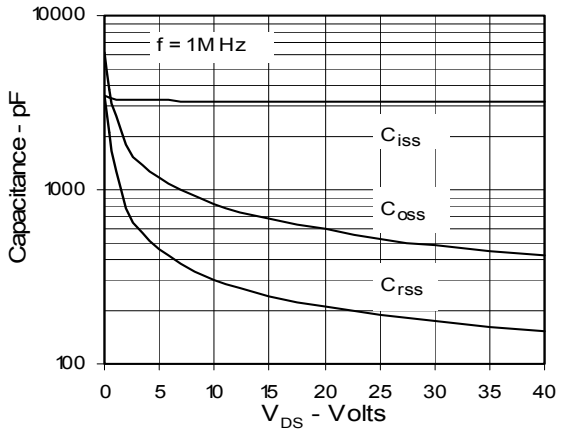
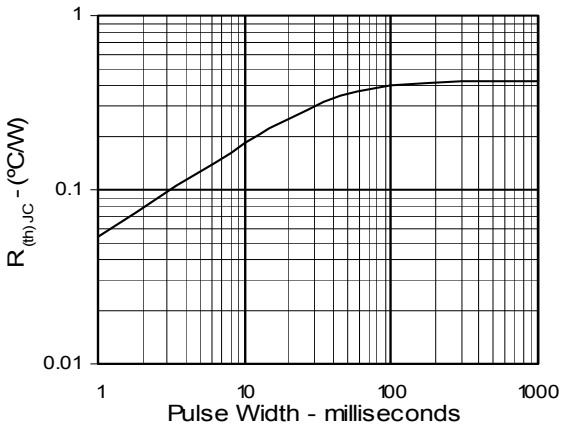


Fig. 12. Maximum Transient Thermal Resistance



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