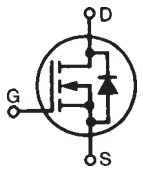
IXYS

High Voltage Power MOSFET

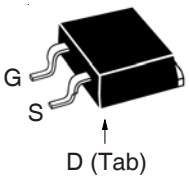
IXTA3N150HV

V_{DSS} = 1500V
I_{D25} = 3A
$R_{DS(on)}$ ≤ 7.3Ω

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



TO-263



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	1500	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	3	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	9	A
I_A	T_C = 25°C	3	A
E_{AS}	T_C = 25°C	250	mJ
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	5	V/ns
P_D	T_C = 25°C	250	W
T_J		- 55 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
Weight		2.5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA	1500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.5		5.0	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			10	μA
	T_J = 125°C			100	μA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			7.3	Ω

Features

- High Voltage package
- Fast Intrinsic Diode
- Avalanche Rated
- Molding Epoxies meet UL 94 V-0 Flammability Classification
- High Blocking Voltage

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits

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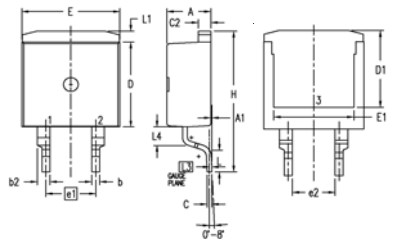
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	V_{DS} = 20V, I_D = 0.5 • I_{D25}, Note 1	2.2	3.6	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		1375	pF
C_{oss}			90	pF
C_{rss}			30	pF
$t_{d(on)}$	**Resistive Switching Times**		19	ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		21	ns
$t_{d(off)}$	R_G = 5Ω (External)		42	ns
t_f			25	ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		38.6	nC
Q_{gs}			6.5	nC
Q_{gd}			19.0	nC
R_{thJC}				0.50 °C/W

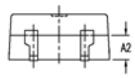
Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			3	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			12	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.3	V
t_{rr}	I_F = I_D = 0.5 • I_{D25}, -di/dt = 100A/μs		0.9		μs
I_{RM}	V_R = 100V, V_{GS} = 0V		15.0		A
Q_{RM}			6.7		μC

Note: 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

TO-263 (HV) Outline





PIN: 1 - Gate
2 - Source
3 - Drain

SYM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.054	1.18	1.38
C	.018	.024	0.45	0.60
C2	.049	.055	1.25	1.40
D	.354	.370	9.00	9.40
D1	.311	.327	7.90	8.30
E	.386	.402	9.80	10.20
E1	.307	.323	7.80	8.20
e1	.200 BSC		5.08 BSC	
(e2)	.163	.174	4.13	4.43
H	.591	.614	15.00	15.60
L	.079	.102	2.00	2.60
L1	.039	.055	1.00	1.40
L3	.010 BSC		0.254 BSC	
(L4)	.071	.087	1.80	2.20

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25°C

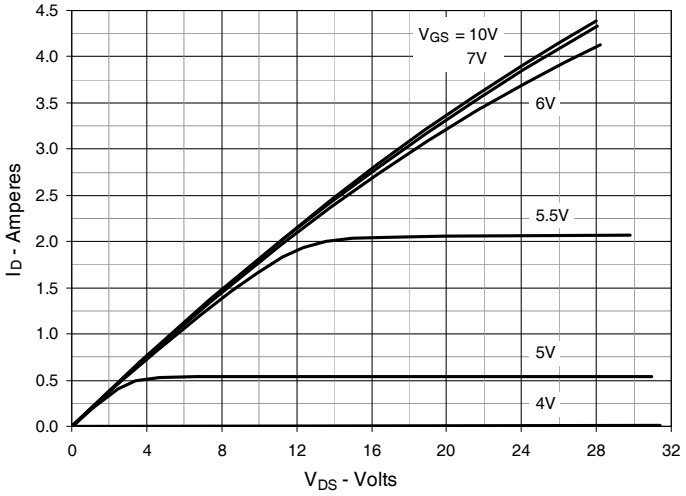


Fig. 2. Output Characteristics @ T_J = 125°C

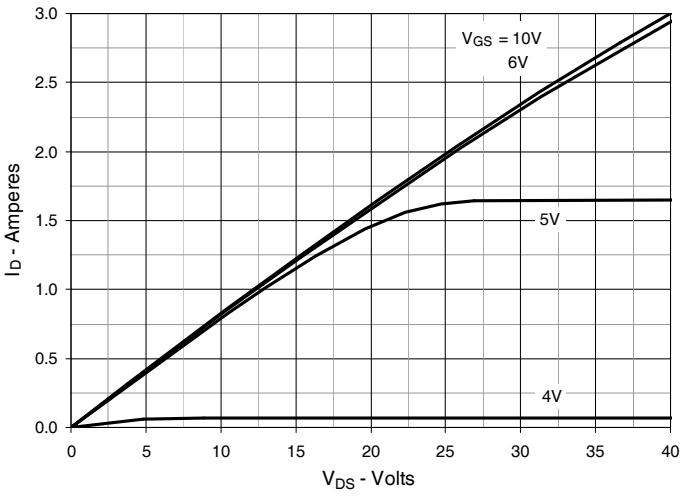


Fig. 3. $R_{DS(on)}$ Normalized to I_D = 1.5A Value vs. Junction Temperature

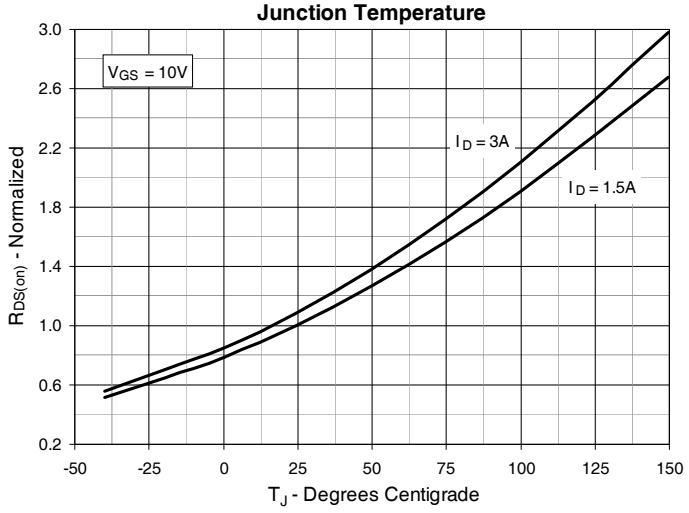


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 1.5A Value vs. Drain Current

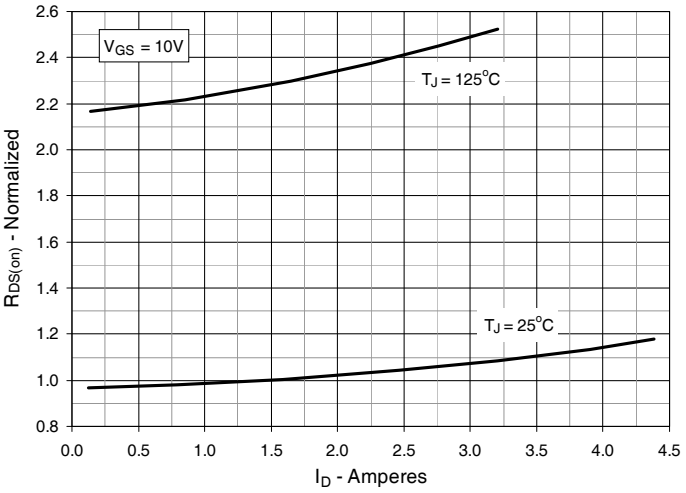


Fig. 5. Maximum Drain Current vs. Case Temperature

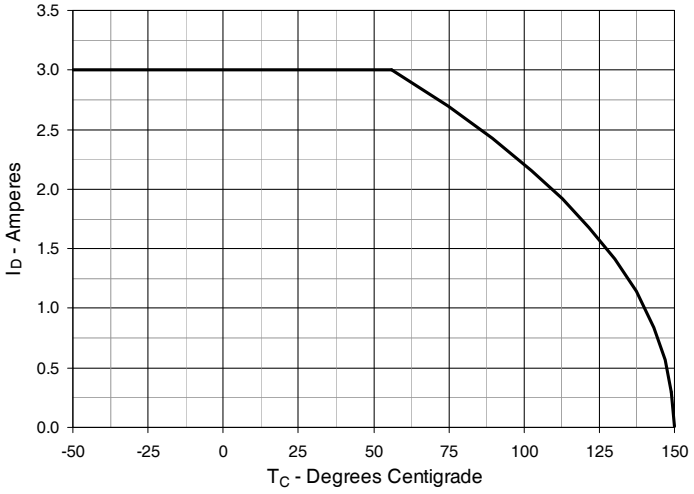
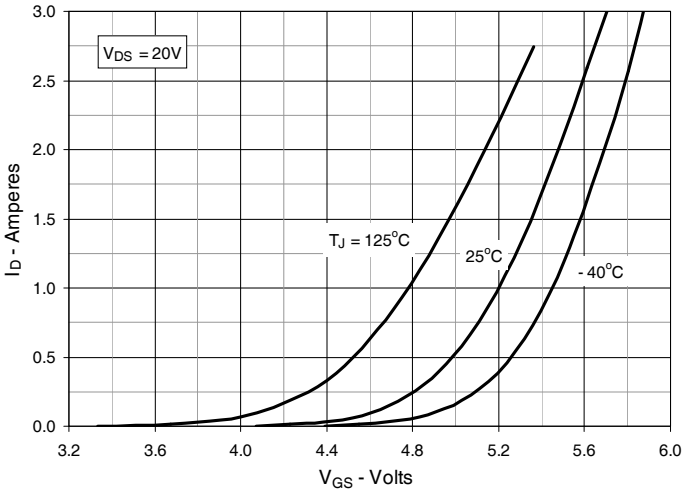


Fig. 6. Input Admittance



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Fig. 7. Transconductance

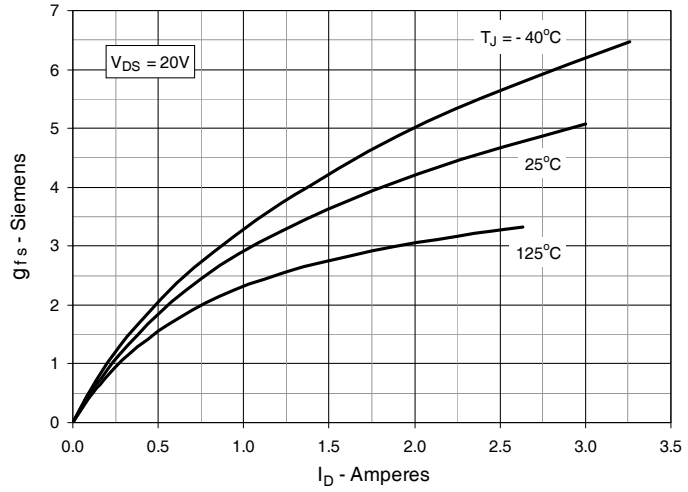


Fig. 8. Forward Voltage Drop of Intrinsic Diode

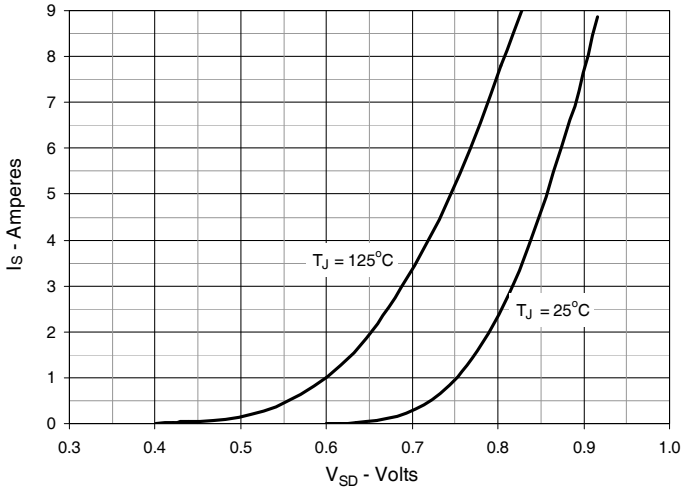


Fig. 9. Gate Charge

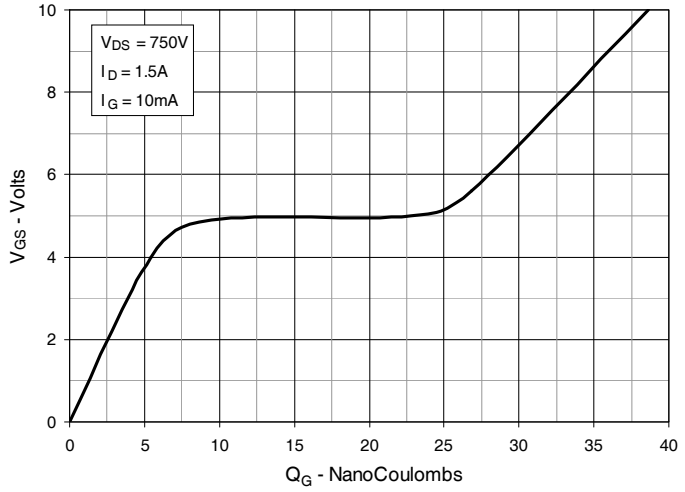


Fig. 10. Capacitance

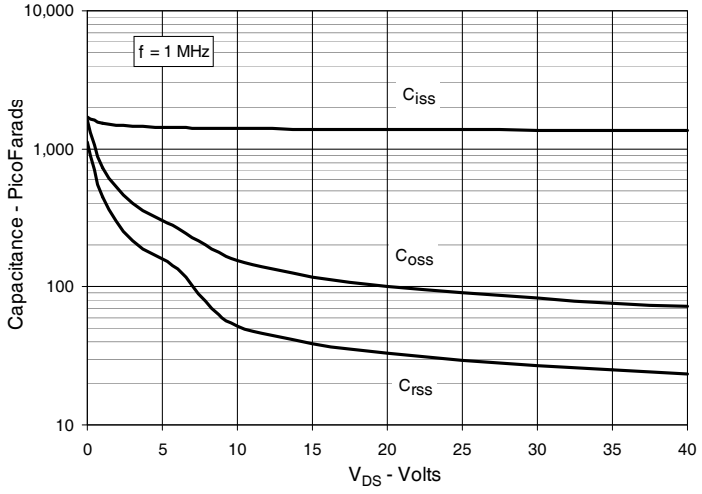


Fig. 11. Maximum Transient Thermal Impedance

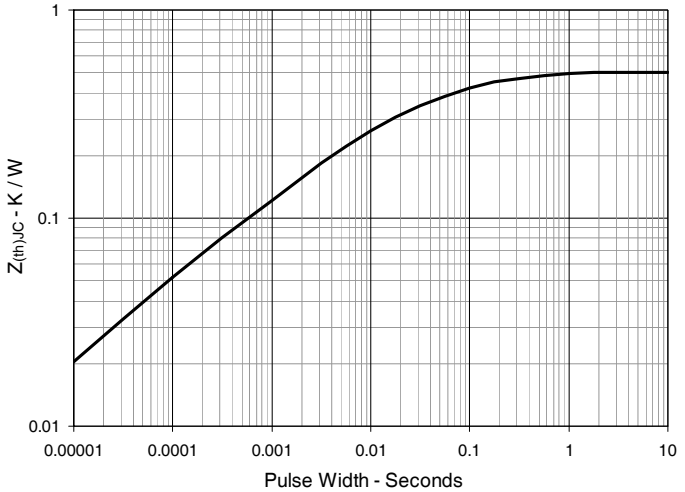
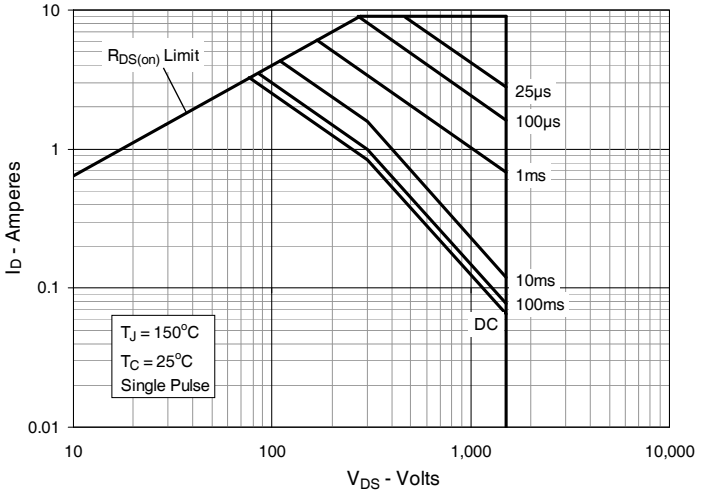


Fig. 12. Forward-Bias Safe Operating Area



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