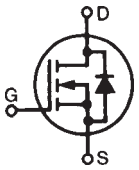
IXYS

X2-Class Power MOSFET

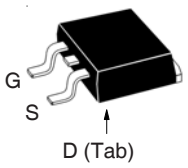
IXTA34N65X2

V_{DSS} = 650V
I_{D25} = 34A
$R_{DS(on)}$ ≤ 96mΩ

N-Channel Enhancement Mode
Avalanche Rated



TO-263



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	650	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	650	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	34	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	68	A
I_A	T_C = 25°C	17	A
E_{AS}	T_C = 25°C	1	J
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	540	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
dT/dt	Heating / Cooling rate, 175°C - 210°C	50	°C/min
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
F_C	Mounting Force	10..65 / 2.2..14.6	N/lb
Weight		2.5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	650			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.0		5.0	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			10	μA
	T_J = 125°C			150	μA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			96	mΩ

Features

- International Standard Package
- Low $R_{DS(ON)}$ and Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

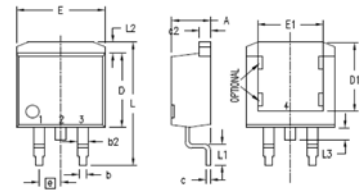
Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

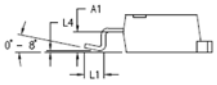
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Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
g_{fs}	V_{DS} = 10V, I_D = 0.5 • I_{D25}, Note 1	20	33		S
R_{Gi}	Gate Input Resistance		0.90		Ω
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		3000		pF
C_{oss}			2180		pF
C_{rss}			1.7		pF
	Effective Output Capacitance				
$C_{o(er)}$	Energy related; V_{GS} = 0V		125		pF
$C_{o(tr)}$	Time related; V_{DS} = 0.8 • V_{DSS}		490		pF
$t_{d(on)}$	**Resistive Switching Times**		30		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		48		ns
$t_{d(off)}$	R_G = 10Ω (External)		68		ns
t_f			30		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		54		nC
Q_{gs}			15		nC
Q_{gd}			20		nC
R_{thJC}				0.23	°C/W

TO-263 (IXTA) Outline



1 = Gate
2 = Drain
3 = Source
4 = Drain



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
I_S	V_{GS} = 0V			34	A
I_{SM}	Repetitive, pulse Width Limited by T_{JM}			136	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 17A, -di/dt = 100A/μs		390		ns
Q_{RM}	V_R = 100V		4.2		μC
I_{RM}			21.8		A

Note: 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123B1 6,306,728B1 6,404,065B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478B2 7,005,734B2 7,063,975B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25°C

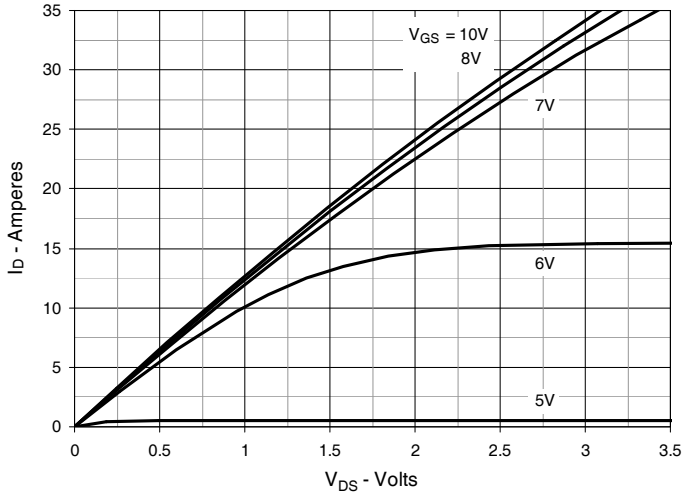


Fig. 2. Extended Output Characteristics @ T_J = 25°C

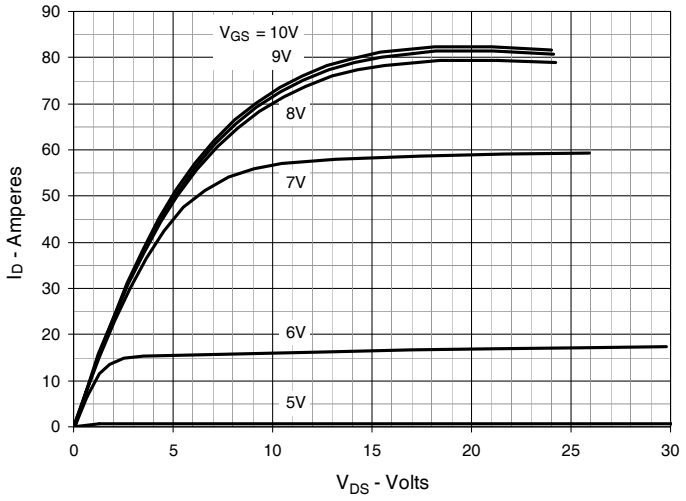


Fig. 3. Output Characteristics @ T_J = 125°C

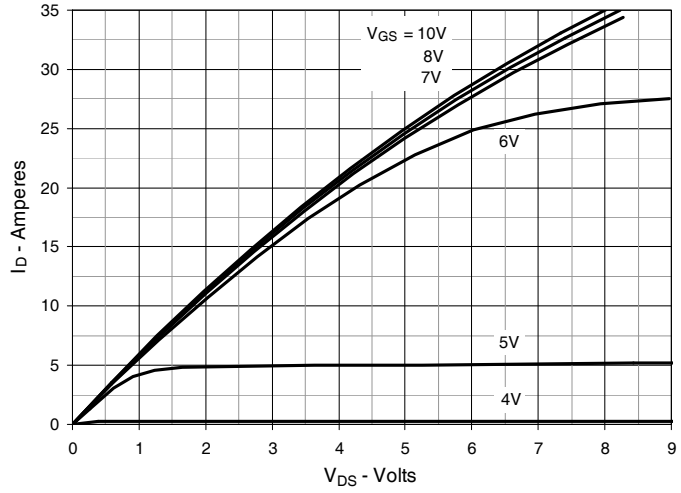


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 17A Value vs. Junction Temperature

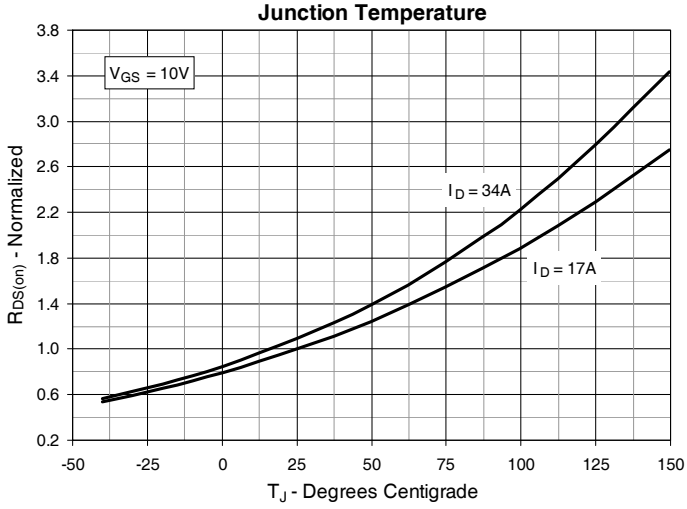


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 17A Value vs. Drain Current

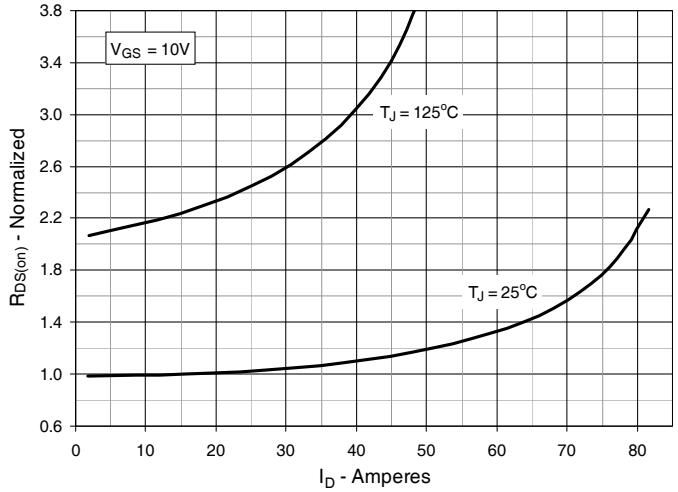
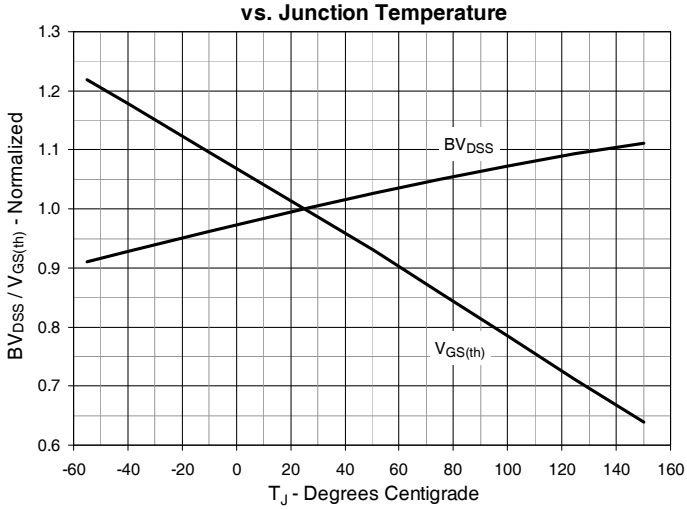


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature



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Fig. 7. Maximum Drain Current vs. Case Temperature

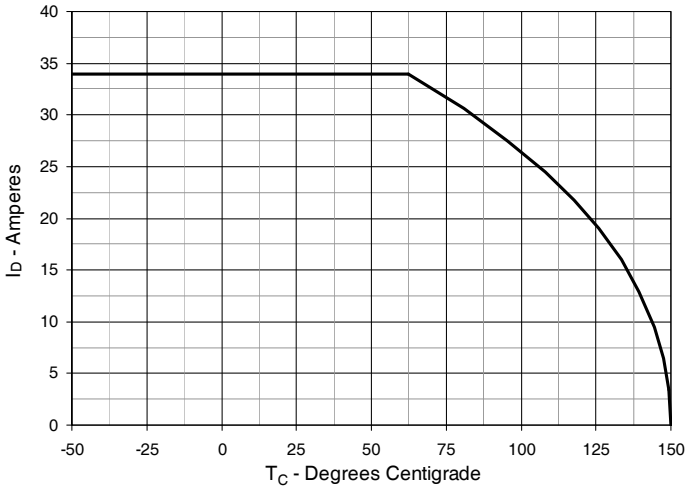


Fig. 8. Input Admittance

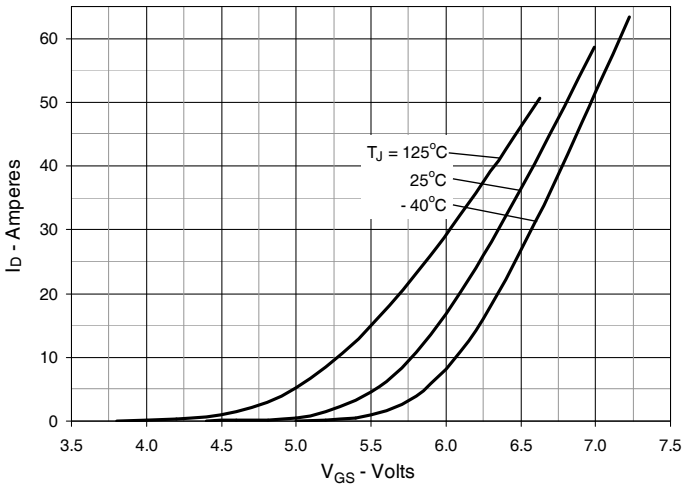


Fig. 9. Transconductance

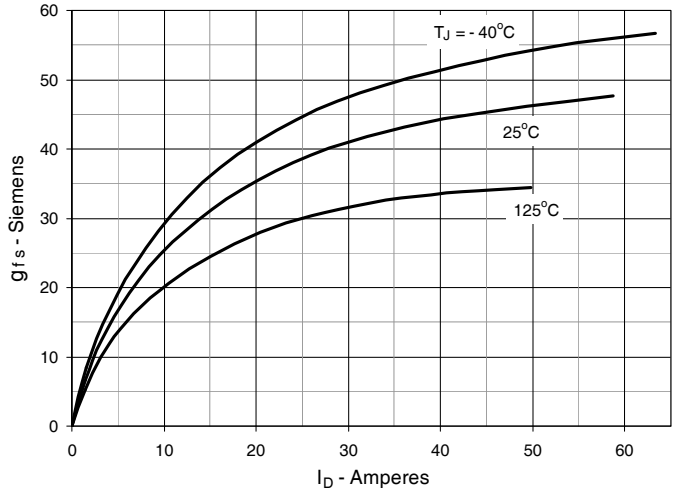


Fig. 10. Forward Voltage Drop of Intrinsic Diode

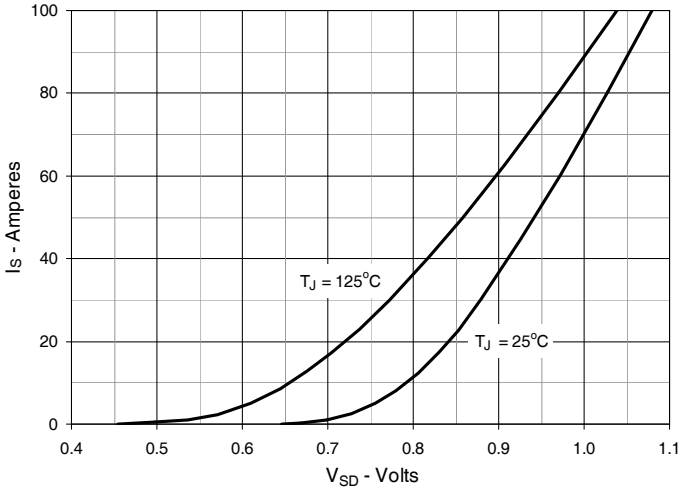


Fig. 11. Gate Charge

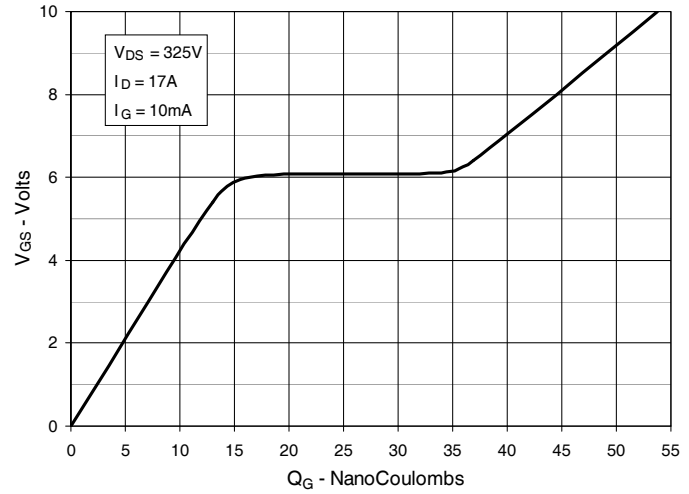
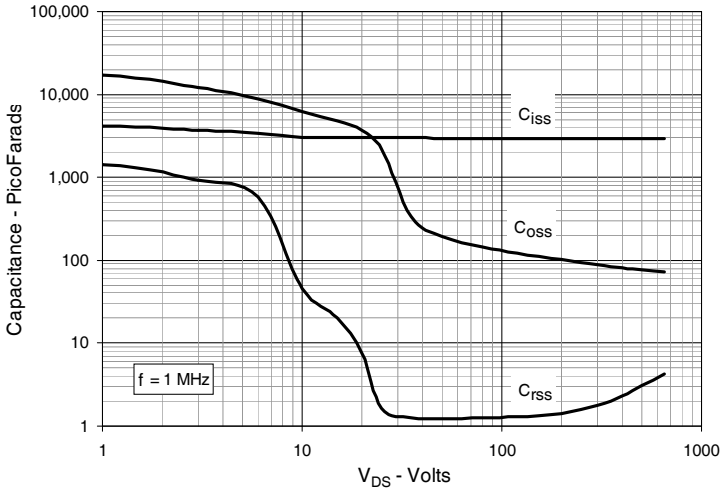


Fig. 12. Capacitance



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Fig. 13. Output Capacitance Stored Energy

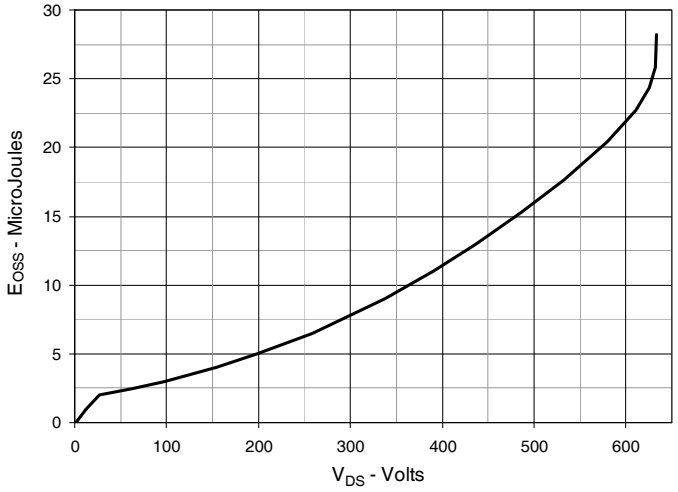


Fig. 14. Forward-Bias Safe Operating Area

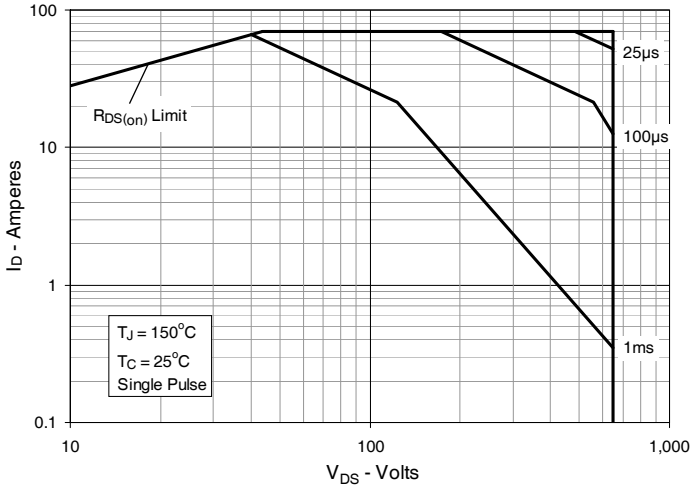
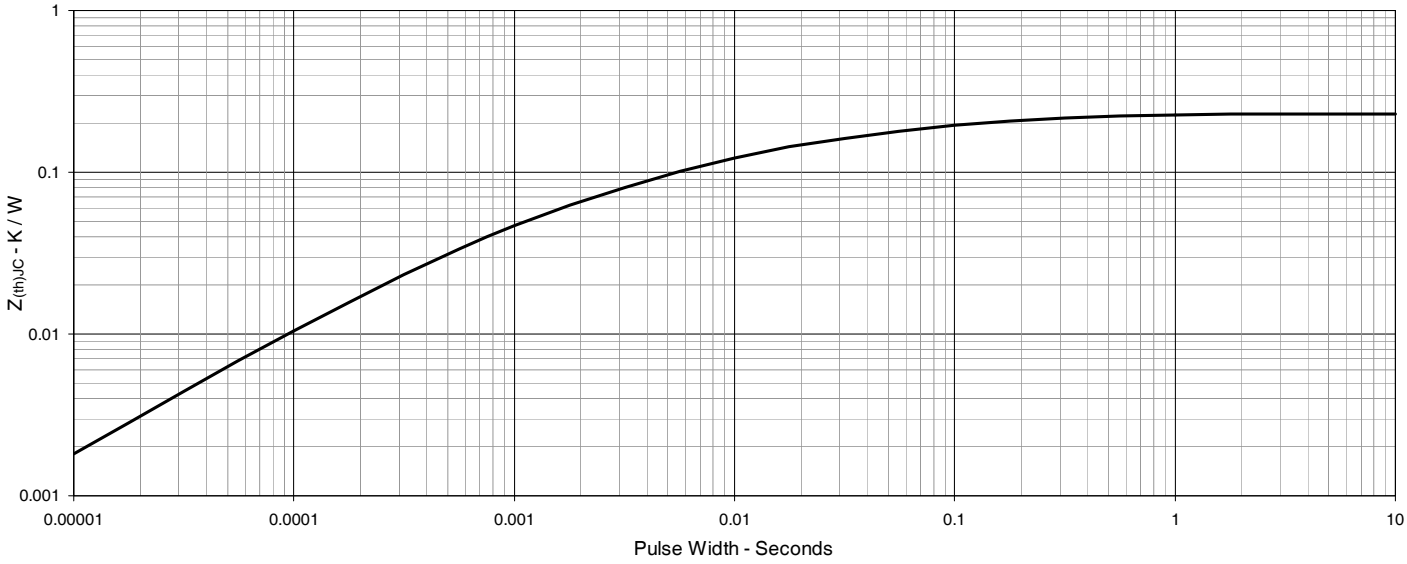


Fig. 15. Maximum Transient Thermal Impedance



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