IXYS

Low $V_{CE(sat)}$ IGBT with Diode

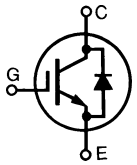
IXGR 60N60U1

ISOPLUS247™

(Electrically Isolated Back Surface)

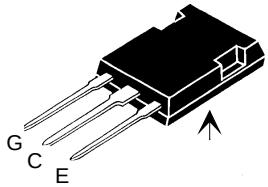
V_{CES} = 600 V
I_{C25} = 75 A
$V_{CE(sat)}$ = 1.7 V

Preliminary data



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	75	A
I_{C100}	T_C = 90°C	60	A
I_{CM}	T_C = 25°C, 1 ms	200	A
SSOA (RBSOA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 10 Ω Clamped inductive load; V_{CL} = 0.8 V_{CES}	I_{CM} = 100	A
P_C	T_C = 25°C	300	W
T_J		-55 ..+ 150	°C
T_{JM}		150	°C
T_{stg}		-55...+ 150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60Hz, RMS, t = 1minute, leads-to tab	2500	V
Weight		5	g

ISOPLUS247™



Isolated back surface*

G = Gate, C = Collector,
E = Emitter, TAB = Collector

* Patent pending

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{CES}	I_C = 1 mA, V_{GE} = 0 V		600			V
$V_{GE(th)}$	I_C = 250 μA, V_{CE} = V_{GE}		2.5		5.5	V
I_{CES}	V_{CE} = V_{CES}	T_J = 25°C			250	μA
	V_{GE} = 0 V	T_J = 150°C			2	mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	I_C = I_{C100}, V_{GE} = 15 V				1.7	V

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low collector to tab capacitance (<25pF)
- Rugged polysilicon gate cell structure
- Fast intrinsic Rectifier
- Low $V_{CE(sat)}$ IGBT and standard diode for minimum on-state conduction losses
- MOS Gate turn-on for drive simplicity

Applications

- Solid state relays
- Capacitor discharge circuits
- High power ignition circuits

Advantages

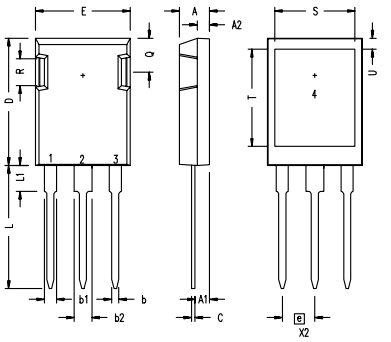
- Space savings (two devices in one package)
- Reduces assembly time and cost
- High power density

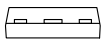
IXYS reserves the right to change limits, test conditions, and dimensions.

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Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	$I_C = I_{C100}$; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %	30	40		S
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		4000		pF
C_{oes}			340		pF
C_{res}			100		pF
Q_g	$I_C = I_{C100}$, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}		200		nC
Q_{ge}			35		nC
Q_{gc}			80		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		50		ns
t_{ri}	$I_C = I_{C100}$, V_{GE} = 15 V, L = 100 µH,		200		ns
$t_{d(off)}$	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 2.7 Ω		600	800	ns
t_{fi}	Remarks: Switching times may increase		500	700	ns
E_{off}	for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		16		mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		50		ns
t_{ri}	$I_C = I_{C100}$, V_{GE} = 15 V, L = 100 µH		240		ns
$t_{d(off)}$	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 2.7 Ω		1000		ns
t_{fi}	Remarks: Switching times may increase		1000		ns
E_{off}	for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		26		mJ
R_{thJC}				0.5	K/W
R_{thCK}			0.15		K/W

ISOPLUS 247 (IXGR) OUTLINE





1 Gate, 2 Drain (Collector)
3 Source (Emitter)
4 no connection

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190
S	13.21	13.72	.520	.540
T	15.75	16.26	.620	.640
U	1.65	3.03	.065	.080

Reverse Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_F	$I_F = I_{C100}$, V_{GE} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			2.2	V
R_{thJC}				1.0	K/W

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IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:
4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

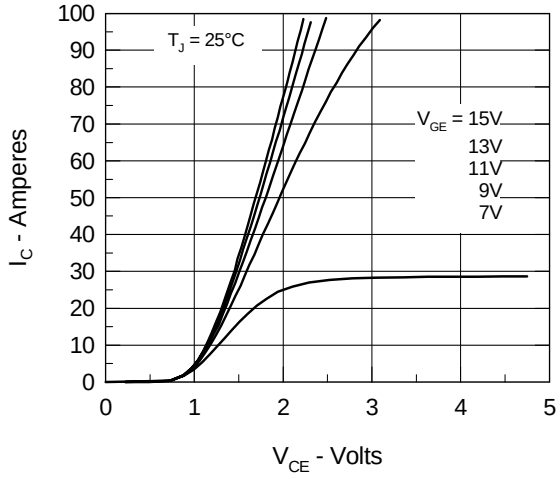


Figure 1. Saturation Voltage Characteristics

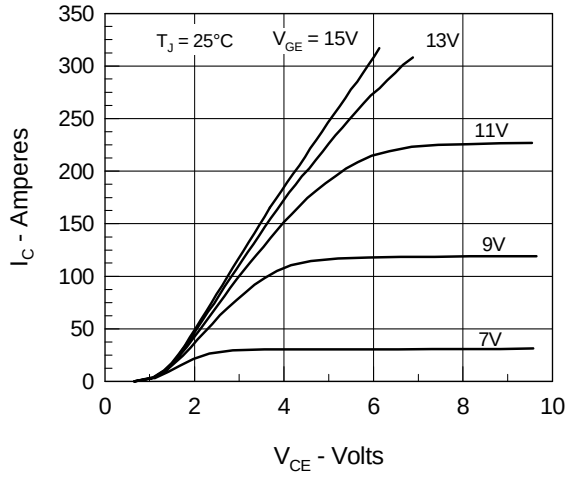


Figure 2. Extended Output Characteristics

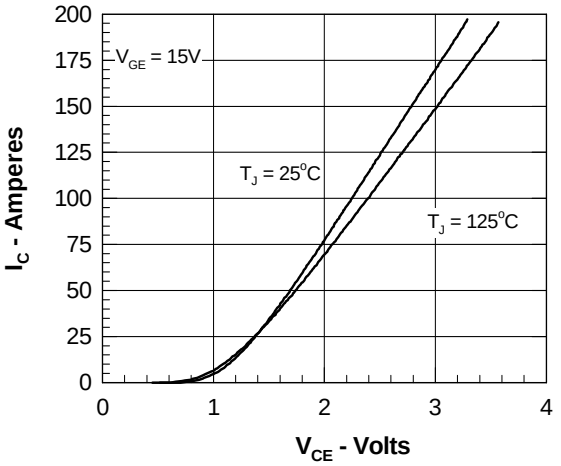


Figure 3. Saturation Voltage Characteristics

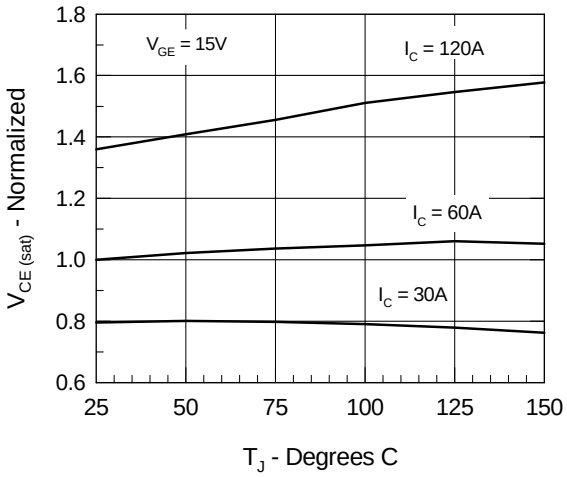


Figure 4. Temperature Dependence of $V_{CE(sat)}$

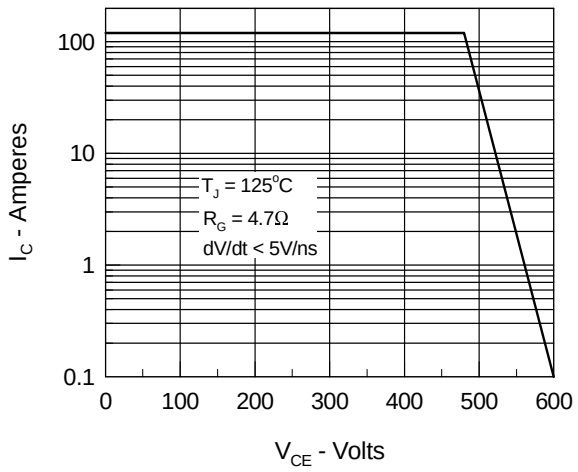


Figure 5. Admittance Curves

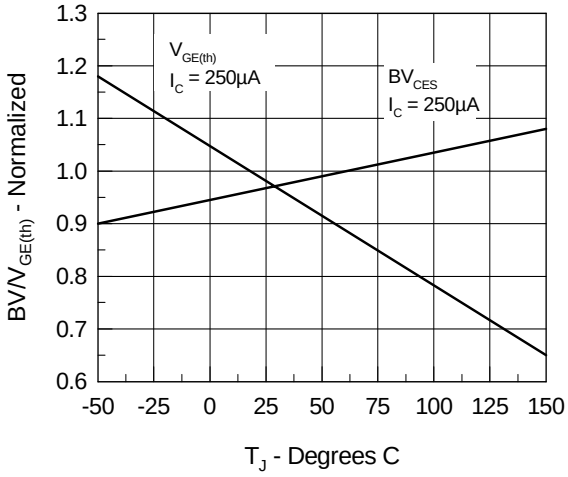


Figure 6. Capacitance Curves

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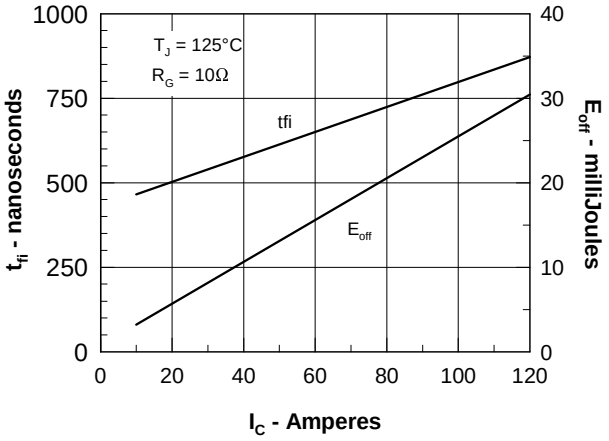


Figure 7. Dependence of E_{ON} and E_{OFF} on I_C.

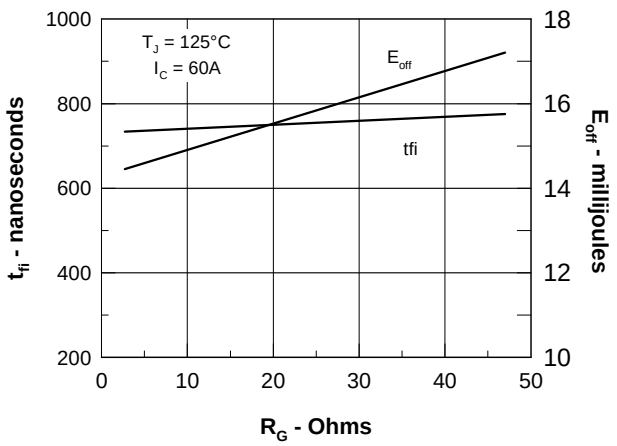


Figure 8. Dependence of E_{ON} and E_{OFF} on R_G.

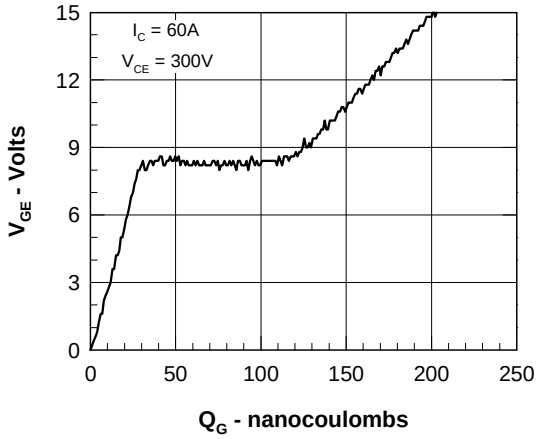


Figure 9. Gate Charge

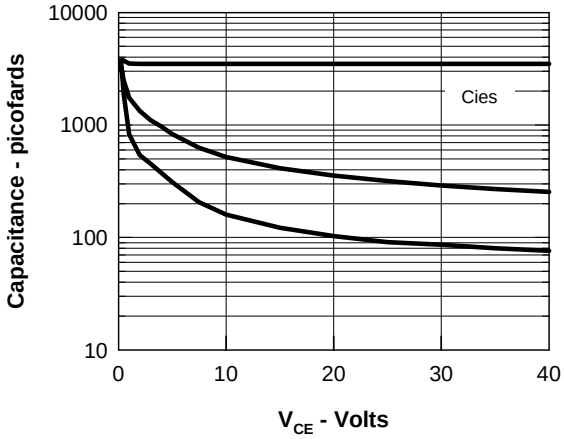


Figure 10. Turn-off Safe Operating Area

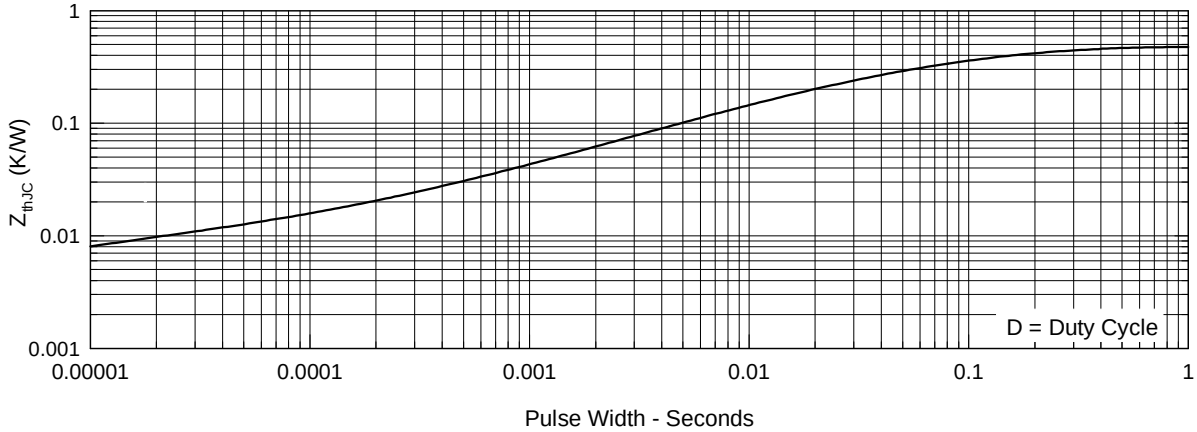


Figure 11. IGBT Transient Thermal Resistance

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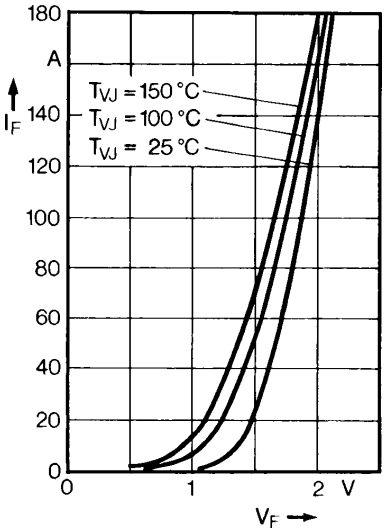


Fig. 12 Forward current versus voltage drop.

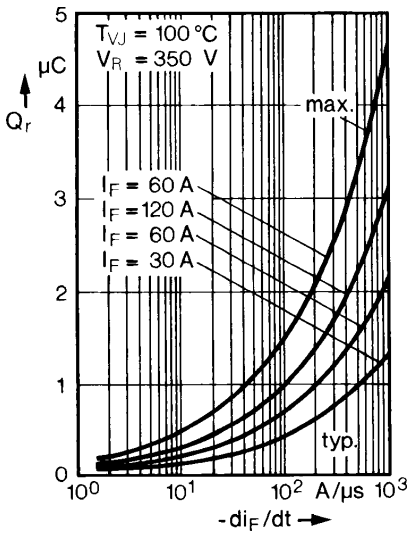


Fig. 13 Recovery charge versus $-di_F/dt$.

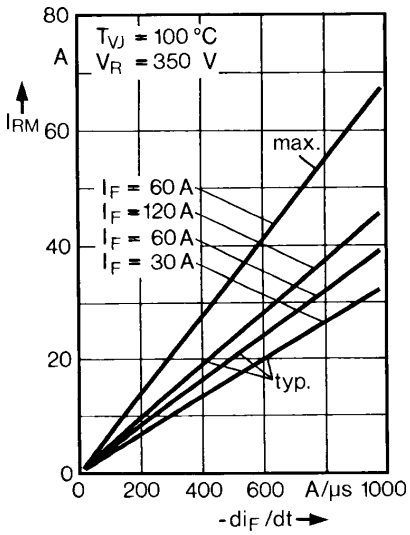


Fig. 14 Peak reverse current versus $-di_F/dt$.

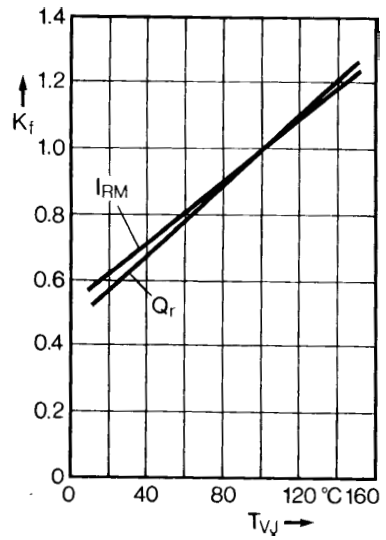


Fig. 15. Dynamic parameters versus junction temperature.

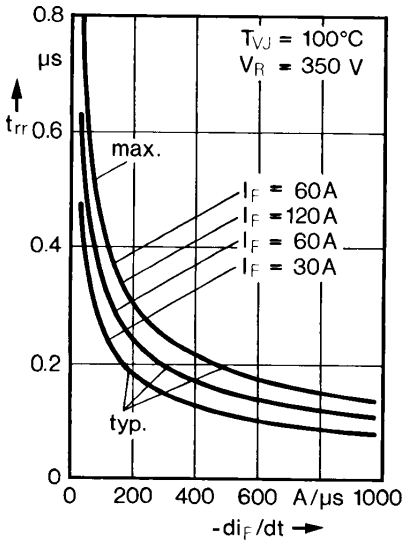


Fig. 16 Recovery time versus $-di_F/dt$.

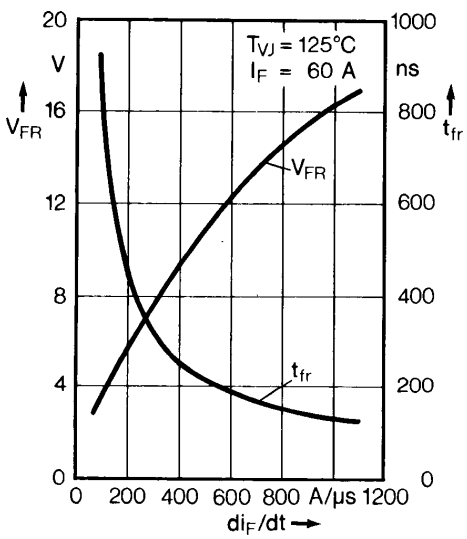


Fig. 17 Peak forward voltage vs. di_F/dt.

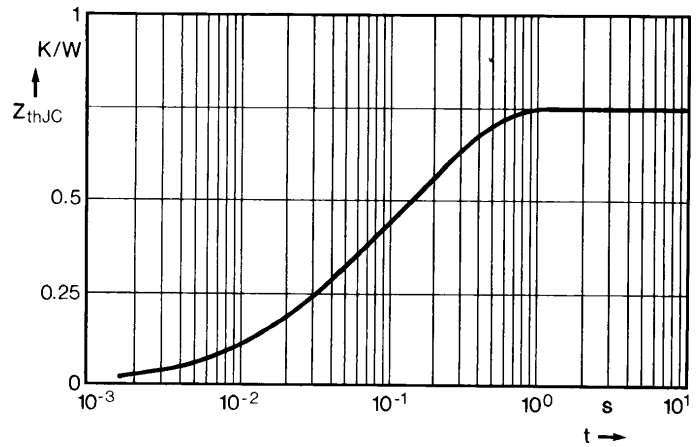


Fig. 18 Transient thermal impedance junction to case.

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