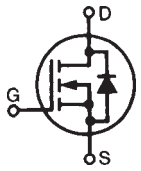
IXYS

Polar™ HiPerFET™ Power MOSFET

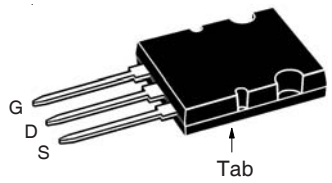
IXFB30N120P

V_{DSS} = 1200V
I_{D25} = 30A
$R_{DS(on)}$ ≤ 350mΩ
t_{rr} ≤ 300ns

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



PLUS264™



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1200	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	1200	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	30	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	75	A
I_A	T_C = 25°C	15	A
E_{AS}	T_C = 25°C	2.0	J
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	1250	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
F_C	Mounting Torque	30..120/6.7..27	N/lb.
Weight		10	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	1200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1mA	3.5		6.5	V
I_{GSS}	V_{GS} = ± 30V, V_{DS} = 0V			± 300	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			50	μA
	T_J = 125°C			5.0	mA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			350	mΩ

Features

- Fast Intrinsic Diode
- Avalanche Rated
- Low $R_{DS(ON)}$ and Q_G
- Low Package Inductance

Advantages

- Plus 264™ Package for Clip or Spring Mounting
- High Power Density
- Easy to Mount
- Space Savings

Applications

- High Voltage Switch-Mode and Resonant-Mode Power Supplies
- High Voltage Pulse Power Applications
- High Voltage Discharge Circuits in Laser Pulsers
  Spark Igniters, RF Generators
- High Voltage DC-DC Coverters
- High Voltage DC-AC Inverters

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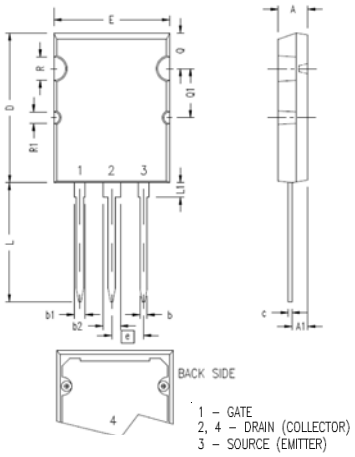
Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20V, I_D = 0.5 • I_{D25}, Note 1	13	22		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		22.5		nF
C_{oss}			950		pF
C_{rss}			28		pF
R_{Gi}	Gate Input Resistance		1.64		Ω
$t_{d(on)}$	**Resistive Switching Times** V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 1Ω (External)		57		ns
t_r			60		ns
$t_{d(off)}$			95		ns
t_f			56		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		310		nC
Q_{gs}			104		nC
Q_{gd}			137		nC
R_{thJC}				0.10	°C/W
R_{thCS}			0.13		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			30	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			120	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.5	V
t_{rr}	I_F = 0.5 • I_{D25}, V_{GS} = 0V -di/dt = 100A/μs V_R = 100V			300	ns
Q_{RM}			1.6		μC
I_{RM}			14		A

Note 1: Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PLUS264™ (IXFB) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = @ 25ºC

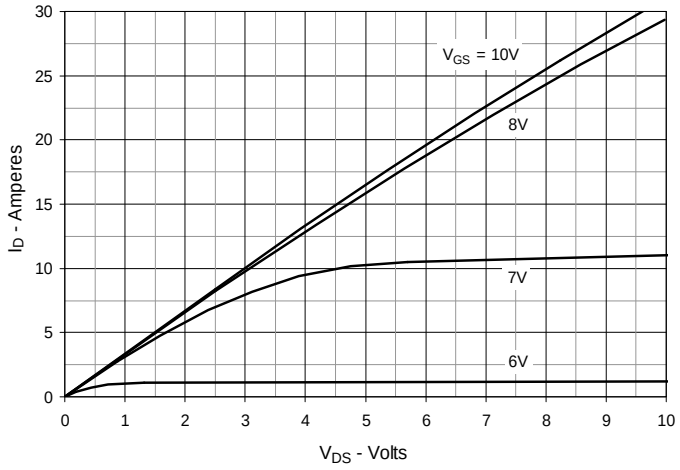


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

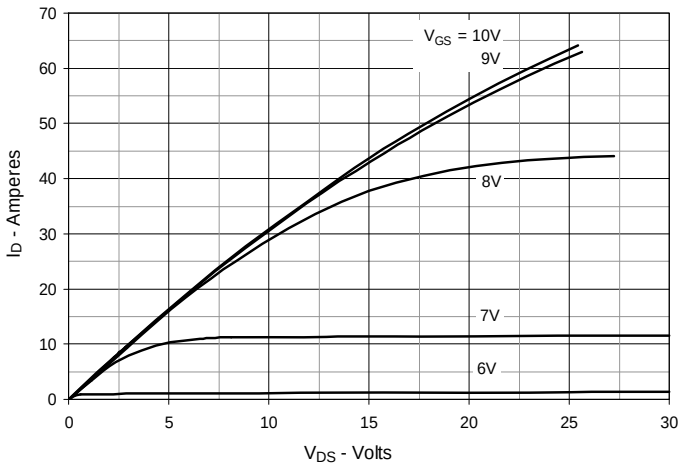


Fig. 3. Output Characteristics @ T_J = 125ºC

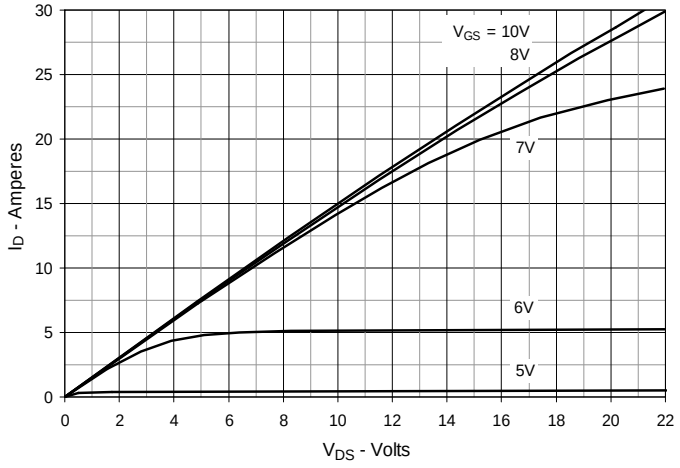


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 15A Value vs. Junction Temperature

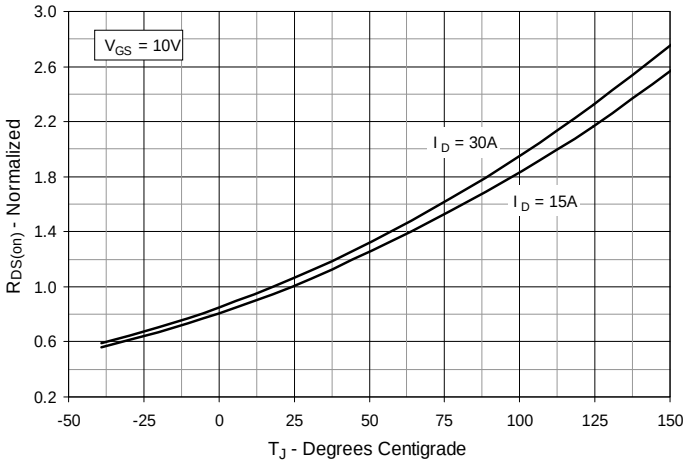


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 15A Value vs. Drain Current

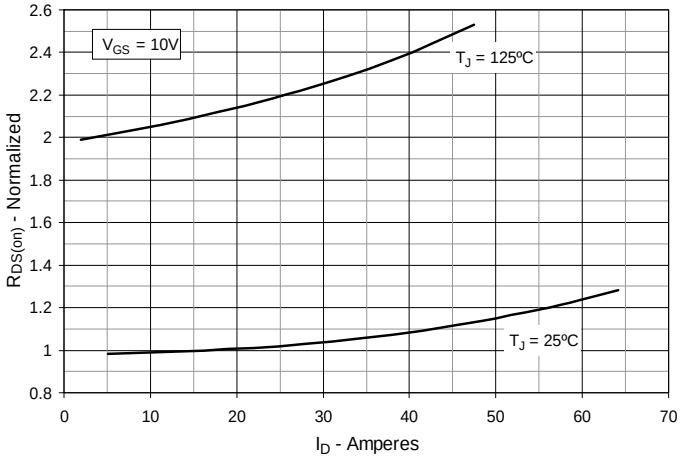
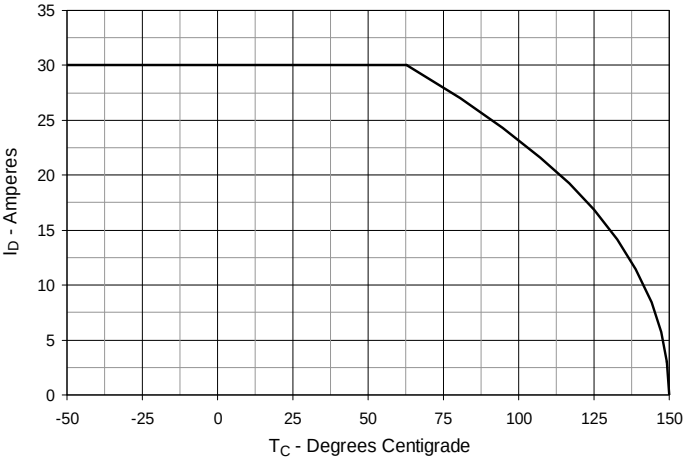


Fig. 6. Maximum Drain Current vs. Case Temperature



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Fig. 7. Input Admittance

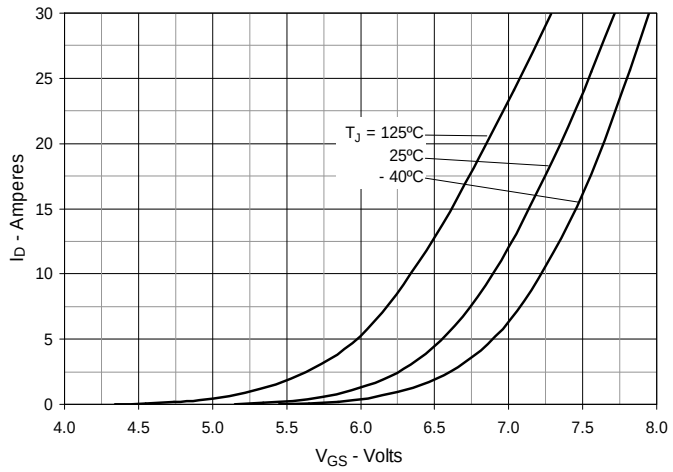


Fig. 8. Transconductance

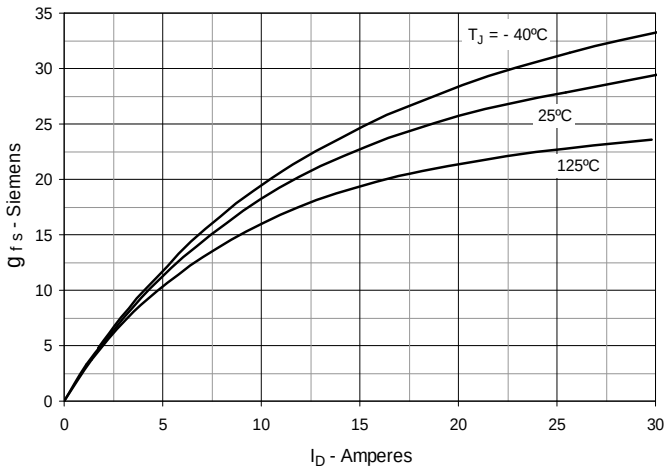


Fig. 9. Forward Voltage Drop of Intrinsic Diode

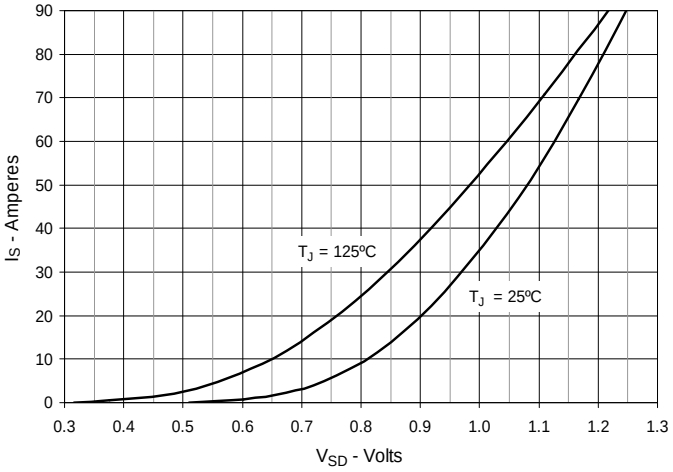


Fig. 10. Gate Charge

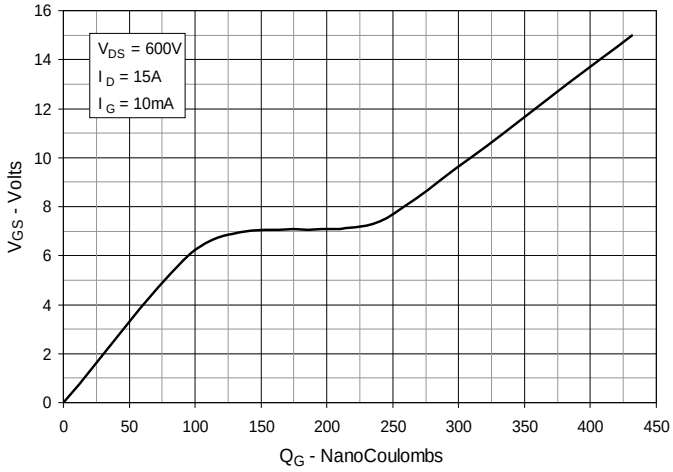


Fig. 11. Capacitance

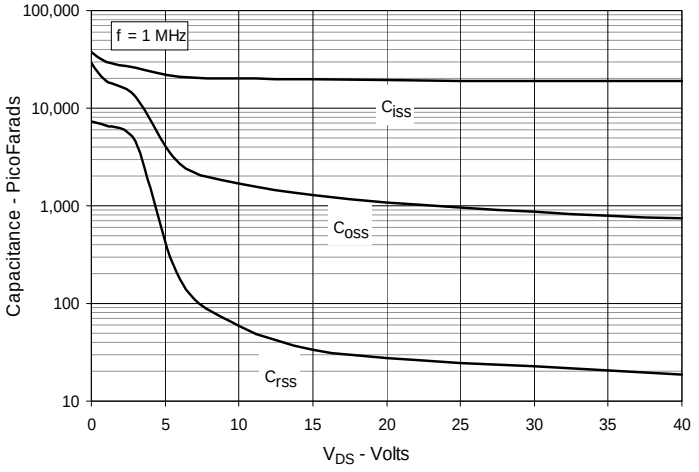
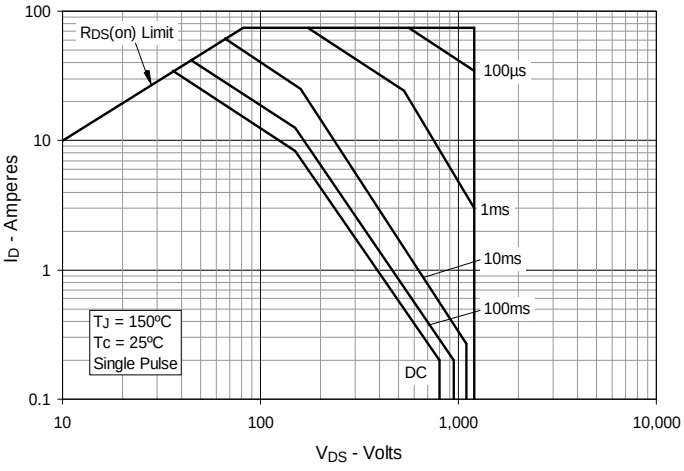
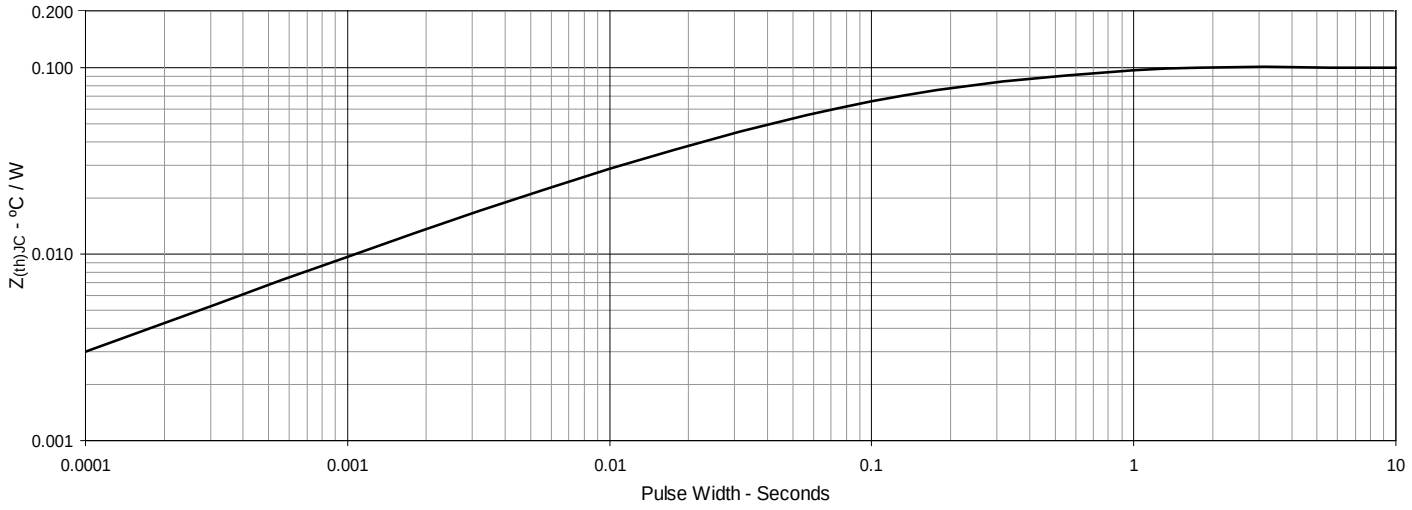


Fig. 12. Forward-Bias Safe Operating Area



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Fig. 13. Maximum Transient Thermal Impedance



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