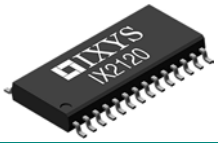
IX2120
1200V High and Low Side Gate Driver

IXYS INTEGRATED CIRCUITS DIVISION



Driver Characteristics

Parameter	Rating	Units
V_{OFFSET}	1200	V
$I_{O +/-}$ (Source/Sink)	2/2	A
V_{OUT}	15-20	V
t_{on}/t_{off}	250/210	ns

Features

- Floating Channel for Bootstrap Operation to +1200V
- Outputs Capable of Sourcing and Sinking 2A
- Gate Drive Supply Range From 15V to 20V
- Enhanced Robustness due to SOI Process
- Tolerant to Negative Voltage Transients: dV/dt Immune
- 3.3V Logic Compatible
- Undervoltage Lockout for Both High-Side and Low-Side Outputs

Description

The IX2120 is a high voltage integrated circuit that can drive high speed MOSFETs and IGBTs that operate at up to +1200V. The IX2120 is configured with independent high-side and low-side referenced output channels, both of which can source and sink 2A. The floating high-side channel can drive an N-channel power MOSFET or IGBT 1200V from the common reference.

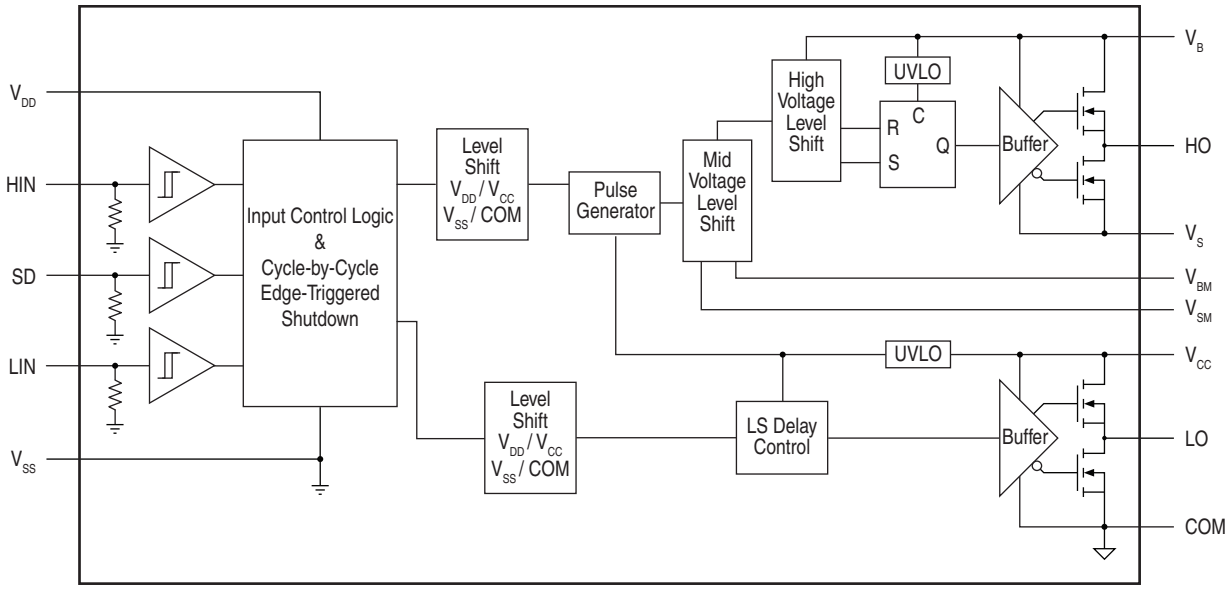
Manufactured on IXYS Integrated Circuits Division's proprietary high-voltage BCDMOS on SOI (silicon on insulator) process, the IX2120 is extremely robust, and is virtually immune to negative transients. The UVLO circuit prevents turn-on of the MOSFET or IGBT until there is sufficient V_{BS} or V_{CC} supply voltage.

The IX2120 is available in a 28-pin SOIC package.

Ordering Information

Part	Description
IX2120B	28-Pin SOIC (28/Tube)
IX2120BTR	28-Pin SOIC (1000/Reel)

IX2120 Functional Block Diagram



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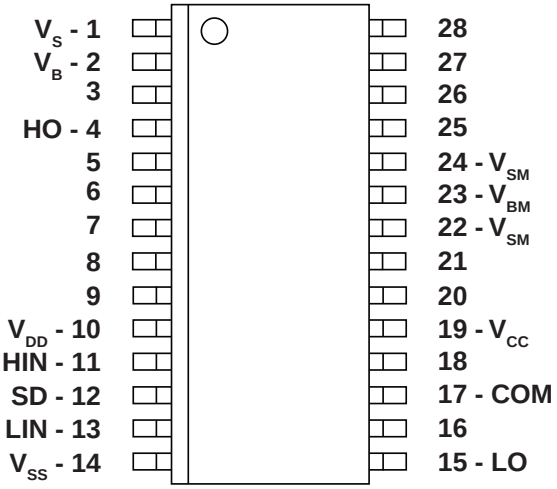
1 Specifications

Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

1.1 Package Pinout: 28-Pin SOIC Package



1.2 Pin Description: 28-Pin SOIC Package

Pin#	Name	Description
1	V_S	High-Side Floating Supply Return
2	V_B	High-Side Floating Supply
3	-	No Connection
4	HO	High-Side Gate Drive Output
5	-	No Connection
6	-	No Connection
7	-	Internal Connection, Do Not Use
8	-	No Connection
9	-	Internal Connection, Do Not Use
10	V_{DD}	Logic Supply
11	HIN	Logic Input for High-Side Gate Drive Output (HO), In-Phase
12	SD	Logic Input for Shutdown
13	LIN	Logic Input for Low-Side Gate Driver Output (LO), In-Phase
14	V_{SS}	Logic Ground
15	LO	Low-Side Gate Drive Output
16	-	No Connection
17	COM	Low-Side Return
18	-	No Connection
19	V_{CC}	Low-Side Supply
20	-	Internal Connection, Do Not Use
21	-	No Connection
22	V_{SM}	Middle Floating Return
23	V_{BM}	Middle Floating Supply
24	V_{SM}	Middle Floating Return
25	-	No Connection
26	-	No Connection
27	-	No Connection
28	-	No Connection

1.3 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min	Max	Units
High-Side Floating Supply Voltage	V_B	-0.3	1400	V
High-Side Floating Supply Offset Voltage	V_S	V_B-20	V_B+0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Middle Floating Supply Voltage	V_{BM}	-0.3	700	V
Middle Floating Supply Offset Voltage	V_{SM}	V_{BM}-20	V_{BM}+0.3	V
Low-Side Fixed Supply Voltage	V_{CC}	-0.3	20	V
Low-Side Output Voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Logic Supply Voltage	V_{DD}	-0.3	V_{SS}+20	V
Logic Supply Offset Voltage	V_{SS}	V_{CC}-20	V_{CC}+0.3	V
Logic Input Voltage (HIN, LIN, SD)	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Allowable Offset Supply Voltage Transient	dV_S/dt	-	50	V/ns
Package Power Dissipation @25°C	P_D	-	1.3	W
Junction Temperature	T_J	-40	+150	°C
Storage Temperature	T_S	-55	+150	°C

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Impedance, Junction to Ambient	Θ_{JA}	74	°C/W

1.5 Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. The V_S, V_{SM}, and V_{SS} offset ratings are tested with all supplies biased at a 15V differential.

Parameter	Symbol	Min	Max	Units
High-Side Floating Supply Absolute Voltage	V_B	V_S+15	V_S+20	V
High-Side Floating Supply Offset Voltage	V_S	-	1200	
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	
Middle Floating Supply Absolute Voltage	V_{BM}	V_{SM}+15	V_{SM}+20	
Middle Floating Supply Offset Voltage	V_{SM}	-	600	
Low-Side Fixed Supply Voltage	V_{CC}	15	20	
Low-Side Output Voltage	V_{LO}	0	V_{CC}	
Logic Supply Voltage	V_{DD}	V_{SS}+3	V_{SS}+20	
Logic Supply Offset Voltage	V_{SS}	-5	+5	
Logic Input Voltage (HIN, LIN, SD)	V_{IN}	V_{SS}	V_{DD}	

1.6 Dynamic Electrical Characteristics

V_{CC}, V_{DD}=15V; V_{BS}, V_{BMSM}=13.5V; C_L=1000 pF; and V_{SS}=COM unless otherwise specified. See **"Test Waveforms" on page 6**.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Turn-On propagation Delay	V_S=0V	t_{on}	-	254	-	ns
Turn-Off propagation Delay	V_{SM}=600V, V_S=1200V	t_{off}	-	213	-	
Shutdown propagation Delay		t_{SD}	-	207	-	
Turn-On Rise Time	-	t_r	-	9.4	-	
Turn-Off Fall Time	-	t_f	-	9.7	-	
Delay Matching, HS & LS Turn-On/Off	-	MT	-	-	60	

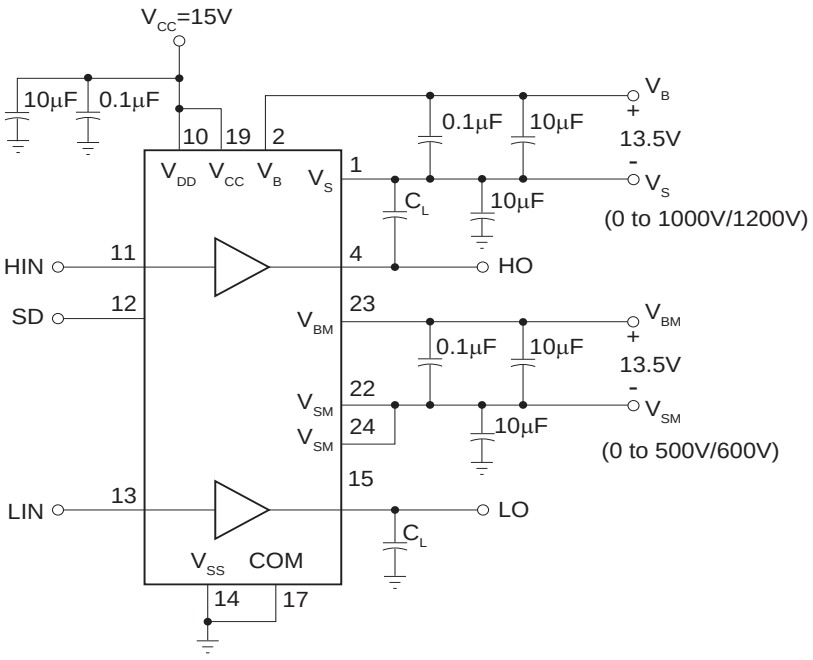
1.7 Static Electrical Characteristics

V_{CC}, V_{BMSM}, V_{BS}, V_{DD}=15V, and V_{SS}=COM unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

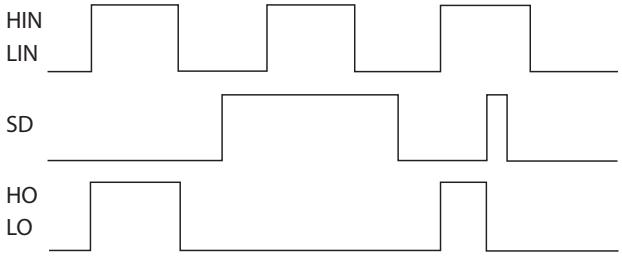
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Logic "1" Input Voltage	V_{DD}=15V	V_{IH}	9.5	-	-	V
Logic "0" Input Voltage		V_{IL}	-	-	6	
Logic "1" Input Voltage	V_{DD}=3V	V_{IH}	2.5	-	-	V
Logic "0" Input Voltage		V_{IL}	-	-	0.8	
High-Level Output Voltage, V_{BIAS}-V_O	I_O=0A	V_{OH}	-	1.6	2.5	V
Low-Level Output Voltage, V_O	I_O=20mA	V_{OL}	-	-	0.15	
High Offset Supply Leakage Current	V_B=V_S=600V	I_{HLK}	-	32	60	µA
Middle Offset Supply Leakage Current	V_{BM}=V_{SM}=600V	I_{MLK}	-	32	60	
Quiescent V_{BS} Supply Current	V_{IN}=0V or V_{DD}	I_{QBS}	-	187	310	
Quiescent V_{BMSM} Supply Current	V_{IN}=0V or V_{DD}	I_{QBMSM}	-	487	730	
Quiescent V_{CC} Supply Current	V_{IN}=0V or V_{DD}	I_{QCC}	-	300	420	
Quiescent V_{DD} Supply Current	V_{IN}=0V or V_{DD}	I_{QDD}	-	-	1	
Logic "1" Input Bias Current	V_{IN}=V_{DD}	I_{IN+}	-	22	40	µA
Logic "0" Input Bias Current	V_{IN}=0V	I_{IN-}	-	-	5	
V_{BS} Supply Undervoltage Positive Going Threshold	-	V_{BSUV+}	7.5	8.4	9.7	V
V_{BS} Supply Undervoltage Negative Going Threshold	-	V_{BSUV-}	7	7.8	9.4	
V_{CC} Supply Undervoltage Positive Going Threshold	-	V_{CCUV+}	7.4	8.4	9.6	
V_{CC} Supply Undervoltage Negative Going Threshold	-	V_{CCUV-}	7	7.8	9.4	
Output High Short Circuit Pulsed Current	V_O=0V, V_{IN}=V_{DD} , PW≤10µs	I_{O+}	2	-	-	A
Output Low Short Circuit Pulsed Current	V_O=15V, V_{IN}=0V, PW≤10µs	I_{O-}	2	-	-	

1.8 Test Waveforms

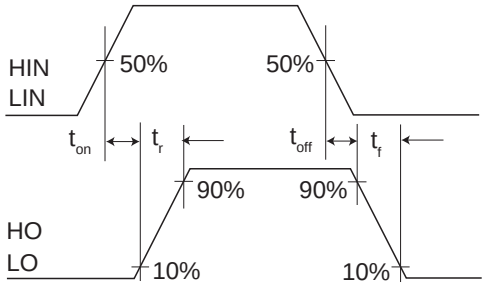
1.8.1 Switching Time Test Circuit



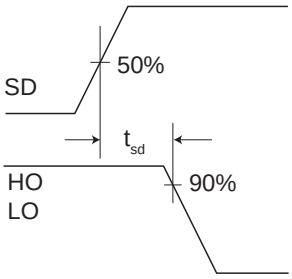
1.8.2 Input/Output Timing Waveform



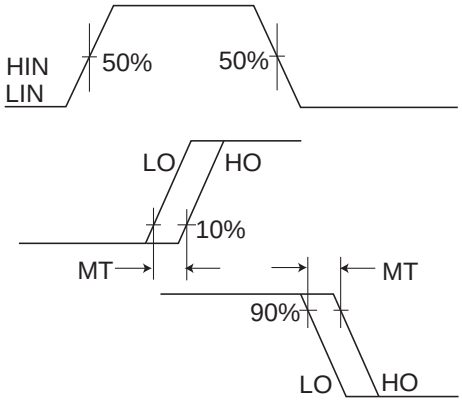
1.8.3 Switching Time Waveform Definition



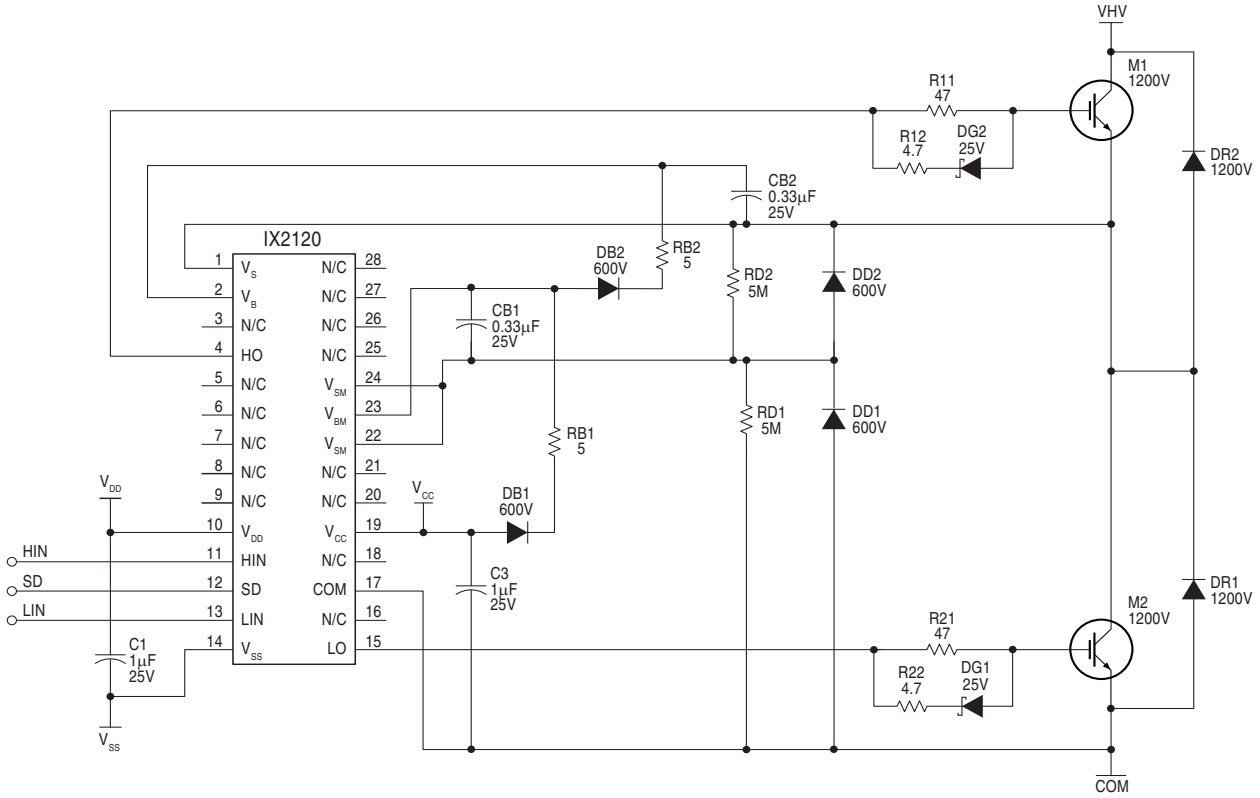
1.8.4 Shutdown Waveform Definitions



1.8.5 Delay Matching Waveform Definitions



1.9 IX2120 Typical Application



The IX2120 is a 1200V half bridge gate driver for high voltage IGBTs and MOSFETs. Three input signals (HIN, LIN, and SD) determine the state of the gate driver outputs (HO and LO). HIN controls HO via a high voltage interface. The high voltage interface is integrated into the bootstrap supply by using two 600V diodes (DD1 and DD2).

A two-stage bootstrap supplies current to the high side and mid level circuitry. The two bootstrap circuits are identical, and careful board layout and positioning of the bootstrap components are required. Resistors RD1 and RD2 form a resistive divider to keep the mid supply very near the center of the high voltage supply range. High value resisters (5MΩ) are recommended to minimize power dissipation. The two-stage bootstrap supply reduces the high side gate drive voltage (V_B-V_S) by two diode forward voltage drops ($2V_F$). Therefore, the V_{CC} supply range for the application circuit shown is:

$$20V > V_{CC} > (V_{BSUV+} + 2V_F + V_{CE(sat)}M2)$$

Where $V_{CE(sat)}$M2 is the saturation voltage of IGBT, M2.

The high side bootstrap capacitor selection is a function of the switching frequency and the on-time (t_{ONTIME}) of the high side source driver. The quiescent V_{BS} current (I_{QBS}) is supplied by bootstrap capacitor CB2, and the quiescent V_{BMSM} supply current (I_{QBMSM}) is supplied by bootstrap capacitor CB1. To insure adequate supply current:

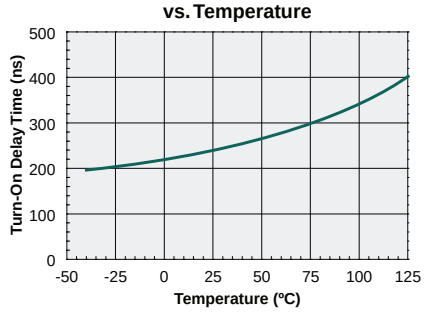
$$CB1 > I_{QBS} \bullet \frac{t_{ONTIME}}{V_{CC} - (V_{BSUV+} + 2VF + V_{CE(sat)}M2)}$$

and:

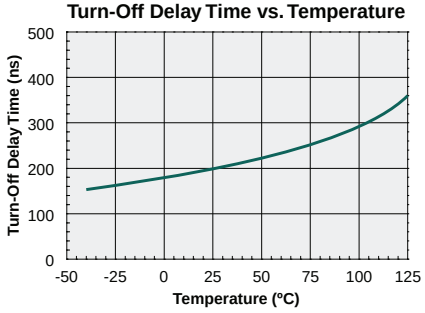
$$CB2 > I_{QBMSM} \bullet \frac{t_{ONTIME}}{V_{CC} - (V_{BSUV+} + 2VF + V_{CE(sat)}M2)}$$

2 Typical Performance Data

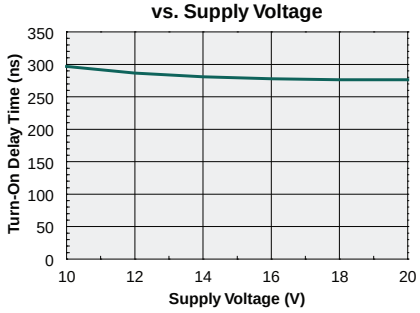
Turn-On Delay Time vs. Temperature



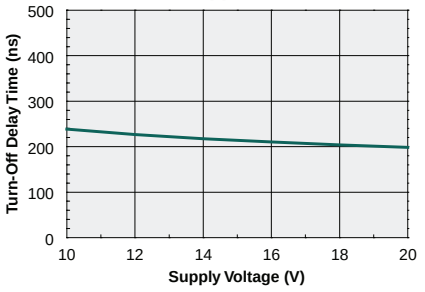
Turn-Off Delay Time vs. Temperature



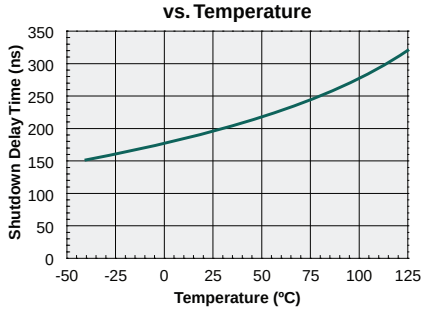
Turn-On Delay Time vs. Supply Voltage



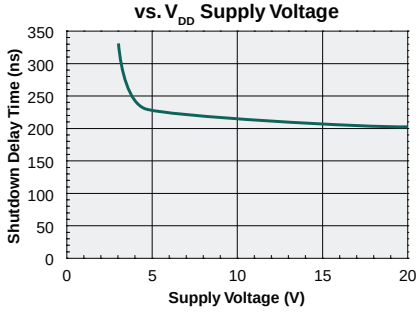
Turn-Off Delay Time vs. Supply Voltage



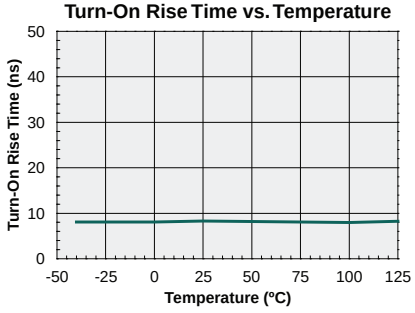
Shutdown Delay Time vs. Temperature



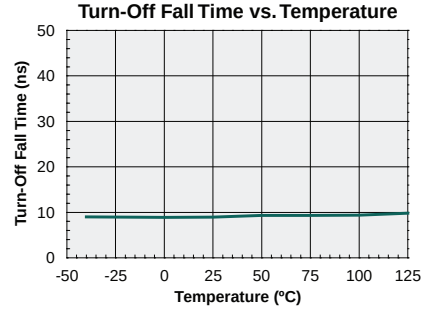
Shutdown Delay Time vs. V_{DD} Supply Voltage



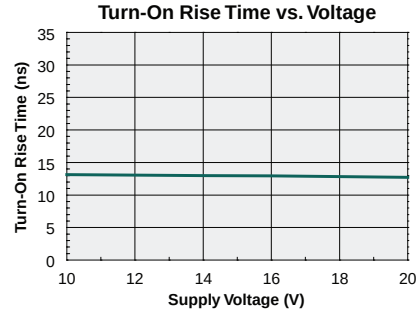
Turn-On Rise Time vs. Temperature



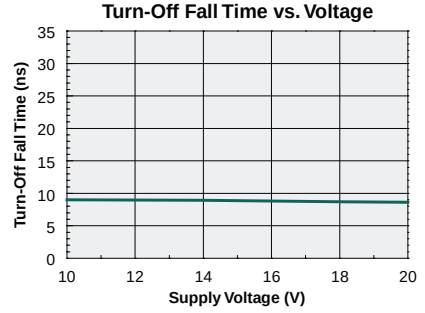
Turn-Off Fall Time vs. Temperature



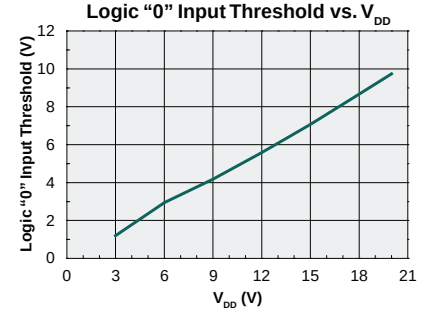
Turn-On Rise Time vs. Voltage



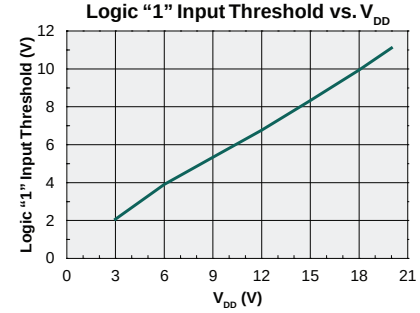
Turn-Off Fall Time vs. Voltage



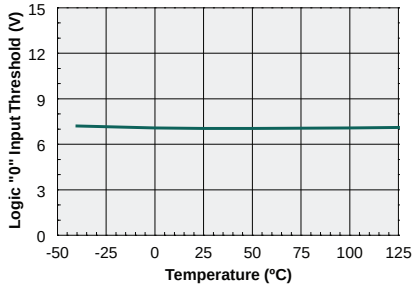
Logic “0” Input Threshold vs. V_{DD}



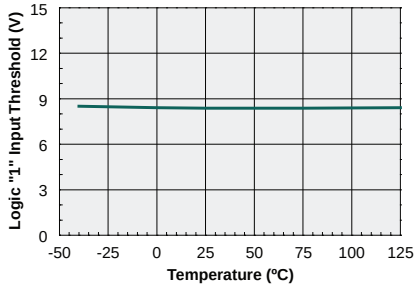
Logic “1” Input Threshold vs. V_{DD}



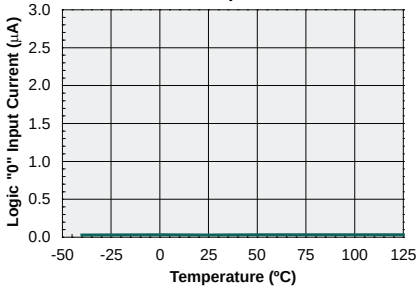
Logic "0" Input Threshold vs. Temperature



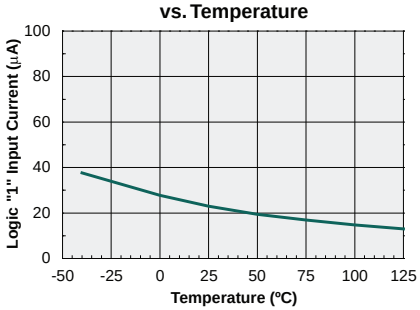
Logic "1" Input Threshold vs. Temperature



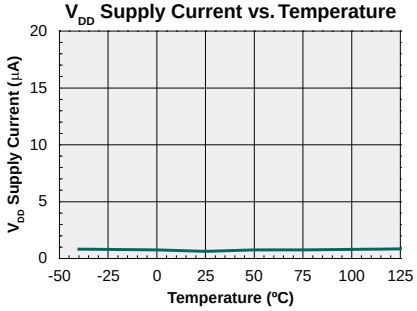
Logic "0" Input Current vs. Temperature



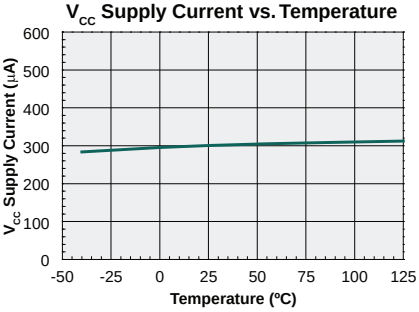
Logic "1" Input Current vs. Temperature



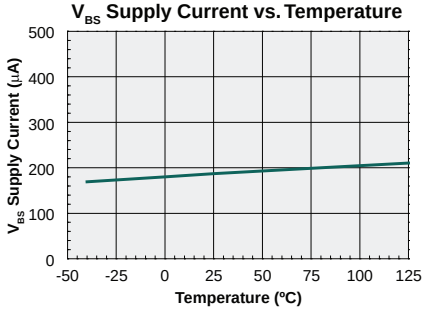
V_{DD} Supply Current vs. Temperature



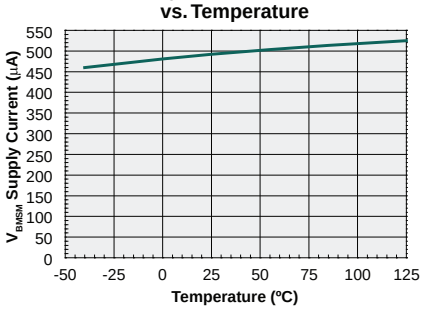
V_{CC} Supply Current vs. Temperature



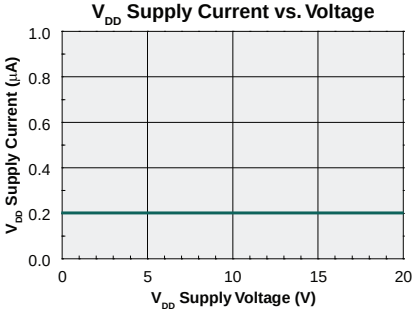
V_{BS} Supply Current vs. Temperature



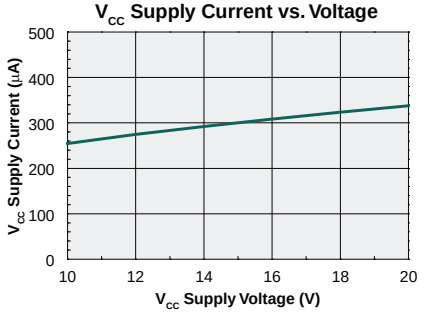
V_{BMSM} Supply Current vs. Temperature



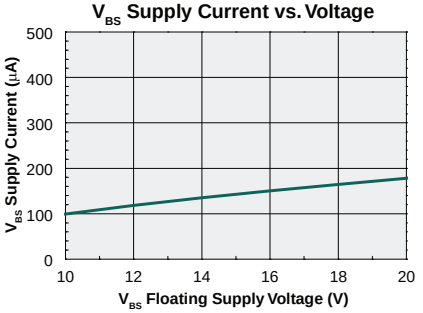
V_{DD} Supply Current vs. Voltage



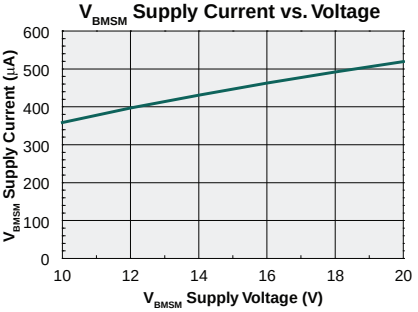
V_{CC} Supply Current vs. Voltage



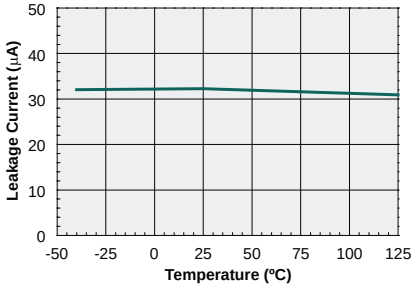
V_{BS} Supply Current vs. Voltage



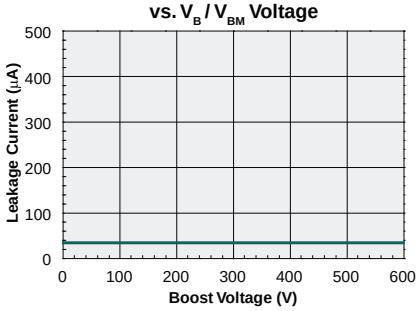
V_{BMSM} Supply Current vs. Voltage



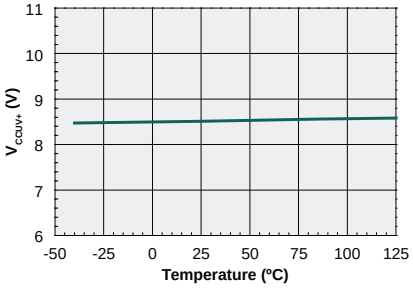
High/Middle Supply Leakage Current vs. Temperature



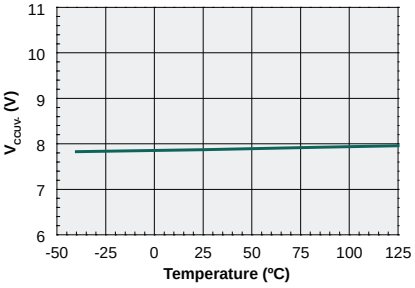
High/Middle Supply Leakage Current vs. V_B / V_{BM} Voltage



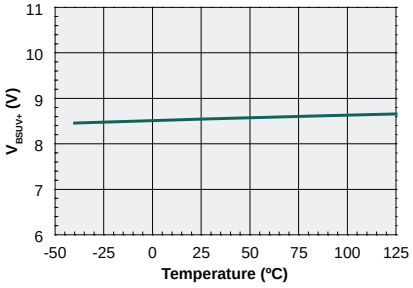
V_{CCUV+} vs. Temperature



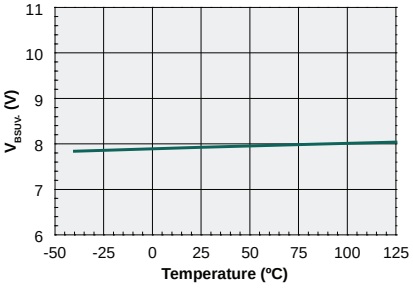
V_{CCUV-} vs. Temperature



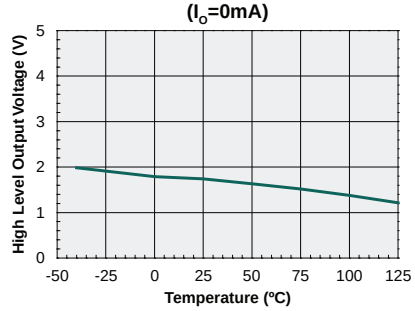
V_{BSUV+} vs. Temperature



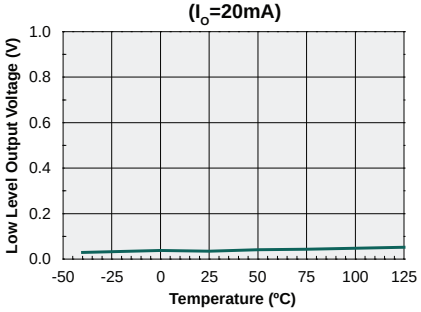
V_{BSUV-} vs. Temperature



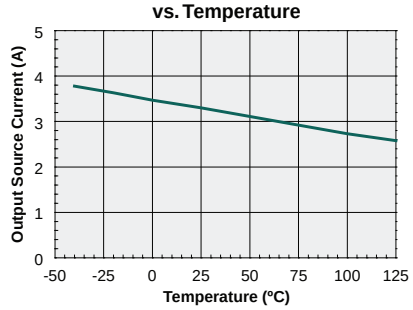
High Level Output Voltage vs. Temperature (I_O=0mA)



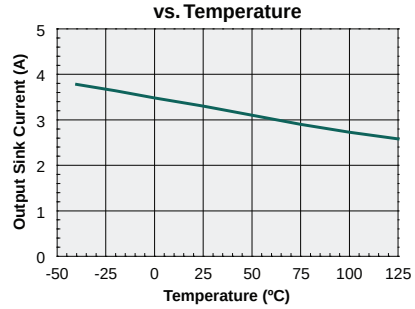
Low Level Output Voltage vs. Temperature (I_O=20mA)



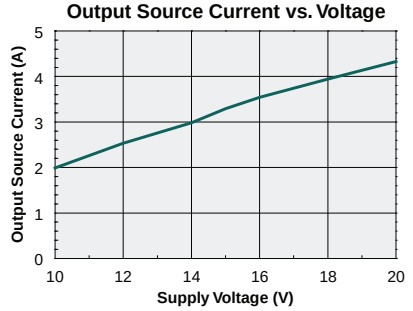
Output Source Current vs. Temperature



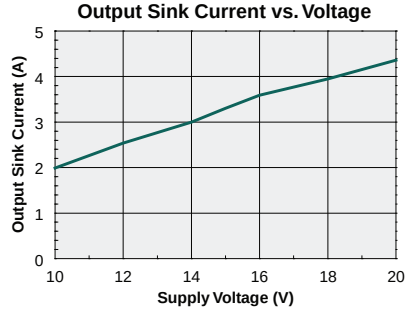
Output Sink Current vs. Temperature

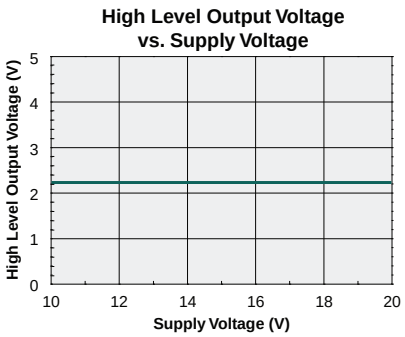


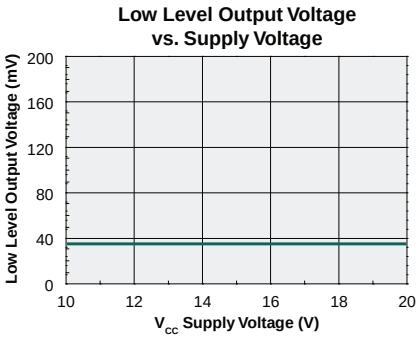
Output Source Current vs. Voltage



Output Sink Current vs. Voltage




High Level Output Voltage
vs. Supply Voltage
High Level Output Voltage (V)
0
1
2
3
4
5
10
12
14
16
18
20
Supply Voltage (V)


Low Level Output Voltage
vs. Supply Voltage
Low Level Output Voltage (mV)
0
40
80
120
160
200
10
12
14
16
18
20
Vcc Supply Voltage (V)

3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX2120B	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be above (T_C - 5)ºC. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

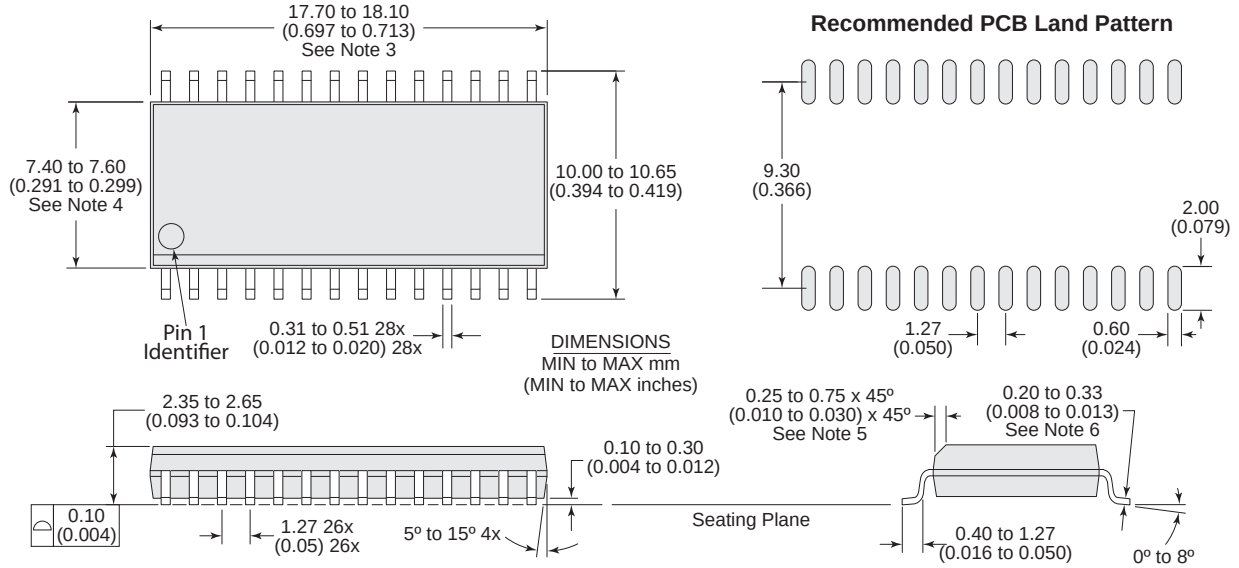
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX2120B	260°C	30 seconds	3

3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include, but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

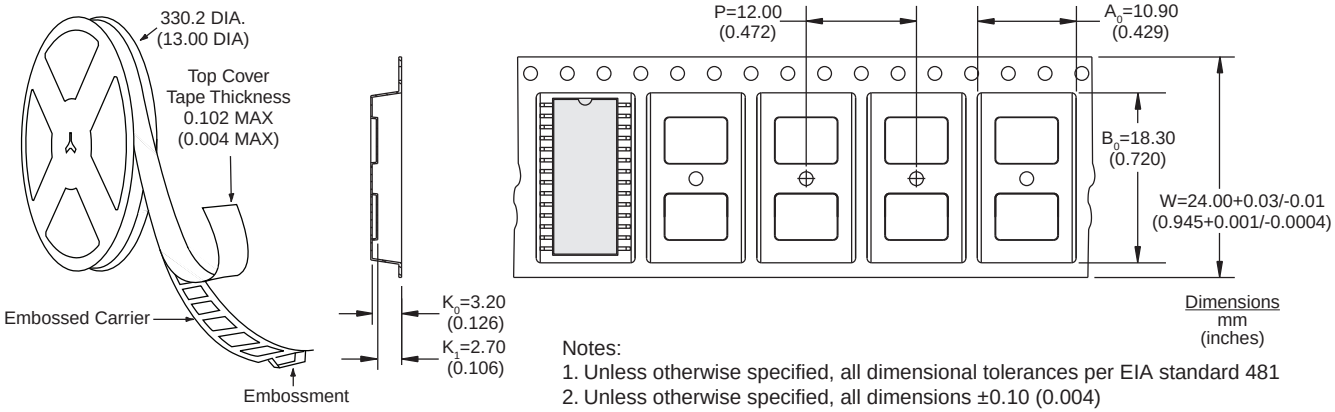
3.5 Mechanical Dimensions

3.5.1 IX2120: 28-Pin SOIC Package



Notes:
1. All dimensions are in mm / (inches).
2. This package conforms to JEDEC Standard MS-013, variation AE issue C.
3. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
4. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
5. This chamfer is optional. If it is not present, then a Pin 1 identifier must be located as shown.
6. The dimension applies to the flat section of the lead between 0.10mm to 0.25mm from the lead tip.

3.5.2 IX2120 Tape & Reel Information



Notes:
1. Unless otherwise specified, all dimensional tolerances per EIA standard 481
2. Unless otherwise specified, all dimensions ±0.10 (0.004)

For additional information please visit our website at: www.ixysic.com

Specification: DS-IX2120-R02

2/3/2016