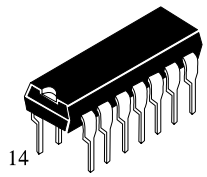
**IW4001B**

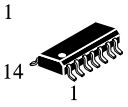
# Quad 2-Input NOR Gate
# High-Voltage Silicon-Gate CMOS

The IW4001B NOR gates provide the system designer with direct emplementation of the NOR function.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  0.5 V min @ 5.0 V supply
  1.0 V min @ 10.0 V supply
  1.5 V min @ 15.0 V supply



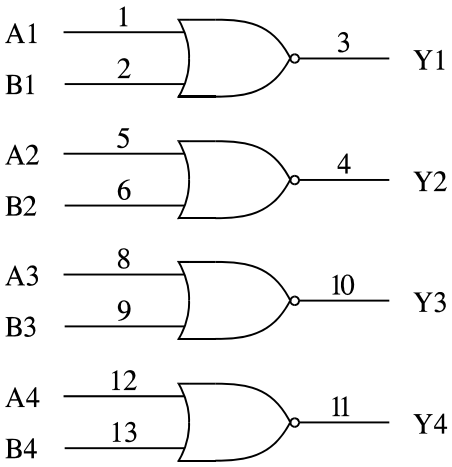

N SUFFIX
PLASTIC




D SUFFIX
SOIC

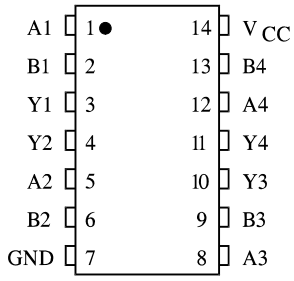
**ORDERING INFORMATION**
IW4001BN Plastic
IW4001BD SOIC
$T_A$ = -55° to 125° C for all packages

## LOGIC DIAGRAM




PIN 14 =$V_{CC}$
PIN 7 = GND

## PIN ASSIGNMENT




## FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

L – LOW voltage level

H – HIGH voltage level

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +20 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±10 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+ | 500<br>500 | mW |
| Ptot | Power Dissipation per Output Transistor | 100 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 3.0 | 18 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | -55 | +125 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit ≥-55°C | Guaranteed Limit 25°C | Guaranteed Limit ≤125 °C | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{OUT}$=0.5V<br>$V_{OUT}$=1.0 V<br>$V_{OUT}$=1.5V | 5.0<br>10<br>15 | 3.5<br>7<br>11 | 3.5<br>7<br>11 | 3.5<br>7<br>11 | V |
| $V_{IL}$ | Maximum Low - Level Input Voltage | $V_{OUT}$=0.5 V or $V_{CC}$ - 0.5 V<br>$V_{OUT}$=1.0 V or $V_{CC}$ - 1.0 V<br>$V_{OUT}$=1.5 V or $V_{CC}$ - 1.5 V | 5.0<br>10<br>15 | 1.5<br>3<br>4 | 1.5<br>3<br>4 | 1.5<br>3<br>4 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{IN}$=GND | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | 4.95<br>9.95<br>14.95 | 4.95<br>9.95<br>14.95 | V |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{IN}$=GND or $V_{CC}$ | 5.0<br>10<br>15 | 0.05<br>0.05<br>0.05 | 0.05<br>0.05<br>0.05 | 0.05<br>0.05<br>0.05 | V |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$= GND or $V_{CC}$ | 18 | ±0.1 | ±0.1 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{IN}$= GND or $V_{CC}$ | 5.0<br>10<br>15<br>20 | 0.25<br>0.5<br>1.0<br>5.0 | 0.25<br>0.5<br>1.0<br>5.0 | 7.5<br>15<br>30<br>150 | μA |
| $I_{OL}$ | Minimum Output Low (Sink) Current | $V_{IN}$= GND or $V_{CC}$<br>$U_{OL}$=0.4 V<br>$U_{OL}$=0.5 V<br>$U_{OL}$=1.5 V | <br>5.0<br>10<br>15 | <br>0.64<br>1.6<br>4.2 | <br>0.51<br>1.3<br>3.4 | <br>0.36<br>0.9<br>2.4 | mA |
| $I_{OH}$ | Minimum Output High (Source) Current | $V_{IN}$= GND or $V_{CC}$<br>$U_{OH}$=2.5 V<br>$U_{OH}$=4.6 V<br>$U_{OH}$=9.5 V<br>$U_{OH}$=13.5 V | <br>5.0<br>5.0<br>10<br>15 | <br>-2.0<br>-0.64<br>-1.6<br>-4.2 | <br>-1.6<br>-0.51<br>-1.3<br>-3.4 | <br>-1.15<br>-0.36<br>-0.9<br>-2.4 | mA |

## AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF, $R_L$=200kΩ, Input $t_r$=$t_f$=20 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit ≥-55°C | Guaranteed Limit 25°C | Guaranteed Limit ≤125°C | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A or B to Output Y (Figure 1) | 5.0<br>10<br>15 | 250<br>120<br>90 | 250<br>120<br>90 | 250<br>120<br>90 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figure 1) | 5.0<br>10<br>15 | 200<br>100<br>80 | 200<br>100<br>80 | 200<br>100<br>80 | ns |
| $C_{IN}$ | Maximum Input Capacitance | - | | 7.5 | | pF |

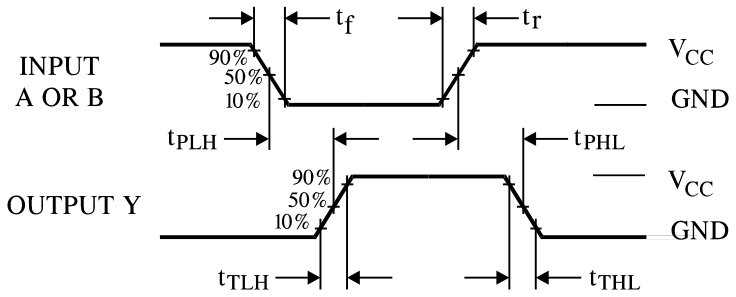
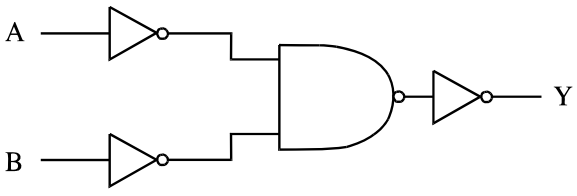
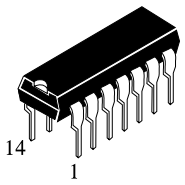


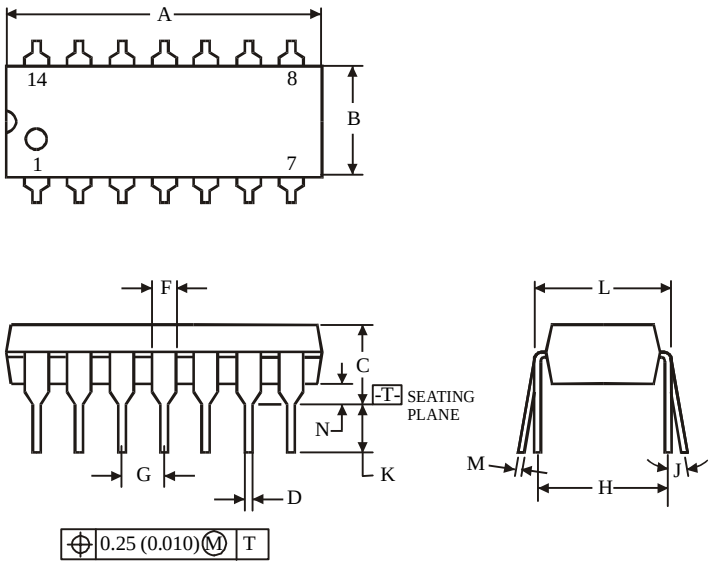

**Figure 1. Switching Waveforms**

## EXPANDED LOGIC DIAGRAM
## (1/4 of the Device)



## N SUFFIX PLASTIC DIP
## (MS - 001AA)

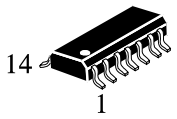


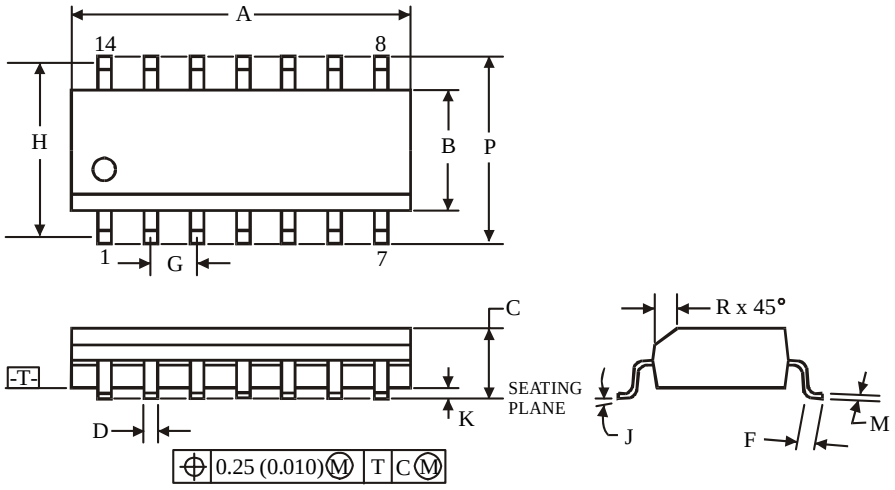




| Symbol | Dimensions, mm | |
|---|---|---|
| | MIN | MAX |
| A | 18.67 | 19.69 |
| B | 6.10 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.20 | 0.36 |
| N | 0.38 | |

**NOTES:**
1. Dimensions “A”, “B” do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

## D SUFFIX SOIC
## (MS - 012AB)




| Symbol. | Dimensions, mm | |
|---|---|---|
| | MIN | MAX |
| A | 8.55 | 8.75 |
| B | 3.80 | 4.00 |
| C | 1.35 | 1.75 |
| D | 0.33 | 0.51 |
| F | 0.40 | 1.27 |
| G | 1.27 | |
| H | 5.72 | |
| J | 0° | 8° |
| K | 0.10 | 0.25 |
| M | 0.19 | 0.25 |
| P | 5.80 | 6.20 |
| R | 0.25 | 0.50 |

**NOTES:**
1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.