

512K x 8 HIGH-SPEED CMOS STATIC RAM

DECEMBER 2016

FEATURES

HIGH SPEED: (IS61/64C5128AL)

- High-speed access time: 10ns, 12 ns
- Low Active Power: 150 mW (typical)
- Low Standby Power: 10 mW (typical)
CMOS standby

LOW POWER: (IS61/64C5128AS)

- High-speed access time: 25ns
- Low Active Power: 75 mW (typical)
- Low Standby Power: 1 mW (typical)
CMOS standby
- TTL compatible interface levels
- Single 5V $\pm$ 10% power supply
- Fully static operation: no clock or refresh required
- Available in 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

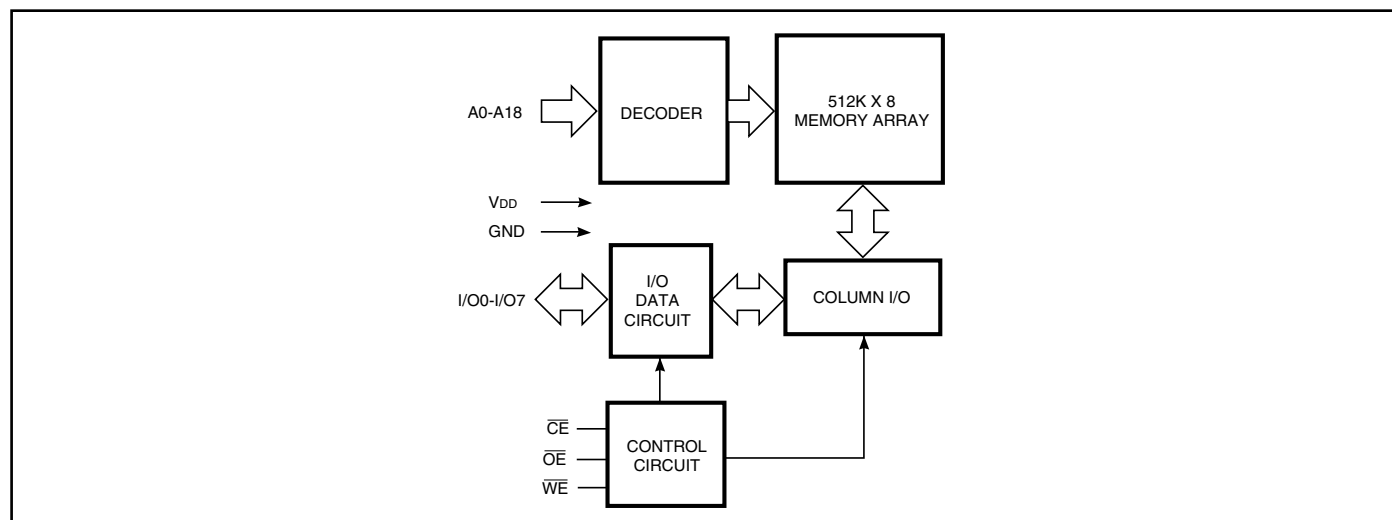
The *ISSI* IS61C5128AL/AS and IS64C5128AL/AS are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61C5128AL/AS and IS64C5128AL/AS are packaged in the JEDEC standard 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32-pin TSOP-II packages

FUNCTIONAL BLOCK DIAGRAM



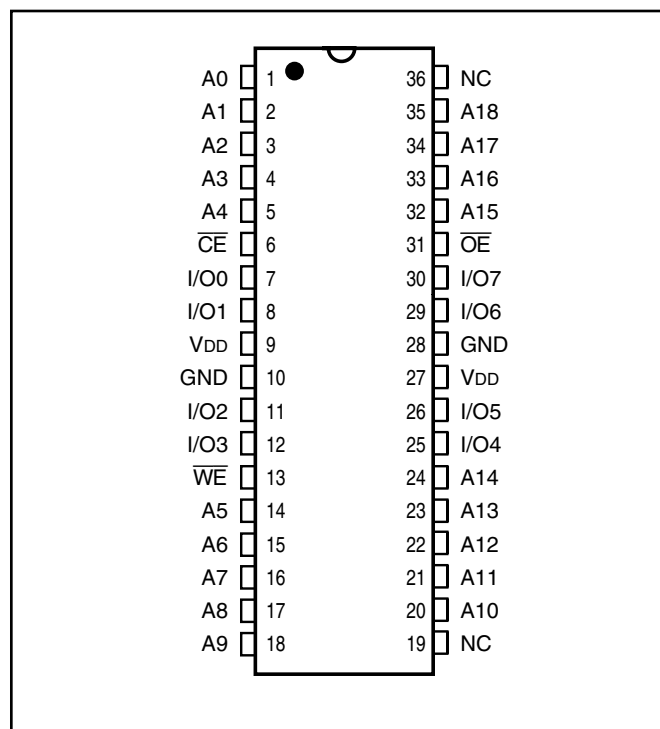
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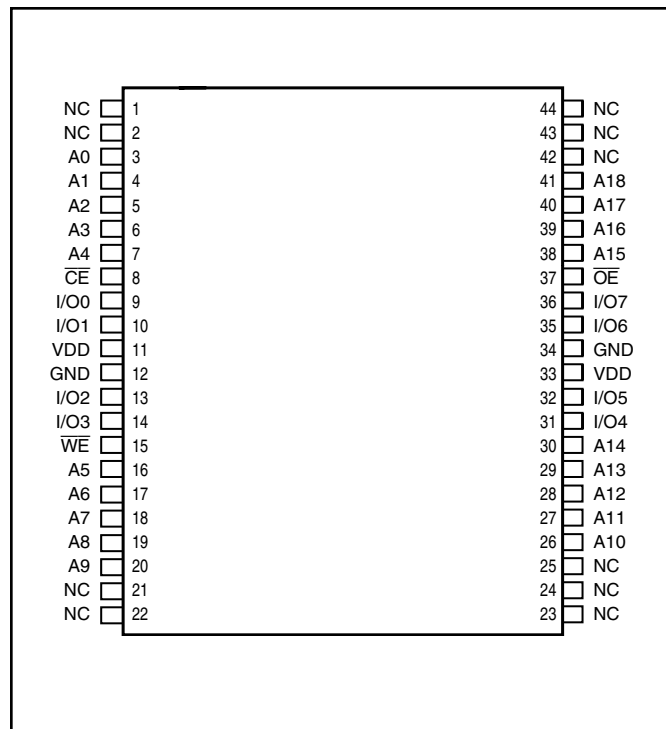
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

HIGH SPEED (IS61/64C5128AL) PIN CONFIGURATION

36-Pin SOJ (400-mil)



44-Pin TSOP (Type II)



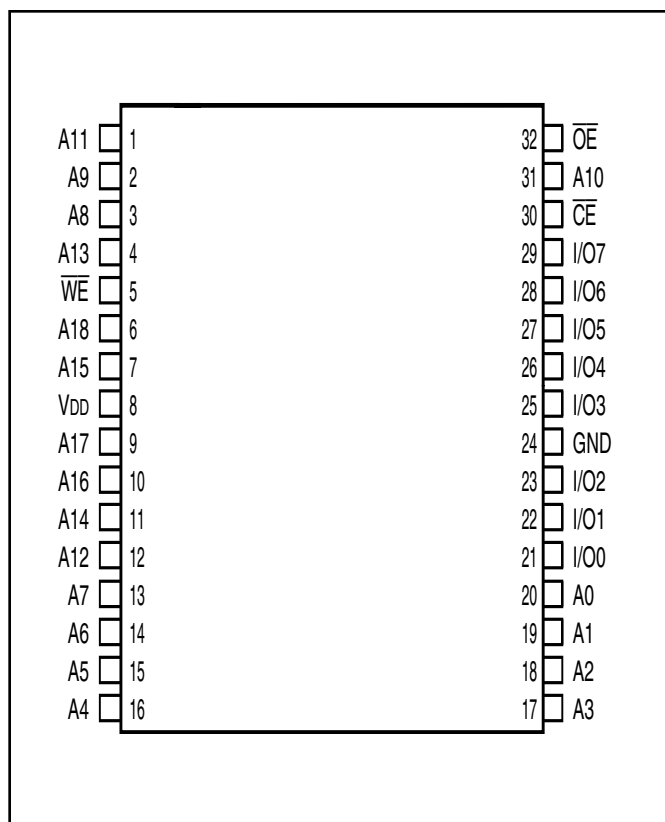
PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
VDD	Power
GND	Ground
NC	No Connection

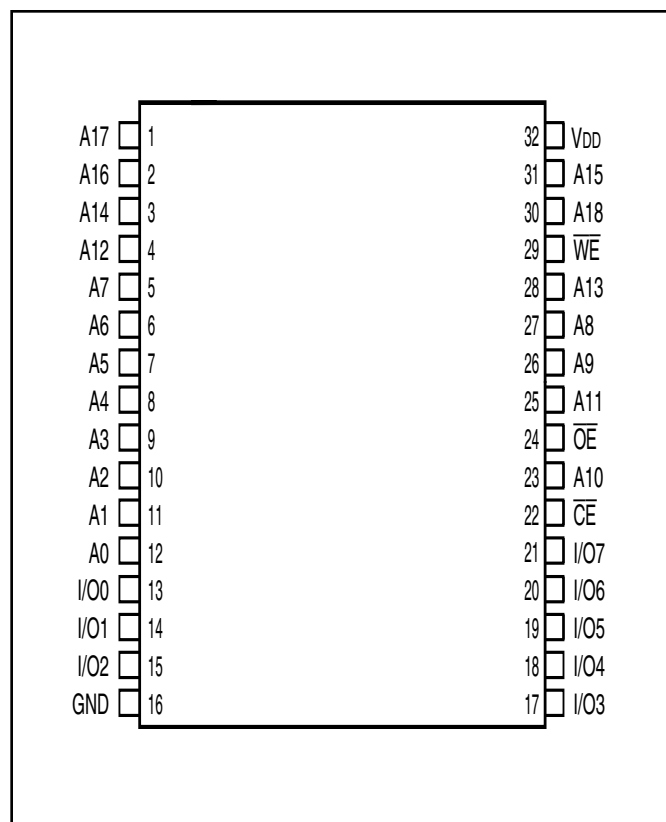
IS61C5128AL/AS IS64C5128AL/AS

LOW POWER (IS61/64C5128AS) PIN CONFIGURATION

32-pin sTSP (TYPE I)



32-pin SOP 32-pin TSOP (TYPE II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O0-I/O7	I/O PIN
					V _{DD} Current
Not Selected	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC1} , I _{CC2}
Read	H	L	L	D _{OUT}	I _{CC1} , I _{CC2}
Write	L	L	X	D _{IN}	I _{CC1} , I _{CC2}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = −4.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{DD} + 0.5	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		−0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com.	−1	1	μA
			Ind.	−2	2	
			Auto.	−5	5	
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled	Com.	−1	1	μA
			Ind.	−2	2	
			Auto.	−5	5	

Note: 1. V_{IL} = −3.0V for pulse width less than 10 ns.

OPERATING RANGE: HIGH SPEED OPTION (IS61/64C5128AL)

Range	Ambient Temperature	V _{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	10
Industrial	-40°C to +85°C	5V ± 10%	10
Automotive	-40°C to +125°C	5V ± 10%	12

OPERATING RANGE: LOW POWER OPTION (IS61/64C5128AS)

Range	Ambient Temperature	V _{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	25
Industrial	-40°C to +85°C	5V ± 10%	25
Automotive	-40°C to +125°C	5V ± 10%	25

HIGH SPEED OPTION (IS61/64C5128AL)
POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns		-12 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = V _{DD} MAX., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = 0	Com.	—	45	—	45	mA
			Ind.	—	50	—	50	
			Auto.	—	55	—	55	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = V _{DD} MAX., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	50	—	45	mA
			Ind.	—	55	—	50	
			Auto.	—	70	—	60	
			typ. ⁽²⁾	30		25		
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = V _{DD} MAX., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	30	—	30	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = V _{DD} MAX., $\overline{CE} \leq V_{DD} - 0.2V$, V _{IN} $\geq$ V _{DD} - 0.2V, or V _{IN} $\leq$ 0.2V, f = 0	Com.	—	8	—	8	mA
			Ind.	—	12	—	12	
			Auto.	—	20	—	20	
			typ. ⁽²⁾	2				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

LOW POWER OPTION (IS61/64C5128AS)
POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns		Unit
				Min.	Max.	
I _{CC}	Average operating Current	$\overline{CE}$ = V _{IL} , V _{DD} = Max. I _{OUT} = 0 mA, f = 0	Com.	—	10	mA
			Ind.	—	15	
			Auto.	—	20	
I _{CC1}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	25	mA
			Ind.	—	30	
			Auto.	—	40	
			typ. ⁽²⁾	15		
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1	mA
			Ind.	—	1.5	
			Auto.	—	2	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} $\geq$ V _{DD} - 0.2V, or V _{IN} $\leq$ V _{SS} + 0.2V, f = 0	Com.	—	0.8	mA
			Ind.	—	0.9	
			Auto.	—	2	
			typ.	0.2		

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-10		-12		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	15	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	5	0	6	0	8	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	2	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	5	0	6	0	8	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	2	—	2	—	2	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

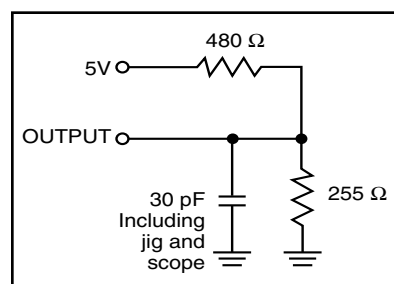
AC TEST LOADS


Figure 1

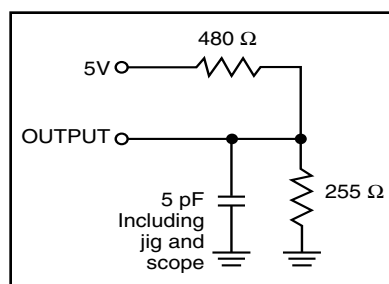
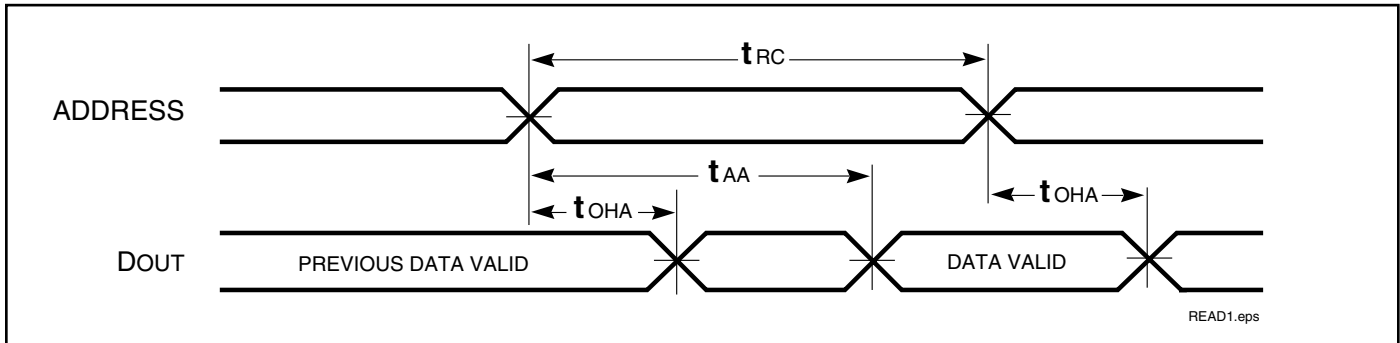
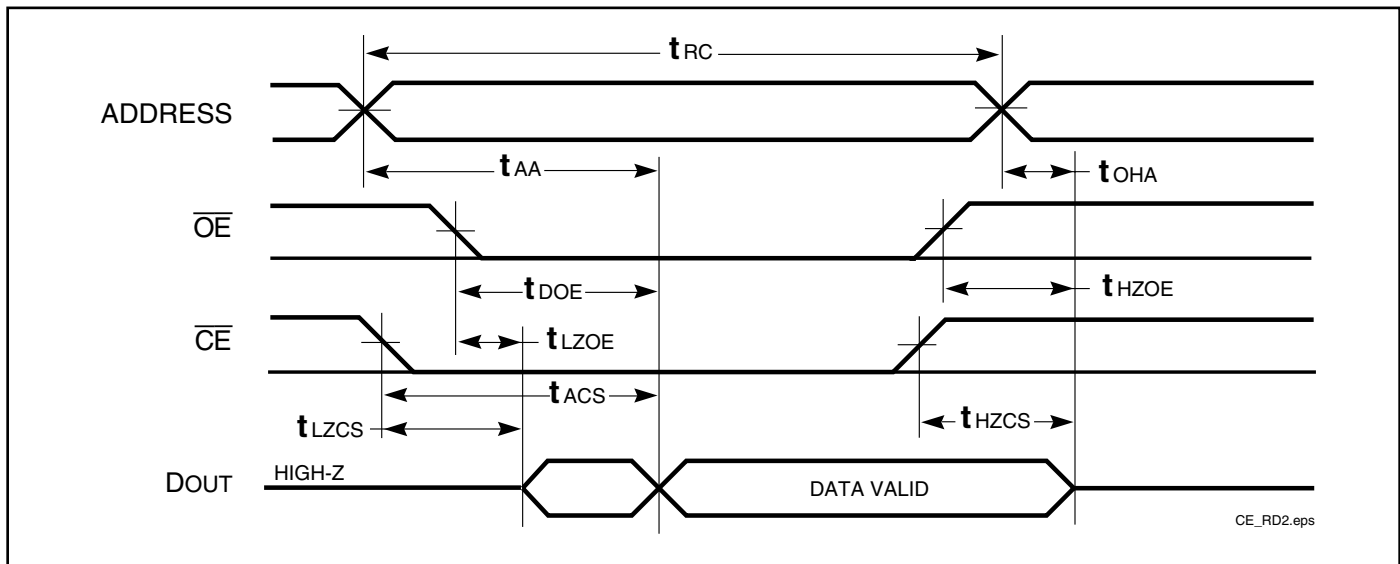


Figure 2

AC WAVEFORMS
READ CYCLE NO. 1^(1,2)

READ CYCLE NO. 2^(1,3)

Notes:

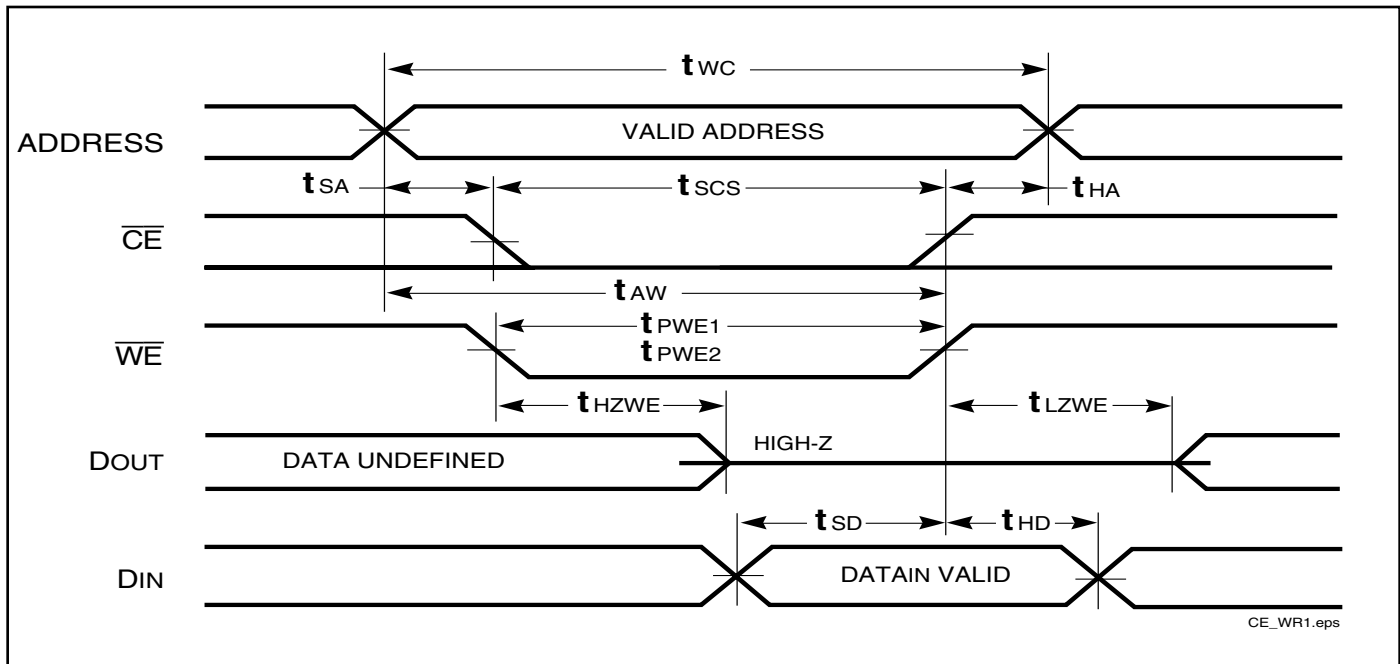
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-10		-12		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	10	—	12	—	25	—	ns
t _{SCE}	$\overline{CE}$ to Write End	7	—	9	—	18	—	ns
t _{AW}	Address Setup Time to Write End	7	—	9	—	18	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	7	—	9	—	15	—	ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =Low)	7	—	9	—	15	—	ns
t _{SD}	Data Setup to Write End	6	—	6	—	15	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	15	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	ns

Notes:

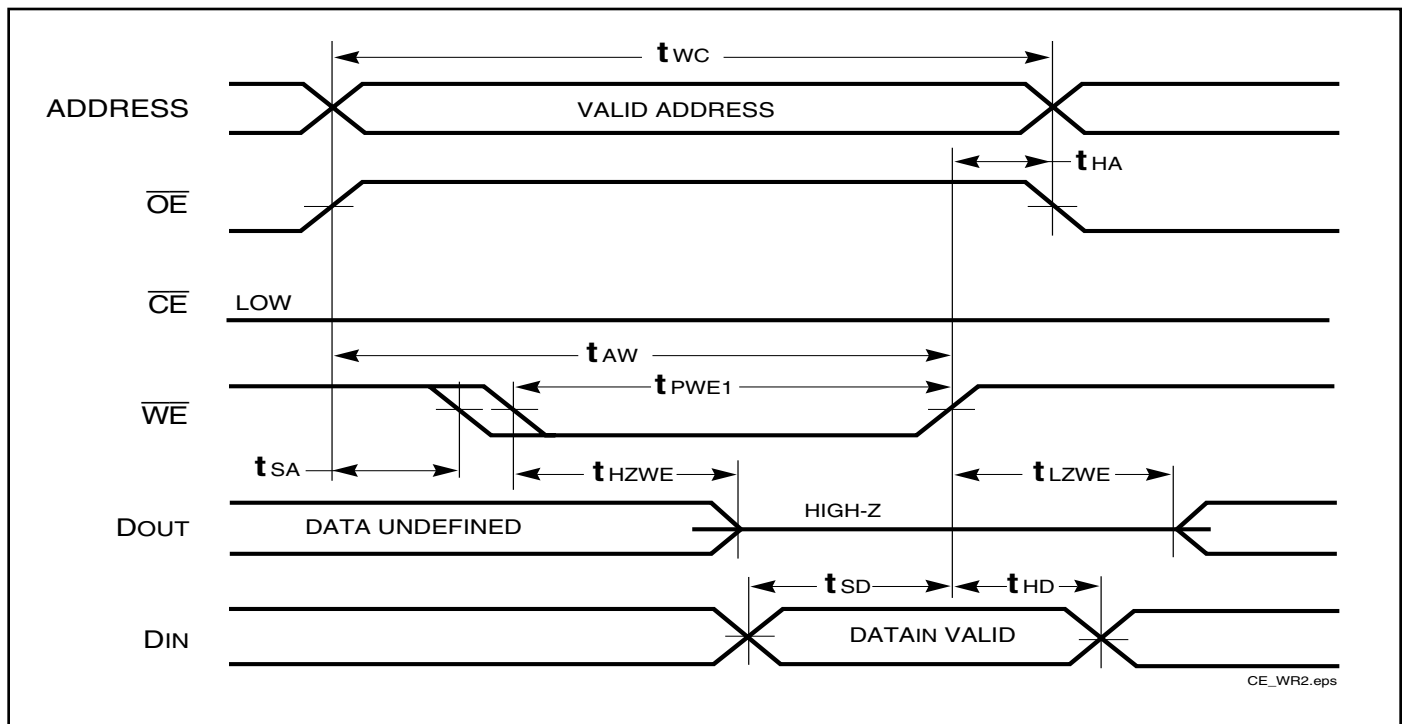
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)

Notes:

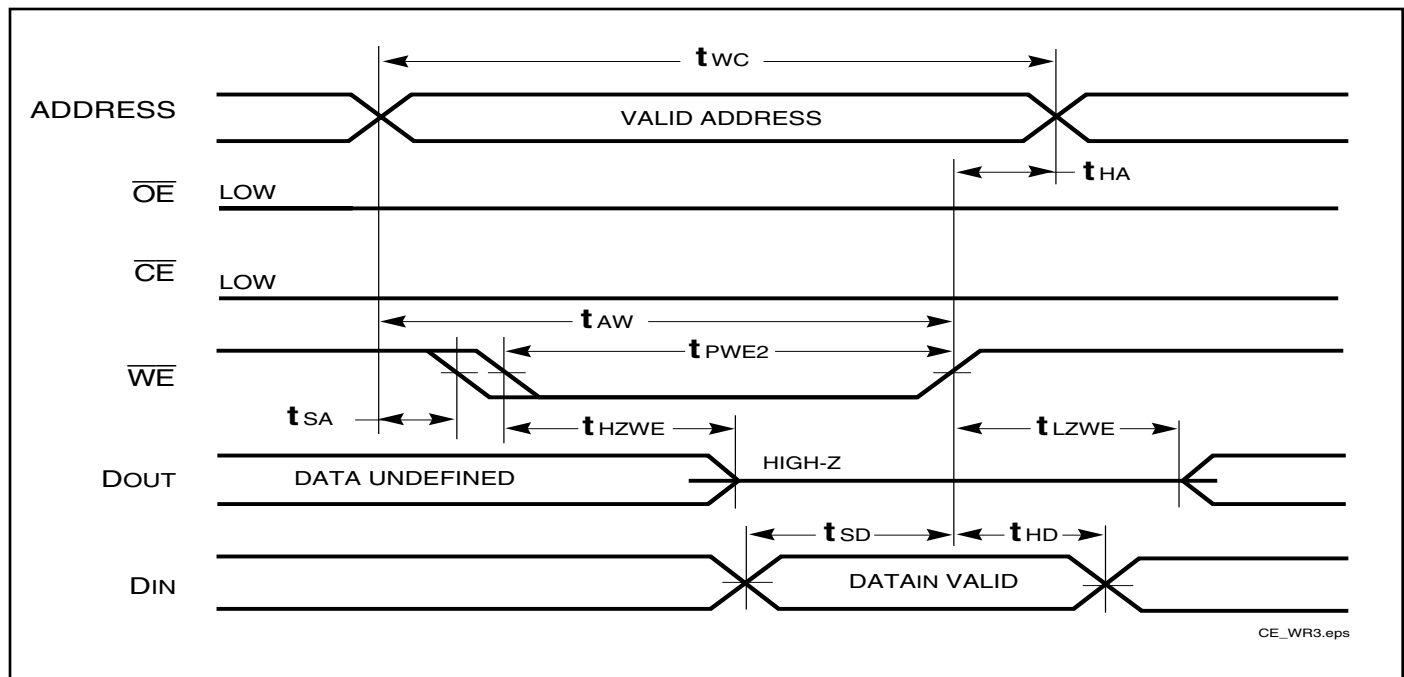
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

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WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) ^(1,2)



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾



Notes:

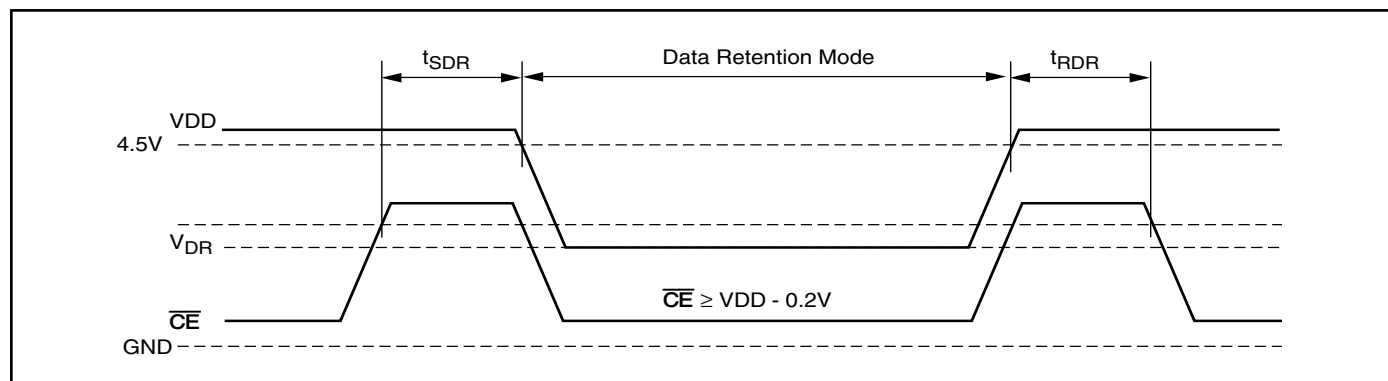
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C5128AL)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform	2.9	5.5	V
I _{DR}	Data Retention Current	V _{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$ V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ V _{SS} + 0.2V	Com. Ind. Auto. typ. ⁽¹⁾	8 10 15	mA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform	t _{RC}	—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

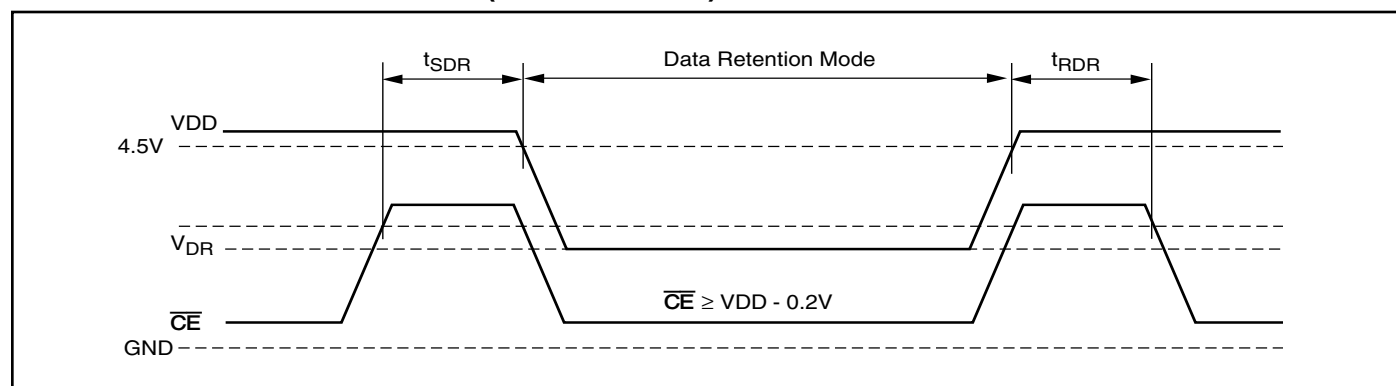
DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)


DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C5128AS)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.9	5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.9V, \overline{CE} \geq V_{DD} - 0.2V$	—	0.8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	—	0.9	
		Auto.	—	2	
		typ. ⁽¹⁾	0.2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

Note:

1. Typical Values are measured at $V_{DD} = 5V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)


HIGH SPEED (IS61/64C5128AL)**ORDERING INFORMATION****Industrial Range: –40°C to +85°C**

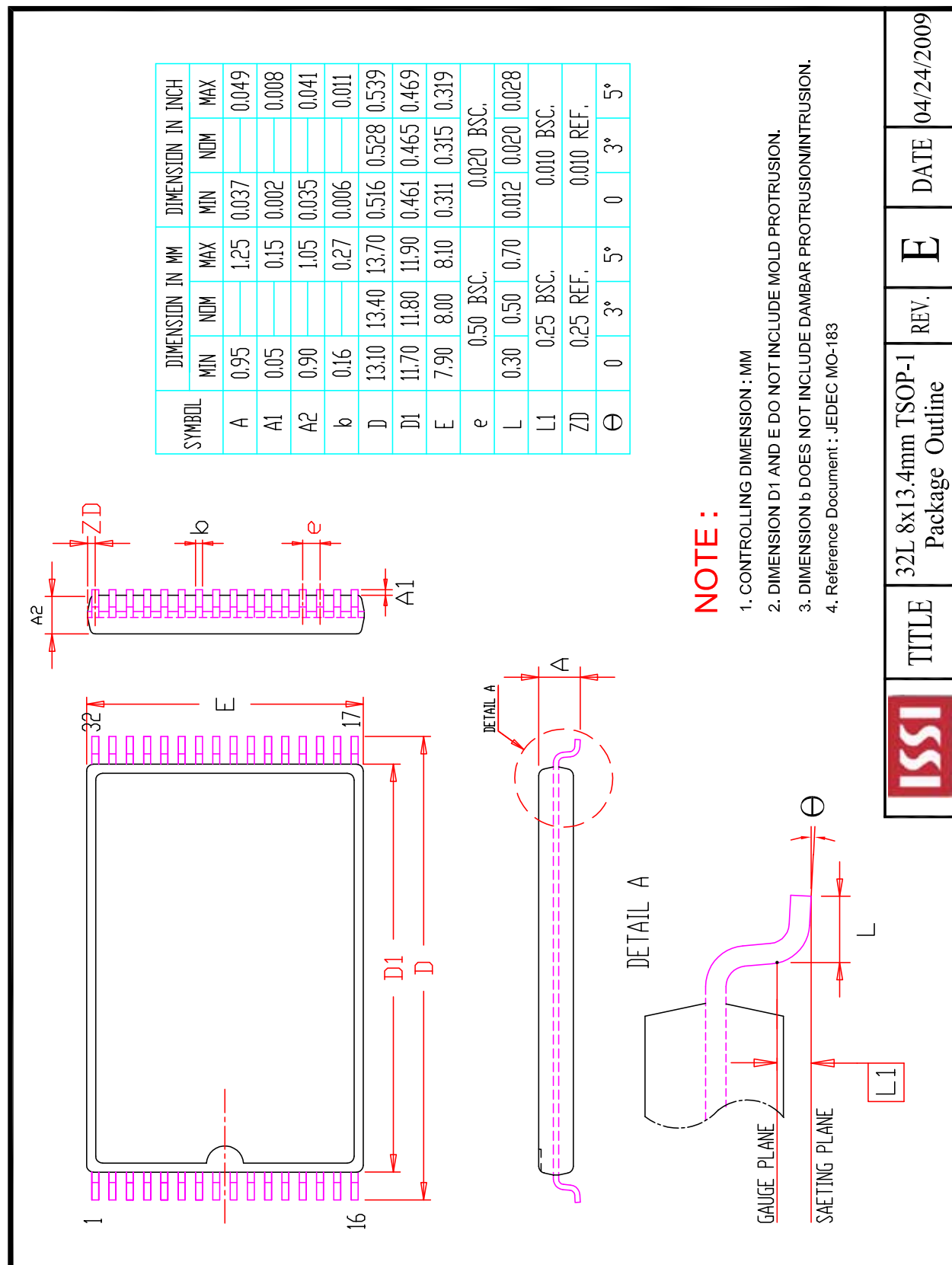
Speed (ns)	Order Part No.	Package
10	IS61C5128AL-10KLI	400-mil Plastic SOJ, Lead-free
	IS61C5128AL-10TLI	44-pin TSOP-II, Lead-free

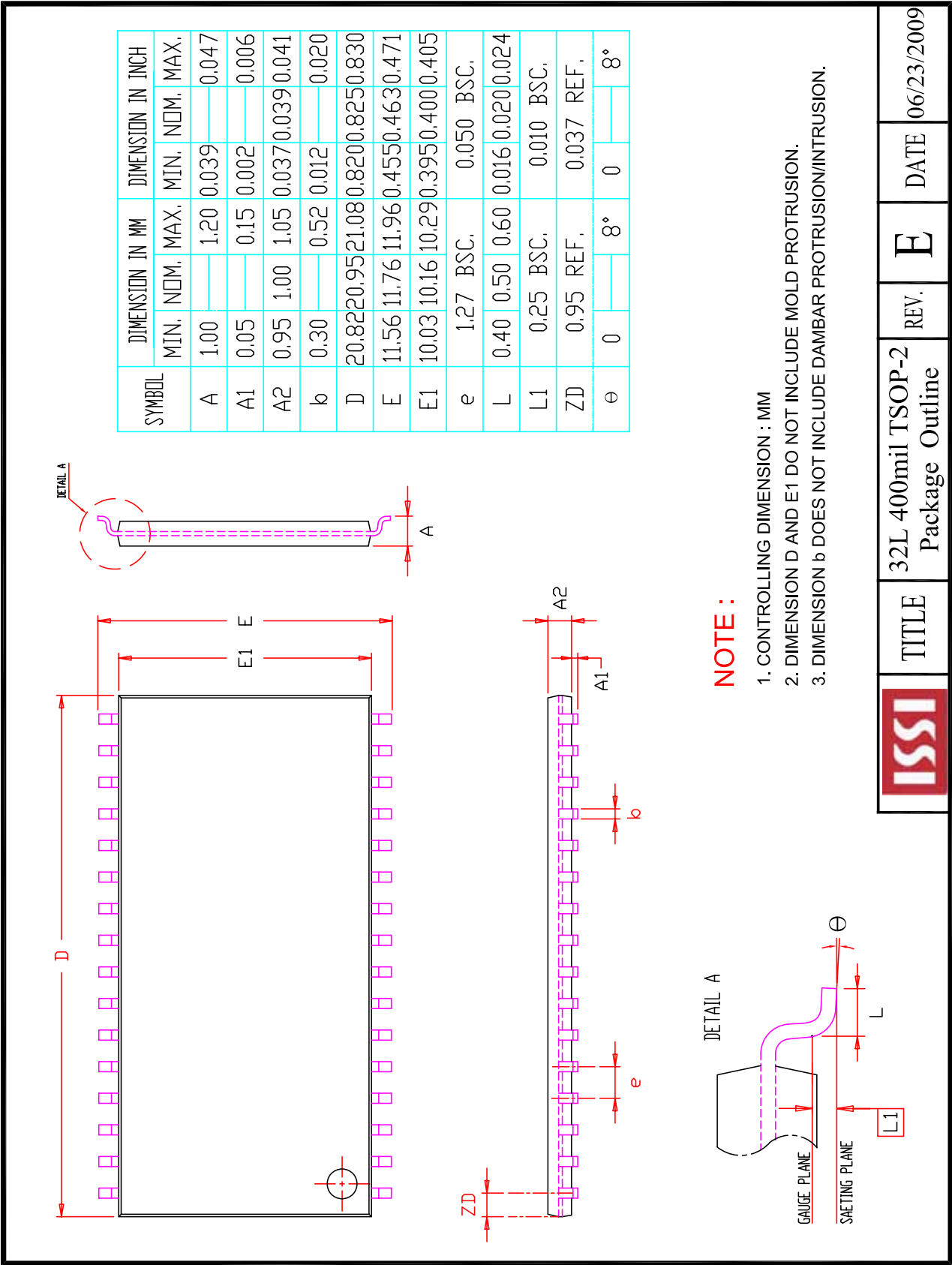
Automotive Range: –40°C to +125°C

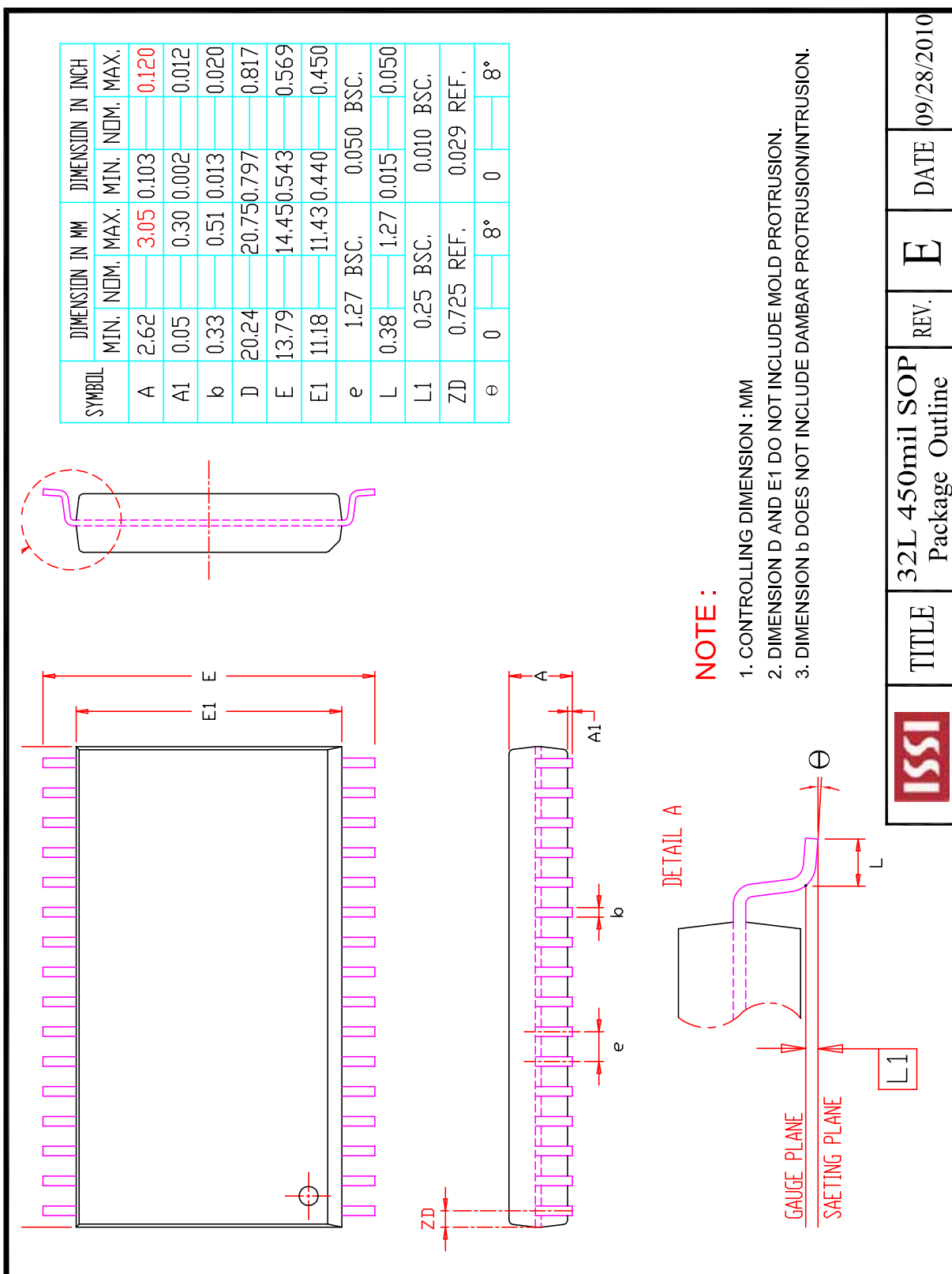
Speed (ns)	Order Part No.	Package
12	IS64C5128AL-12KLA3	400-mil Plastic SOJ, Lead-free
	IS64C5128AL-12CTLA3	44-pin TSOP-II, Lead-free, Copper Leadframe

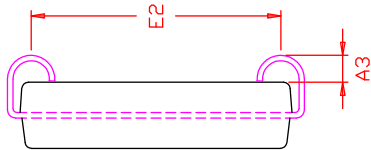
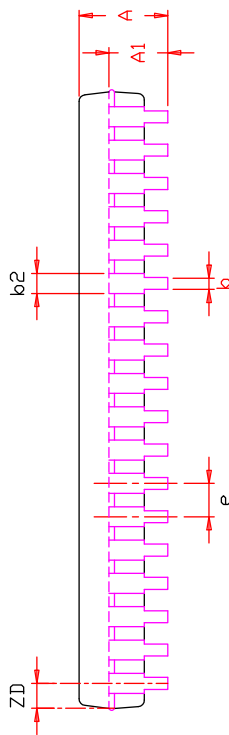
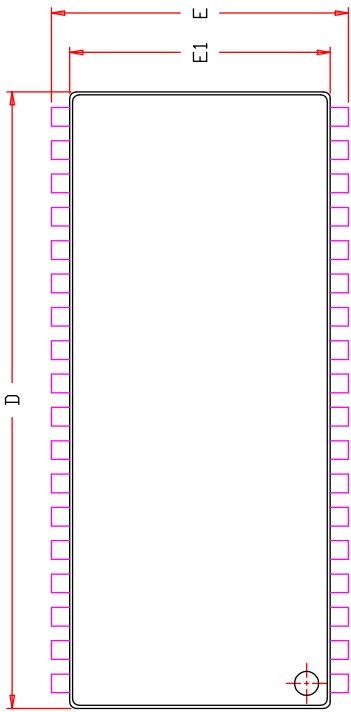
LOW POWER (IS61/64C5128AS)**ORDERING INFORMATION****Industrial Range: –40°C to +85°C**

Speed (ns)	Order Part No.	Package
25	IS61C5128AS-25QLI	450-mil Plastic SOP, Lead-free
	IS61C5128AS-25HLI	32-pin STSOP-I, Lead-free
	IS61C5128AS-25TLI	32-pin TSOP-II, Lead-free









SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	3.25	3.76	0.128	0.148
A1	2.08		0.082	
A3	0.635		0.025	
b	0.38	0.51	0.015	0.020
b2	0.66	0.71	0.026	0.028
D	23.36	23.49	0.920	0.925
E	11.05	11.18	0.435	0.440
E1	10.03	10.16	0.395	0.400
E2	9.40	BSC.	0.370	BSC.
e	1.27	BSC.	0.050	BSC.
ZD	0.95	REF.	0.037	REF.

NOTE :

- 1. Controlling dimension : mm
- 2. Dimension D and E1 do not include mold protrusion .
- 3. Dimension b2 does not include dambar protrusion/intrusion.
- 4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
- 5. Reference document : JEDEC SPEC MS-027.



36L 400mil SOJ
Package Outline

REV.

F

DATE

12/20/2007

