



ISO7741E-Q1 Grade 0, High-Speed, Robust-EMC Reinforced Quad-Channel Digital Isolator

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 0: -40°C to 150°C ambient operating temperature
- 100 Mbps data rate
- Robust isolation barrier:
 - >100-year projected lifetime at 1500 V_{RMS} working voltage
 - Up to 5000 V_{RMS} isolation rating
 - Up to 12.8 kV surge capability
 - ± 100 kV/ μs typical CMTI
- Wide supply range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V level translation
- Default output *high* (ISO7741) and *low* (ISO7741F) options
- Low power consumption, typical 1.5 mA per channel at 1 Mbps
- Low propagation delay: 10.7 ns typical (5-V Supplies)
- Robust electromagnetic compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - ± 8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
 - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-related certifications:
 - DIN VDE V 0884-11:2017-01
 - UL 1577 component recognition program
 - CSA certification according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 end equipment standards
 - CQC approval per GB4943.1-2011
 - TUV certification according to EN 60950-1, EN 62368-1 and EN 61010-1

2 Applications

- Hybrid, electric and power train system (EV/HEV)
 - Battery management system (BMS)
 - On-board charger
 - Traction inverter
 - DC/DC converter
 - Starter/generator
- Body electronics
 - Automotive parking heater module
 - HVAC compressor module
 - HVAC control module
 - HVAC sensor
 - Interior heater module

3 Description

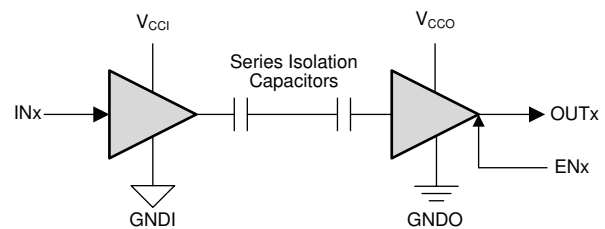
The ISO7741E-Q1 device is a grade 0, high-performance, quad-channel digital isolator with 5000 V_{RMS} isolation ratings per UL 1577. This device has reinforced insulation ratings according to VDE, CSA, TUV and CQC. The high temperature range up to 150°C makes this device suitable for applications like belt starter generators, water pumps, cooling fans, soot sensors etc., which may experience greater than 125°C ambient temperature.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7741E-Q1	SOIC (DW)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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V_{CCI}=Input supply, V_{CCO}=Output supply

GNDI=Input ground, GNDO=Output ground



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2019) to Revision A	Page
• Changed device status to production data	1

5 Description Continued

The ISO7741E-Q1 device provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO₂) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7741E-Q1 device has three forward and one reverse-direction channels. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the [Device Functional Modes](#) section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO7741E-Q1 device havehas been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO7741E-Q1 device is available in 16-pin SOIC package.

6 Pin Configuration and Functions

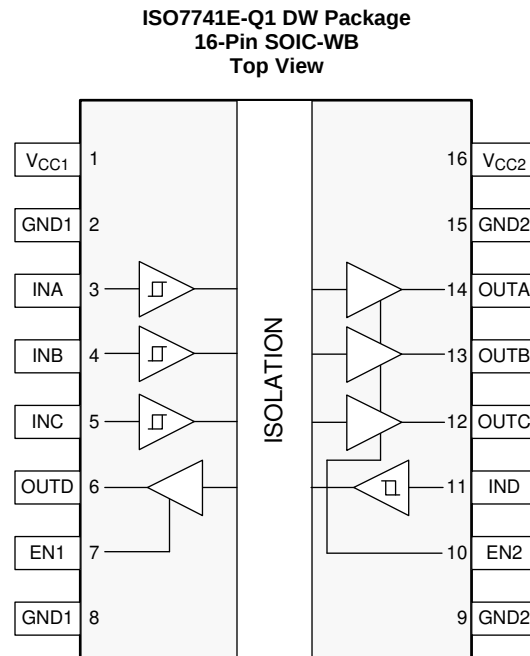


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V _{CC1}
	8		
GND2	9	—	Ground connection for V _{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V _{CC1}	1	—	Power supply, side 1
V _{CC2}	16	—	Power supply, side 2

7 Specifications

7.1 Absolute Maximum Ratings

See ⁽¹⁾

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage ⁽²⁾	−0.5	6	V
V	Voltage at INx, OUTx, ENx	−0.5	$V_{CCx} + 0.5^{(3)}$	V
I_O	Output current	−15	15	mA
T_J	Junction temperature		175	°C
T_{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	
		Contact Discharge per IEC 61000-4-2 Isolation Barrier Withstand Test ⁽²⁾⁽³⁾	±8000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	$V_{CCO}^{(1)} = 5\text{ V}$	−4			mA
		$V_{CCO} = 3.3\text{ V}$	−2			
		$V_{CCO} = 2.5\text{ V}$	−1			
I_{OL}	Low-level output current	$V_{CCO} = 5\text{ V}$			4	mA
		$V_{CCO} = 3.3\text{ V}$			2	
		$V_{CCO} = 2.5\text{ V}$			1	
V_{IH}	High-level input voltage		$0.7 \times V_{CCI}^{(1)}$		V_{CCI}	V
V_{IL}	Low-level input voltage		0		$0.3 \times V_{CCI}$	V
DR	Data rate		0		100	Mbps
T_A	Ambient temperature		−40	25	150	°C

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO7741E-Q1	UNIT
		DW (SOIC)	
		16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

7.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 175^\circ\text{C}$, $C_L = 15\text{ pF}$, Input a 50-MHz 50% duty cycle square wave			200	mW
P_{D1}	Maximum power dissipation by side-1				75	mW
P_{D2}	Maximum power dissipation by side-2				125	mW

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN VDE V 0884-11:2017-01 ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDb) Test; See Figure 22	1500	V _{RMS}
		DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 x V _{IOTM} , t= 1 s (100% production)	8000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.6 x V _{IOSM} (qualification)	8000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, After Input-output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 x V _{IORM} , t _m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 x V _{IORM} , t _m = 10 s	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 x V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 x V _{IORM} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 x sin (2pft), f = 1 MHz	~1	pF
R _{IO}	Isolation resistance ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1 s (100% production)	5000	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Maximum transient isolation voltage, 8000 V _{PK} Maximum repetitive peak isolation voltage, 2121 V _{PK} Maximum surge isolation voltage, 8000 V _{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1:2014 800 V _{RMS} max working voltage (pollution degree 2, material group I); Reinforced insulation per CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed. 300 V _{RMS} max working voltage (overvoltage category III)	Single protection, 5000 V _{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage;	5000 V _{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} 5000 V _{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V _{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 83.4 °C/W, V _I = 5.5 V, T _J = 175°C, T _A = 25°C, see Figure 1			327	mA
		R _{θJA} = 83.4 °C/W, V _I = 3.6 V, T _J = 175°C, T _A = 25°C, see Figure 1			500	
		R _{θJA} = 83.4 °C/W, V _I = 2.75 V, T _J = 175°C, T _A = 25°C, see Figure 1			654	
P _S	Safety input, output, or total power	R _{θJA} = 83.4 °C/W, T _J = 175°C, T _A = 25°C, see Figure 2			1799	mW
T _S	Maximum safety temperature				175	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.

P_S = I_S × V_I, where V_I is the maximum input voltage.

7.9 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -4\text{ mA}$; see Figure 9	$V_{CCO}^{(1)} - 0.4$	4.8		V
V_{OL}	Low-level output voltage $I_{OL} = 4\text{ mA}$; see Figure 9		0.2	0.4	V
$V_{IT+(IN)}$	Rising input voltage threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0\text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 12	85	100		kV/ μs
C_i	Input Capacitance ⁽²⁾ $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

(2) Measured from input pin to ground.

7.10 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	$EN1 = EN2 = 0\text{ V}$; $V_I = V_{CCI}^{(1)}$ (ISO7741E-Q1); $V_I = 0\text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1	1.7	mA
		I_{CC2}		0.7	1.3	
	$EN1 = EN2 = 0\text{ V}$; $V_I = 0\text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.3	6.5	
		I_{CC2}		1.8	2.9	
Supply current - DC signal	$EN1 = EN2 = V_{CCI}$; $V_I = V_{CCI}$ (ISO7741E-Q1); $V_I = 0\text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1.5	2.4	
		I_{CC2}		2	3.5	
	$EN1 = EN2 = V_{CCI}$; $V_I = 0\text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.8	7.3	
		I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}	3.2	5	
			I_{CC2}	2.8	4.4	
		10 Mbps	I_{CC1}	3.7	5.2	
			I_{CC2}	4.2	6.2	
		100 Mbps	I_{CC1}	8.6	11.3	
			I_{CC2}	18	22	

(1) V_{CCI} = Input-side V_{CC}

7.11 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -2 \text{ mA}$; see Figure 9	$V_{CCO}^{(1)} - 0.3$	3.2		V
V_{OL}	Low-level output voltage $I_{OL} = 2 \text{ mA}$; see Figure 9		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0 \text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; see Figure 12	85	100		kV/ μs

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

7.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CCI}^{(1)}$ (ISO7741E-Q1); $V_I = 0 \text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1	1.7	mA
		I_{CC2}		0.7	1.3	
	EN1 = EN2 = 0 V; $V_I = 0 \text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.3	6.4	
		I_{CC2}		1.9	2.8	
Supply current - DC signal	EN1 = EN2 = V_{CCI} ; $V_I = V_{CCI}$ (ISO7741E-Q1); $V_I = 0 \text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1.5	2.4	
		I_{CC2}		2	3.5	
	EN1 = EN2 = V_{CCI} ; $V_I = 0 \text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.8	7.2	
		I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps				
		I_{CC1}		3.2	4.6	
		I_{CC2}		2.7	4.3	
		10 Mbps				
		I_{CC1}		3.5	5	
		I_{CC2}		3.7	5.4	
		100 Mbps				
		I_{CC1}		6.8	9.3	
		I_{CC2}		13.7	16.5	

 (1) V_{CCI} = Input-side V_{CC}

7.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -1 \text{ mA}$; see Figure 9	$V_{CCO}^{(1)} - 0.2$	2.45		V
V_{OL}	Low-level output voltage $I_{OL} = 1 \text{ mA}$; see Figure 9		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0 \text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; see Figure 12	85	100		kV/ μs

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

7.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	$EN1 = EN2 = 0 \text{ V}$; $V_I = V_{CCI}^{(1)}$ (ISO7741E-Q1); $V_I = 0 \text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1	1.7	mA
		I_{CC2}		0.7	1.2	
	$EN1 = EN2 = 0 \text{ V}$; $V_I = 0 \text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.3	6.4	
		I_{CC2}		1.8	2.8	
Supply current - DC signal	$EN1 = EN2 = V_{CCI}$; $V_I = V_{CCI}$ (ISO7741E-Q1); $V_I = 0 \text{ V}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		1.4	2.4	mA
		I_{CC2}		2	3.4	
	$EN1 = EN2 = V_{CCI}$; $V_I = 0 \text{ V}$ (ISO7741E-Q1); $V_I = V_{CCI}$ (ISO7741E-Q1 with F suffix)	I_{CC1}		4.7	7.2	
		I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps	I_{CC1}	3.1	5	
			I_{CC2}	2.7	4.4	
		10 Mbps	I_{CC1}	3.4	4.9	
			I_{CC2}	3.5	5.1	
		100 Mbps	I_{CC1}	6.2	8.3	
			I_{CC2}	10.8	13.8	

(1) V_{CCI} = Input-side V_{CC}

7.15 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	6	10.7	16.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.4	ns
t_r	Output signal rise time	See Figure 9		2.4	4.1	ns
t_f	Output signal fall time			2.4	4.1	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		9	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			9	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			7	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 12		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.8		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.16 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	6	11	16.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.5	ns
t_r	Output signal rise time	See Figure 9		1.3	3.1	ns
t_f	Output signal fall time			1.3	3.1	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3.2	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3.2	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 12		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.9		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	7.5	12	19	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.2	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction Channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.6	ns
t_r	Output signal rise time	See Figure 9		1	3.6	ns
t_f	Output signal fall time			1	3.6	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3.3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3.3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 12		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.7		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.18 Insulation Characteristics Curves

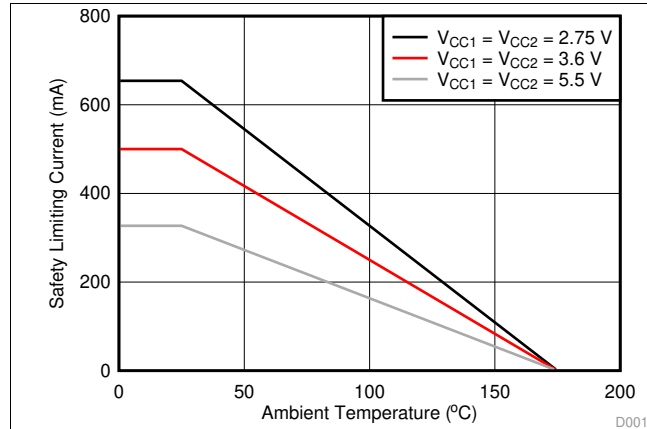


Figure 1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

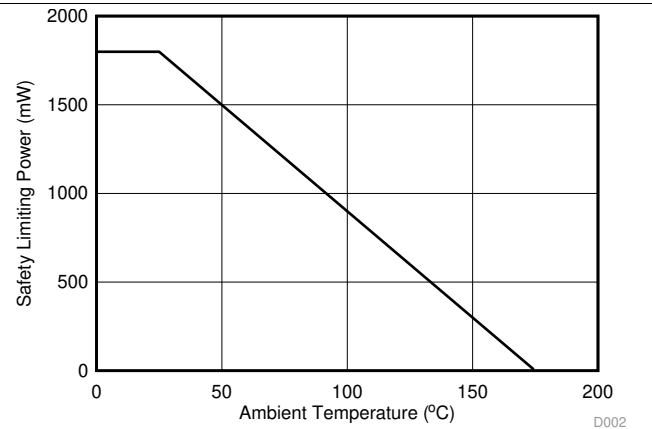


Figure 2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

7.19 Typical Characteristics

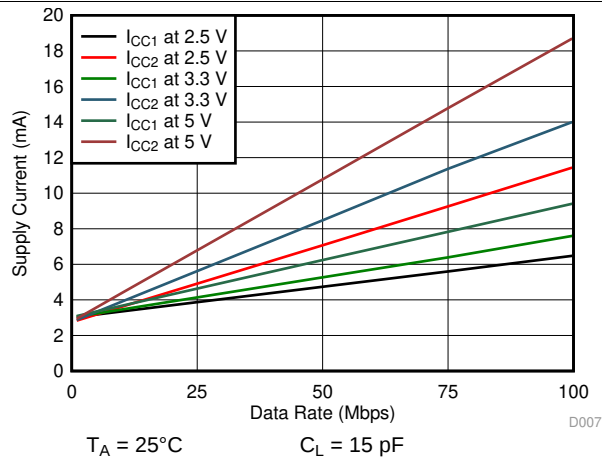


Figure 3. Supply Current vs Data Rate (With 15-pF Load)

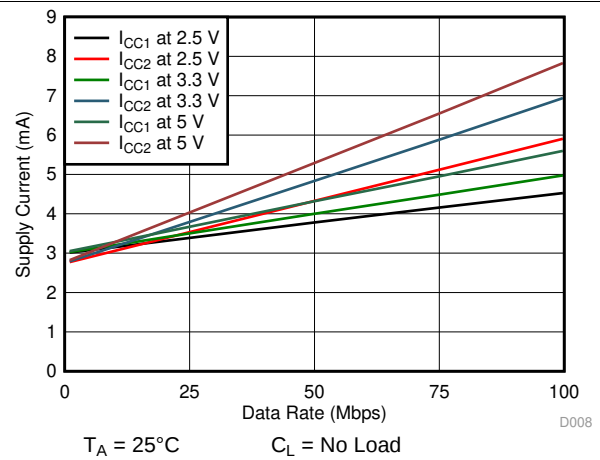


Figure 4. Supply Current vs Data Rate (With No Load)

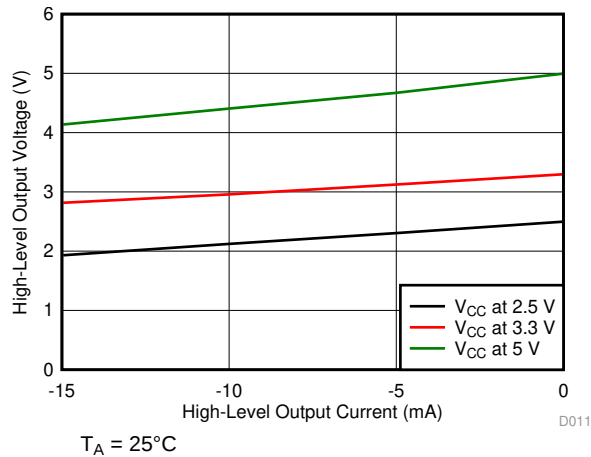


Figure 5. High-Level Output Voltage vs High-level Output Current

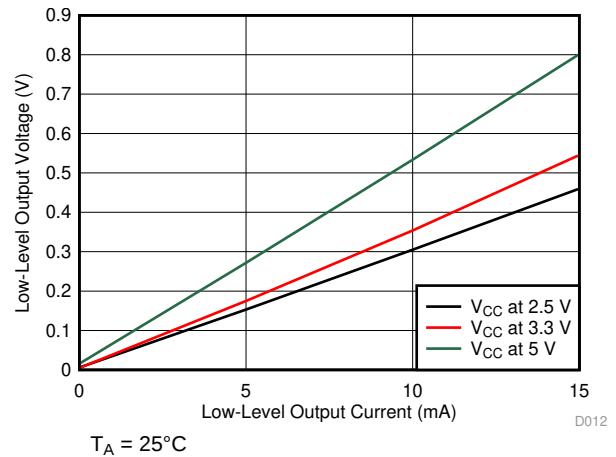


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

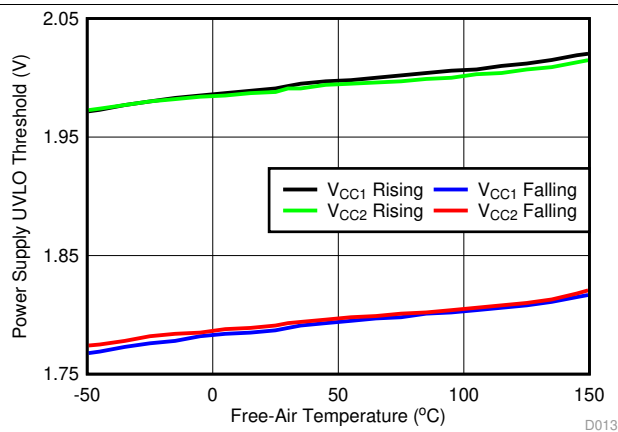


Figure 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

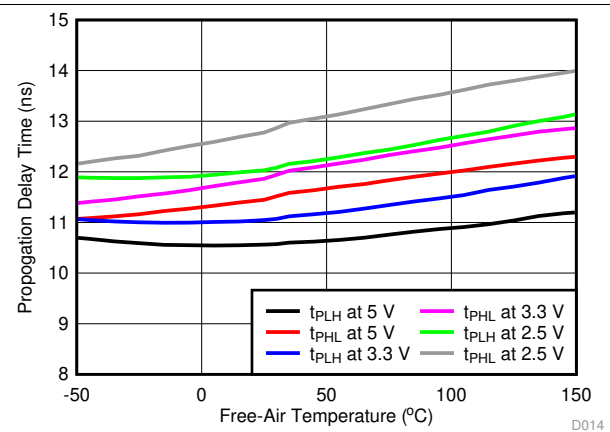
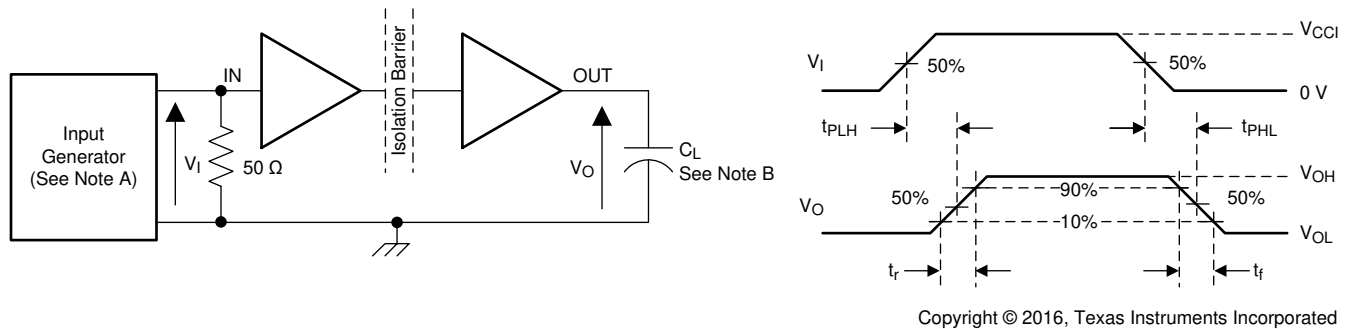


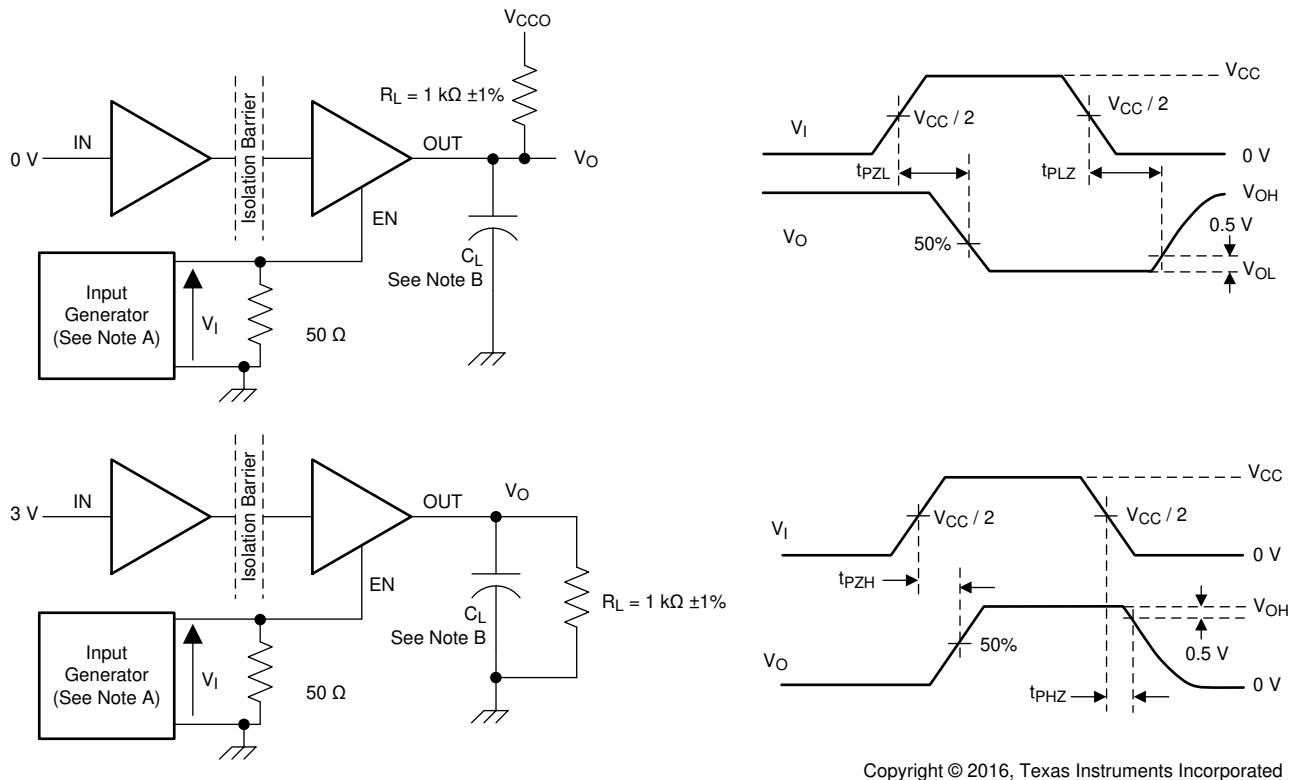
Figure 8. Propagation Delay Time vs Free-Air Temperature

8 Parameter Measurement Information



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 9. Switching Characteristics Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 10$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 10. Enable/Disable Propagation Delay Time Test Circuit and Waveform

IN = 0 V (Devices without suffix F)
IN = V_{CC} (Devices with suffix F)

See Note B

See Note A

Timing diagram showing input voltage V_I and output voltage V_O transitions. Key parameters include V_{CC} , 0 V , 1.7 V , t_{DO} , V_{OH} , V_{OL} , and 50% transition point.

- ### Figure 11. Default Output Delay Time Test Circuit and Voltage Waveforms



Figure 12. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISO7741E-Q1 device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO7741E-Q1 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 13](#), shows a functional block diagram of a typical channel.

9.2 Functional Block Diagram

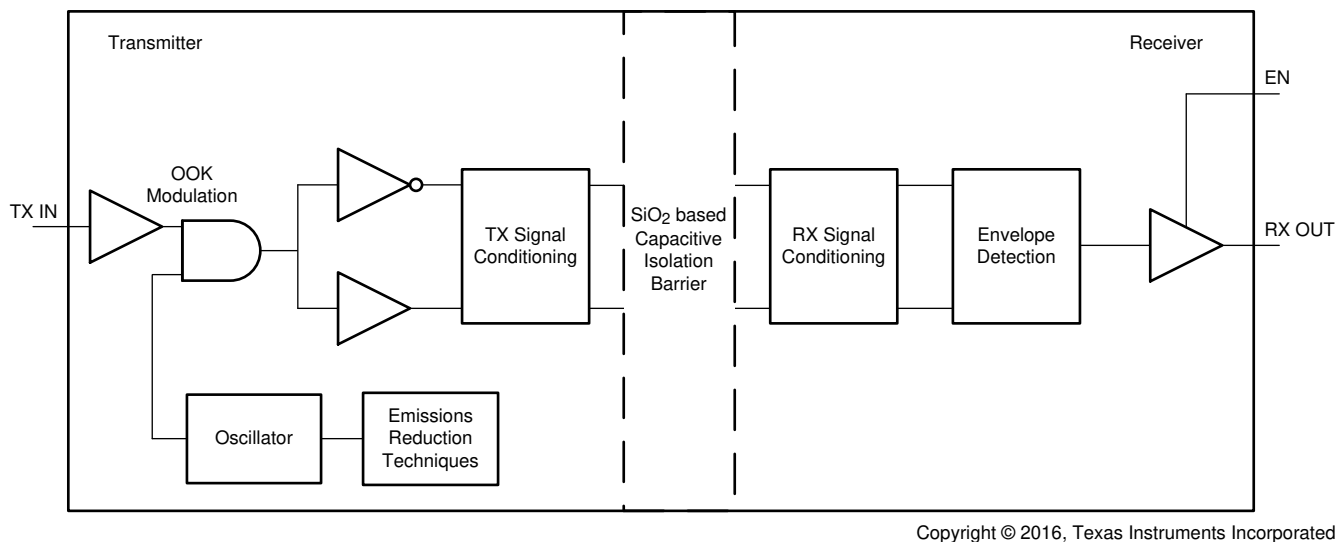


Figure 13. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 14](#) shows a conceptual detail of how the ON-OFF keying scheme works.

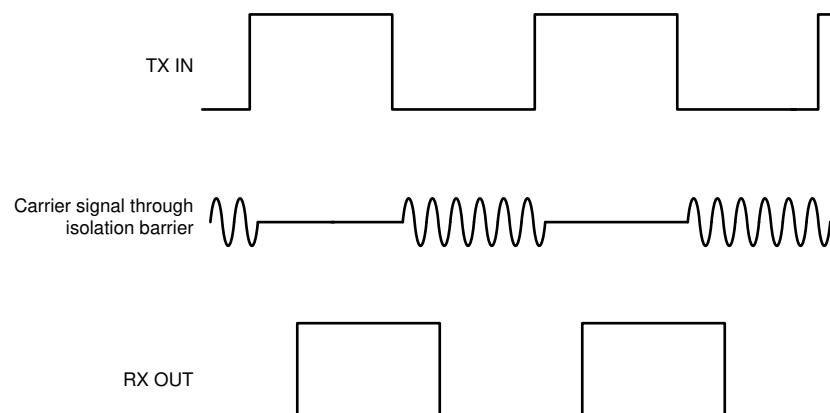


Figure 14. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

provides an overview of the device features.

Table 2. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7741E-Q1	3 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
ISO7741E-Q1 with F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}

9.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7741E-Q1 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.4 Device Functional Modes

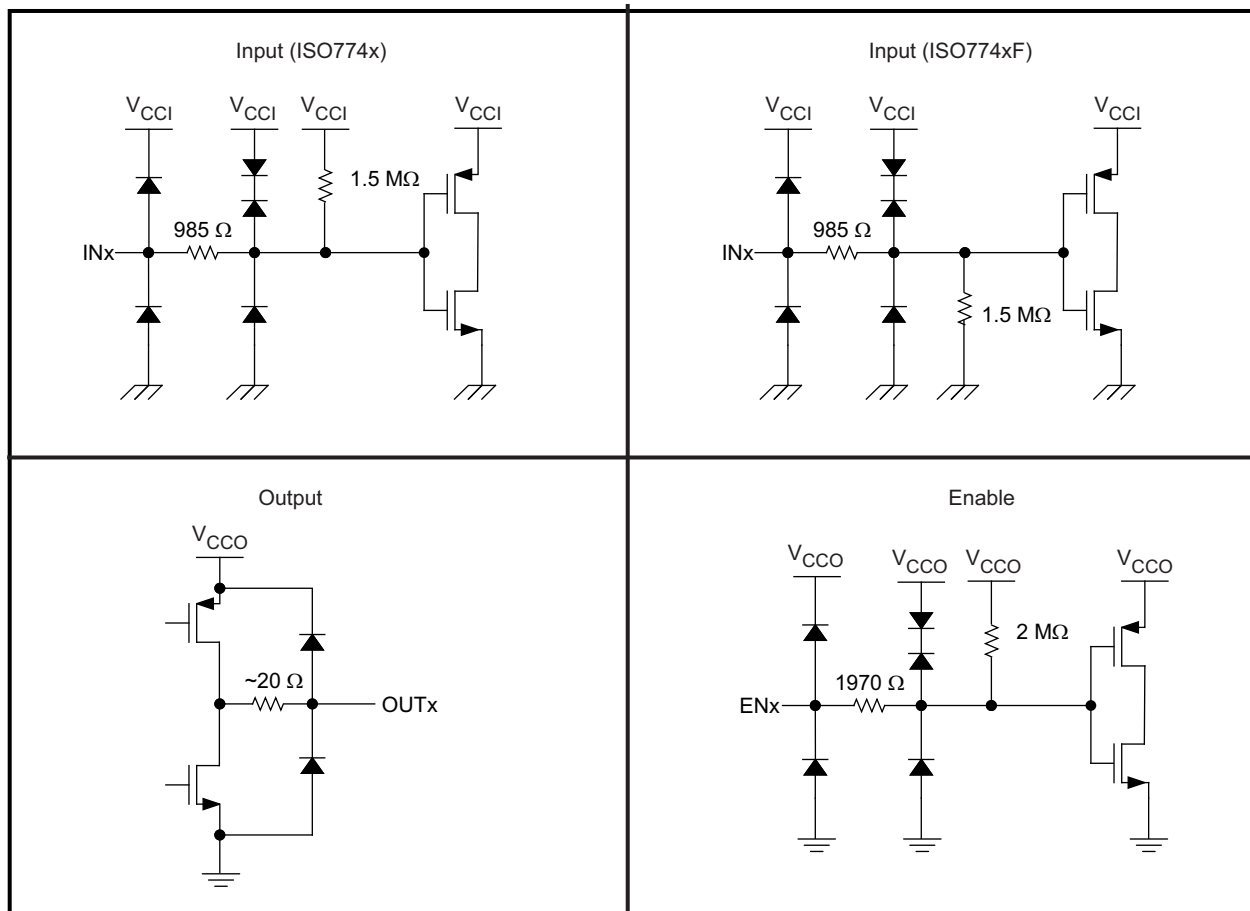
Table 3 lists the functional modes for the ISO7741E-Q1 device.

Table 3. Function Table⁽¹⁾

V_{CCI}	V_{CCO}	INPUT (INx) ⁽²⁾	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for ISO7741E-Q1 and <i>Low</i> for ISO7741E-Q1 with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO7741E-Q1 and <i>Low</i> for ISO7741E-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined ⁽³⁾ . When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.7$ V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
- (2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
- (3) The outputs are in undetermined state when 1.7 V < V_{CCI} , $V_{CCO} < 2.25$ V.

9.4.1 Device I/O Schematics



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Figure 15. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO7741E-Q1 devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. The ISO7741E-Q1 devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

Figure 16 shows ISO7741E-Q1 in belt starter generator application.

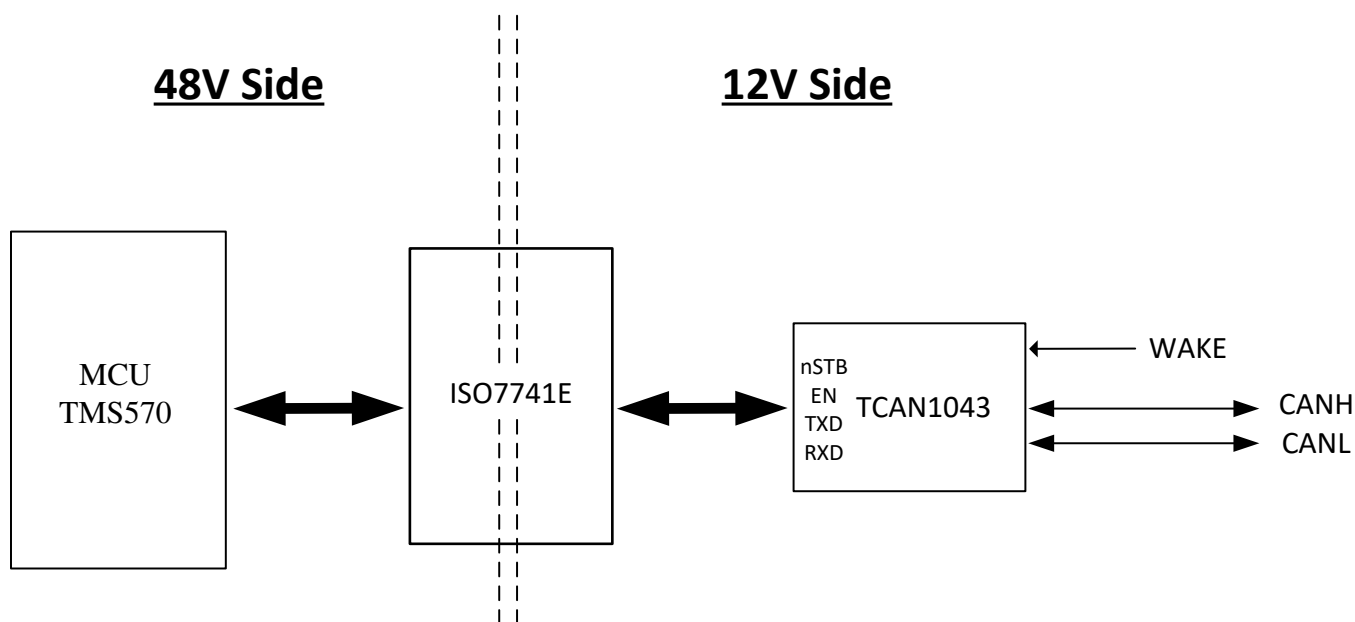


Figure 16. Belt Starter Generator Application

Typical Application (continued)

10.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 4](#).

Table 4. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

10.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7741E-Q1 device only require two external bypass capacitors to operate.

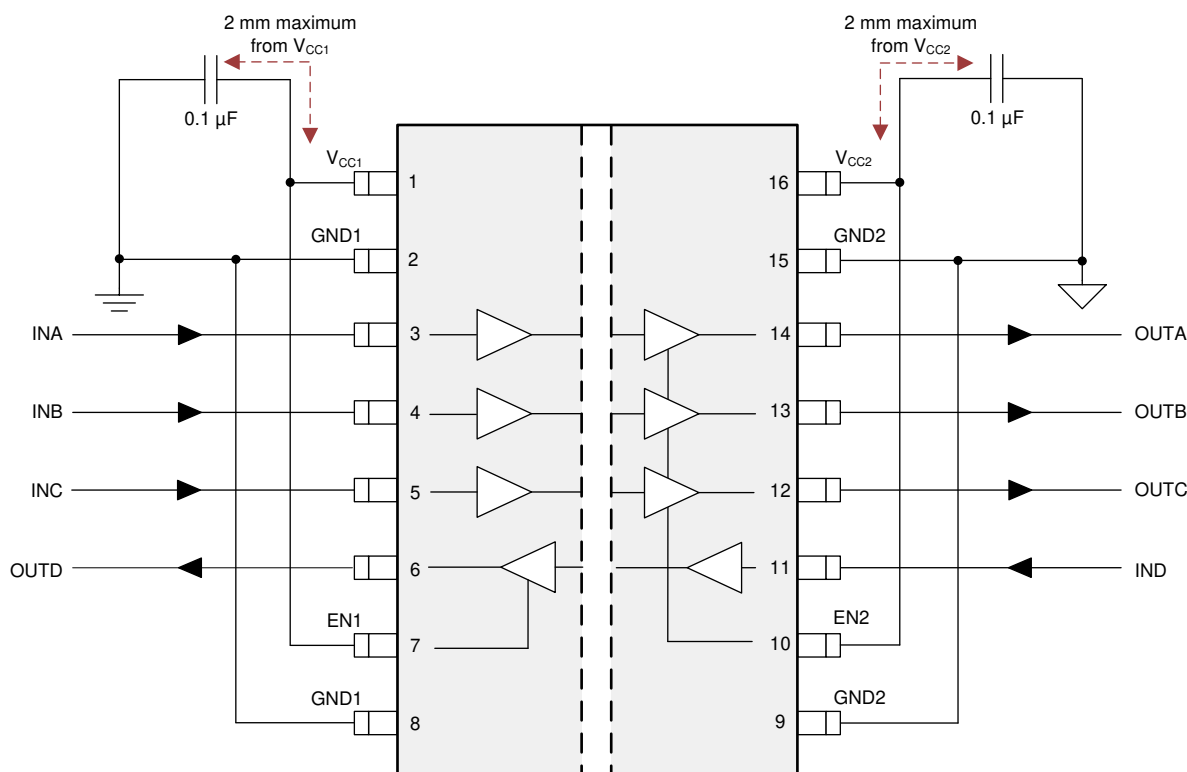


Figure 17. Typical ISO7741E-Q1 Circuit Hook-up

10.2.3 Application Curve

The following typical eye diagrams of the ISO7741E-Q1 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

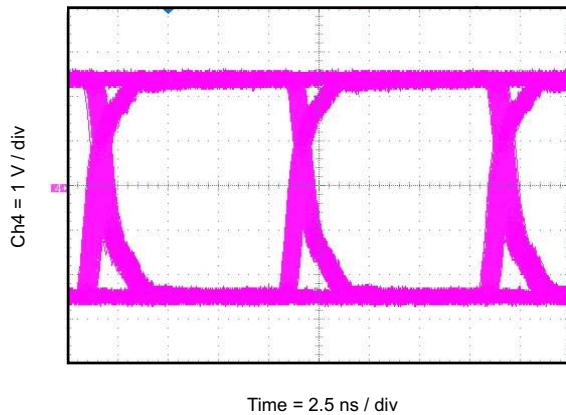


Figure 18. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 5 V and 25°C

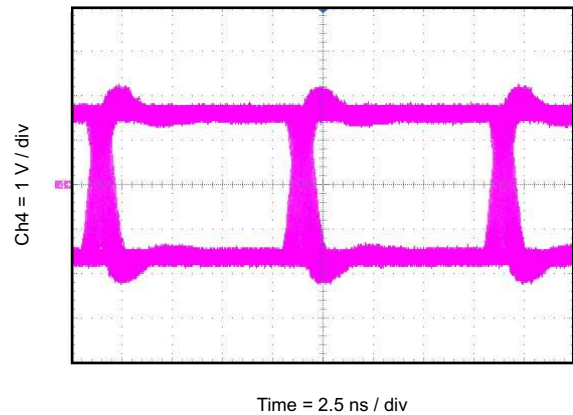


Figure 19. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 3.3 V and 25°C

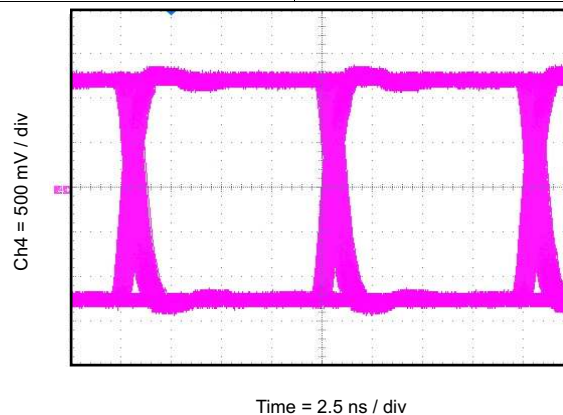


Figure 20. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 2.5 V and 25°C

10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 21](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

[Figure 22](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS} and DBQ-16 package up to 400 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

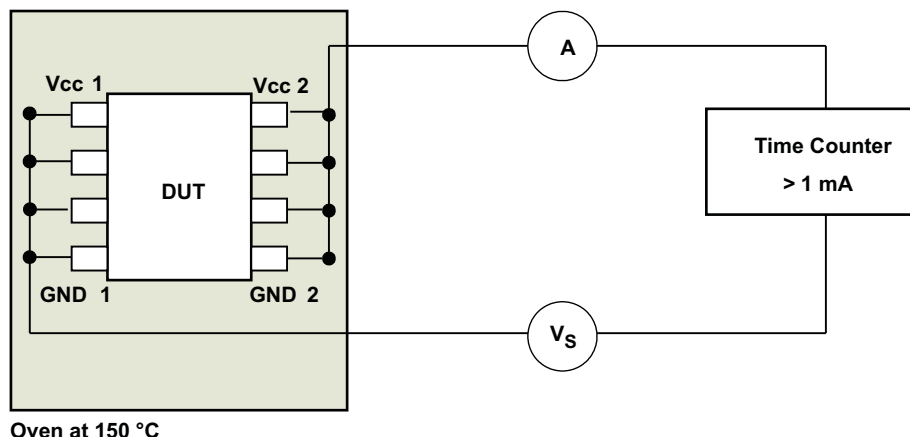


Figure 21. Test Setup for Insulation Lifetime Measurement

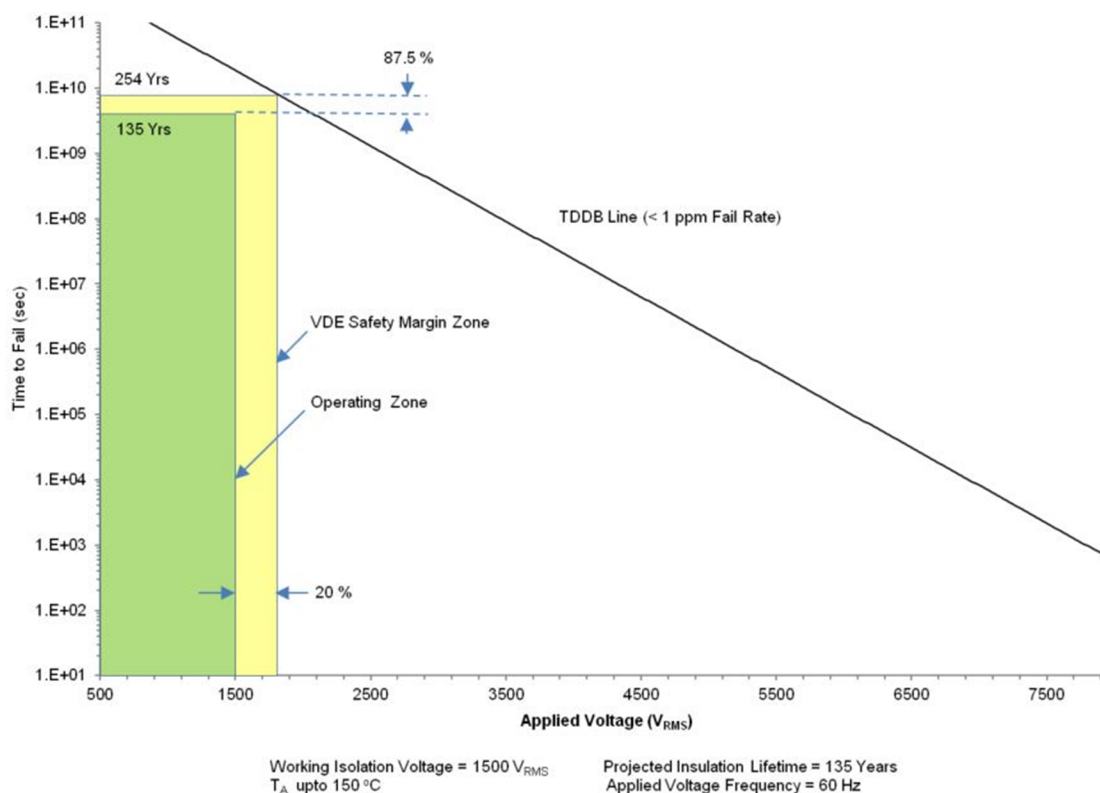


Figure 22. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501-Q1](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501-Q1 Transformer Driver for Isolated Power Supplies data sheet](#).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 23](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

12.2 Layout Example

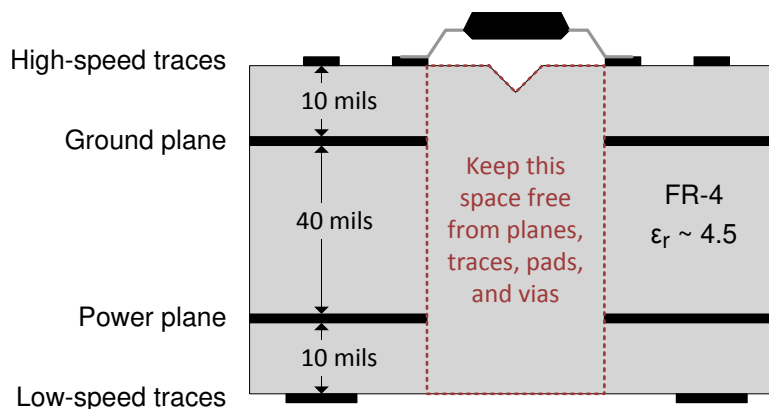


Figure 23. Layout Example Schematic

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems application report](#)
- Texas Instruments, [TCAN1043xx-Q1 Low-Power Fault Protected CAN Transceiver with CAN FD and Wake data sheet](#)
- Texas Instruments, [TMS570LS0714 16- and 32-Bit RISC Flash Microcontroller data sheet](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7741EDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741E	Samples
ISO7741EDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741E	Samples
ISO7741FEDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741FE	Samples
ISO7741FEDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741FE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

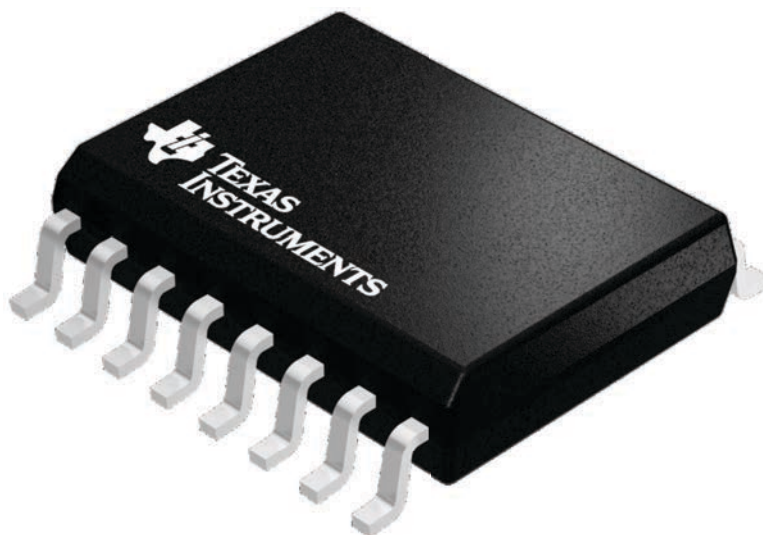
DW 16

SOIC - 2.65 mm max height

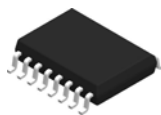
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

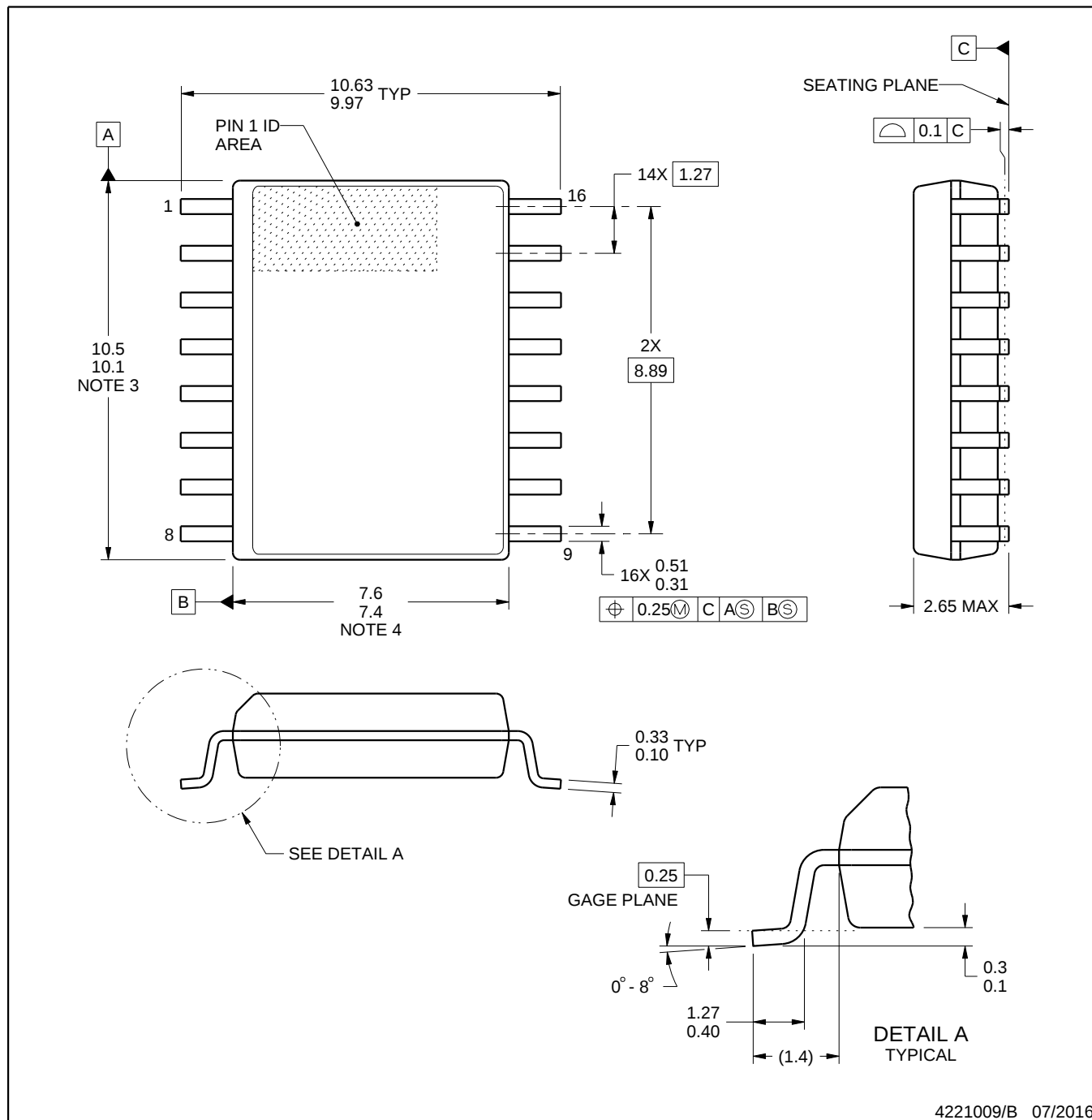


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

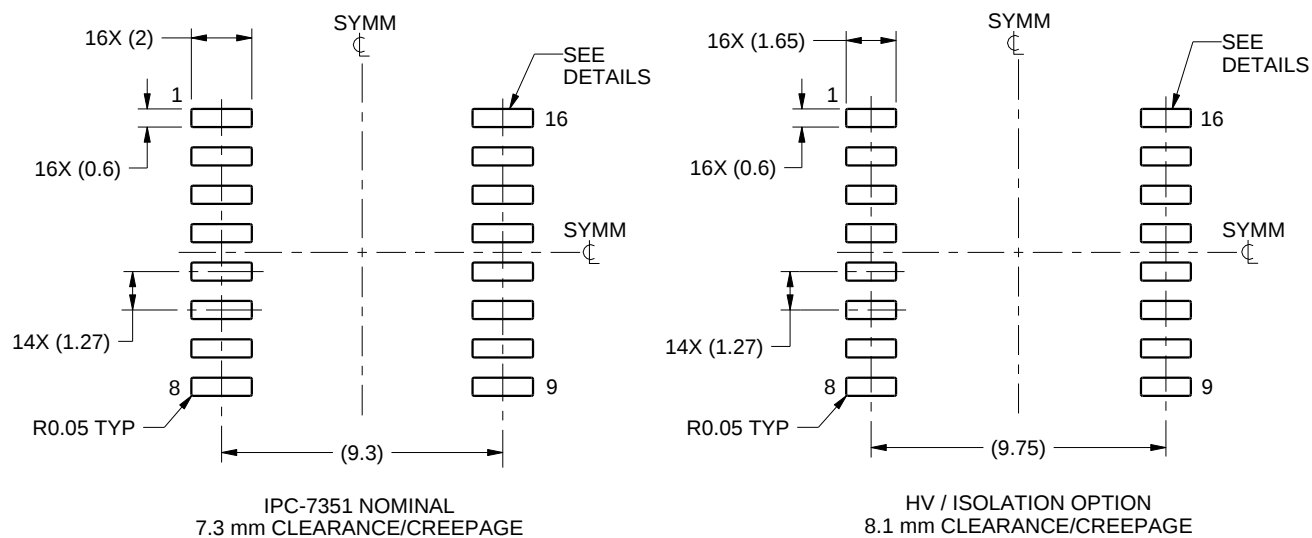
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

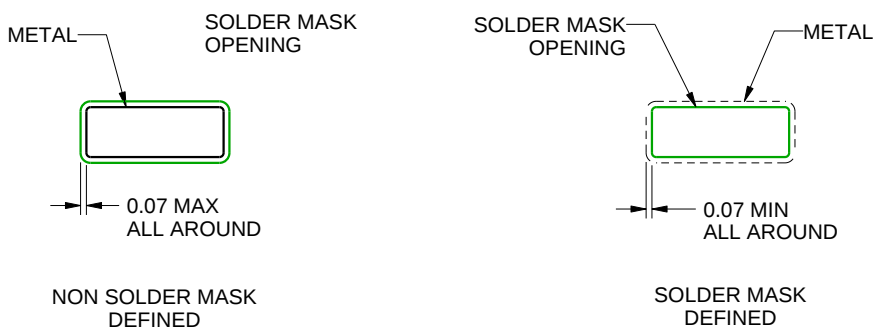
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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NOTES: (continued)

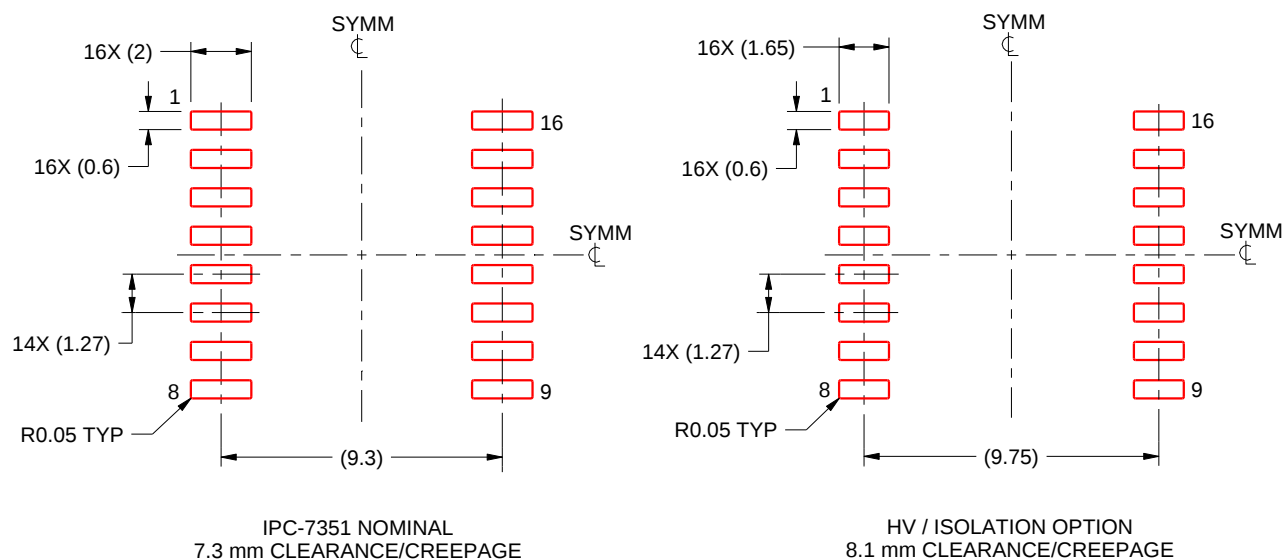
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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