ISO734x-Q1 Robust EMC, Low-Power, Quad-Channel Reinforced Digital Isolators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 3A
  - Device CDM Classification Level C6
- Signaling Rate: 25 Mbps
- Integrated Noise Filter on the Inputs
- Default Output *High* and *Low* Options
- Low Power Consumption, Typical I_{CC} per Channel at 1 Mbps:
  - ISO7340-Q1: 0.9 mA (5-V Supplies), 0.7 mA (3.3-V Supplies)
  - ISO7341-Q1: 1.2 mA (5-V Supplies), 0.9 mA (3.3-V Supplies)
  - ISO7342-Q1: 1.3 mA (5-V Supplies), 0.9 mA (3.3-V Supplies)
- Low Propagation Delay: 31 ns Typical (5-V Supplies)
- 3.3-V and 5-V Level Translation
- 70-KV/µs Transient Immunity, Typical (5-V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and Surge Immunity
  - Low Emissions
- Operates from 3.3-V and 5-V Supplies
- Wide-Body SOIC-16 Package
- Safety-Related Certifications:
  - 4242-V_{PK} Basic Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 3-KV_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - GB4943.1-2011 CQC Certified

2 Applications

- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

The ISO734x-Q1 family of devices provides galvanic isolation up to 3000 V_{RMS} for 1 minute per UL 1577 and 4242 V_{PK} per VDE V 0884-10. These devices have four isolated channels comprised of logic input and output buffers separated by a silicon dioxide (SiO_2) insulation barrier.

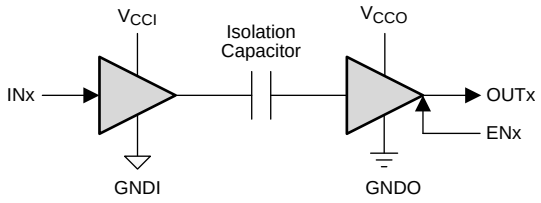
The ISO7340-Q1 device has four channels in forward direction, the ISO7341-Q1 device has three forward and one reverse-direction channels, and the ISO7342-Q1 device has two forward and two reverse-direction channels. In case of input power or signal loss, the default output is *low* for orderable part numbers with suffix *F* and *high* for orderable part numbers without suffix *F*. See the *Device Functional Modes* section for further details.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
ISO7340-Q1	SOIC (16)	10.30 mm × 7.50 mm
ISO7341-Q1		
ISO7342-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to Revision A	Page
• CQC certification is now certified instead of planned	1
• Changed the minimum air gap (clearance) parameter (L(I01)) to the external clearance parameter	7
• Changed the minimum external tracking (creepage) parameter (L(I02)) to the external creepage parameter	7
• Changed the input-to-output test voltage parameter (V_{PR}) to the apparent charge parameter (q_{pd})	7
• Changed the typ value for the enable propagation delay, high impedance-to-high output parameter of the FC devices and the typ value for the enable propagation delay, high impedance-to-low output parameter of the C devices from 16 to 16000 in the *Switching Characteristics—3.3-V Supply* table	11
• Added the *Receiving Notification of Documentation Updates* section	26

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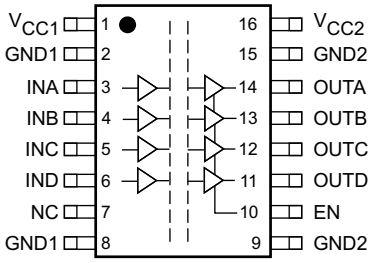
5 Description (continued)

Used in conjunction with isolated power supplies, these devices help prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The ISO734x-Q1 device has integrated noise filter for harsh industrial environment where short noise pulses may be present at the device input pins. The ISO734x-Q1 device has TTL input thresholds and operates from 3-V to 5.5-V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO734x-Q1 family of devices has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance.

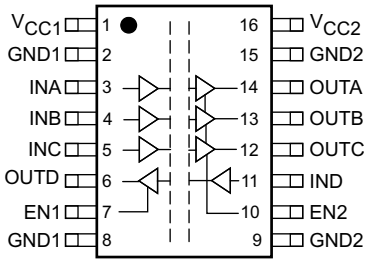
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6 Pin Configuration and Functions

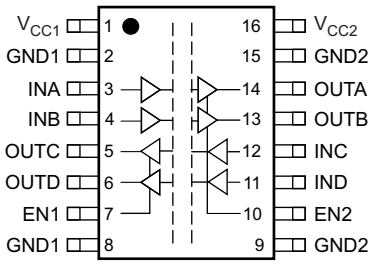
DW Package
16-Pin SOIC
ISO7340-Q1 Top View



DW Package
16-Pin SOIC
ISO7341-Q1 Top View



DW Package
16-Pin SOIC
ISO7342-Q1 Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	ISO7340-Q1	ISO7341-Q1	ISO7342-Q1		
EN	10	—	—	I	Output enable. All output pins are enabled when EN is high or disconnected and disabled when EN is low.
EN1	—	7	7	I	Output enable 1. Output pins on side-1 are enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN2 is high or disconnected and disabled when EN2 is low.
GND1	2	2	2	—	Ground connection for V_{CC1}
	8	8	8		
GND2	9	9	9	—	Ground connection for V_{CC2}
	15	15	15		
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
NC	7	—	—	—	No connect pins are floating with no internal connection
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	—	Power supply, V_{CC2}

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7 Specifications

7.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (2)	V_{CC1}, V_{CC2}	–0.5	6	V
	Voltage	INx, OUTx, ENx	–0.5	V_{CC} + 0.5 (3)	V
I_O	Output current			±15	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
1 / t_{ui}	Signaling rate	0		25	Mbps
T_J	Junction temperature (1)			136	°C
T_A	Ambient temperature	–40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

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7.4 Thermal Information

THERMAL METRIC[1]		ISO734x-Q1 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5-MHz 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation by both sides of ISO7340-Q1				92	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7340-Q1				24	
P_{D2}	Maximum power dissipation by side-2 of ISO7340-Q1				68	
P_D	Maximum power dissipation by both sides of ISO7341-Q1				102	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7341-Q1				42	
P_{D2}	Maximum power dissipation by side-2 of ISO7341-Q1				60	
P_D	Maximum power dissipation by both sides of ISO7342-Q1				111	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7342-Q1				55.5	
P_{D2}	Maximum power dissipation by side-2 of ISO7342-Q1				55.5	

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7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>13	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group		II	
	Overvoltage Category	Rated mains voltage ≤ 300 V_{RMS}	I–IV	
		Rated mains voltage ≤ 600 V_{RMS}	I–III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1697\ V_{PK}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2262\ V_{PK}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2651\ V_{PK}$, t_m = 1 s (100% production)	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	2.4	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ x°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 3000\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 3600\ V_{RMS}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

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7.7 Safety-Related Certifications

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized component under UL 1577	Certified according to GB4943.1-2011
Basic Insulation; Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Surge Isolation Voltage, 6000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 1414 V_{PK}	800 V_{RMS} Basic Insulation and 400 V_{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

(1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.4 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			290	mA
		$R_{\theta JA}$ = 78.4 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			443	
T_S	Safety temperature				150	

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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7.9 Electrical Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 14	V_{CCO} (1) – 0.5	4.7		V
		I_{OH} = –20 μA; see Figure 14	V_{CCO} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 14		0.2	0.4	V
		I_{OL} = 20 μA; see Figure 14		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			480		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 17	25	70		kV/μs
C_I	Input capacitance (2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		3.4		pF

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.
(2) Measured from input pin to ground.

7.10 Supply Current Characteristics—5-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7340-Q1							
Supply current	EN = 0 V	Disable	I_{CC1}		0.6	1.4	mA
			I_{CC2}		0.4	0.8	
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}		0.6	1.4	
			I_{CC2}		3.2	4.8	
		10 Mbps	I_{CC1}		1.4	2.3	
			I_{CC2}		5.6	7.1	
		25 Mbps	I_{CC1}		2.7	4	
			I_{CC2}		9.3	12	
ISO7341-Q1							
Supply current	EN1 = EN2 = 0 V	Disable	I_{CC1}		0.8	1.8	mA
			I_{CC2}		0.7	1.3	
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}		2	3.2	
			I_{CC2}		2.9	4.4	
		10 Mbps	I_{CC1}		3.2	4.5	
			I_{CC2}		4.9	6.5	
		25 Mbps	I_{CC1}		5	7	
			I_{CC2}		7.8	11	
ISO7342-Q1							
Supply current	EN1 = EN2 = 0 V	Disable	I_{CC1}, I_{CC2}		0.7	1.6	mA
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}, I_{CC2}		2.5	4	
		10 Mbps	I_{CC1}, I_{CC2}		4.1	5.6	
		25 Mbps	I_{CC1}, I_{CC2}		6.4	9	

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7.11 Electrical Characteristics—3.3-V Supply

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 14	V_{CCO} (1) – 0.5	3		V
		I_{OH} = –20 μA; see Figure 14	V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 14		0.2	0.4	V
		I_{OL} = 20 μA; see Figure 14		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 17	25	50		kV/μs

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

7.12 Supply Current Characteristics—3.3-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7340-Q1							
Supply current	EN = 0 V	Disable	I_{CC1}		0.4	0.7	mA
			I_{CC2}		0.3	0.6	
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}		0.4	0.7	
			I_{CC2}		2.3	3.6	
		10 Mbps	I_{CC1}		0.9	1.3	
			I_{CC2}		3.9	5.1	
		25 Mbps	I_{CC1}		1.6	2.4	
			I_{CC2}		6.3	8	
ISO7341-Q1							
Supply current	EN1 = EN2 = 0 V	Disable	I_{CC1}		0.6	1	mA
			I_{CC2}		0.5	0.8	
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}		1.4	2.3	
			I_{CC2}		2.2	3.2	
		10 Mbps	I_{CC1}		2.2	3	
			I_{CC2}		3.4	4.5	
		25 Mbps	I_{CC1}		3.3	4.7	
			I_{CC2}		5.2	7.2	
ISO7342-Q1							
Supply current	EN1 = EN2 = 0 V	Disable	I_{CC1}, I_{CC2}		0.5	0.9	mA
	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF	DC to 1 Mbps	I_{CC1}, I_{CC2}		1.8	2.8	
		10 Mbps	I_{CC1}, I_{CC2}		2.8	4	
		25 Mbps	I_{CC1}, I_{CC2}		4.3	5.8	

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7.13 Switching Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 14	20	31	58	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$					4	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time		Same-direction Channels			2.5	ns
			Opposite-direction Channels			17	ns
$t_{sk(pp)}$(3)	Part-to-part skew time					23	ns
t_r	Output signal rise time		See Figure 14		2.1		ns
t_f	Output signal fall time				1.7		ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 15		7	13	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				7	13	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO734xCQDWQ1 and ISO734xCQDWRQ1			7	13	ns
		ISO734xFCQDWQ1 and ISO734xFCQDWRQ1			15000	23000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO734xCQDWQ1 and ISO734xCQDWRQ1			15000	23000(4)	ns
		ISO734xFCQDWQ1 and ISO734xFCQDWRQ1			7	13	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 16		9.4		µs

(1) Also known as *Pulse Skew*.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 43 Kbps.

7.14 Switching Characteristics—3.3-V Supply

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 14	22	35	66	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$					2.5	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time		Same-direction Channels			3	
			Opposite-direction Channels			16	
$t_{sk(pp)}$ (3)	Part-to-part skew time					28	
t_r	Output signal rise time		See Figure 14		2.8		ns
t_f	Output signal fall time				2.1		
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 15		9	18	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				9	18	
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO734xCQDWQ1 and ISO734xCQDWRQ1			9	18	
		ISO734xFCQDWQ1 and ISO734xFCQDWRQ1			16000	24000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO734xCQDWQ1 and ISO734xCQDWRQ1			16000	24000(4)	
		ISO734xFCQDWQ1 and ISO734xFCQDWRQ1			9	18	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 16		9.4		µs

(1) Also known as *Pulse Skew*.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 45 Kbps.

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7.15 Insulation Characteristics Curves

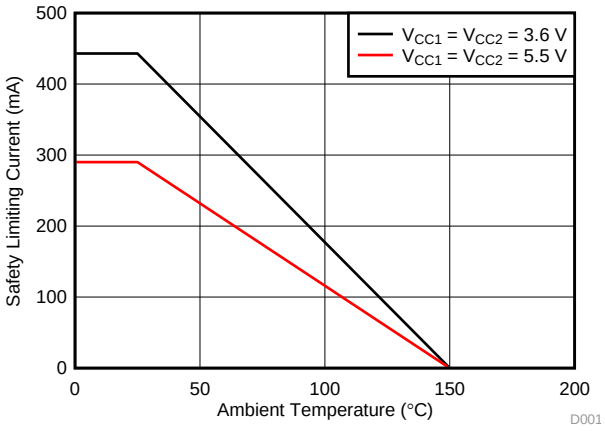
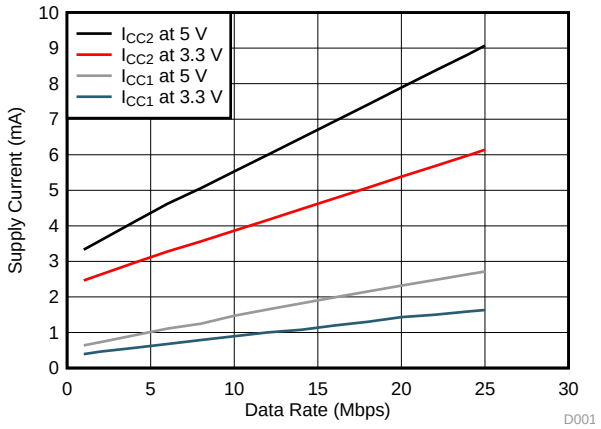


Figure 1. Thermal Derating Curve for Limiting Current per VDE

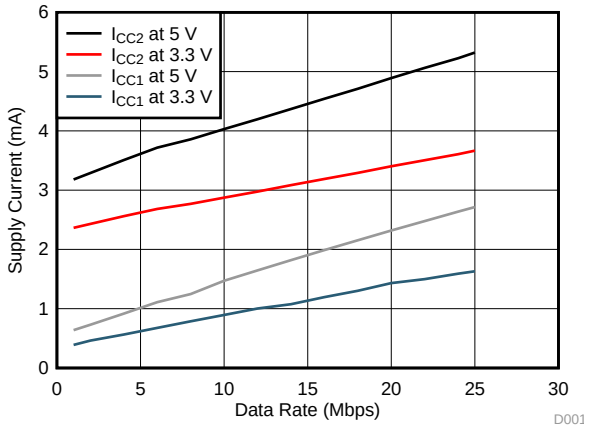
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7.16 Typical Characteristics



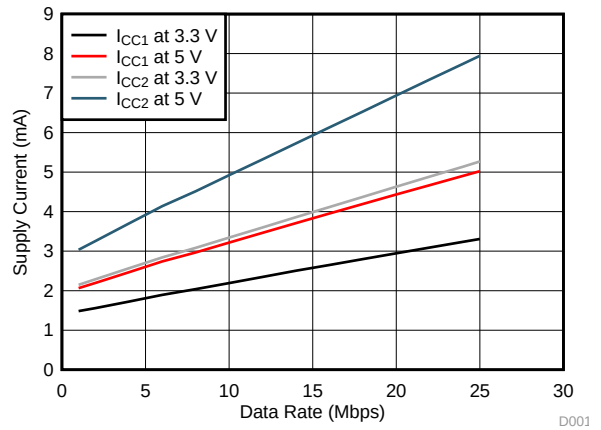
T_A = 25°C C_L = 15 pF

Figure 2. ISO7340-Q1 Supply Current vs Data Rate (15-pF Load)



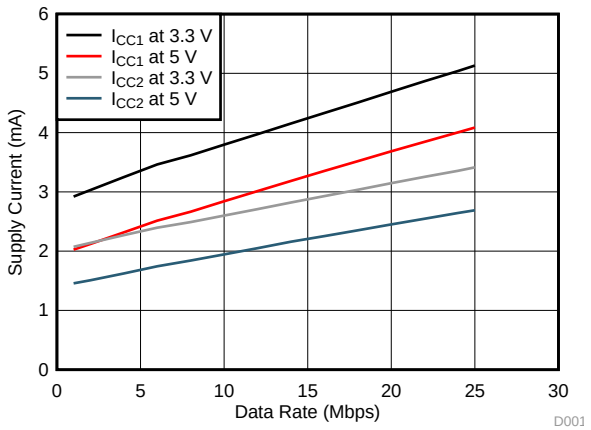
T_A = 25°C C_L = No Load

Figure 3. ISO7340-Q1 Supply Current vs Data Rate (No Load)



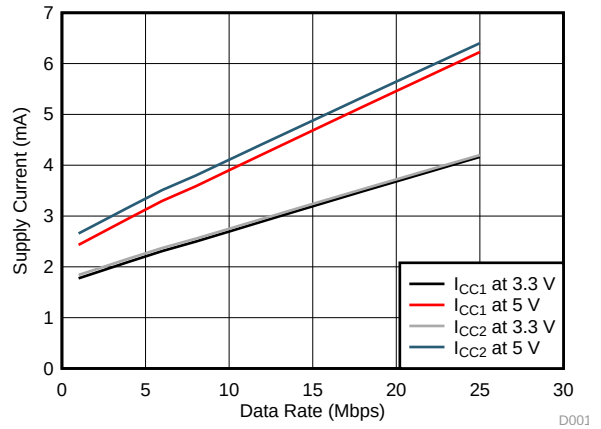
T_A = 25°C C_L = 15 pF

Figure 4. ISO7341x-Q1 Supply Current vs Data Rate (15-pF Load)



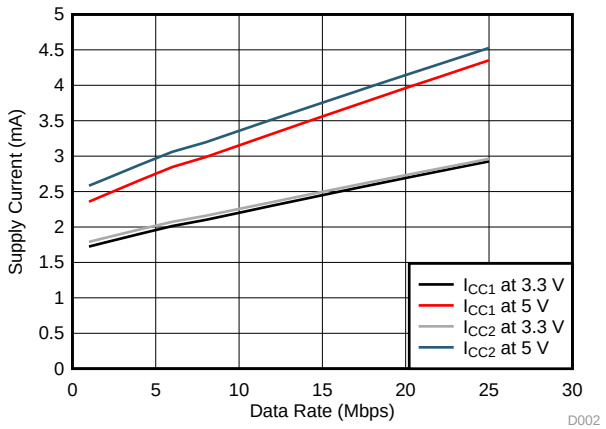
T_A = 25°C C_L = No Load

Figure 5. ISO7341x-Q1 Supply Current vs Data Rate (No Load)



T_A = 25°C C_L = 15 pF

Figure 6. ISO7342x-Q1 Supply Current vs Data Rate (15-pF Load)



T_A = 25°C C_L = No Load

Figure 7. ISO7342x-Q1 Supply Current vs Data Rate (No Load)

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Typical Characteristics (continued)

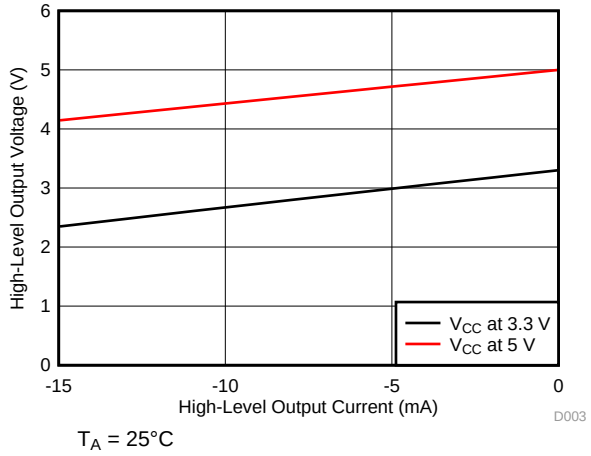


Figure 8. High-Level Output Voltage vs High-level Output Current

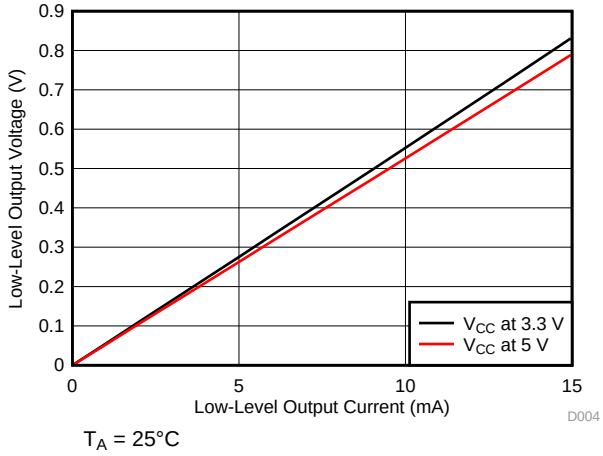


Figure 9. Low-Level Output Voltage vs Low-Level Output Current

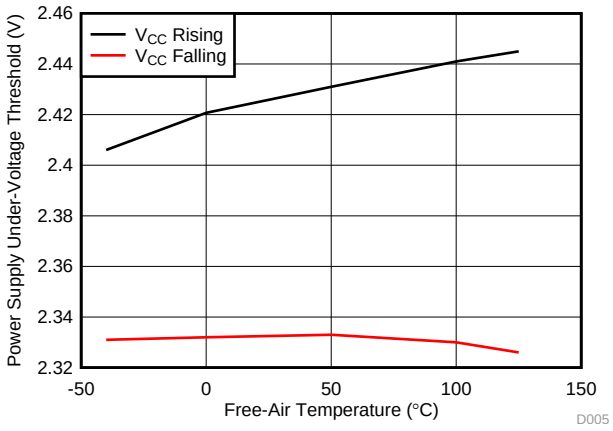


Figure 10. Power Supply Undervoltage Threshold vs Free-Air Temperature

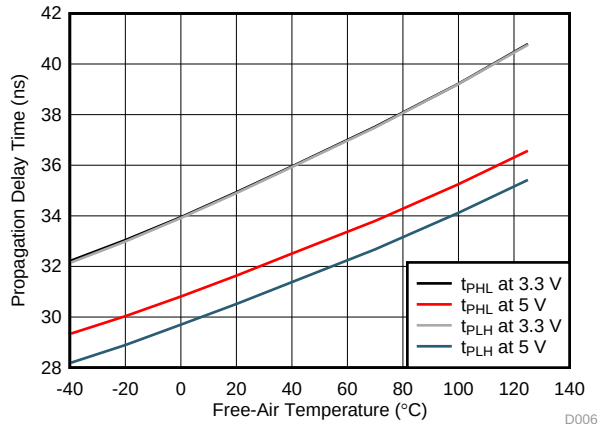


Figure 11. Propagation Delay Time vs Free-Air Temperature

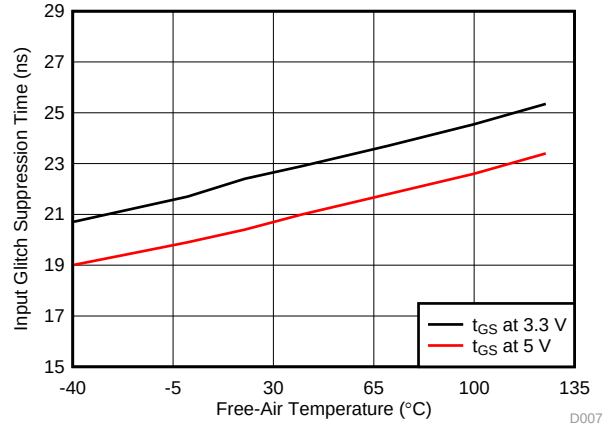


Figure 12. Input Glitch Suppression Time vs Free-Air Temperature

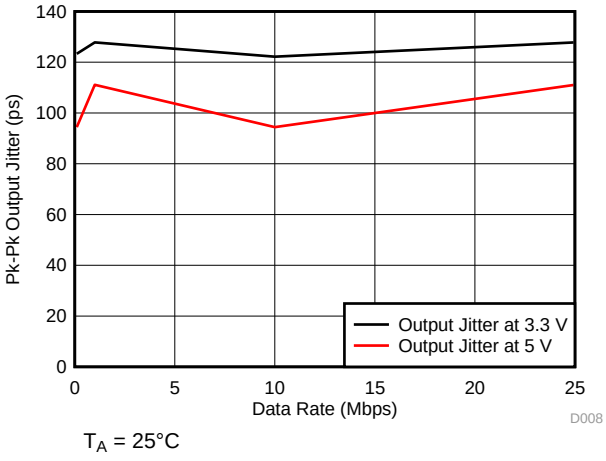
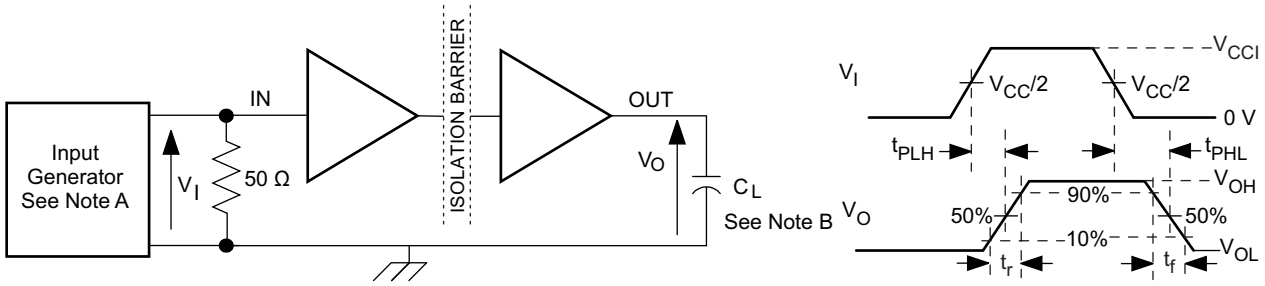


Figure 13. Output Jitter vs Data Rate

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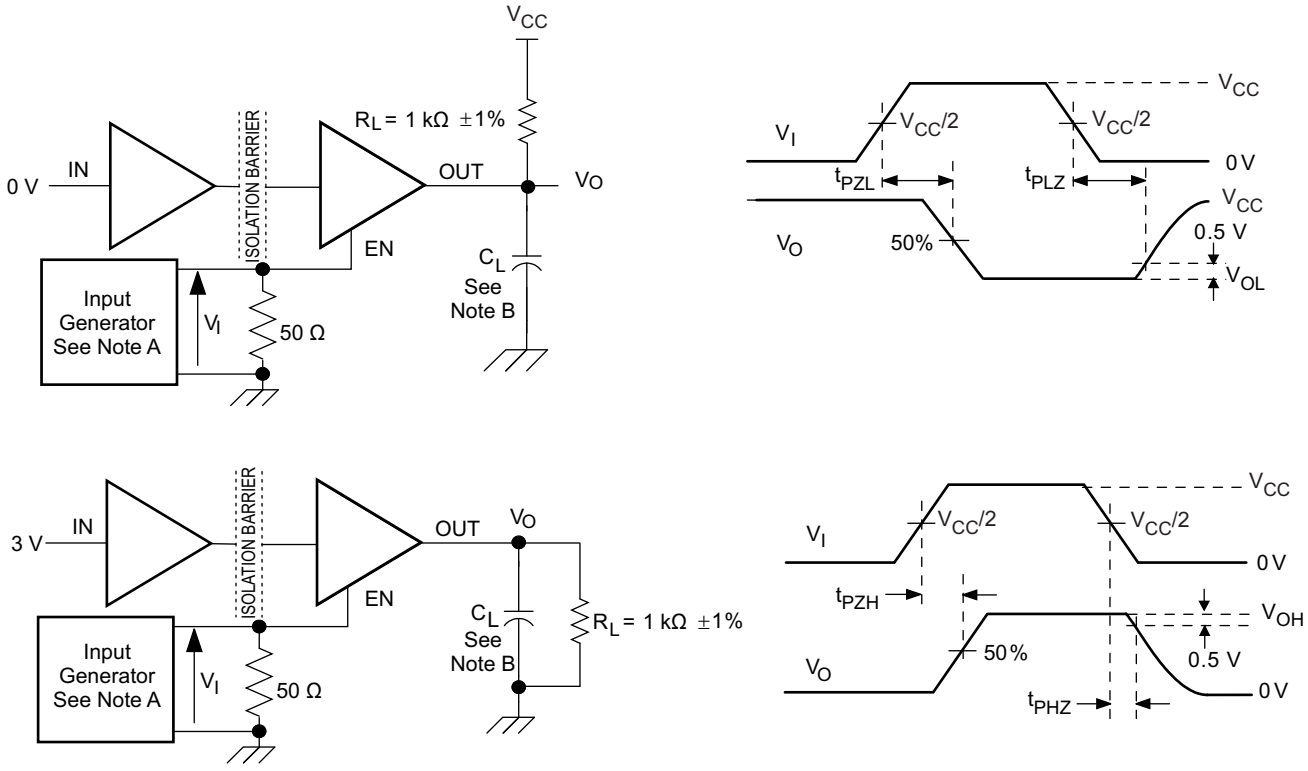
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Switching Characteristics Test Circuit and Voltage Waveforms

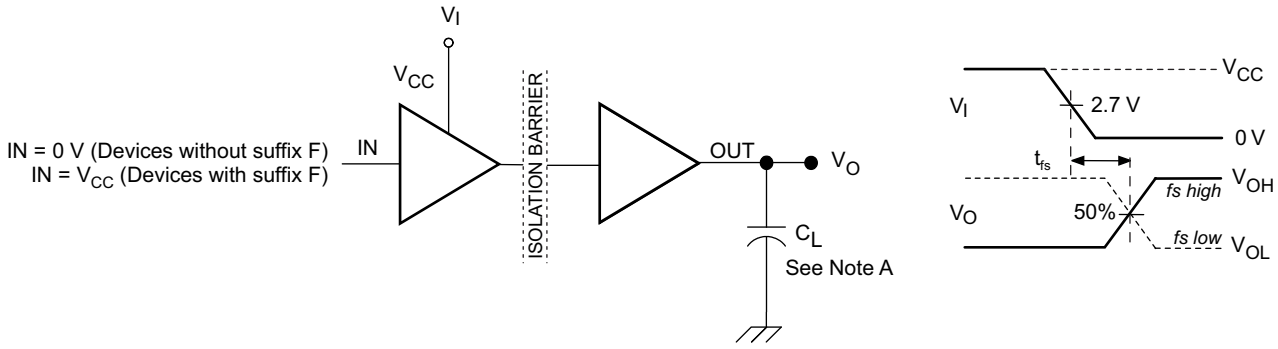


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

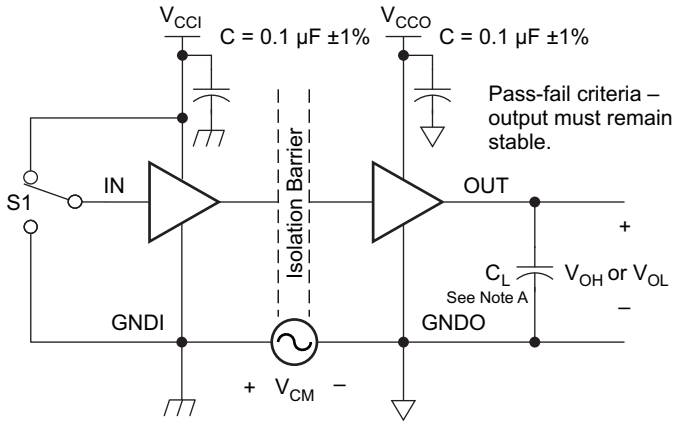
Figure 15. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 16. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 17. Common-Mode Transient Immunity Test Circuit

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9 Detailed Description

9.1 Overview

The isolator in Figure 18 is based on a capacitive isolation-barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common-mode voltage VREF depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

9.2 Functional Block Diagram

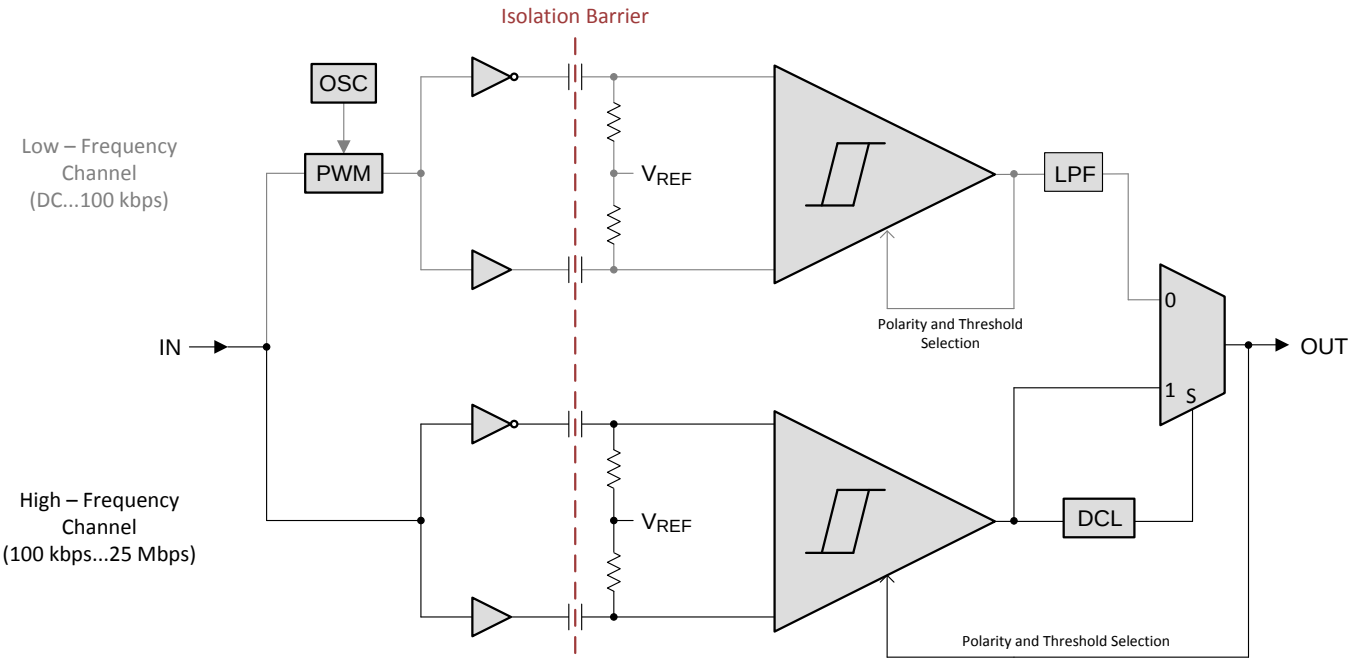


Figure 18. Conceptual Block Diagram of a Digital Capacitive Isolator

9.3 Feature Description

The ISO734x-Q1 family of devices are available in multiple channel configurations and default output state options to enable wide variety of application uses.

ORDERABLE DEVICE	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7340CQDWQ1 and ISO7340CQDWRQ1	4 Forward, 0 Reverse	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
ISO7340FCQDWQ1 and ISO7340FCQDWRQ1				Low
ISO7341CQDWQ1 and ISO7341CQDWRQ1	3 Forward, 1 Reverse			High
ISO7341FCQDWQ1 and ISO7341FCQDWRQ1				Low
ISO7342CQDWQ1 and ISO7342CQDWRQ1	2 Forward, 2 Reverse			High
ISO7342FCQDWQ1 and ISO7342FCQDWRQ1				Low

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

9.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge, and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO734x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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9.4 Device Functional Modes

Table 1 lists the functional modes for the ISO734x-Q1 family of devices.

Table 1. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO734xCQDWQ1 AND ISO734xCQDWRQ1	ISO734xFCQDWQ1 AND ISO734xFCQDWRQ1
PU	PU	H	H or Open	H	H
		L	H or Open	L	L
		X	L	Z	Z
		Open	H or Open	H(2)	L(3)
PD	PU	X	H or Open	H(2)	L(3)
X	PU	X	L	Z	Z
X	PD	X	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

9.4.1 Device I/O Schematics

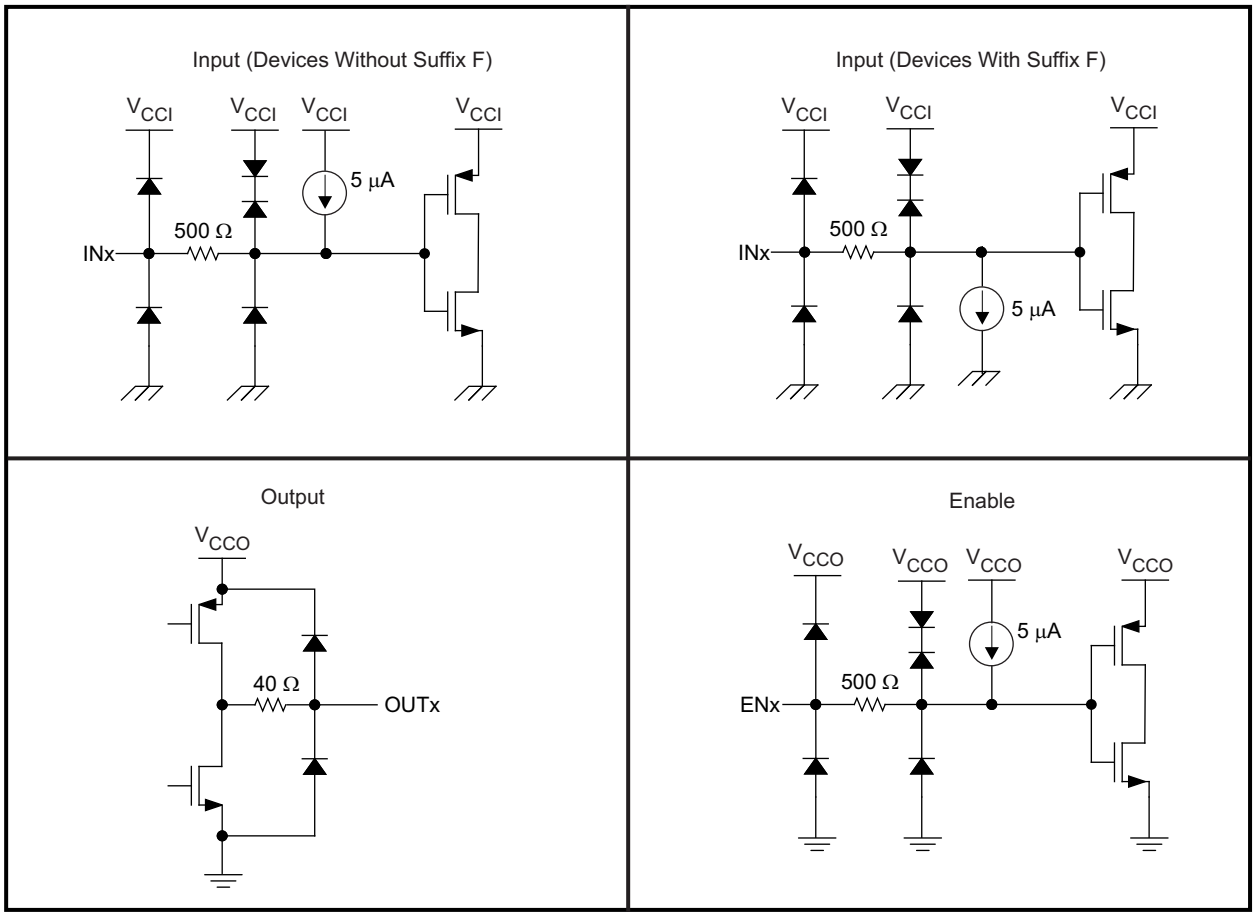


Figure 19. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO734x-Q1 family of devices use single-ended TTL-logic switching technology. The supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

10.2.1 Isolated Data Acquisition System for Process Control

The ISO734x-Q1 family of devices combined with Texas Instruments' precision analog-to-digital converter and mixed signal micro-controller can create an advanced isolated data acquisition system as shown in Figure 20.

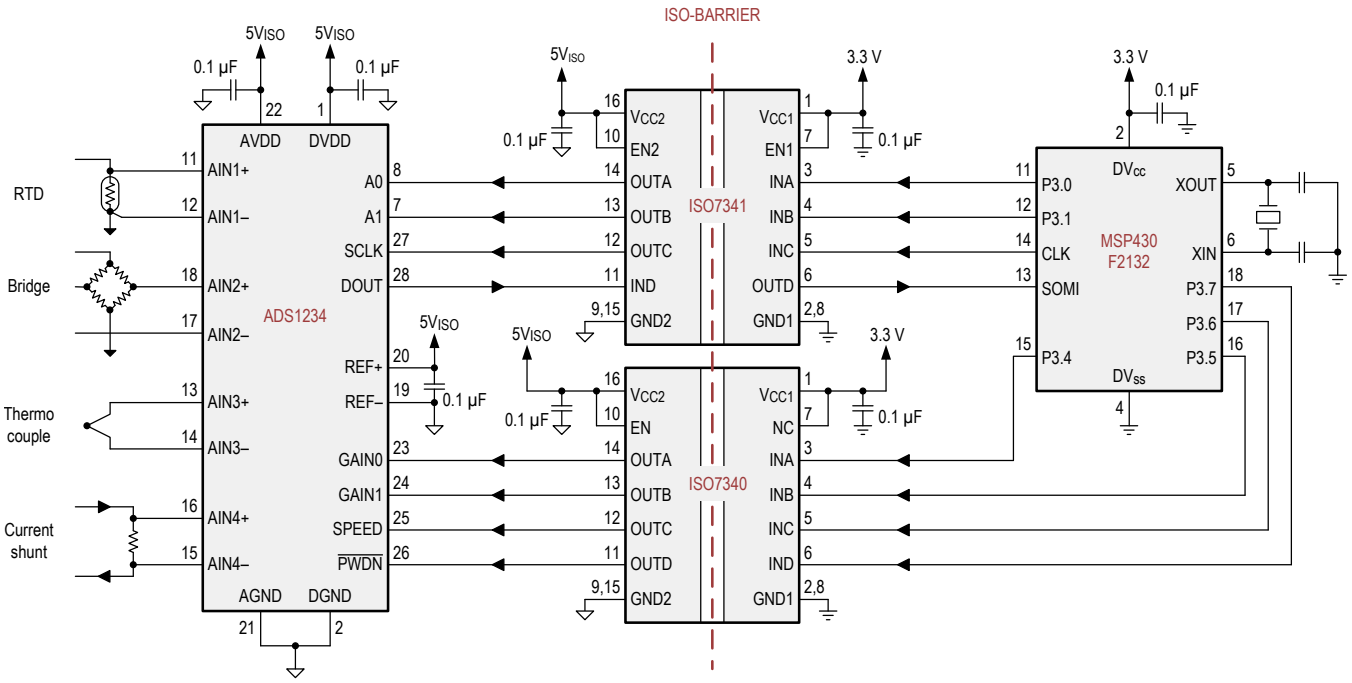


Figure 20. Isolated Data-Acquisition System for Process Control

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Typical Application (continued)

10.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO734-Q1 family of devices only requires two external bypass capacitors to operate.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Typical Supply Current Equations

For the equations in this section, the following is true:

- I_{CC1} and I_{CC2} are typical supply currents measured in mA
- f is data rate measured in Mbps
- C_L is the capacitive load measured in pF

10.2.1.2.1.1 ISO7340-Q1

At $V_{CC1} = V_{CC2} = 5$ V:

$$I_{CC1} = 0.54366 + (0.0873 \times f) \quad (1)$$

$$I_{CC2} = 2.74567 + (0.08433 \times f) + (0.01 \times f \times C_L) \quad (2)$$

At $V_{CC1} = V_{CC2} = 3.3$ V:

$$I_{CC1} = 0.3437 + (0.04922 \times f) \quad (3)$$

$$I_{CC2} = 2.1068 + (0.04374 \times f) + (0.007045 \times f \times C_L) \quad (4)$$

10.2.1.2.1.2 ISO7341-Q1

At $V_{CC1} = V_{CC2} = 5$ V:

$$I_{CC1} = 1.7403 + (0.1006 \times f) + (0.001711 \times f \times C_L) \quad (5)$$

$$I_{CC2} = 2.502 + (0.09629 \times f) + (0.00687 \times f \times C_L) \quad (6)$$

At $V_{CC1} = V_{CC2} = 3.3$ V:

$$I_{CC1} = 1.2915 + (0.046 \times f) + (0.00185 \times f \times C_L) \quad (7)$$

$$I_{CC2} = 1.8833 + (0.0566 \times f) + (0.004514 \times f \times C_L) \quad (8)$$

10.2.1.2.1.3 ISO7342-Q1

At $V_{CC1} = V_{CC2} = 5$ V:

$$I_{CC1}, I_{CC2} = 2.1254 + (0.08694 \times f) + (0.004868 \times f \times C_L) \quad (9)$$

At $V_{CC1} = V_{CC2} = 3.3$ V:

$$I_{CC1}, I_{CC2} = 1.5912 + (0.0410 \times f) + (0.003785 \times f \times C_L) \quad (10)$$

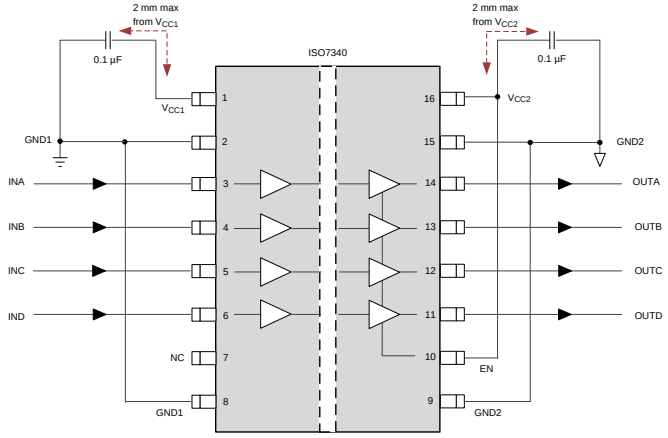


Figure 21. Typical ISO7340-Q1 Circuit Hook-up

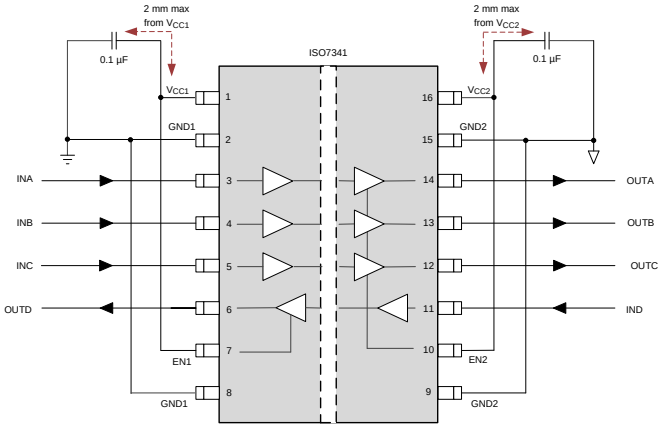


Figure 22. Typical ISO7341-Q1 Circuit Hook-up

Typical Application (continued)

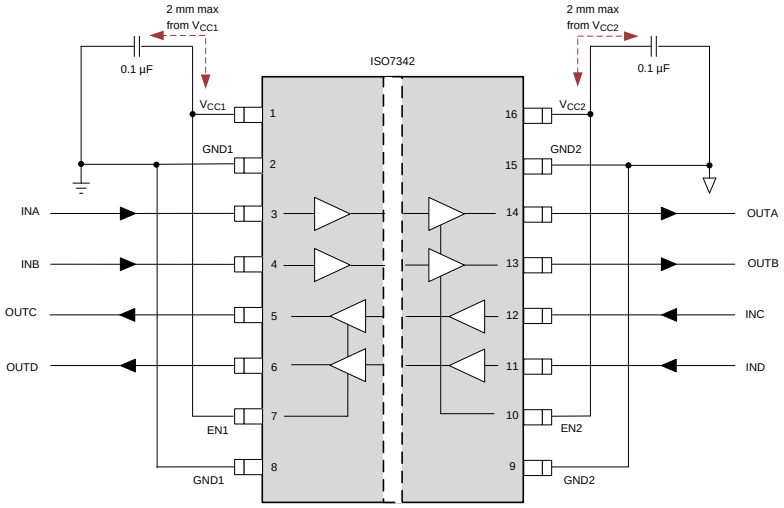


Figure 23. Typical ISO7342-Q1 Circuit Hook-up

10.2.1.3 Application Curves

The typical eye diagrams of the ISO734x-Q1 family of devices indicate low jitter and a wide open eye at the maximum data rate of 25 Mbps.

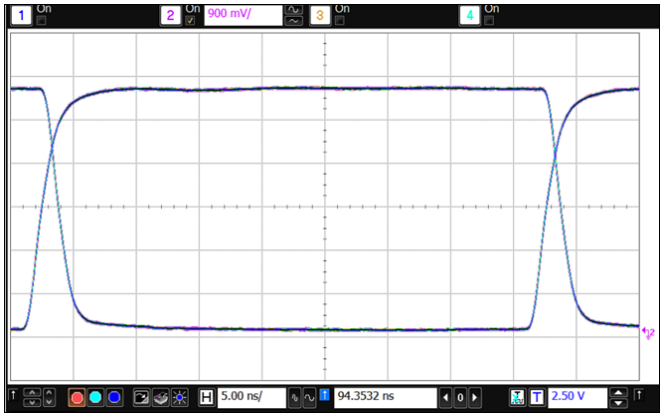


Figure 24. Eye Diagram at 25 Mbps, 5 V and 25°C

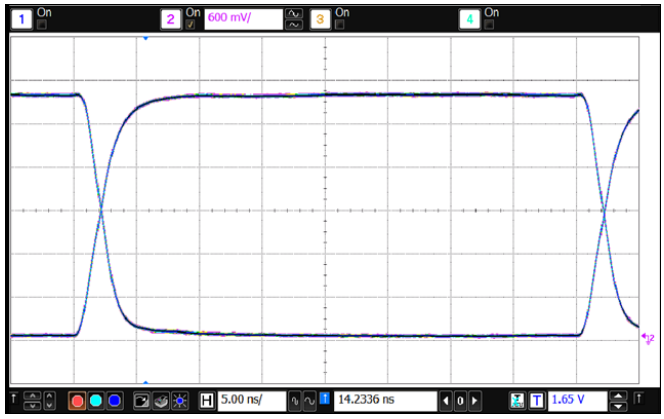


Figure 25. Eye Diagram at 25 Mbps, 3.3 V and 25°C

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Typical Application (continued)

10.2.2 Typical Application for Module with 16 Inputs

The ISO7341x-Q1 device and several other components from Texas Instruments can be used to create an isolated serial peripheral interface (SPI) for input module with 16 inputs.

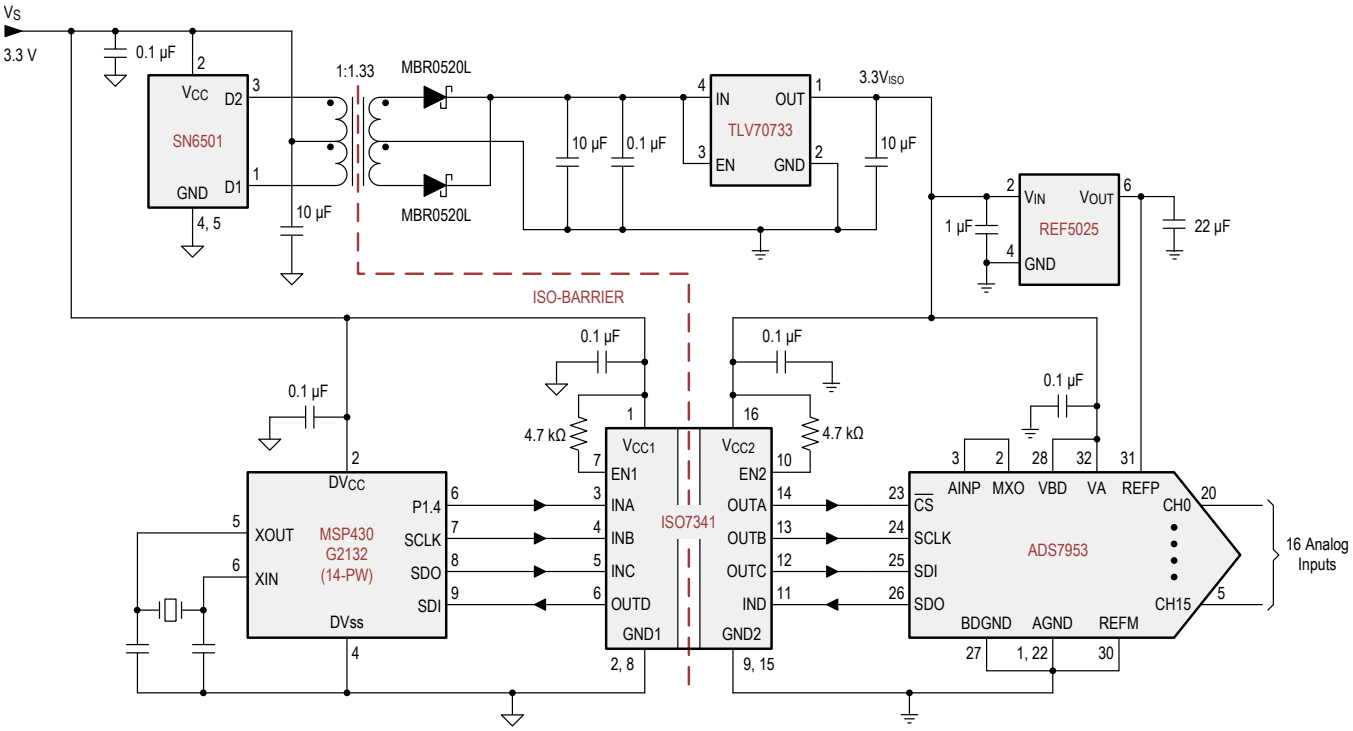


Figure 26. Isolated SPI for an Analog Input Module With 16 Inputs

10.2.2.1 Design Requirements

Refer to *Isolated Data Acquisition System for Process Control* for the design requirements.

10.2.2.2 Detailed Design Procedure

Refer to *Isolated Data Acquisition System for Process Control* for the detailed design procedures.

10.2.2.3 Application Curves

Refer to *Isolated Data Acquisition System for Process Control* for the application curves.

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Typical Application (continued)

10.2.3 Typical Application for RS-232 Interface

Typical isolated RS-232 interface implementation is shown in Figure 27.

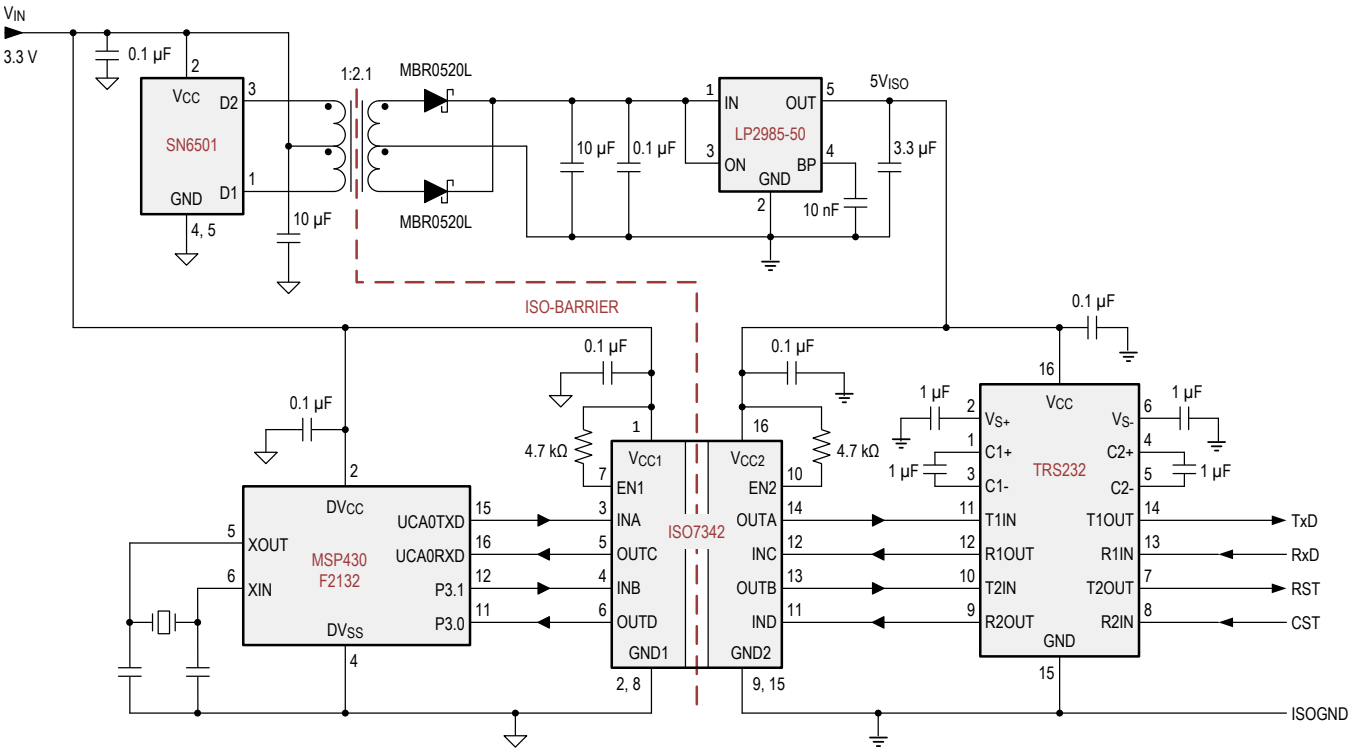


Figure 27. Isolated RS-232 Interface

10.2.3.1 Design Requirements

Refer to *Isolated Data Acquisition System for Process Control* for the design requirements.

10.2.3.2 Detailed Design Procedure

Refer to *Isolated Data Acquisition System for Process Control* for the detailed design procedures.

10.2.3.3 Application Curves

Refer to *Isolated Data Acquisition System for Process Control* for the application curves.

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* (SLLSEF3).

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12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 28). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284).

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

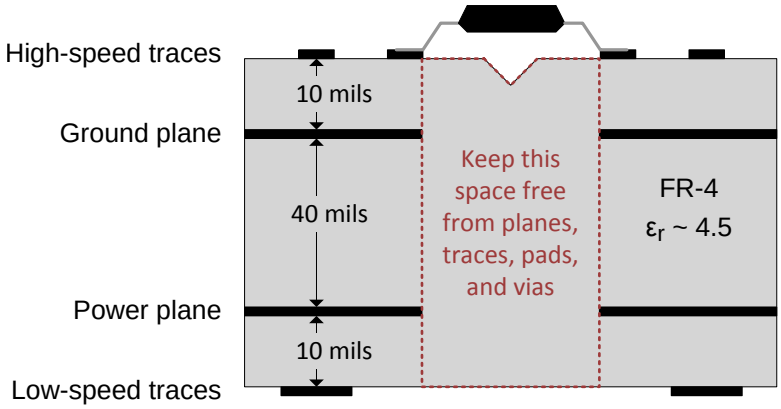


Figure 28. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary* (SLLA353)
- *Digital Isolator Design Guide* (SLLA284)
- *SN6501-Q1 Transformer Driver for Isolated Power Supplies* (SLLSEF3)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7340-Q1	Click here	Click here	Click here	Click here	Click here
ISO7341-Q1	Click here	Click here	Click here	Click here	Click here
ISO7342-Q1	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

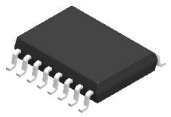
This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

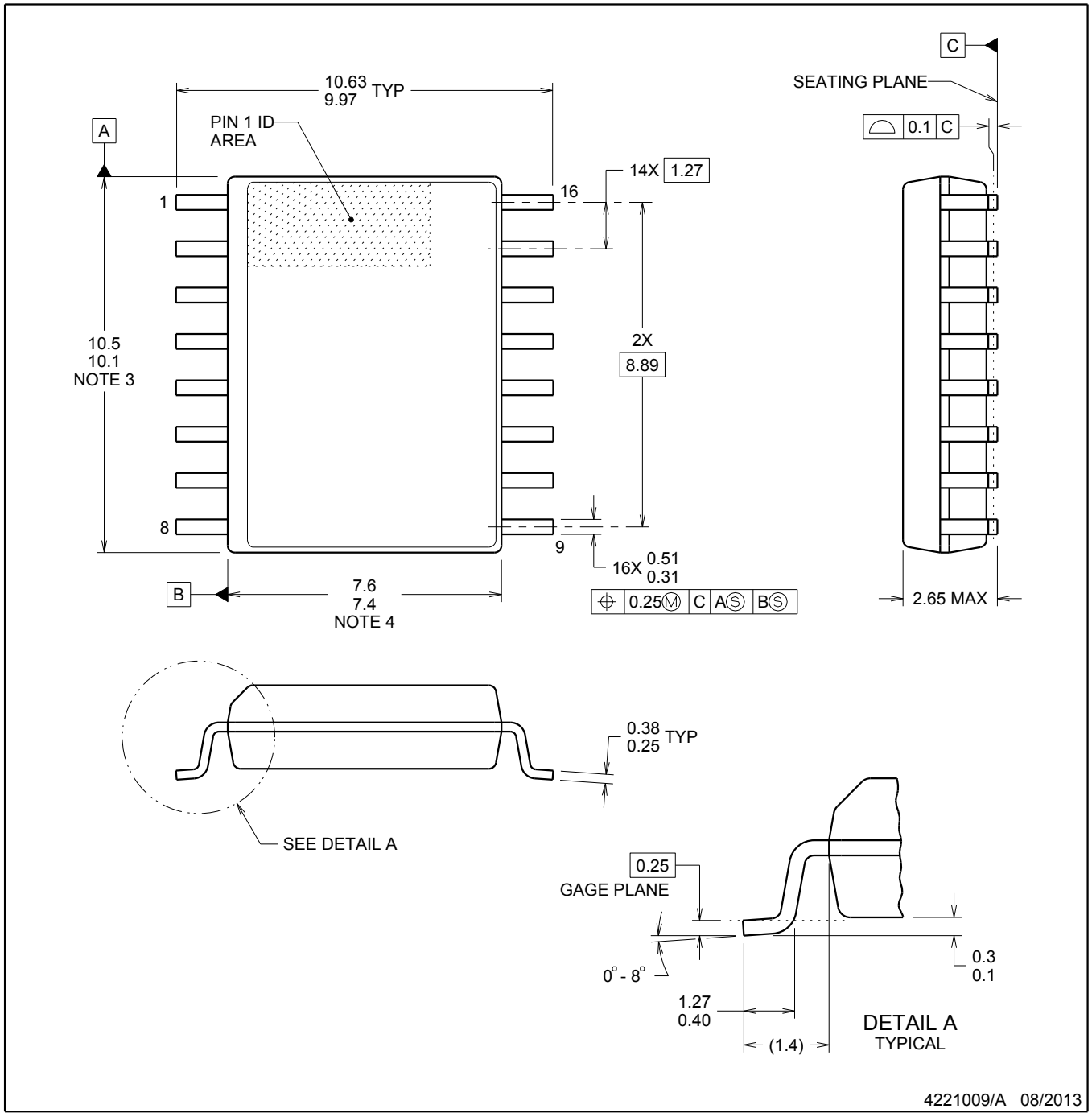
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DW0016B

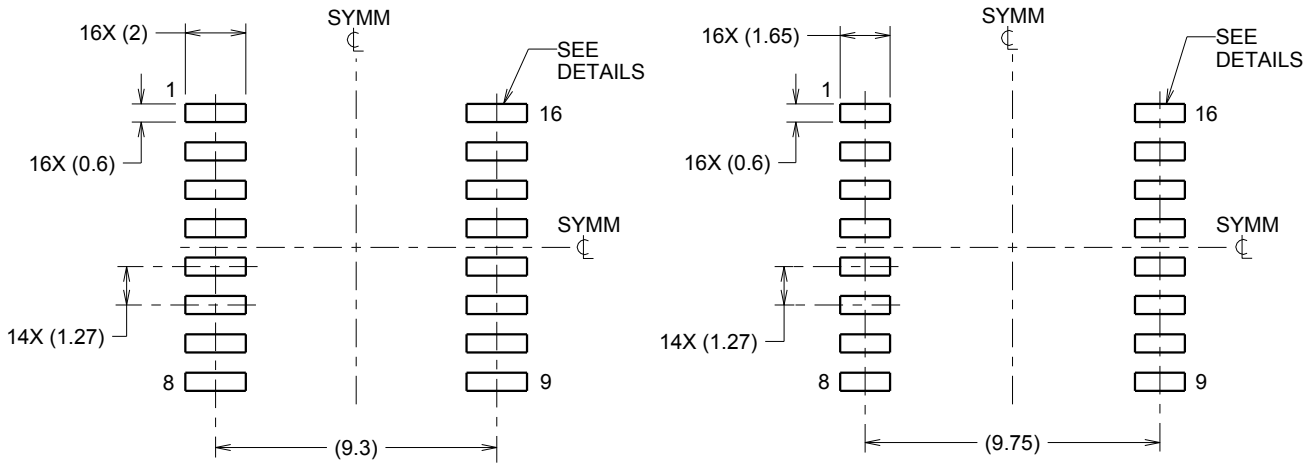
SOIC - 2.65 mm max height

SOIC



NOTES:

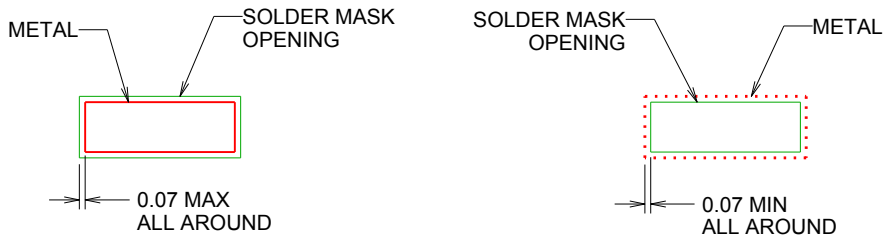
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/A 08/2013

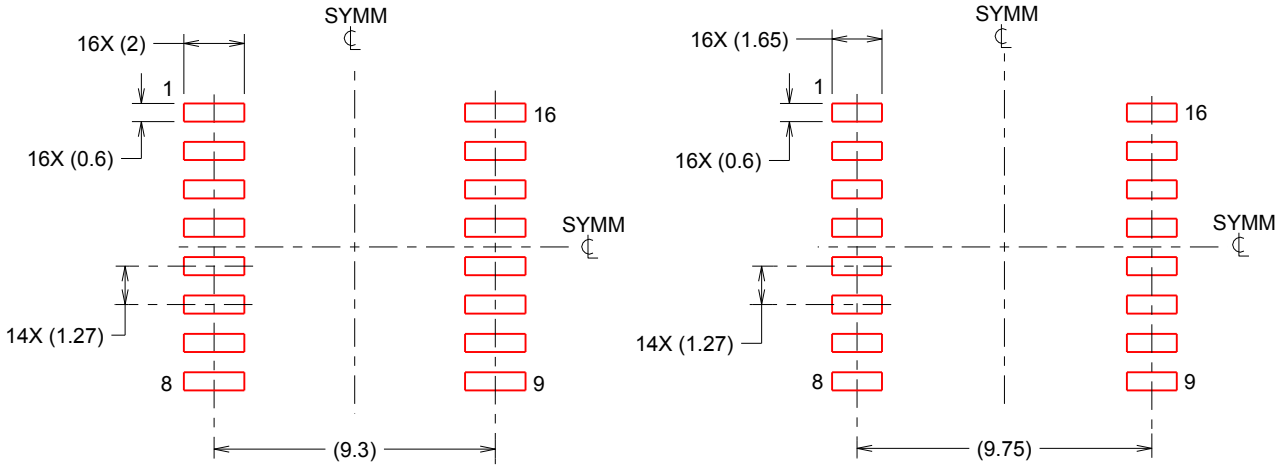
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/A 08/2013

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7340CQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340CQ	Samples
ISO7340CQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340CQ	Samples
ISO7340FCQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340FCQ	Samples
ISO7340FCQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340FCQ	Samples
ISO7341CQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341CQ	Samples
ISO7341CQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341CQ	Samples
ISO7341FCQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341FCQ	Samples
ISO7341FCQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341FCQ	Samples
ISO7342CQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342CQ	Samples
ISO7342CQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342CQ	Samples
ISO7342FCQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342FCQ	Samples
ISO7342FCQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342FCQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

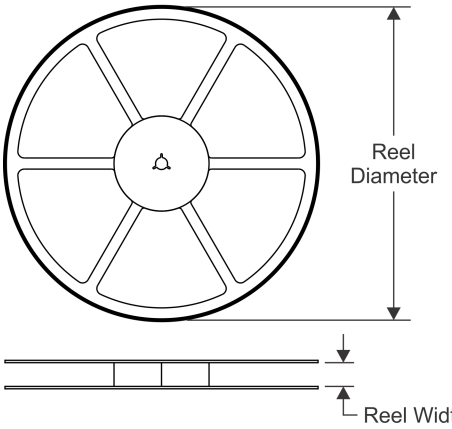
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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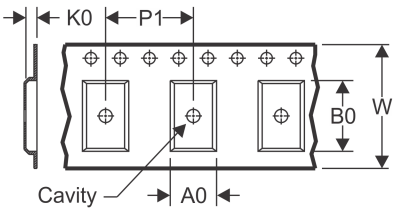
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

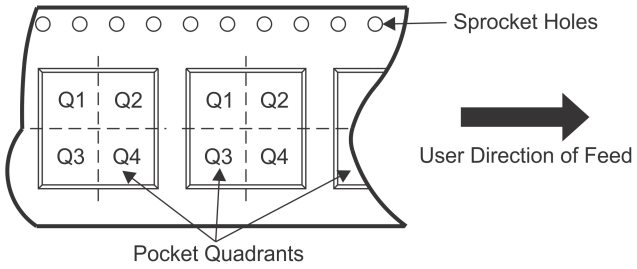


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

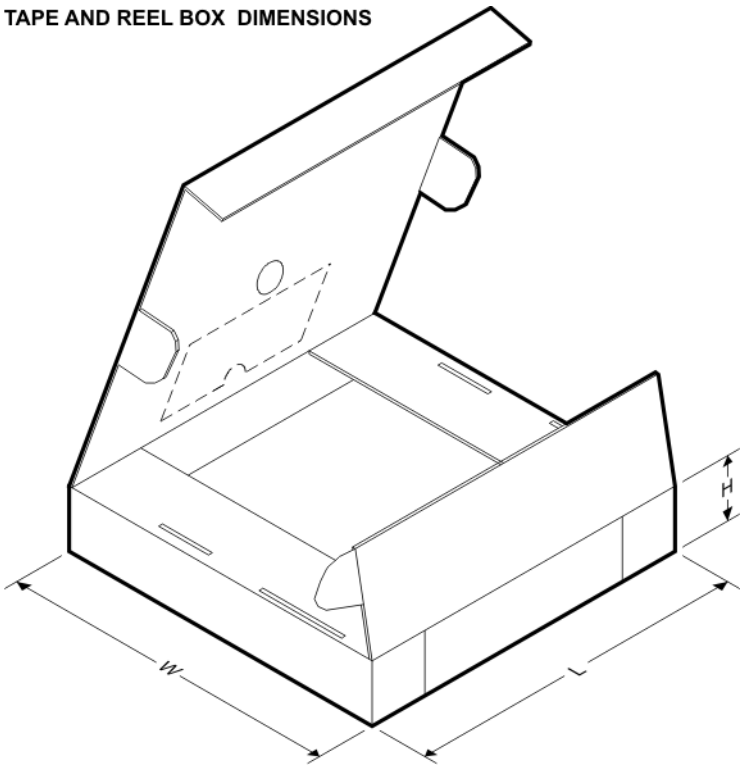
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7340CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7340FCQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7341CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7341FCQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7342CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7342FCQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7340CQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7340FCQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7341CQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7341FCQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7342CQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7342FCQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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