ISO7021 Ultra-Low Power Two-Channel Digital Isolator

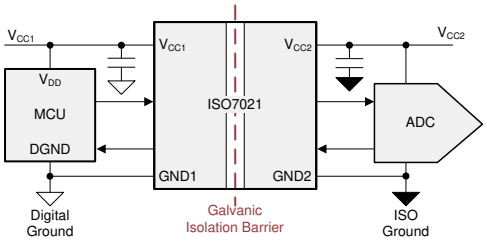
1 Features

- Ultra-low power consumption
  - 4.8 μA per channel quiescent current (3.3 V)
  - 15 μA per channel at 100 kbps (3.3 V)
  - 120 μA per channel at 1 Mbps (3.3 V)
- Robust isolation barrier
  - >100-year projected lifetime
  - 3000 V_{RMS} isolation rating
  - ±100 kV/μs typical CMTI
- Wide supply range: 1.71 V to 1.89 V and 2.25 V to 5.5 V
- Wide temperature range: –55°C to +125°C
- Small 8-SOIC package (8-D)
- Signaling rate: Up to 4 Mbps
- Default output *High* (ISO7021) and *Low* (ISO7021F) options
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Very low emissions
- Safety-related certifications (planned):
  - UL 1577 Component Recognition Program
  - DIN V VDE V 0884-11
  - CQC, TUV and CSA certifications

2 Applications

- 4-mA to 20-mA loop powered field transmitters
- Factory automation, process automation
- Low-power GPIO, UART isolation

Simplified Application Schematic



3 Description

The ISO7021 device is an ultra-low power, multichannel digital isolator that can be used to isolate CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. Innovative edge based architecture combined with an ON-OFF keying modulation scheme allows these isolators to consume very-low power while meeting 3000-V_{RMS} isolation rating per UL1577. The per channel dynamic current consumption of the device is under 120 μA/Mbps and the per channel static current consumption is 4.8 μA at 3.3 V, allowing for use of the ISO7021 in both power and thermal constrained system designs.

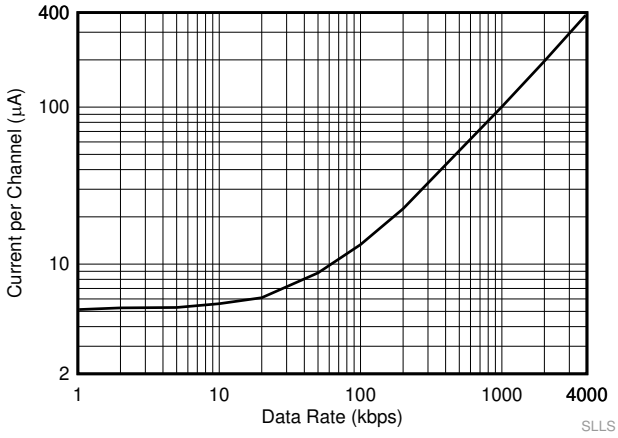
The device can operate as low as 1.71 V, as high as 5.5 V, and is fully functional with different supply voltages on each side of isolation barrier. The two-channel isolator comes in a narrow body 8-SOIC package with one forward and one reverse-direction channel in a 8-SOIC package. The device has default output high and low options. If the input power or signal is lost, default output is *high* for the ISO7021 device without the suffix F and *low* for the ISO7021F device with the F suffix. See the Device Functional Modes section for more information.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7021	SOIC (8-D)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Data Rate vs Power Consumption at 3.3 V



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2019) to Revision A	Page
• RTM release	1

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5 Device Comparison Table

Table 1. Device Features

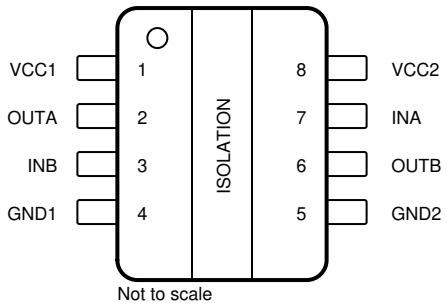
PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7021	1 Forward, 1 Reverse	4 Mbps	High	SOIC-8	3000 V_{RMS} / 4242 V_{PK}
ISO7021 with F suffix	1 Forward, 1 Reverse	4 Mbps	Low	SOIC-8	3000 V_{RMS} / 4242 V_{PK}

(1) See for detailed isolation ratings.

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6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground connection for V_{CC1}
GND2	5	—	Ground connection for V_{CC2}
INA	7	I	Input, channel A
INB	3	I	Input, channel B
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	8	—	Power supply, side 2

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply Voltage	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5	
Output Current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3)(4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1	V_{CCO} (2)= 1.8 V	1.71		1.89	V
V_{CC1} (1)	Supply Voltage Side 1	V_{CCO} = 2.5 V to 5 V	2.25		5.5	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CCO} = 1.8 V	1.71		1.89	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CCO} = 2.5 V to 5 V	2.25		5.5	V
V_{IH}	High level Input voltage		0.7 x V_{CCI}		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
		V_{CCO} = 1.8 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
		V_{CCO} = 1.8 V			1	mA
DR	Data Rate		0		4	Mbps
T_A	Ambient temperature		-55		125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

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7.4 Thermal Information

THERMAL METRIC		ISO7021 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L =$ 15 pF, Input a 2-MHz 50% duty cycle square wave			8.4	mW
P_{D1}	Maximum power dissipation (side-1)				4.2	mW
P_{D2}	Maximum power dissipation (side-2)				4.2	mW

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7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			8-D	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	4	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ = TBD V_{PK} (qualification)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

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7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11:2017- 01	Certified according to IEC 60950-1 and IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950- 1:2006/A2:2013
Maximum transient isolation voltage, 4242 V_{PK}; Maximum repetitive peak isolation voltage, 566 V_{PK}; Maximum surge isolation voltage, 4000 V_{PK}	3000 V_{RMS} insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014 370 V_{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I)	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	3000 V_{RMS} insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 300 V_{RMS} 3000 V_{RMS} insulation per EN 60950-1:2006/A2:2013 up to working voltage of 370 V_{RMS}
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 94.3°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			241	mA
		$R_{\theta JA}$ = 94.3°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			368	mA
		$R_{\theta JA}$ = 94.3°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			482	
		$R_{\theta JA}$ = 94.3°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C			701	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 94.3°C/W, T_J = 150°C, T_A = 25°C			1325	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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7.9 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -4 mA	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

7.10 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	I_{CC1}		5.9	11.8	µA
		I_{CC2}		5.9	11.8	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		6.5	11.9	µA
		I_{CC2}		6.5	11.9	µA
Supply current - AC signal	10 kbps, No Load	I_{CC1}		7.2	12.2	µA
		I_{CC2}		7.2	12.2	µA
	100 kbps, No Load	I_{CC1}		15.9	27.7	µA
		I_{CC2}		15.9	27.7	µA
	1 Mbps, No Load	I_{CC1}		129.0	175.0	µA
		I_{CC2}		129.0	175.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.9	11.4	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		6.5	11.8	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		7.2	12.2	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		15.9	27.8	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		129.0	175.0	µA

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7.11 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.3	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 3.3 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

7.12 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	I_{CC1}		4.8	7.8	µA
		I_{CC2}		4.8	7.8	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		5.2	8.4	µA
		I_{CC2}		5.2	8.4	µA
Supply current - AC signal	10 kbps, No Load	I_{CC1}		5.7	8.8	µA
		I_{CC2}		5.7	8.8	µA
	100 kbps, No Load	I_{CC1}		15.0	23.0	µA
		I_{CC2}		15.0	23.0	µA
	1 Mbps, No Load	I_{CC1}		120.0	153.0	µA
		I_{CC2}		120.0	155.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.8	7.8	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.2	8.4	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.7	8.8	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		15.0	23.0	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		120.0	153.0	µA

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7.13 Electrical Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 2.5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

7.14 Supply Current Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	I_{CC1}		4.4	6.9	µA
		I_{CC2}		4.3	6.9	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		4.8	7.4	µA
		I_{CC2}		4.8	7.4	µA
Supply current - AC signal	10 kbps, No Load	I_{CC1}		5.0	7.8	µA
		I_{CC2}		5.0	7.8	µA
	100 kbps, No Load	I_{CC1}		12.4	21.2	µA
		I_{CC2}		12.4	21.2	µA
	1 Mbps, No Load	I_{CC1}		112.0	144.0	µA
		I_{CC2}		113.0	144.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.4	6.9	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.8	7.4	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.0	7.8	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		12.4	21.2	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		113.0	144.0	µA

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7.15 Electrical Characteristics 1.8V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 1.8 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

7.16 Supply Current Characteristics 1.8V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	I_{CC1}		3.4	5.7	µA
		I_{CC2}		3.4	5.7	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		3.8	6.2	µA
		I_{CC2}		3.8	6.2	µA
Supply current - AC signal	10 kbps, No Load	I_{CC1}		4.1	6.7	µA
		I_{CC2}		4.1	6.7	µA
	100 kbps, No Load	I_{CC1}		9.9	19.3	µA
		I_{CC2}		9.9	19.3	µA
	1 Mbps, No Load	I_{CC1}		90.0	134.0	µA
		I_{CC2}		90.0	134.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0 V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.4	5.7	µA
	V_I = 0 V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.8	6.2	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.9	6.7	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		9.9	19.3	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		90.0	134.0	µA

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7.17 Switching Characteristics

V_{CC1}, V_{CC2} = 1.71 V to 1.89 V or 2.25 V to 5.5 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11		140	165	ns
$t_{P(dft)}$	Propagation delay drift			15		ps/°C
t_{UI}	Minimum pulse width	See Figure 11	250			ns
PWD	Pulse width distortion				10	ns
$t_{sk(o)}$	Channel to channel output skew time				10	ns
$t_{sk(p-p)}$	Part to part skew time				70	ns
t_r	Output signal rise time	V_{CC} = 1.71 V to 1.9 V, See Figure 11			8	ns
		V_{CC} = 2.25 V to 5.5 V, See Figure 11			5	ns
t_f	Output signal fall time	V_{CC} = 1.71 V to 1.9 V, See Figure 11			8	ns
		V_{CC} = 2.25 V to 5.5 V, See Figure 11			5	ns
t_{DO}	Default output delay time from input power loss	See Figure 12		400	750	us
t_{PU}	Time from UVLO to valid output data		1		5	ms
F_R	Refresh rate		5	10		kbps

7.18 Insulation Characteristics Curves

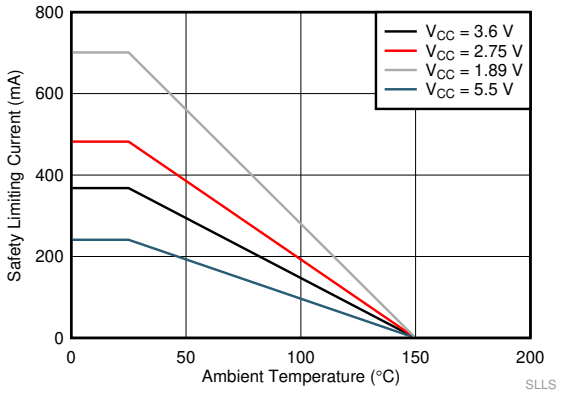


Figure 1. Thermal Derating Curve for Limiting Current per VDE

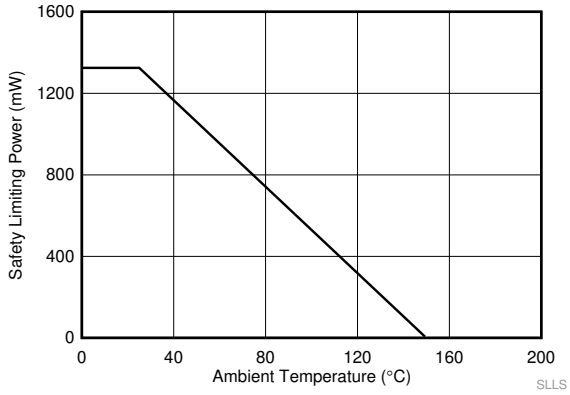
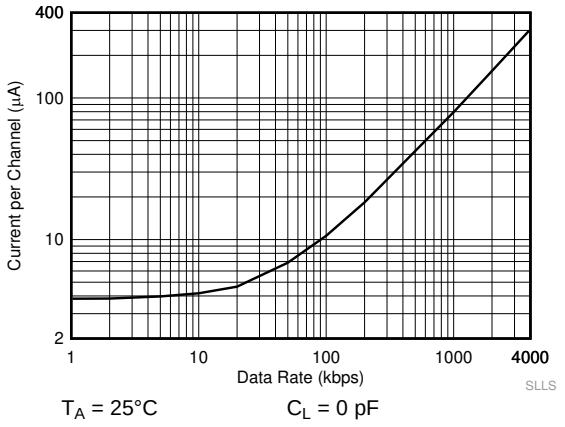


Figure 2. Thermal Derating Curve for Limiting Power per VDE

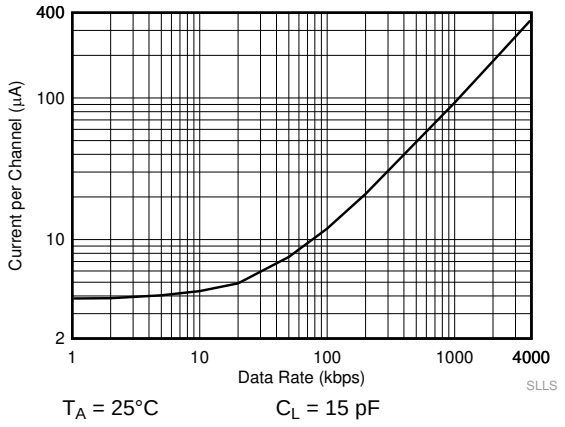
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7.19 Typical Characteristics



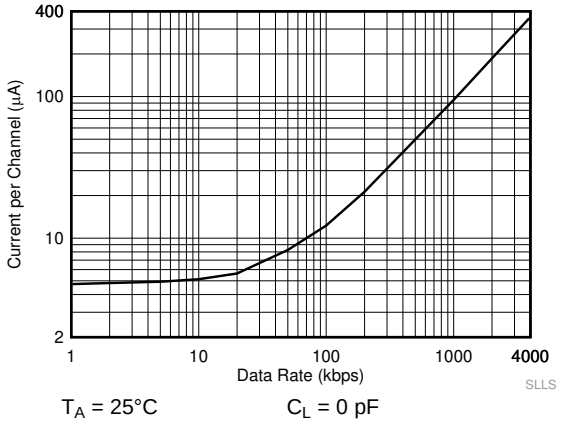
T_A = 25°C C_L = 0 pF

Figure 3. ISO7021 Supply Current vs Data Rate at 1.8 V (With No Load)



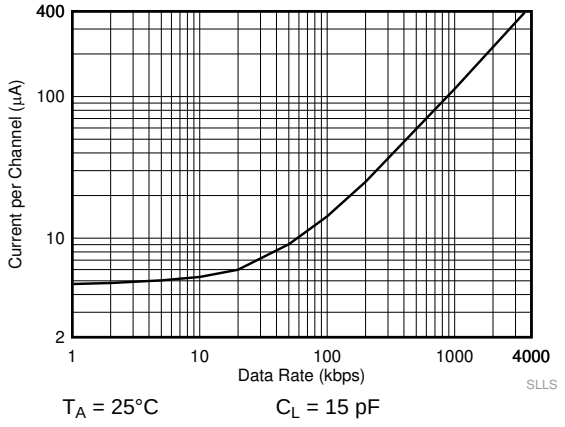
T_A = 25°C C_L = 15 pF

Figure 4. ISO7021 Supply Current vs Data Rate at 1.8 V (With 15-pF Load)



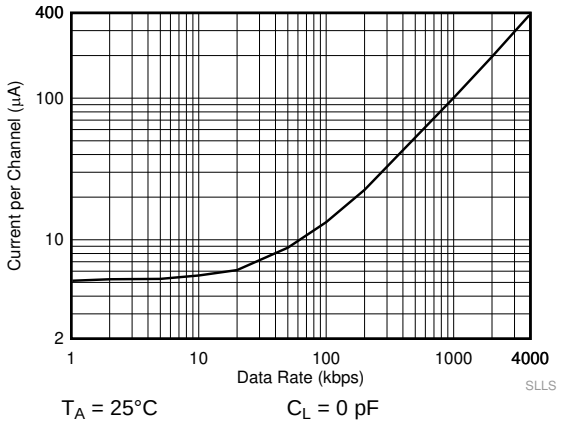
T_A = 25°C C_L = 0 pF

Figure 5. ISO7021 Supply Current vs Data Rate at 2.5 V (With No Load)



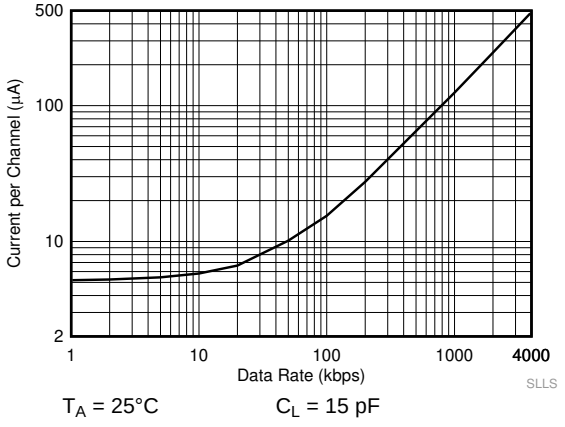
T_A = 25°C C_L = 15 pF

Figure 6. ISO7021 Supply Current vs Data Rate at 2.5 V (With 15-pF Load)



T_A = 25°C C_L = 0 pF

Figure 7. ISO7021 Supply Current vs Data Rate at 3.3 V (With No Load)

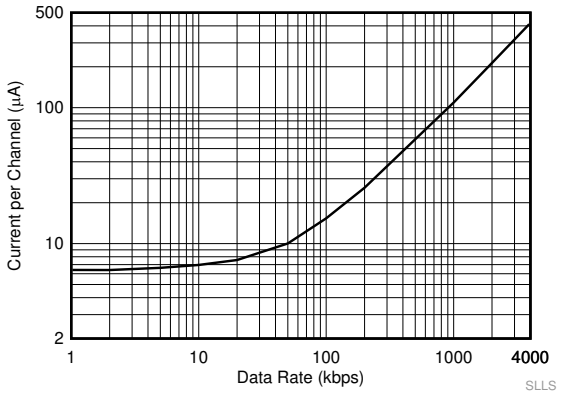


T_A = 25°C C_L = 15 pF

Figure 8. ISO7021 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)

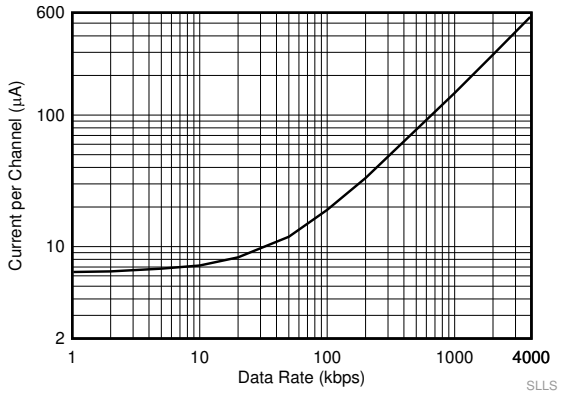
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Typical Characteristics (continued)



T_A = 25°C C_L = 0 pF

Figure 9. ISO7021 Supply Current vs Data Rate at 5 V (With No Load)

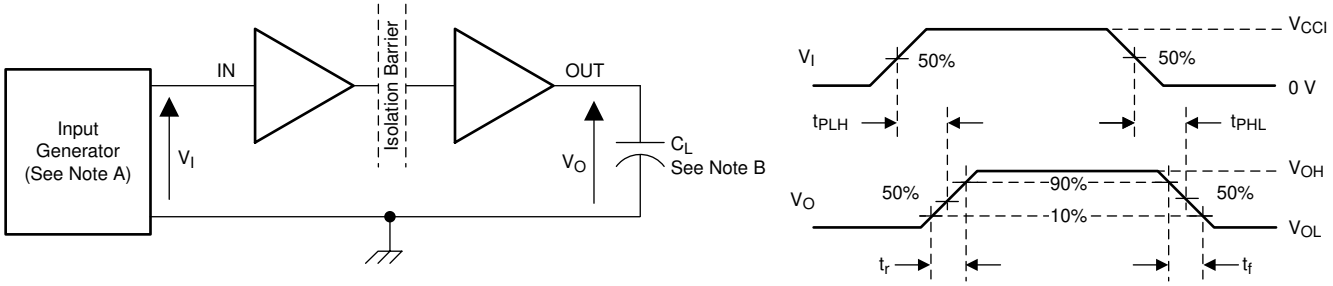


T_A = 25°C C_L = 15 pF

Figure 10. ISO7021 Supply Current vs Data Rate at 5 V (With 15-pF Load)

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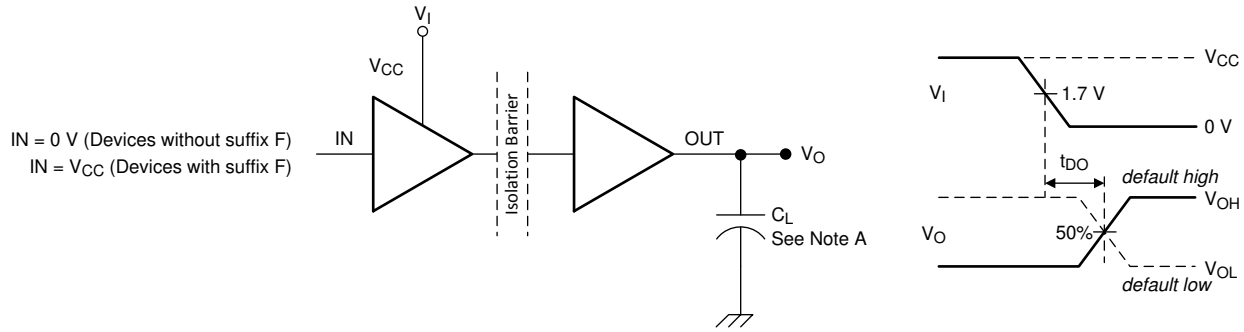
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

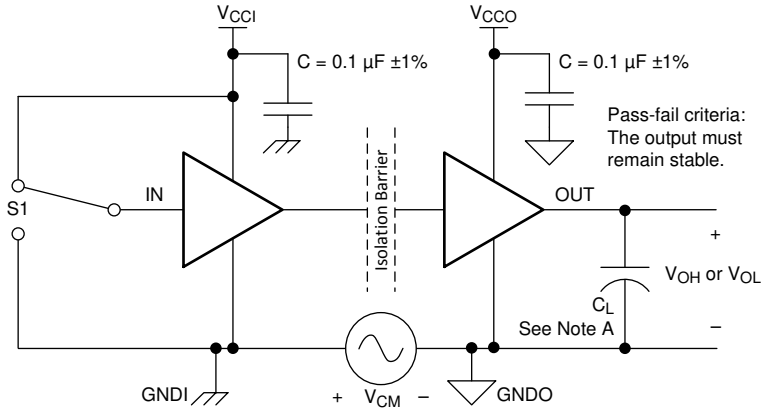
Figure 11. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 12. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISO7021 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 14, shows a functional block diagram of a typical channel.

9.2 Functional Block Diagram

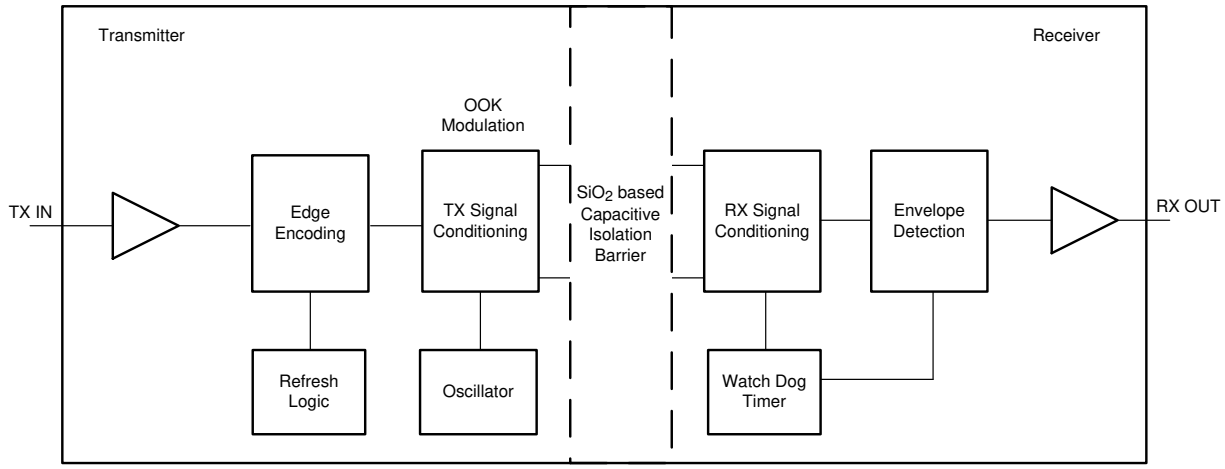


Figure 14. Conceptual Block Diagram of a Digital Capacitive Isolator

9.3 Feature Description

9.3.1 Refresh

The ISO7021 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. The built in refresh function consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 µs. This ensures that the input and output state of the isolator always match.

9.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.

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Feature Description (continued)

- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

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9.4 Device Functional Modes

Table 2 shows the functional modes for the device.

Table 2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	
		X	Default	The channel output assumes the selected default option.
PD	PU	X	Default	When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined and tri state. When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the selected default option.

9.4.1 Device I/O Schematics

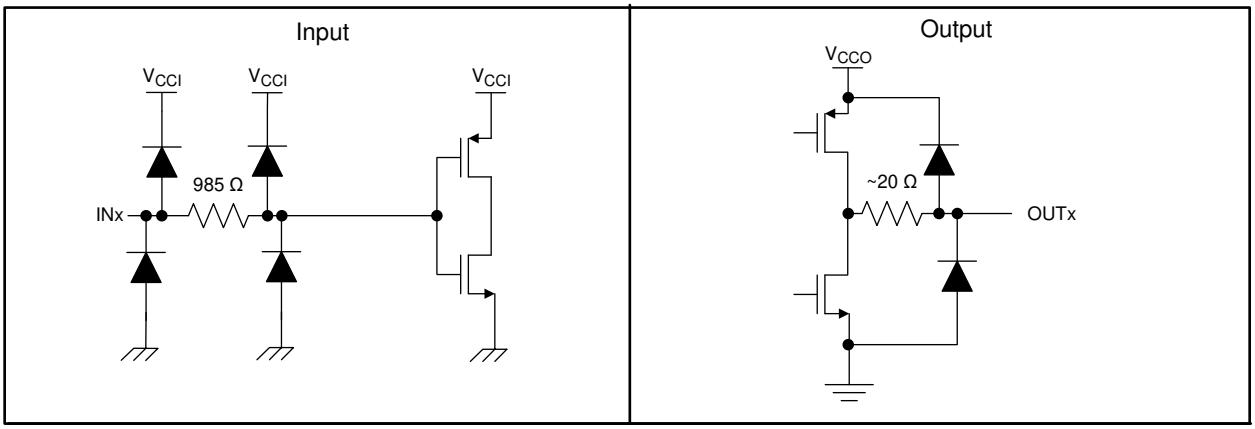


Figure 15. Device I/O Schematics

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO7021 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 1.71 V to 1.89 V and 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See *Isolated power and data interface for low-power applications reference design* TI Design for detailed information on designing the ISO70xx in low-power applications.

10.1.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see Figure 16 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

Figure 17 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

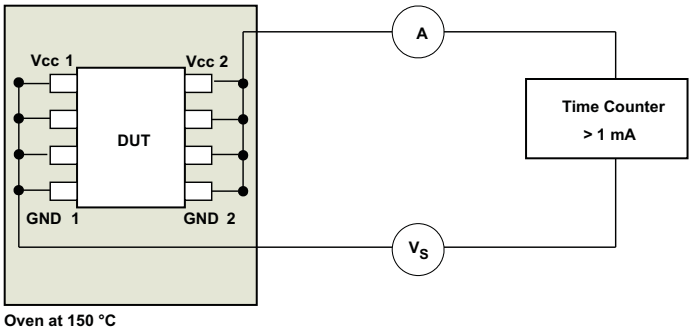


Figure 16. Test Setup for Insulation Lifetime Measurement

Application Information (continued)

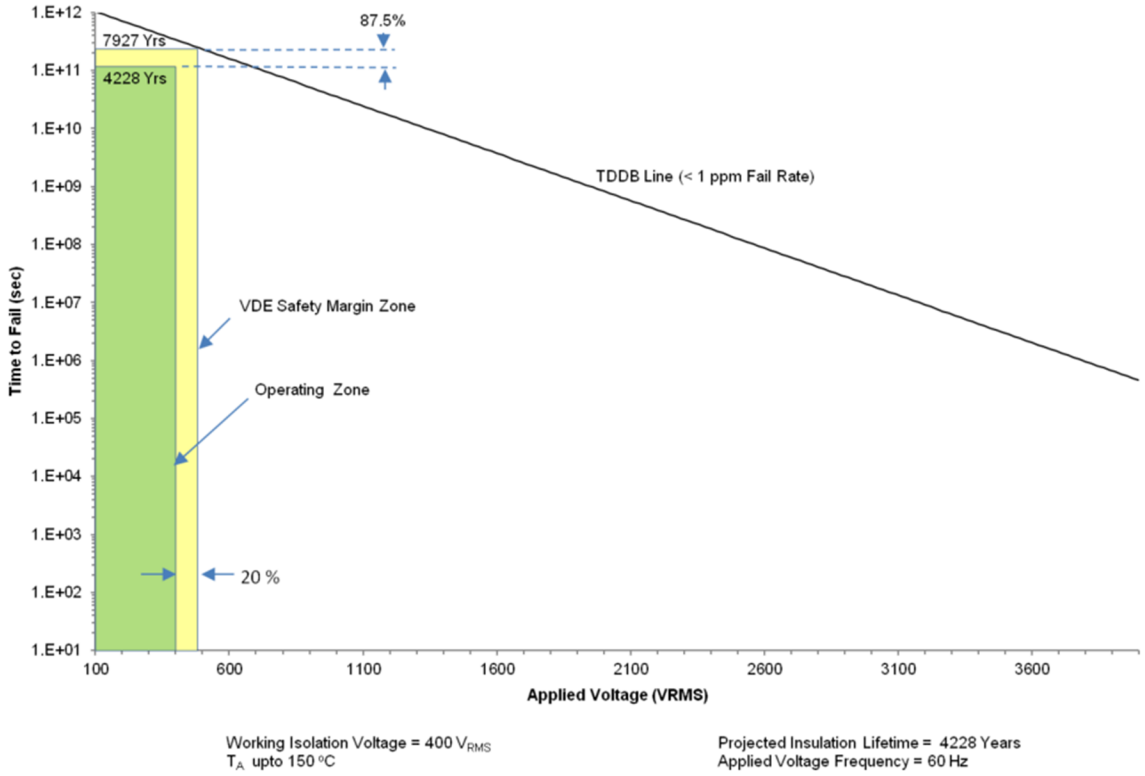


Figure 17. Insulation Lifetime Projection Data

10.2 Typical Application

Figure 18 shows the isolated UART.

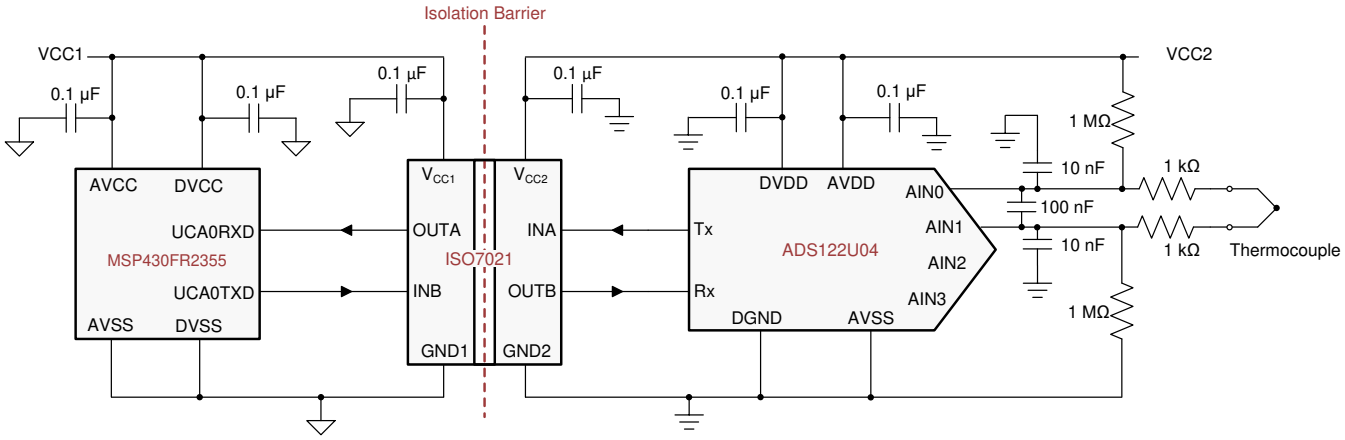


Figure 18. Isolated UART for a Temperature Field Transmitter

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Typical Application (continued)

10.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V or 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

10.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

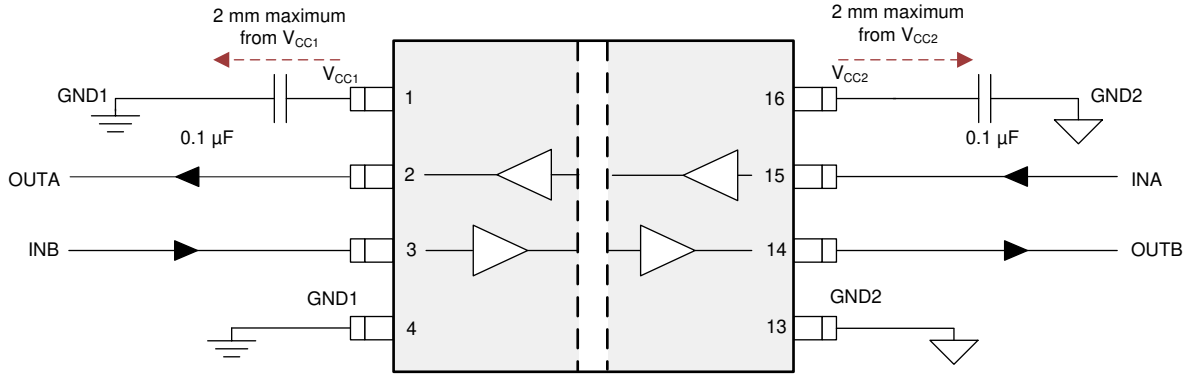


Figure 19. Typical ISO7021 Circuit Hook-up

10.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 4 Mbps.

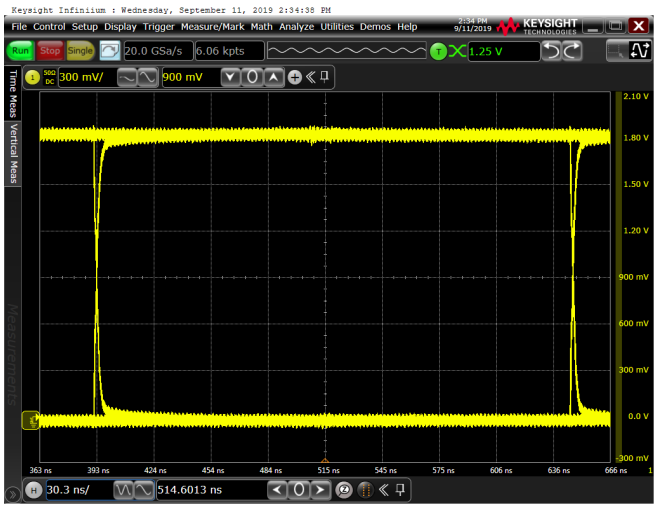


Figure 20. Eye Diagram at 4 Mbps PRBS 2^{16} – 1, 1.8 V and 25°C

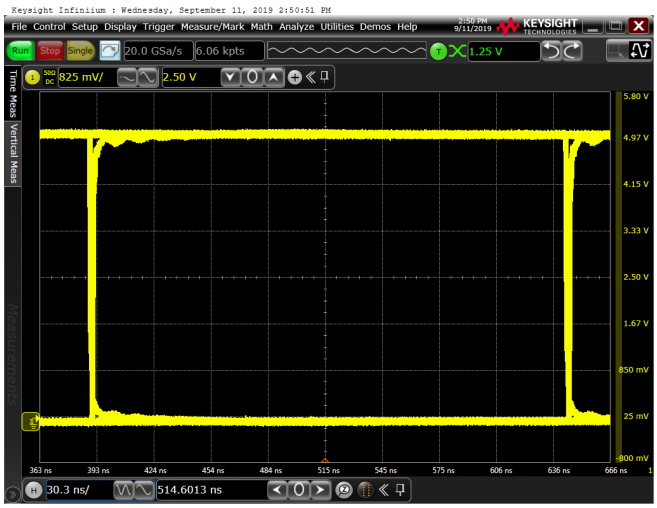


Figure 21. Eye Diagram at 4 Mbps PRBS 2^{16} – 1, 5 V and 25°C

11 Power Supply Recommendations

Put a 0.1-µF bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.

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12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 22). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations,.

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

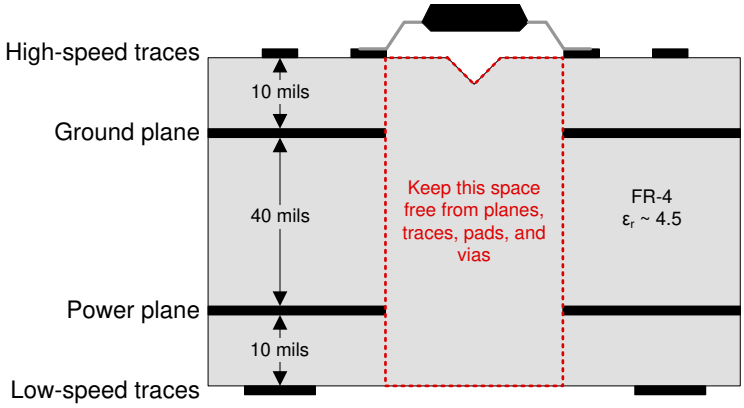


Figure 22. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *ADS1220 4-Channel, 2-kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference* data sheet
- Texas Instruments, *ADS122U04 24-Bit, 4-Channel, 2-kSPS, Delta-Sigma ADC With UART Interface* data sheet
- Texas Instruments, *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet
- Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications* TI Design
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated power and data interface for low-power applications reference design* TI Design

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13.4 Trademarks

E2E is a trademark of Texas Instruments.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7021D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021	Samples
ISO7021DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021	Samples
ISO7021FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021F	Samples
ISO7021FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

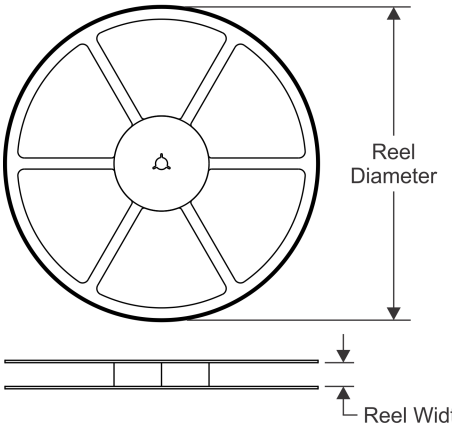
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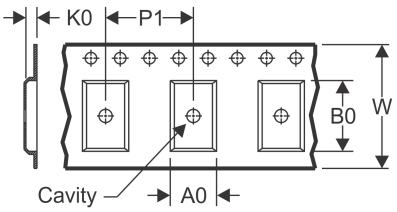
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

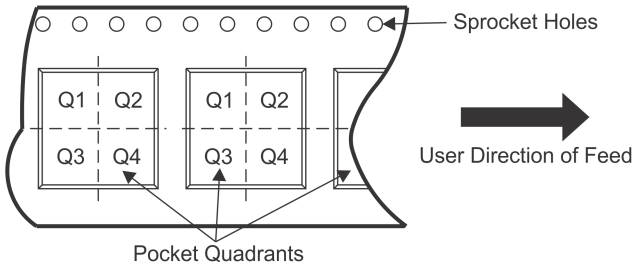


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

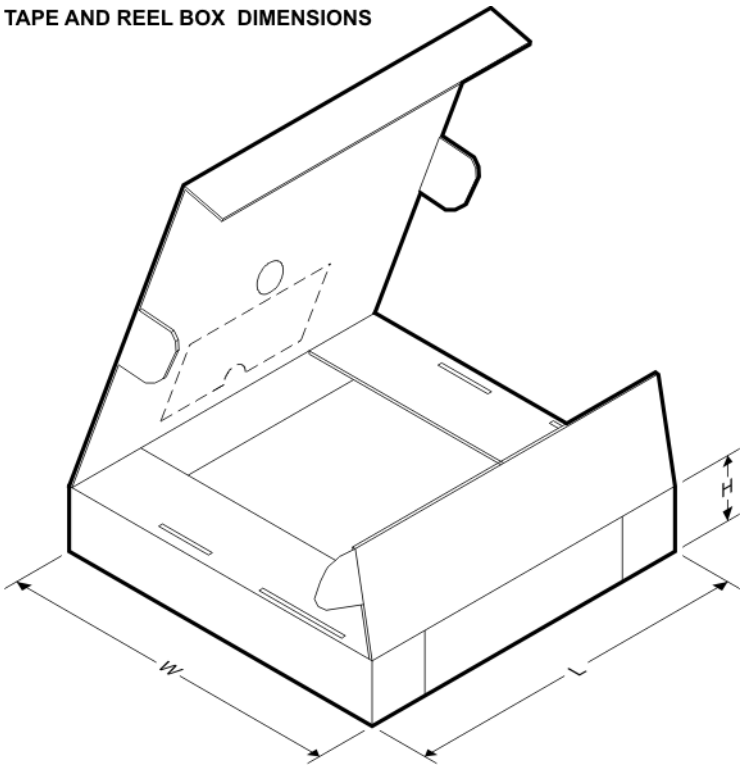
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

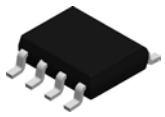
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7021DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7021FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7021DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7021FDR	SOIC	D	8	2500	367.0	367.0	38.0

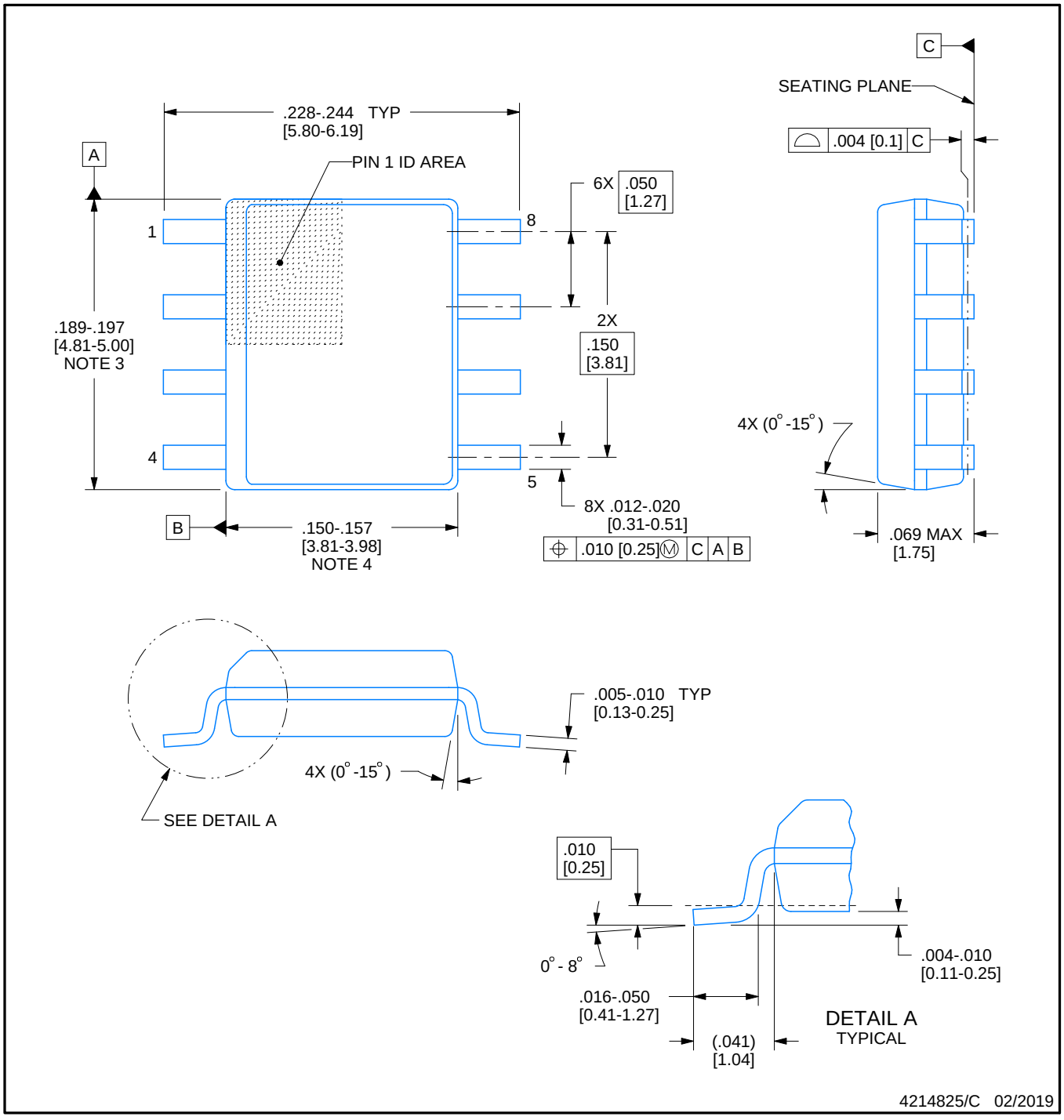


PACKAGE OUTLINE

D0008A

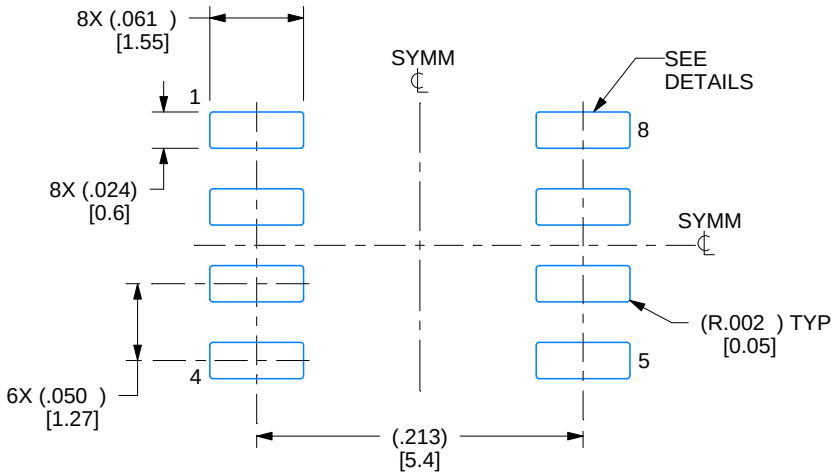
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

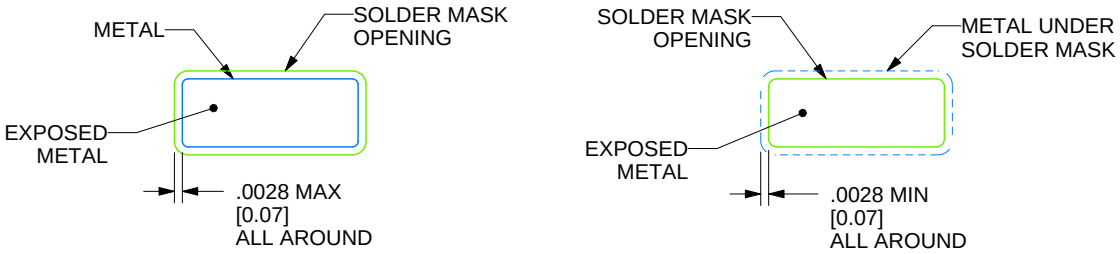


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

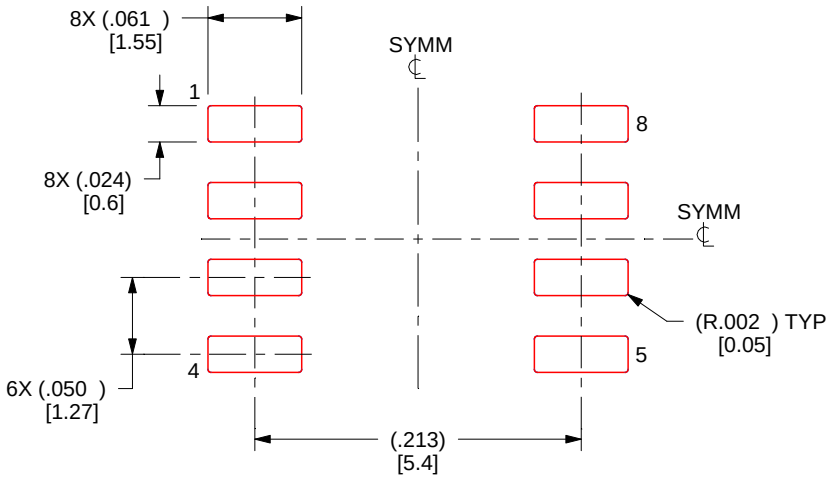
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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