User's Guide
SLLU298–May 2018

ISO5852SDW Driving and Protecting SiC and IGBT Power Modules

This user's guide describes the characteristics, operation, and use of the ISO5852SDWEVM-017 Evaluation Module (EVM). This TI EVM provides driving and protection for popular Silicon Carbide (SiC) MOSFET and Si IGBT Power Modulues. A complete schematic diagram, printed-circuit board layouts, and bill of materials are included in this document.

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1 Overview

The ISO5852SDWEVM-017 is a compact, dual channel isolated gate driver board providing drive, bias voltages, protection and diagnostic needed for half-bridge SiC MOSFET and Si IGBT Power Modules housed in 150-mm × 62-mm × 17-mm packages.

This TI EVM is based on 5.7-kVrms reinforced isolation driver IC ISO5852SDW in SOIC-16DW package with 8.0 mm creepage and clearance. The EVM includes SN6505B based isolated DC-DC transformer bias supplies.

Isolated temperature and input rail monitoring is provided by 5-kVrms isolated amplifiers AMC1301.

Compact form factor 100-mm × 62-mm × 6.6-mm, excluding connector height, allows direct connection to standard 62-mm half-bridge modules.

1.1 Features

This EVM supports the following features:

- 20-A peak split sink and source drive current to optimize turn on and turn off switching time
- Two, 2-W output bias supplies with undervoltage lockout (UVLO) and overvoltage lockout (OVLO) protection
- Turn ON and turn OFF drive voltages can be programmed independently from 12 V to 21 V and from –3.3 V to –7 V respectively by using two input supplies from 3.3 V to 5.3 V
- Robust noise-immune solution with CMTI >100 V/ns
- Supports 5-kVrms Reinforced Isolation for input rail up to 1700-V
- Programmable Short-circuit sensing and Soft Turn-OFF protection by de-saturation circuit
- 2-A Active Miller Clamp
- Output Short Circuit Clamp
- Fault feedback with reset
- Temperature and input rail monitoring

1.2 Applications

This EVM is used in the following applications:

- Solar inverters
- Motor drives
- HEV and EV chargers
- Wind turbines
- Transportation
- UPS

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1.3 Description

Compact driver board ISO5852SDWEVM-017 supports SiC power modules by reducing parasitics, minimizing switching loss and EMI and providing full required protection and diagnostics features.

1.3.1 Specification

Electrical parameters of the board are shown in Table 1.

Table 1. Electrical Specifications

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS						
VCC	Primary supply voltage		4.5	5.0	5.5	V
IVCCQ	Primary quiescent current	IN+, IN- low		30		mA
IVCCS	Primary supply current	FSW = 10kHz, CLOAD = 10nF		210		mA
VCCUR	Vcc rising UVLO threshold			4.5	4.6	V
VCCUF	Vcc falling UVLO threshold		4.2	4.3		V
VCCUH	Vcc UVLO hysteresis			0.2		V
VCCOR	Vcc rising OVLO threshold			5.7	5.8	V
VCCOF	Vcc falling OVLO threshold		5.4	5.5		V
VCCOH	Vcc UVLO hysteresis			0.2		V
VCC2U, VCC2L	Turn ON drive voltages	Transformer 750342879	15	17	19	V
VCC2U, VCC2L	Turn OFF drive voltages	Transformer 750313734	–5.9	–5	–4.7	V
DRIVE CURRENT AND POWER						
IOH	Peak source current	CLOAD = 10nF	15	20		A
IOL	Peak sink current	CLOAD = 10nF	15	20		A
PDRV	Drive power per channel	At 25ºC			2.0	W
INPUT/OUTPUT SIGNALS						
VINR, VRSTR	INL+, INU+, RST rising threshold				0.7 × VCC	V
VINF, VRSTF	INL+, INU+, RST falling threshold		0.3 × VCC			V
VINH, VRSTH	INL+, INU+, RST hysteresis			0.15 × VCC		V
VFLU, VFLL	FL, FU Fault voltage	IFLT = 5 mA			0.2	V
VFLU, VFLL	FL, FU Fault current	Internal pullup current		100		µA
VFLTH	F high level	At VCC = 4.5 V	4.4	4.5		V
VFLTL	F low level	At VCC = 4.5 V			0.1	V
ATEMP	Thermistor monitor gain			8.2		
ARAIL	Input rail monitor gain			8.2		
TIMING PARAMETERS						
TRISE	Drive output rise time	CLOAD = 10nF		30		ns
TFALL	Drive output fall time	CLOAD = 10nF		34		ns
TPROP	Propagation delay	CLOAD = 100nF		130	150	ns
TSKEW	Pulse skew				20	ns
TGLITCH	Input glitch filter		20	30	40	ns
TUVLO	UVLO recovery delay			50		µs
TOVOL	OVLO recovery delay			50		µs

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Table 1. Electrical Specifications (continued)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
SHORT CIRCUIT PROTECTION						
VDESAT	Nominal desaturation threshold	Can be programmed by resistors down to 4 V	8.3	9.0	9.5	V
TDESATBLNK	Blanking time		310	400	480	ns
TDS90	Response time to 90% VOUTHL	CLOAD = 10nF		553	760	ns
TDS10	Response time to 10% VOUTHL	CLOAD = 10nF		2	3.5	µs
ICHARGE	Capacitor charge current		0.42	0.5	0.58	mA
IDISCHARGE	Capacitor discharge current		9	14		mA
VCLAMP	Miller clamp threshold		1.6	2.1	2.5	V
ICLAMP	Miller clamp current			4		A
ISOLATION						
CMTI		CMTI	100			V/ns
VISO	Withstand isolation voltage	Reinforced, 60s	5.0			kVrms
CI	Barrier capacitance				20	pF
TA	Operating Ambient Temperature		-40	25	125	oC
SIZE						
Board size		Without connector	100 x 62 x 6.6			mm

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1.3.2 Block Diagram

The ISO5852SDWEVM-017 board block diagram is shown in Figure 1.

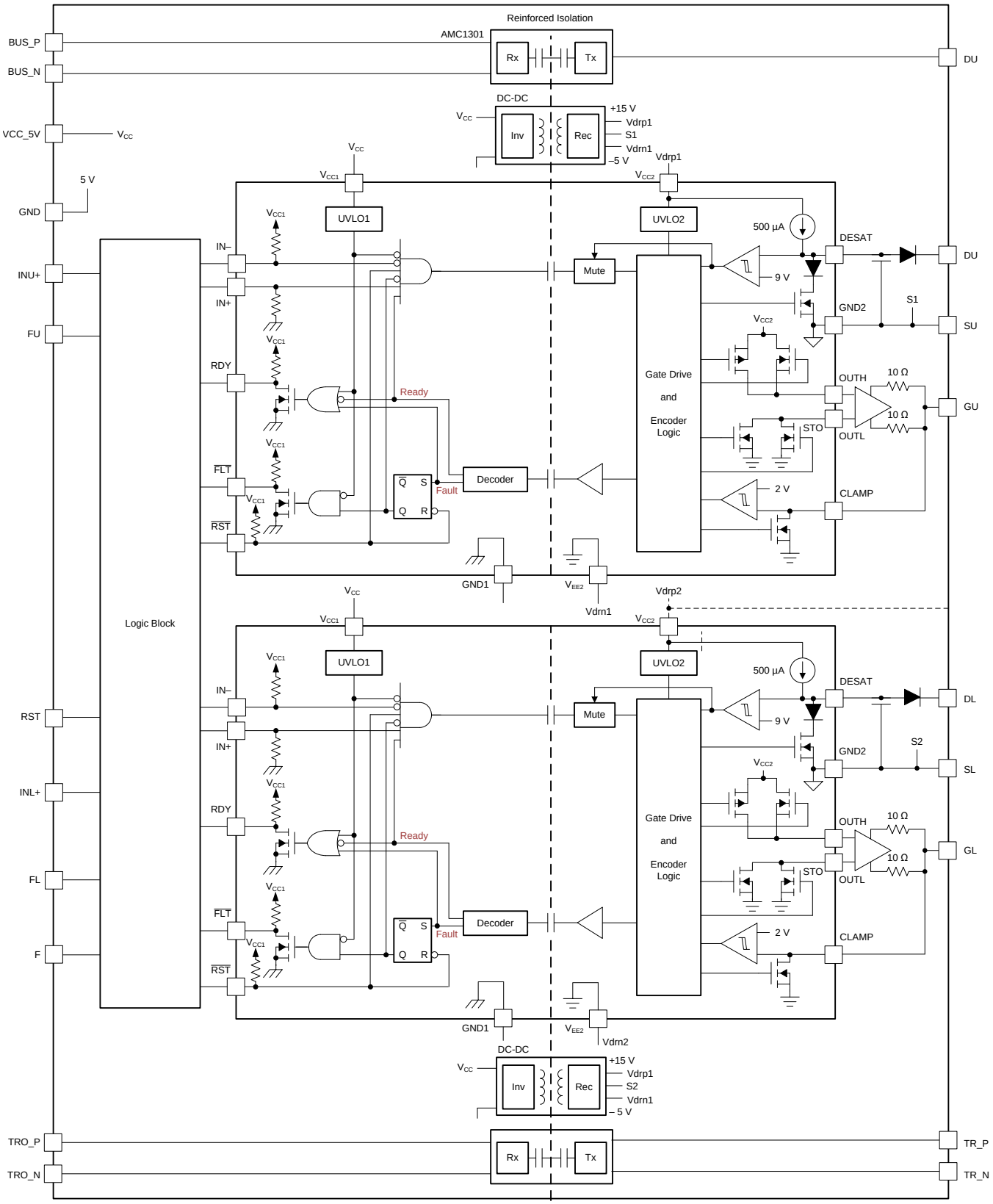


Figure 1. ISO5852SDWEVM-017 EVM Block Diagram

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It includes two isolated channels with the following key functional blocks:

- 20A source/sink 5.7 kVrms Isolated driver using ISO5852SDW driver IC
- Split rail bias supply using two 424 kHz transformer drivers SN6505B to generate separately +17 V rail for turn ON and -5 V rail for turn OFF
- Input logic block with shoot-through prevention
- Output protection and diagnostic block
- Analog amplifiers AMC1301 to monitor temperature inside the module and input voltage rail with 5.0 kVrms isolation

1.3.3 Isolated Gate Driver ISO5852S

ISO5852SDW, isolated driver in SOIC-16DW package with 8.0mm creepage and clearance providing 5.7kVrms reinforced isolation, includes all main short circuit protection features. ISO5852SDW driver IC employs TI proprietary high voltage, low propagation delay, CMTI immune capacitive isolation technology. The list of isolation safety certifications from agencies like VDE, CSA, UL and CQC is provided in related datasheet. Short, 76 ns propagation delay with only 20 ns skew allows accurate control of power devices. Figure 1 includes block diagram of ISO5852SDW driver.

Primary side voltage Vcc1 is controlled by internal UVLO1 circuit with 2.25Vmax rising threshold and 1.7Vmin falling threshold. Inverting and non-inverting input signals IN- and IN+ have CMOS thresholds derived from Vcc1 voltage: 0.7 x Vcc1 max rising and 0.3 x Vcc1 min falling accordingly. Secondary side voltage Vcc2 can go up to 35V abs. max. Turn ON drive voltage between Vcc2 and GND2 pins is controlled by internal UVLO2 circuit with 13Vmax rising threshold and 9.5V min falling threshold. The split sink/source output allows setting optimal turn ON and turn OFF time by selecting separate gate resistors between driver output and gate of power device. This driver has all necessary short circuit protection features including desaturation current sensing, soft short circuit turn OFF, Miller gate clamp, fault, power ready and reset signals.

1.3.4 Split-Rail Bias Supply using SN6505B

Split rail bias supply generates 17V turn ON, and -5V turn OFF voltages using two push-pull transformer drivers SN6505B operating at 424kHz and housed in 6-pin small SOT-23 package.

The SN6505B is supplied through Vcc terminal from external source in the range from 2.25 to 5.5V. Input voltage is controlled by UVLO circuit having rising threshold 2.25Vmax and falling threshold 1.7V min. Internal oscillator operates at 424kHz typical frequency within range from 363 kHz min. to 517 kHz max.. The SN6505 employs spread spectrum clocking technique to minimize EMI. The output stage includes 1A push-pull switches rated up to 16 V abs. max. The switches are protected by current limit circuit tripped at 1.7 A typ. level. The device also protected by thermal shutdown circuit triggered at 168 ºC typical threshold and returning back to normal operation at 150 ºC typical. Additional features include soft start and Enable signal. Because there is no closed feedback loop in this inexpensive bias supply solution, it operates like DC-DC transformer and requires low tolerance primary voltage to maintain output voltages within ±10% range.

1.3.5 Input Logic

Input logic block fulfills the following functions:

- Provides additional UVLO and OVLO protection of secondary side drive voltages using sensing on primary side Vcc based on window comparator TPS3700
- Generates separate fault signals for each channel when the short circuit occurs along with general system fault signal using AND logic CMOS IC SN74AHC1G08QDBVRQ1
- Generates combined Reset signal output for both isolated channels
- Provides isolated differential output signals from temperature and input rail monitoring circuits using isolated amplifiers AMC1301
- Can be set for driver outputs overlapping prevention mode by having shunt resistors R48 and R52 in place. To allow outputs overlapping simply remove shunt resistors R48 and R52.

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1.3.6 Output Protection and Diagnostic

The output boost and protection blocks fulfill the following functions:

- Boost sink and source currents up to 20 A typical
- Determine short circuit conditions using Vds sensing
- Provide analog isolated input rail sensing signal using AMC1301 amplifier
- Provide analog isolated temperature monitoring using thermistor inside the module and AMC1301 amplifier

1.3.7 Isolated Differential Amplifier AMC1301

The AMC1301 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier providing protection from electromagnetic and electrical noise in the system.

The input of the AMC1301 device is optimized for sensing signals in ±250 mV range with high immunity to common mode noise. The amplifier is housed in wide body SOIC-8DWV package with 9 mm creepage and clearance.

1.3.8 Board Views

Top view of the driver board ISO5852SDWEVM-017 is shown in Figure 2. Figure 3 shows the driver EVM soldered on top of power module.

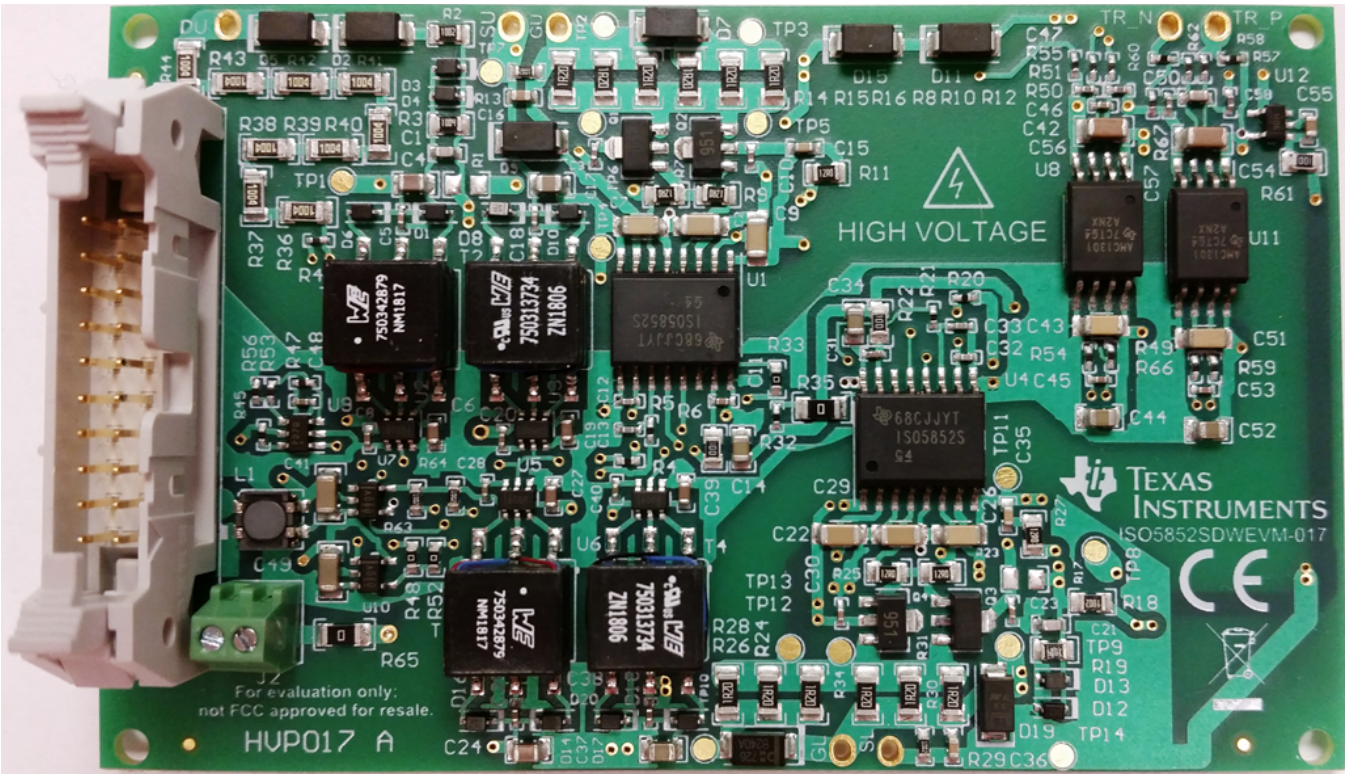


Figure 2. ISO5852SDWEVM-017 Top View

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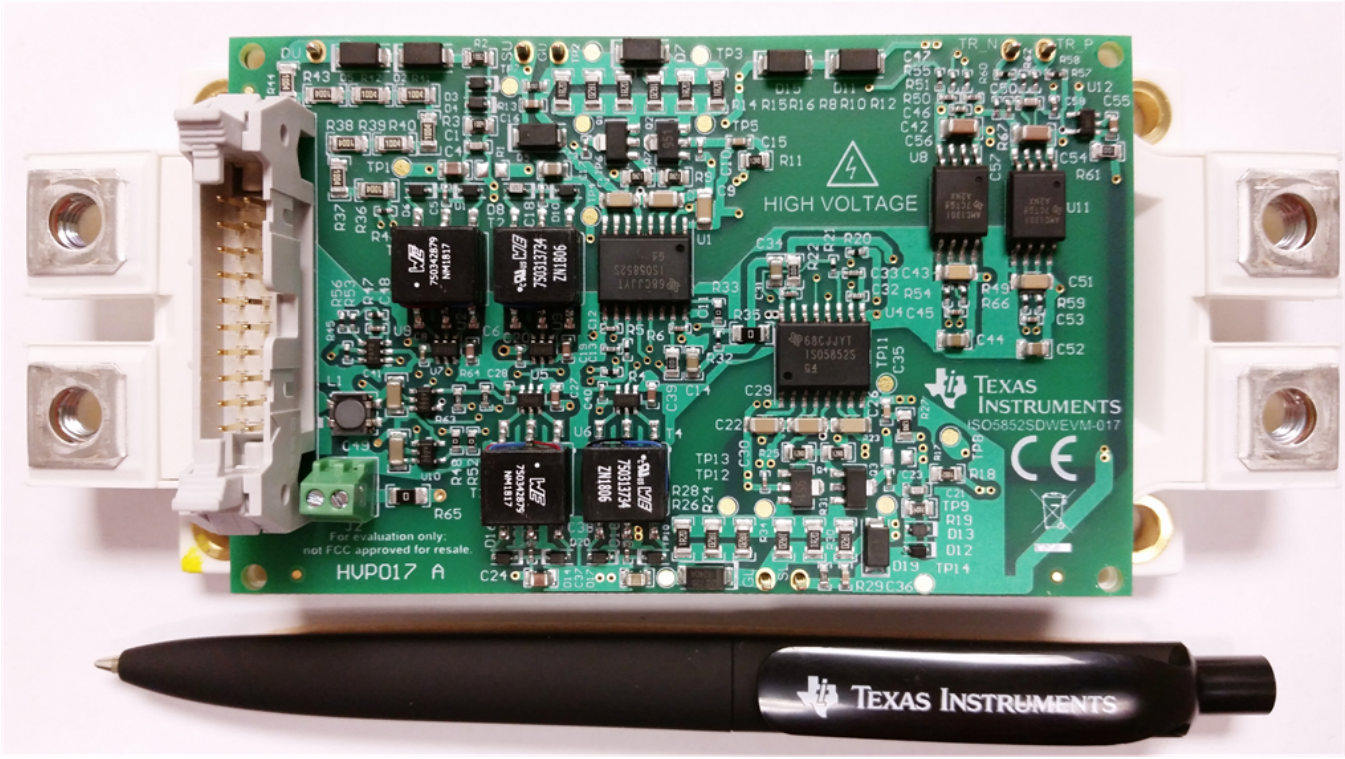


Figure 3. ISO5852SDWEVM-017 Mounted on Top of Power Module

2 Test Setup and Results

Test setup and related waveforms presented in User's Guide are for ISO5852SDWEVM-017 EVM EXCLUDING any user provided power modules attached to backside of the EVM. Capacitive load presented by power module is emulated by 10 nF capacitors C16 and C36. When EVM is attached to and evaluated with power module, capacitors C16 and C36 should be removed.

2.1 Before You Begin

When starting to evaluate and test the ISO5852SDWEVM-017 EVM, it will typically be in a stand-alone configuration, separate from power module. This EVM does not internally generate high voltages or high temperatures.

In the start-up configuration, there will be no high voltage or high temperature capable of presenting the user with an electrical shock hazard or burn resulting from elevated temperature risks provided the EVM is used within its electrical load rating limits established in Table 1.

WARNING

To minimize risk of electric shock hazard always follow safety practices normally followed in a development laboratory. Refer to TI's EVM High Voltage guideline accompanying this EVM.

However, to evaluate isolated input rail amplifier voltages in accordance with the described below test procedure 2.2.4, which requires the addition of an external power source with maximum rating of 300 VDC, high voltage may be accessible between board test points DU and SL.

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To minimize risk of electrical shock hazard, always follow all high voltage safety rules and regulations while operating electrical equipment!

When evaluating ISO5852SDWEVM-017 with EVM attached to its intended vendor provided power module as part of the system level measurements and assessments, the power module will have accessibility of high voltage and high temperatures that impact the EVM's operating conditions as well. High voltages with transients up to 1500Vpk can appear between isolated areas of the EVM, bounded as illustrated in Figure 9. The externally provided power module also radiates heat that indirectly provides air flow and convection that can elevate the temperature of EVM board.

WARNING

To minimize risk of fire hazard, it is critical to assure that the external power module's electrical and thermal ratings are never exceeded as published by the external power module's manufacturer's datasheet, and the maximum temperature of any external power module should never exceed 130 °C.

The EVM provides isolated thermal dissipation diagnostic signals available at connector J1 shown in Figure 9, which measure high voltage input rail and thermistor temperatures inside the external power module. Both BUS_P (pin 17) to BUS_N (pin 18) and TRO_P (pin 20) to TRO_N (pin 19) diagnostic signals must be strictly monitored to assure both high voltage and thermal protective features are being utilized.

The user is required to provide necessary interface controller hardware to shut down and deenergize the system immediately if BUS_P to BUS_N signal exceeds 1.85 VDC, or signal TRO_P to TRO_N drops below 0.135 VDC.

2.2 Equipment

- Power Supplies
  - At least up to 6-V and 1-A power supply for powering EVM, for example: BK Precision, series 1715
  - At least up to 300-V and 10-mA power source for testing bus isolated sense amplifier within EVM
- Function Generator and accessories
  - One 2-channel function generator, for example: Tektronix AFG3102
  - Two standard 50-Ω BNC coaxial cables
  - Two 50-Ω BNC male to female feed-thru terminators, for example: Tektronix 011-0049-02
- Oscilloscope and accessories
  - Oscilloscope 500-MHz or higher with at least 4 channels, for example: Tektronix DPO7104
  - Four at least 500-MHz bandwidth passive voltage probes, for example: P6139A
- Six Digital Multi-Meters (DMM), for example Fluke 187
- Other
  - 20-wire flat cable with receptacle 71600-120LF from FCI with opposite end wired to PCB with related test points
  - Wires 7 to 10 inch long with clips on both ends to make jumpers on some test points
  - Resistance decade box, for example 72-7270 from Tenma

Test procedure includes four main tests with different test setups

1. Power up and bias supply voltages test
2. Input and output pulse switching waveforms test
3. Thermistor isolated amplifier input and output signal test
4. Bus voltage sense isolated amplifier input and output signal test

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All test setups shown in the following figures assume the flat test cable with receptacle and test points is attached to the connector J1 of the EVM.

2.2.1 Power UP Test

Test setup for power up test is shown in Figure 4. For these tests digital multi-metersfor DC voltage measurements are set auto-range. MM1 is set for DC current measurements with expected range up to 500 mA. Here and in all test setups below, red arrows indicate positive terminals and black arrows indicate return terminal.

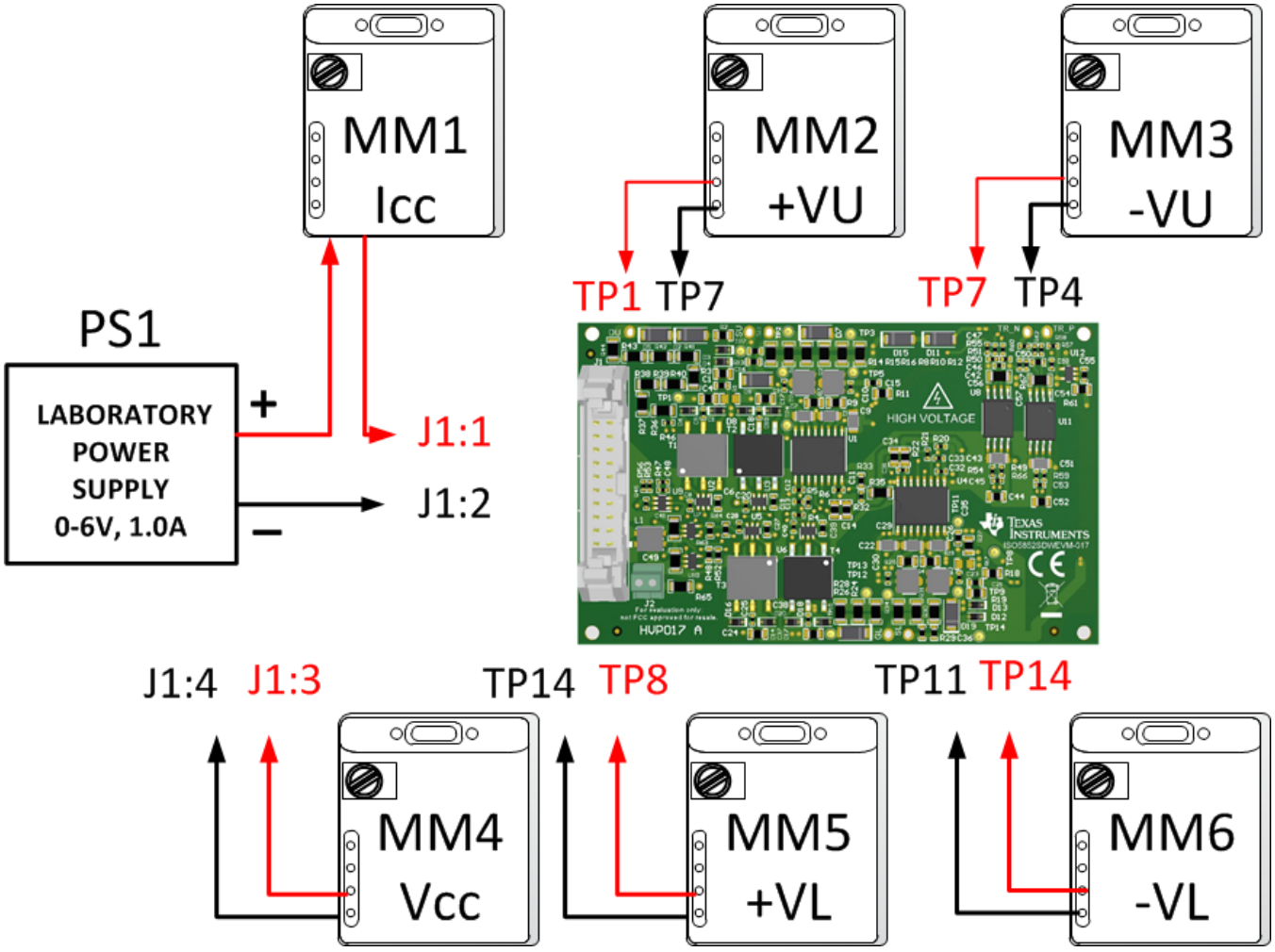


Figure 4. Power Up and Bias Supply Voltages VU and VL Test Setup

WARNING

Before start testing make sure to follow all electrical safety and ESD protection requirements implemented at your company!

1. Enable power supply PS1
2. Gradually increase the voltage at PS1 and monitor voltage using MM4 and current using MM1
3. Verify measured voltage and current in accordance to Table 2. If current or voltage is outside the specified range, stop increasing the voltage at PS1 and return to initial stage
4. Gradually reduce the voltage at PS1 to 0 V and disable it

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Measured voltages and current should be within range shown in Table 2.

Table 2. Voltages and Current During Power Up Test

MM4 (Vcc)	MM1 (Icc)	MM2 (+VU)	MM3 (-VU)	MM5 (+VL)	MM6 (-VL)
2.95 V – 3.05 V	< 30 mA	< ±0.1 V	< ±0.1 V	< ±0.1 V	< ±0.1 V
4.65 V – 4.75 V	130 mA – 145 mA	15.5 V – 16.5 V	4.5 V – 5.2 V	15.4 V – 16.4 V	4.5 V – 5.2 V
4.95 V – 5.05 V	135 mA – 150 mA	16.8 V – 17.5 V	5.0 V – 5.5 V	16.6 V – 17.4 V	5.0 V – 5.5 V
5.4 V – 5.45 V	140 mA – 155 mA	17.5 V – 19.0 V	5.5 V – 6.2 V	17.3 V – 18.8 V	5.5 V – 6.2 V
5.7 V < MM4 < 6 V	< 30 mA	< ±0.1 V	< ±0.1 V	< ±0.1 V	< ±0.1 V

2.2.2 Input and Output Switching Waveforms Test

Test setup for switching waveforms is shown in Figure 5.

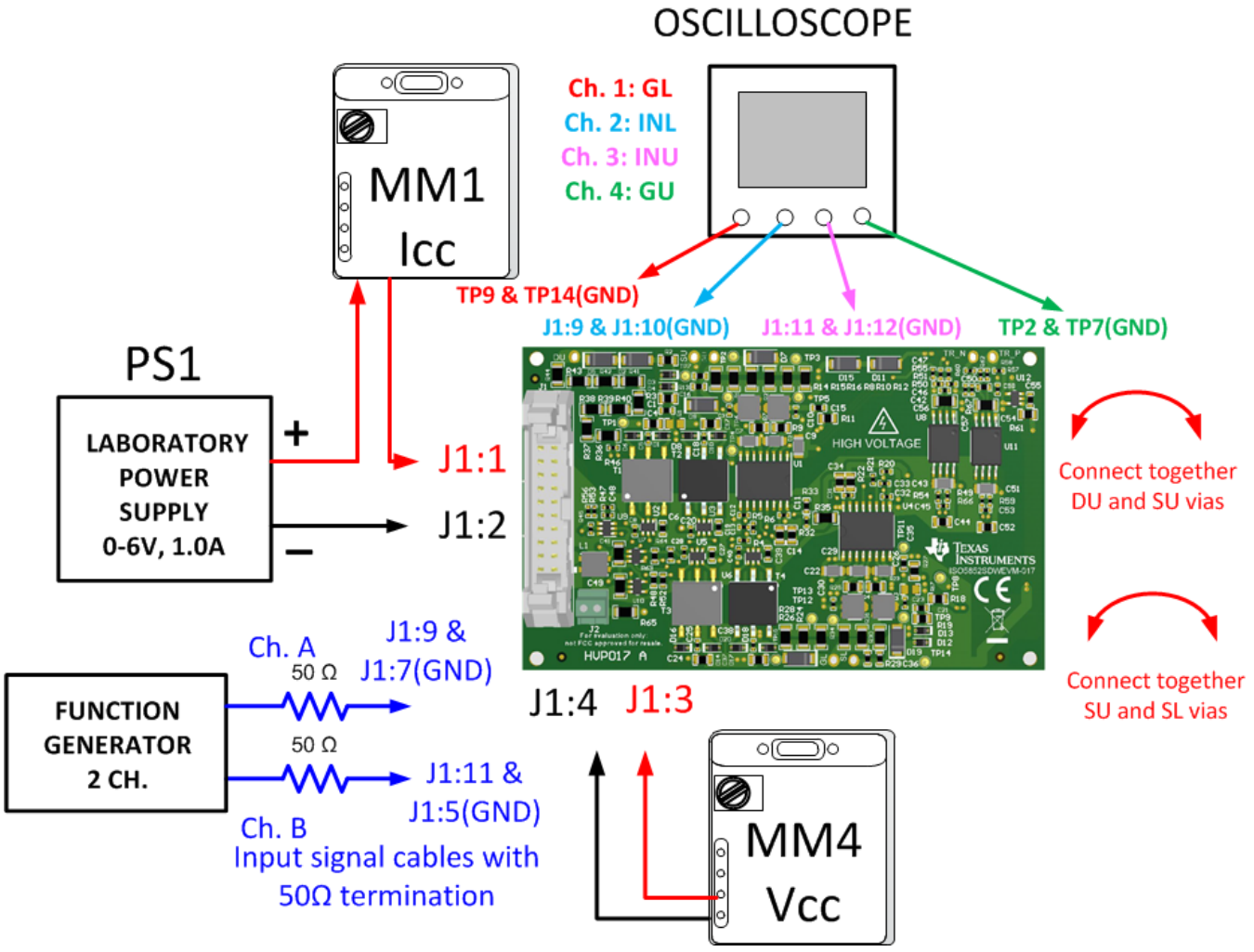


Figure 5. Test Setup for Input and Output Switching Waveforms

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Function generator settings are shown in Table 3.

Table 3. Function Generator Settings

CHANNEL	MODE	FREQ.	WIDTH	DELAY	AMPL.	OFFSET	LOAD IMPED.	FREQUENCY SET
A (Ch.1)	Pulse	10 kHz	80 µs	0	4 Vpp	2.0 V	50 Ω	
B (Ch.2)	Pulse	10 kHz	80 µs	50 µs	4 Vpp	2.0 V	50 Ω	Ch1 = Ch2, ON

Oscilloscope settings are shown in Table 4.

Table 4. Oscilloscope Settings

CHANNEL	VERTICAL SCALE	HORIZONTAL SCALE	BANDWIDTH	COUPLING	TERMINATION	SYNC TRIGGER	RESOLUTION
Ch. 1(red)	10 V/div	50 µs/div	500 MHz or above	DC	1 MΩ		High
Ch. 2(blue)	3 V/div					Ch. 2	
Ch. 3(pink)	3 V/div						
Ch. 4(green)	10 V/div						

1. Enable power supply PS1
2. Gradually increase the voltage at PS1 into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 150 mA
3. Enable channel A (ch.1) and channel B (ch.2) of function generator
4. Monitor current increase at MM1 but does not exceed 250 mA
5. Compare waveforms with typical screen shot showed in Figure 6
6. Disable function generator channels
7. Gradually reduce voltage at PS1 down to 0 and disable it **(Make sure function generator outputs are disabled before this action!)**

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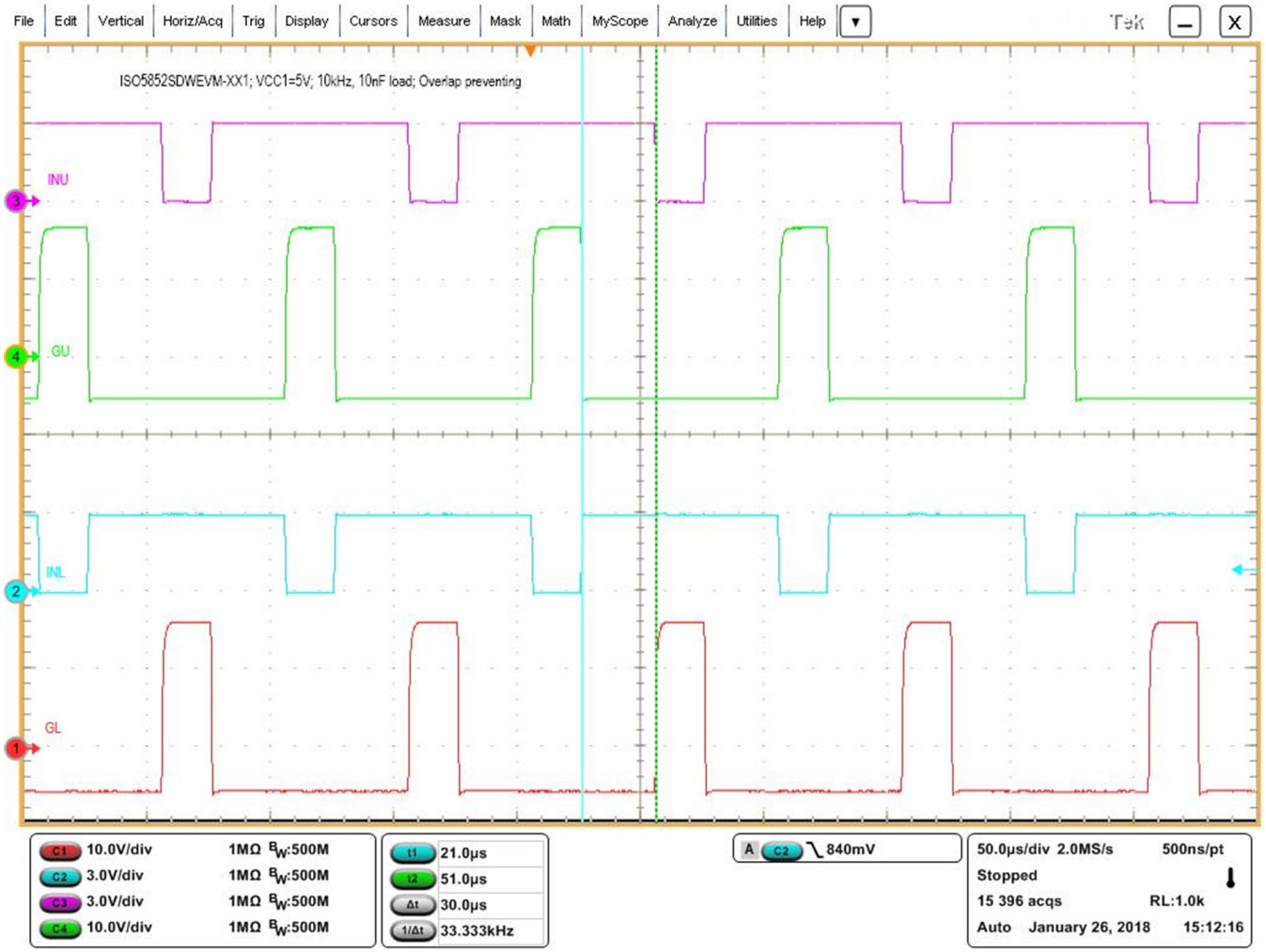


Figure 6. Major Input and Output Waveforms Using Output Overlapping Prevention Feature

- INU (pink) is high side input: 3.0V/div
- OU (green) is high side output: 10V/div
- INL (blue) is low side input: 3.0V/div
- OL (red) is low side output: 10V/div
- Time scale is 50µs/div

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2.2.3 Thermistor Amplifier Test

Test setup for thermistor amplifier test is shown in Figure 7.

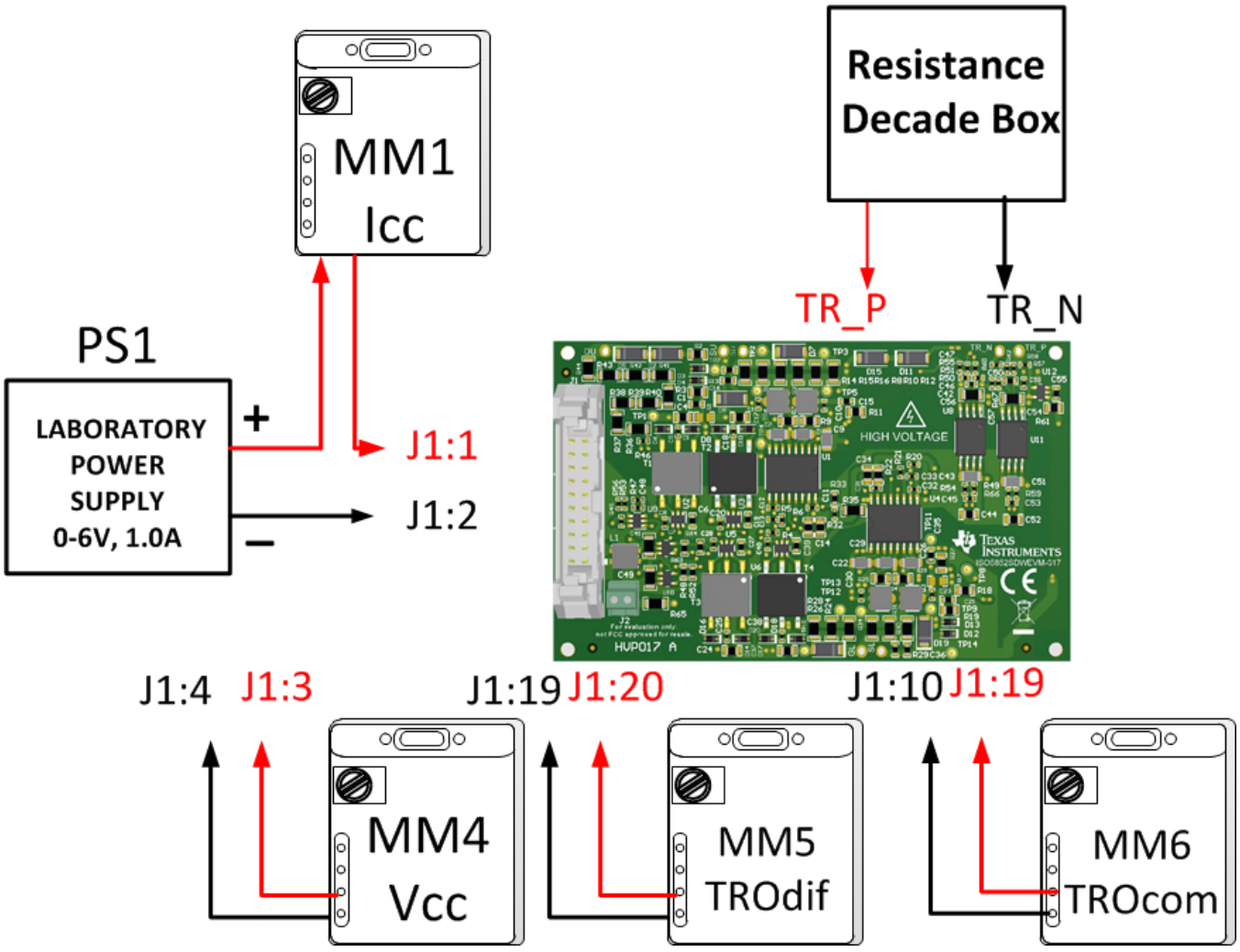


Figure 7. Thermistor Amplifier Test Setup

1. Enable power supply PS1
2. Gradually increase the voltage at PS1 into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 150 mA
3. Set resistances using Resistance Decade Box in accordance to Table 5 and monitor voltages at MM5 and MM6
4. Gradually reduce the voltage of power supply PS1 down to 0 V and disable it

Table 5. Themistor Amplifier Output Signals

RESISTANCE	5.0 kΩ	2.0 kΩ	800 Ω	280 Ω
MM5 (differential output)	1.85 V - 1.91 V	0.85 V - 0.91 V	0.36 V - 0.39 V	0.125 V - 0.145 V
MM6 (common output)	0.4 V - 0.6 V	0.8 V - 1.2 V	1.0 V - 1.4 V	1.2 V - 1.5 V

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2.2.4 7 Sense Amplifier Test

Test setup for input bus voltage sense amplifier test is shown in Figure 8.

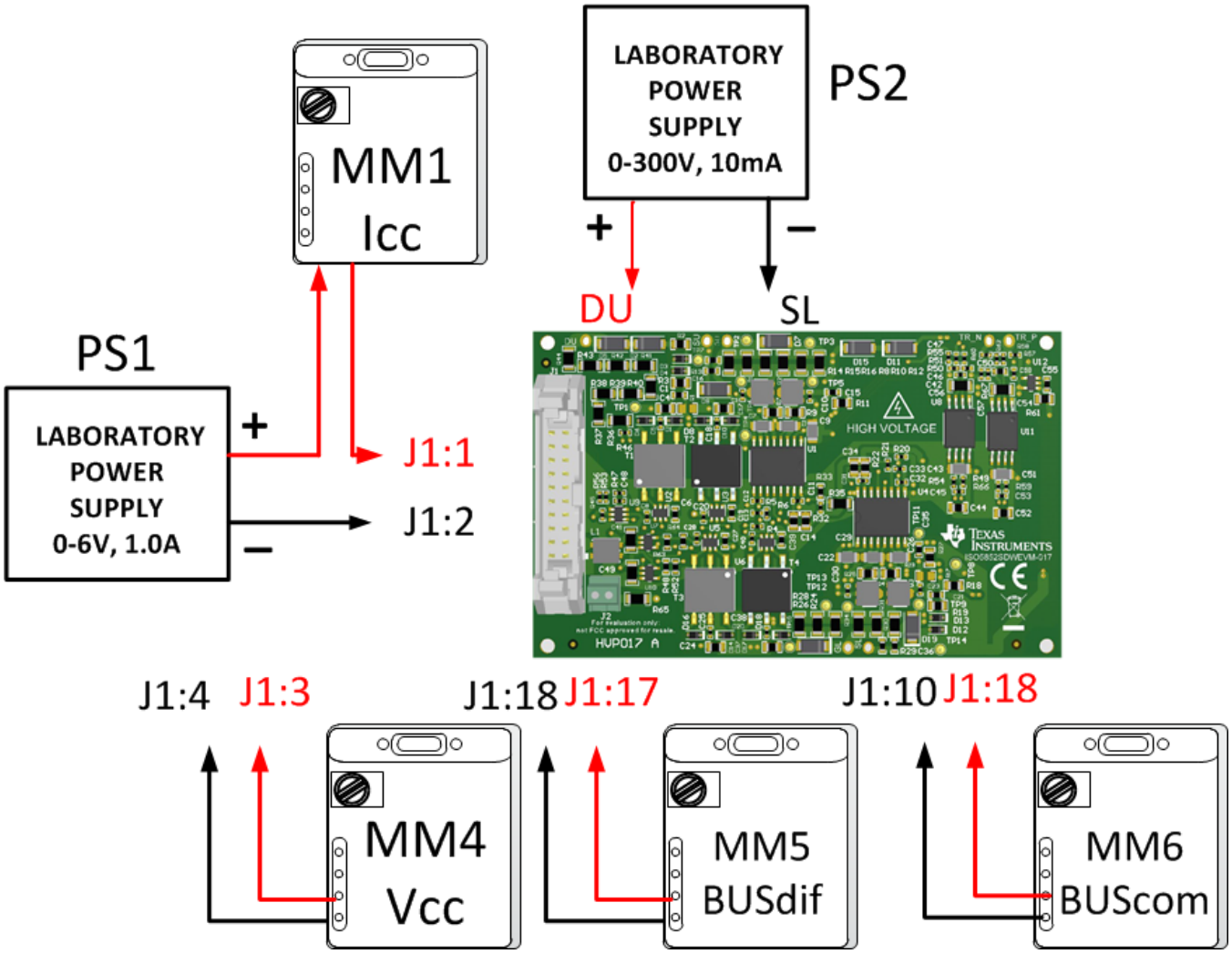


Figure 8. Input Bus Voltage Sense Amplifier Test Setup

1. Enable power supply PS1
2. Gradually increase the voltage at PS1 into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 145 mA
3. Enable power supply PS2
4. Gradually increase the voltage of power supply PS2 from 0 V up to 300 V and monitor voltages in accordance to Table 6
5. Gradually decrease the voltage of power supply PS2 down to 0 and disable it
6. Gradually reduce the voltage of power supply PS1 down to 0 V and disable it

Table 6. Input Bus Voltage Sense Amplifier Outputs

PS2	0 V	49 V - 51 V	99 V - 101 V	149 V - 151 V	299 V - 301 V
MM5 (differential output)	0.28 V - 0.32 V	0.34 V - 0.38 V	0.39 V - 0.43 V	0.42 V - 0.48 V	0.58 V - 0.64 V
MM6 (common output)	1.15 V - 1.45 V	1.1 V - 1.4 V	1.05 V - 1.35 V	1.0 V - 1.3 V	0.95 V - 1.25 V

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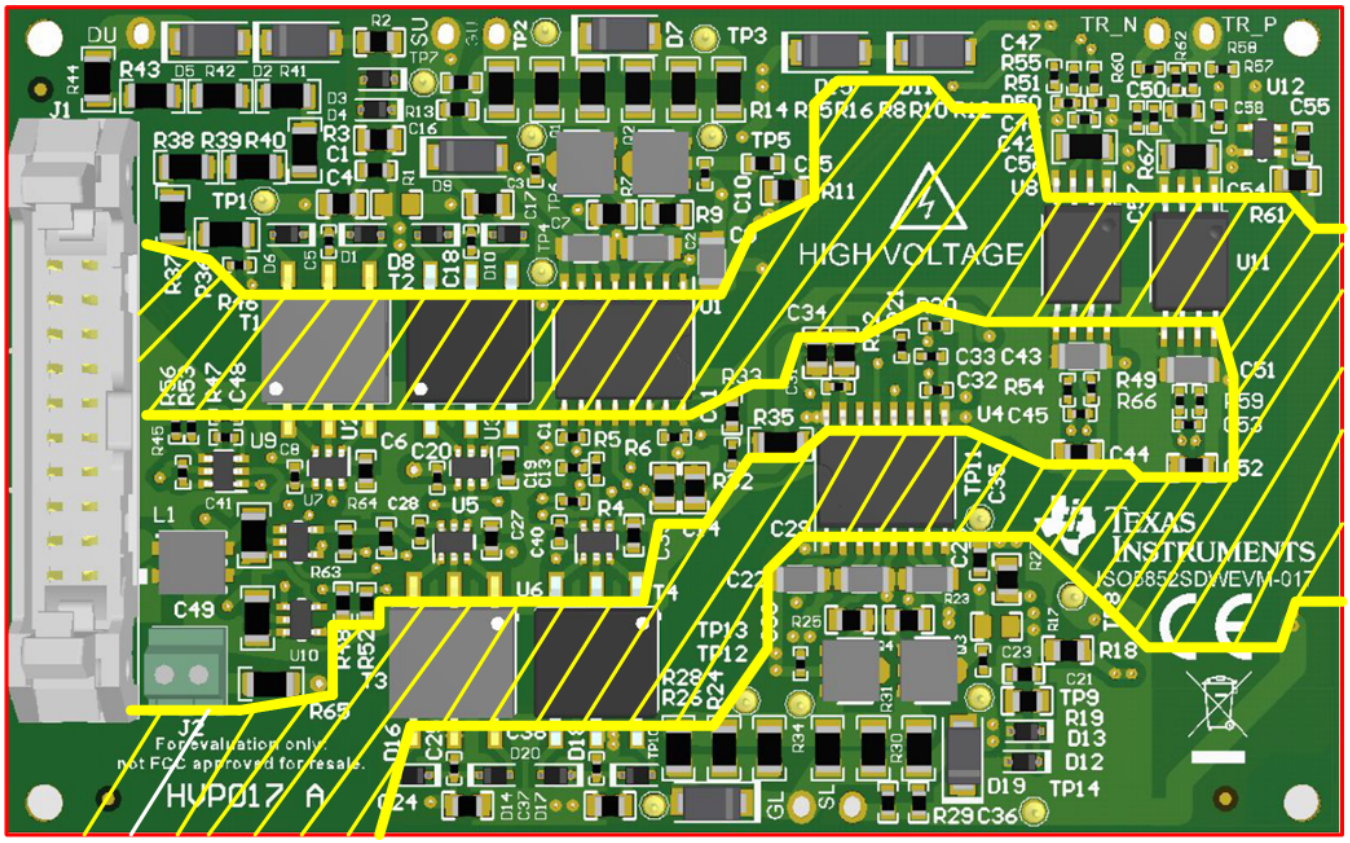


Figure 9. Safety Isolated Regions between High and Low Voltage Board Areas

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3 Board Layout

General top and bottom view, component placement and all four layers are shown in Figure 10 through Figure 16 respectively.

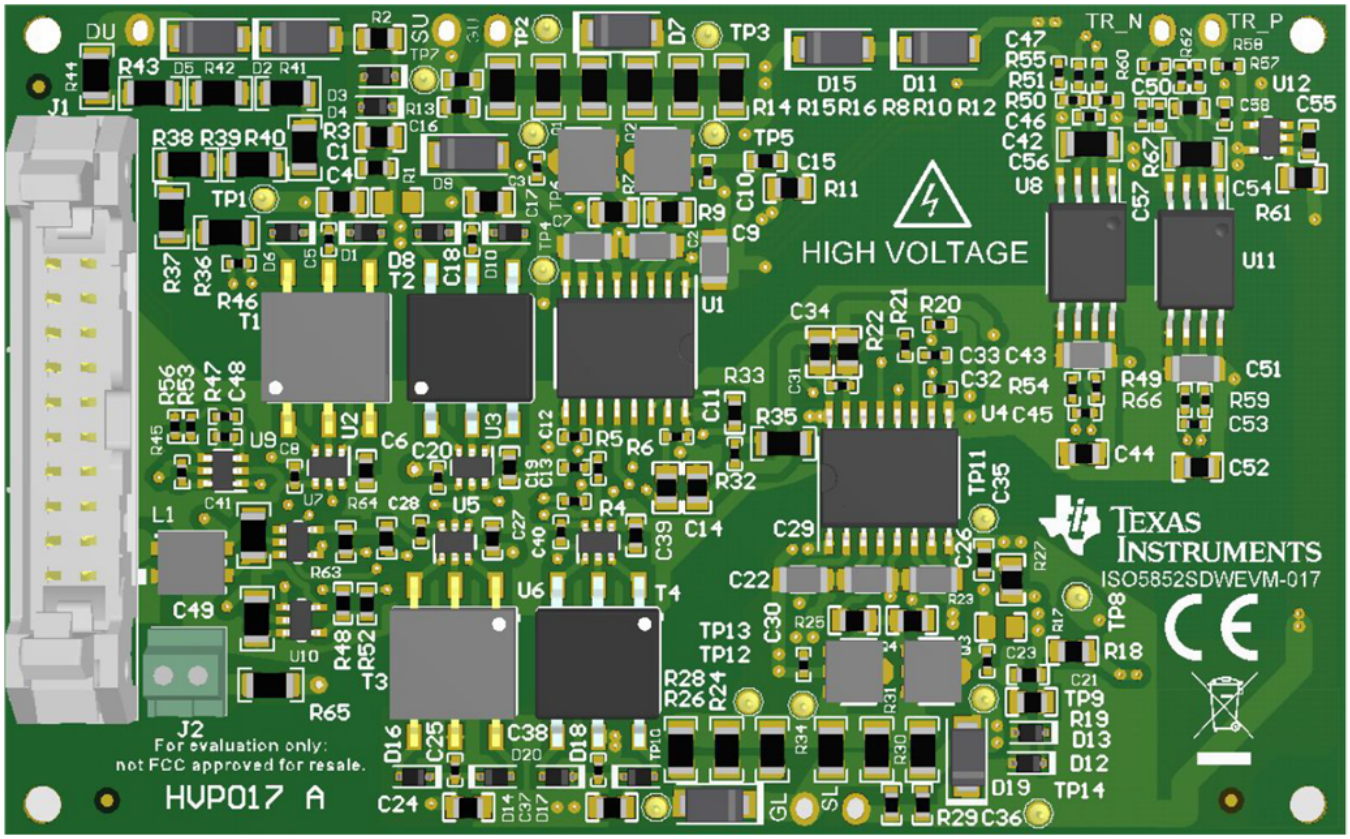


Figure 10. Top View of the Board

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Figure 11. Bottom View Of The Board

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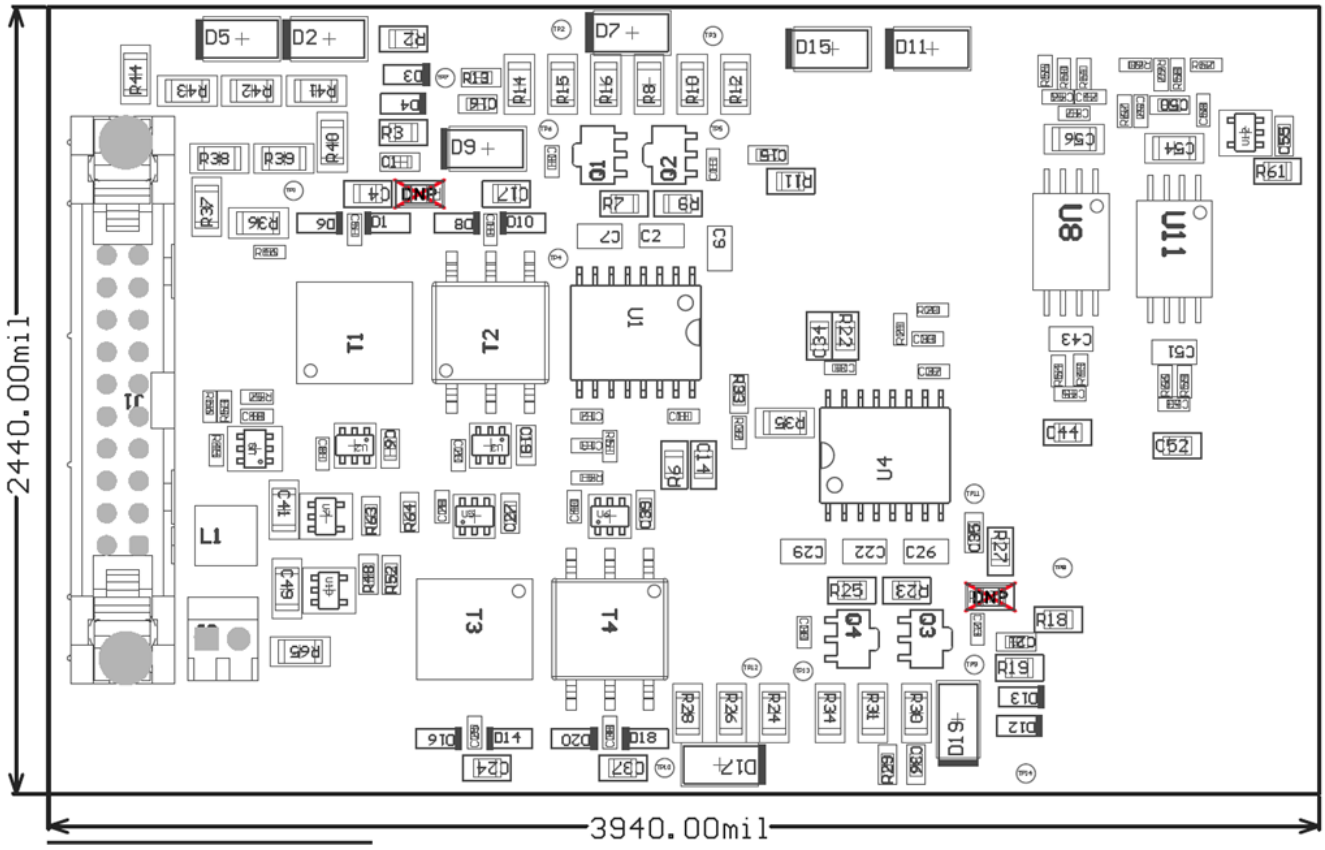


Figure 12. Component Placement

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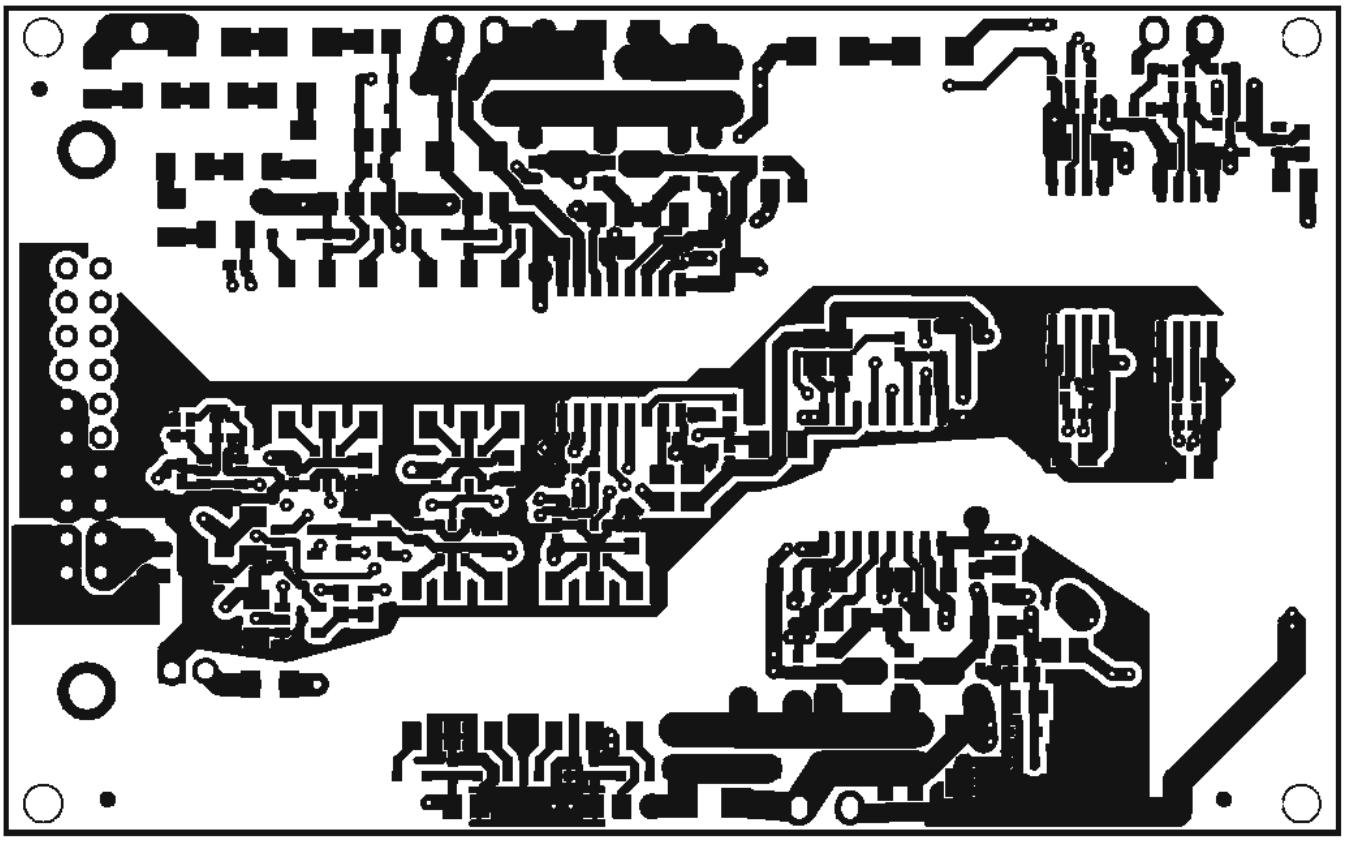


Figure 13. Top Layer

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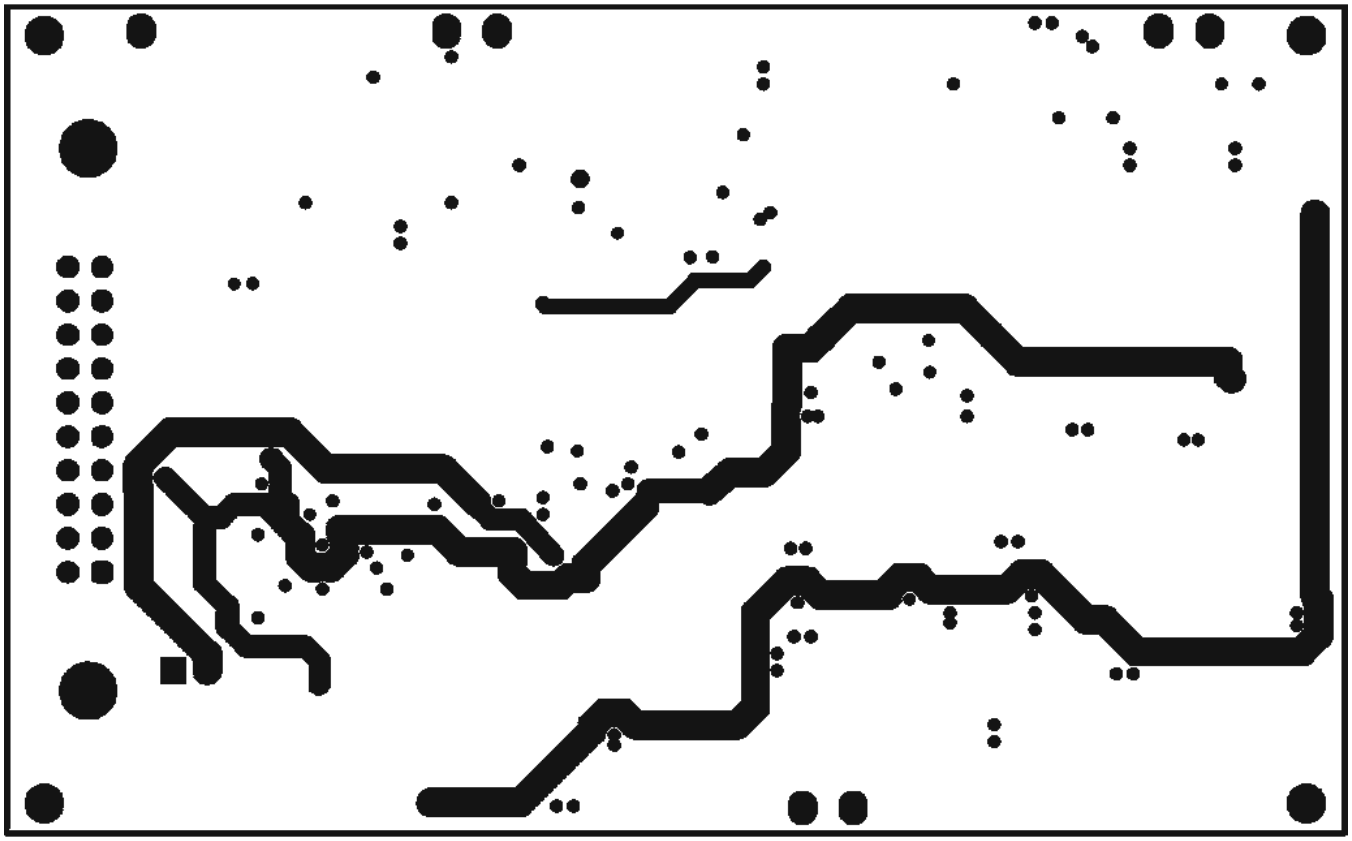


Figure 14. Signal Layer 1

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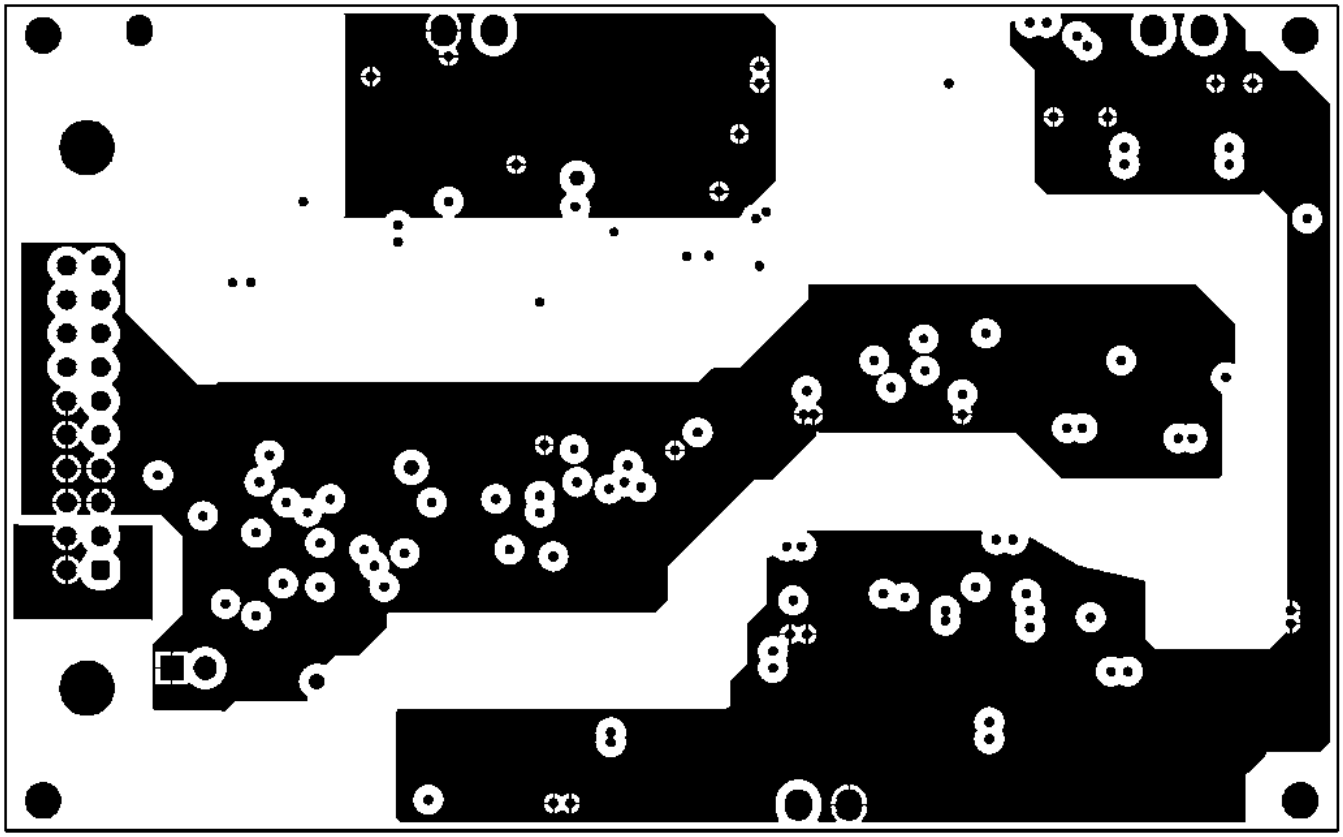


Figure 15. Signal Layer 2

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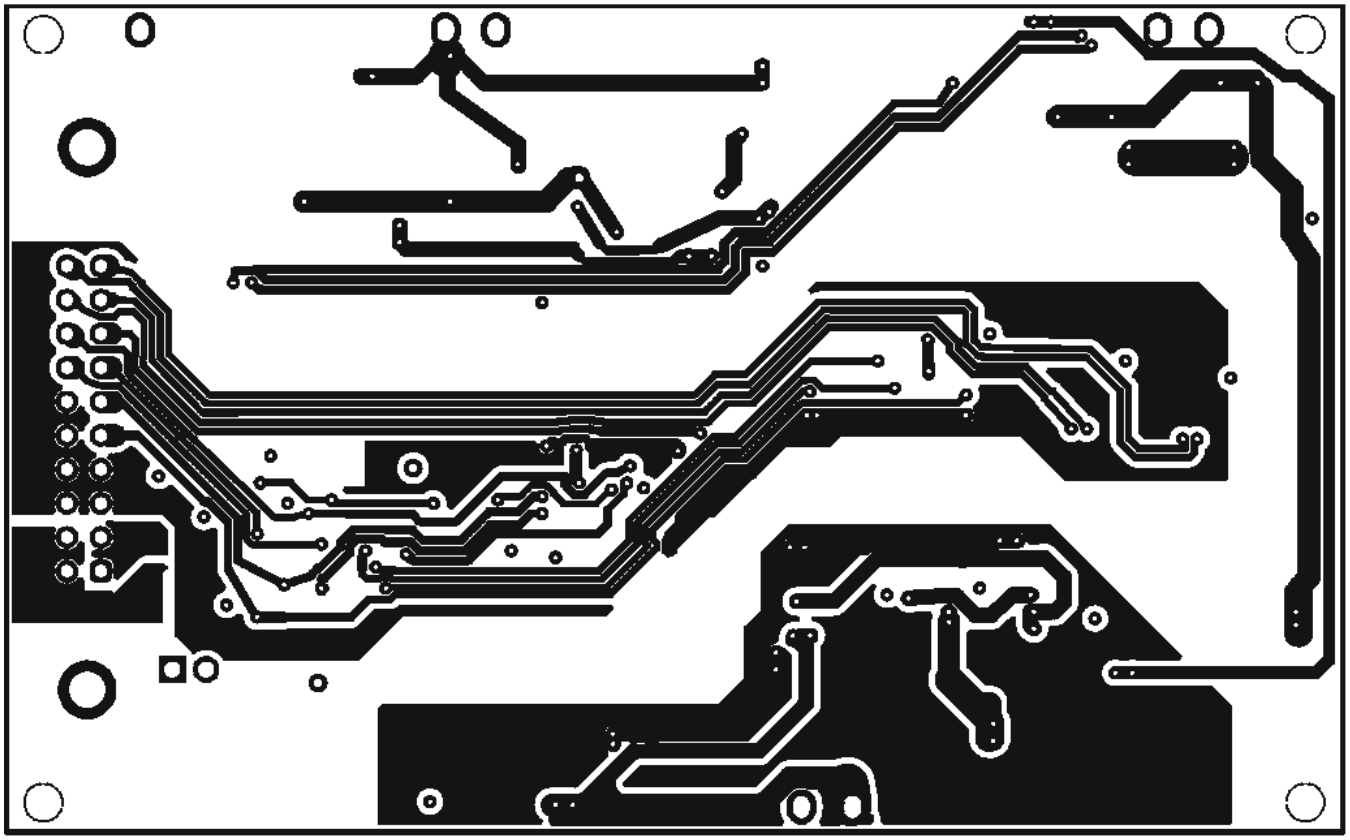


Figure 16. Bottom Layer

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4 Schematic and Bill of Materials

4.1 Schematic

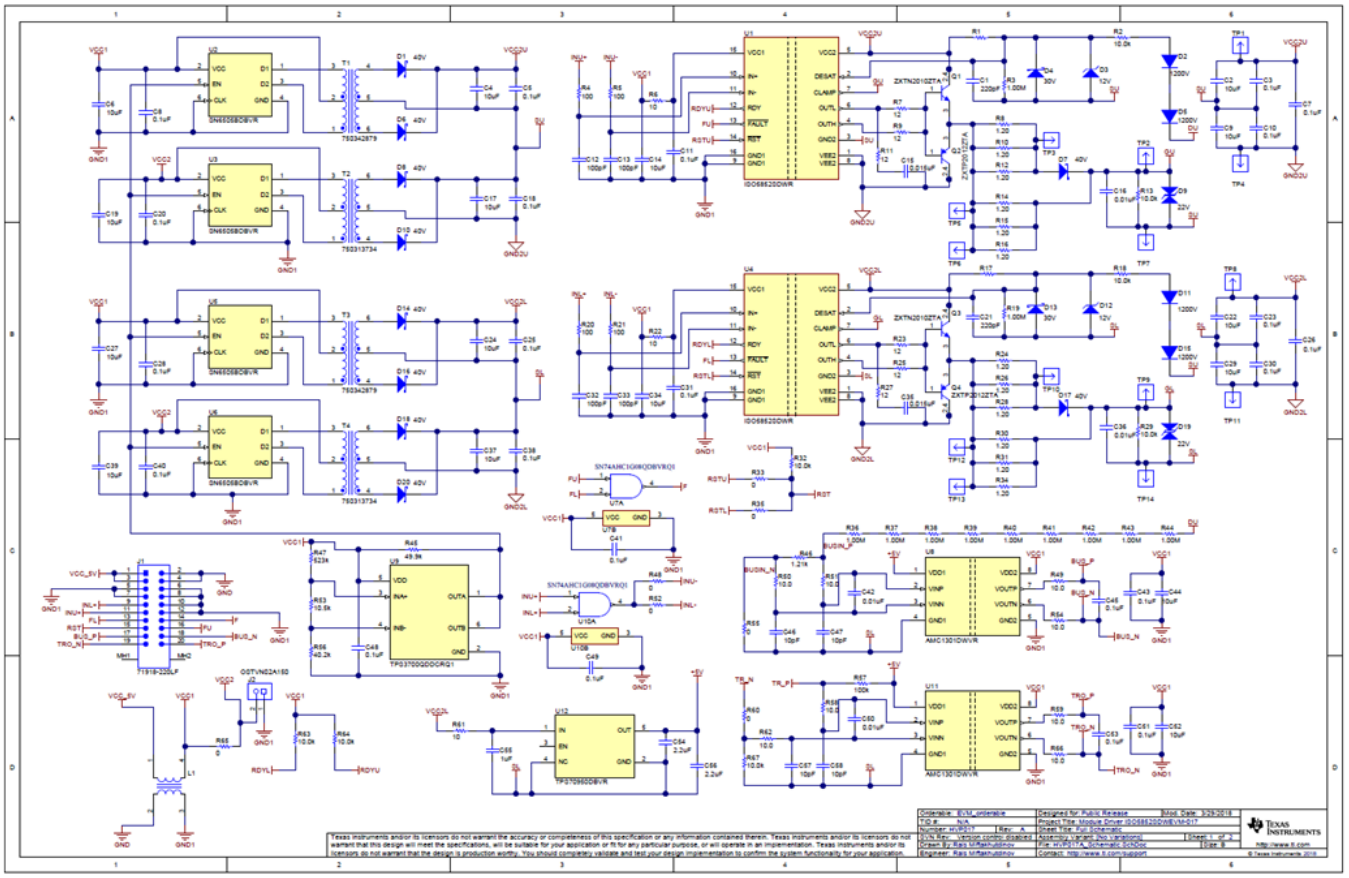
The schematic of ISO5852SDWEVM-017 board is shown in Figure 17. Functional blocks of the schematic are shown in Figure 18 and below are listed the functions that related blocks perform.

- B1 - high side +17.5V/-5V bias supply
- B2 - low side +17.5V/-5V bias supply
- B3 - connectors, UVLO/OVLO protection, fault and reset logic, overlapping option setting
- B4 - high side driver with booster and desaturation protection
- B5 - low side driver with booster and desaturation protection
- B6 - input bus voltage sensing isolated amplifier
- B7 - thermistor based temperature sense isolated amplifier

The ISO5852SDWEVM-017 EVM allows following adjustments depending on applications.

- By default the board set into output overlapping protection mode. Removing resistor shunts R48 and R52 allows output overlapping
- When attaching EVM to power module, it is recommended to remove output load capacitors C16 and C36
- To set turn ON and OFF output driver voltages beoynd the default, UVLO/OVLO protection can be disabled by removing resistor R53
- By removing resistive shunt R65 and using separate input supplies applied to connectors J1 and J2, turn ON and turn OFF drive voltages can be independently adjusted. The EVM maintains functionality if the VCC input supply voltages are within range from 3V to 5.5V. This allows set drive voltages approximately from +12 V to +21 V for turn ON drive voltage and from -3.5 V to -7 V for turn OFF drive voltage
- Change of C15 and C35 values allows soft shutdown adjustment during short circuit protection respectively for high side and low side drivers
- By default resistors R1 and R17 are not included. Adding these resistors provide additional current source for desaturation protection circuit

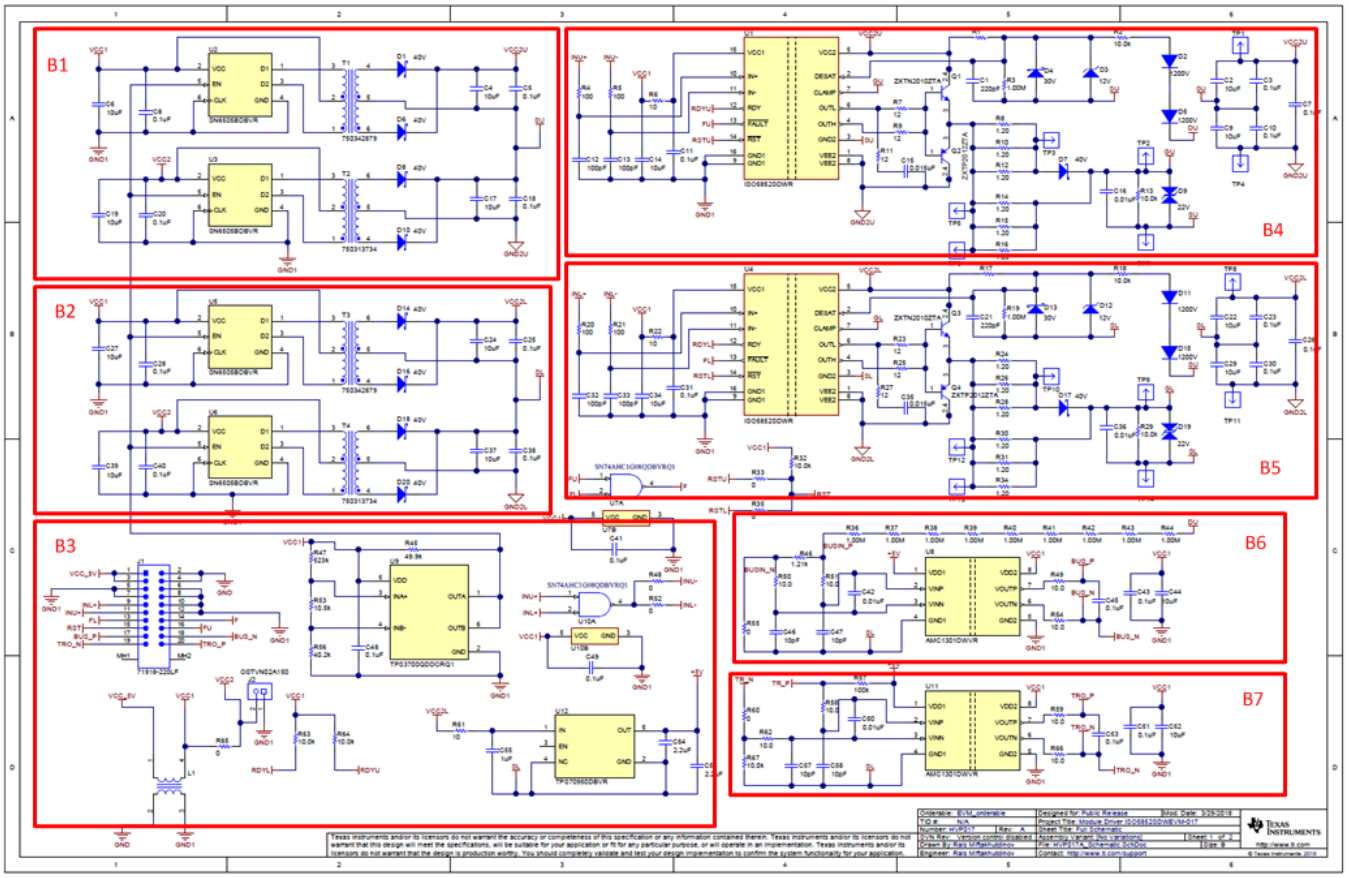
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Figure 17. Electrical Schematic of ISO5852SDWEVM-017

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Figure 18. Electrical Schematic with Functional Blocks Outlined

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Additional waveforms are shown below to illustrate described above adjustments and EVM drive current capabilites. Operation waveforms with overlapping enabled is shown in Figure 19.

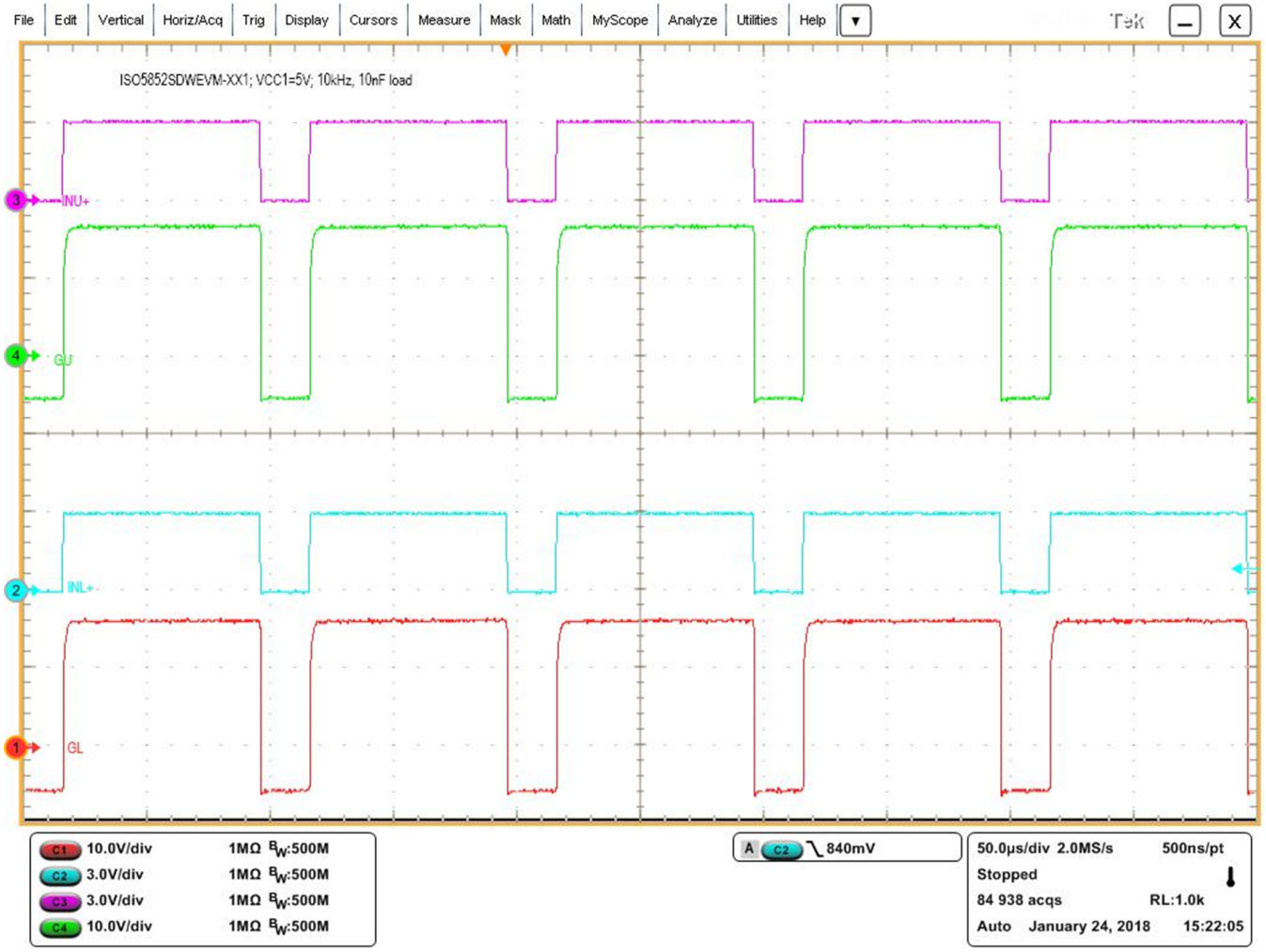


Figure 19. Waveforms with Overlapping Enabled

- INU (pink) is high side input: 3.0V/div
- OU (green) is high side output: 10V/div
- INL (blue) is low side input: 3.0V/div
- OL (red) is low side output: 10V/div
- Time scale is 50µs/div

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Current capability during turn ON is illustrated in Figure 20 by rise time while charging 10 nF load capacitors

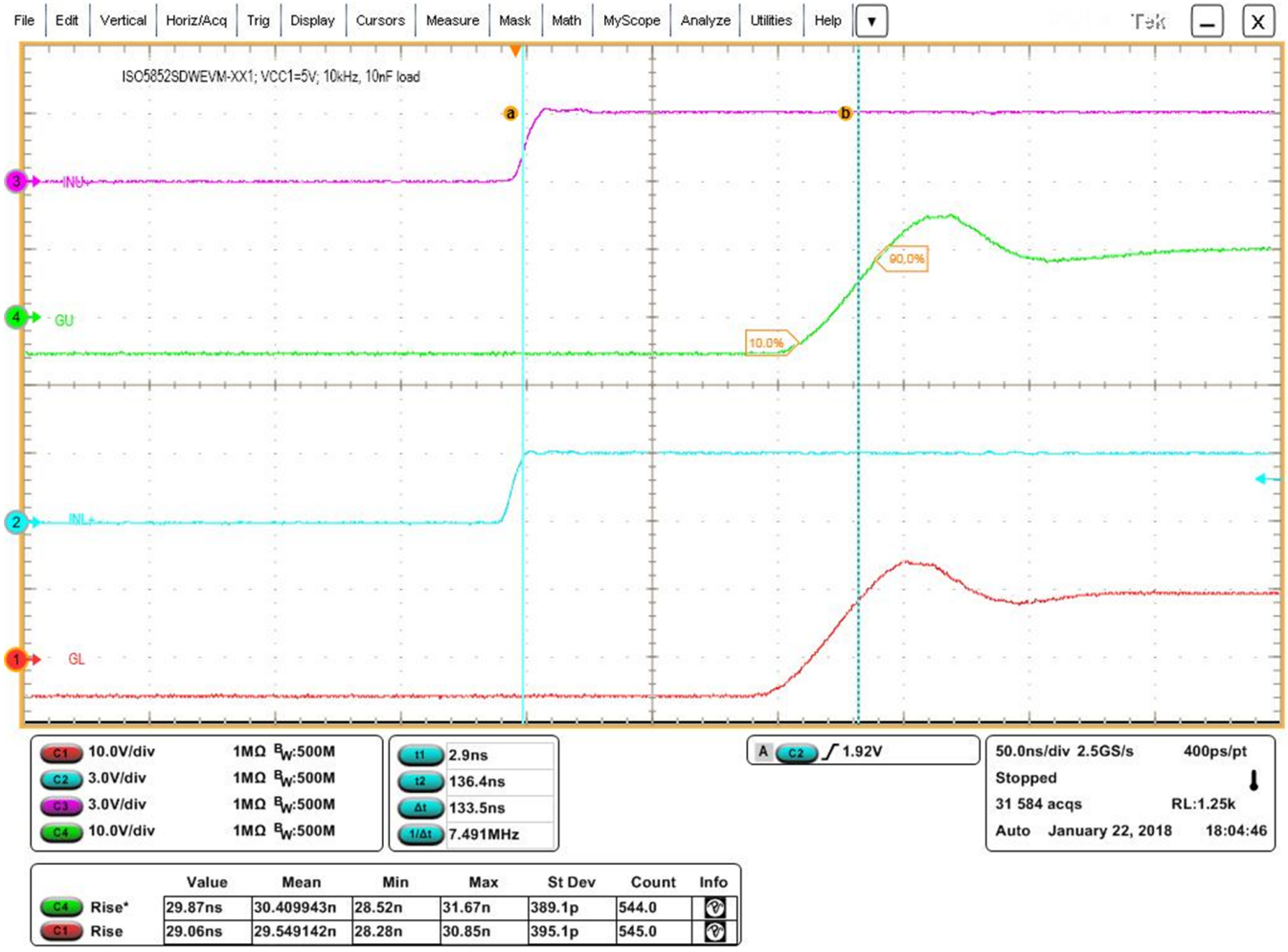


Figure 20. Rise Time and Propagation Delay Waveforms with 10 nF Load

- INU (pink) is high side input: 3.0V/div
- OU (green) is high side output: 10V/div
- INL (blue) is low side input: 3.0V/div
- OL (red) is low side output: 10V/div
- Time scale is 50ns/div
- Rise time is about 30 ns
- Propagation delay is 133.5 ns

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Current capability during turn OFF with 10 nF load capacitors is illustrated in Figure 21.



Figure 21. Fall Time and Propagation Delay Waveforms with 10 nF Load

- INU (pink) is high side input: 3.0V/div
- OU (green) is high side output: 10V/div
- INL (blue) is low side input: 3.0V/div
- OL (red) is low side output: 10V/div
- Time scale is 50ns/div
- Fall time is about 34 ns
- Propagation delay is 98.5 ns

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4.2 Bill of Materials

Table 7. Bill of Materials

DESIGNATOR	QTY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
C1, C21	2	220pF	GRM188R71H221KA01D	MuRata	CAP, CERM, 220 pF, 50 V, +/- 10%, X7R, 0603	0603
C2, C9, C22, C29	4	10uF	C3216X7R1V106M160AC	TDK	CAP, CERM, 10 uF, 35 V, +/- 20%, X7R, 1206_190	1206_190
C3, C5, C10, C11, C18, C23, C25, C30, C31, C38, C45, C53	12	0.1uF	C1005X7R1H104K050BB	TDK	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	0402
C4, C24	2	10uF	GRM21BR6YA106KE43L	MuRata	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	0805
C6, C19, C27, C39	4	10uF	C1608X5R1E106M080AC	TDK	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	0603
C7, C26, C43, C51	4	0.1uF	CGA5L2X7R2A104K160AA	TDK	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206
C8, C20, C28, C40, C48	5	0.1uF	GRM155R61A104KA01D	MuRata	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402
C12, C13, C32, C33	4	100pF	CC0402JRNPO9BN101	Yageo America	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402
C14, C17, C34, C37, C44, C52	6	10uF	C2012X5R1E106K125AB	TDK	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	0805
C15, C35	2	0.015uF	CGA3E2X7R2A153K080AA	TDK	CAP, CERM, 0.015 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603
C16, C36	2	0.01uF	GCM188R71H103KA37D	MuRata	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603
C41, C49	2	0.1uF	12061C104JAT2A	AVX	CAP, CERM, 0.1 uF, 100 V, +/- 5%, X7R, 1206	1206
C42	1	0.01uF	C0402C103J5RACTU	Kemet	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0402	0402
C46, C47, C57, C58	4	10pF	04025U100CAT2A	AVX	CAP, CERM, 10 pF, 50 V,+/- 2.5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402
C50	1	0.01uF	C0603H103J3GACTU	Kemet	CAP, CERM, 0.01 uF, 25 V, +/- 5%, C0G/NP0, 0603	0603
C54, C56	2	2.2uF	C1206C225K4RACTU	Kemet	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 1206	1206
C55	1	1uF	UMK107AB7105KA-T	Taiyo Yuden	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603
D1, D6, D8, D10, D14, D16, D18, D20	8	40V	B0540WS-7	Diodes Inc.	Diode, Schottky, 40 V, 0.5 A, SOD-323	SOD-323
D2, D5, D11, D15	4	1200V	STTH112A	STMicroelectronics	Diode, Ultrafast, 1200 V, 1 A, SMA	SMA
D3, D12	2	12V	MMSZ5242BS-7-F	Diodes Inc.	Diode, Zener, 12 V, 200 mW, SOD-323	SOD-323
D4, D13	2	30V	BAT54WS-7-F	Diodes Inc.	Diode, Schottky, 30 V, 0.2 A, SOD-323	SOD-323
D7, D17	2	40V	B240A-13-F	Diodes Inc.	Diode, Schottky, 40 V, 2 A, SMA	SMA
D9, D19	2	22V	SMAJ22CA	Littelfuse	Diode, TVS, Bi, 22 V, SMA	SMA
FID1, FID2, FID3	3		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
J1	1		71918-220LF	FCI	Header(shrouded), 2.54mm, 10x2, Gold with Tin tail, TH	Header(shrouded), 2.54mm, 10x2, TH
J2	1		OSTVN02A150	On-Shore Technology	Terminal Block, 2.54mm, 2x1, Brass, TH	Terminal Block, 2.54mm, 2-pole, Brass, TH
L1	1		ACM4520-421-2P-T000	TDK	Coupled inductor, 2.8 A, 0.055 ohm, SMD	4.7x4.5mm
Q1, Q3	2	60 V	ZXTN2010ZTA	Diodes Inc.	Transistor, NPN, 60 V, 5 A, AEC-Q101, SOT-89	SOT-89
Q2, Q4	2	60 V	ZXTP2012ZTA	Diodes Inc.	Transistor, PNP, 60 V, 4.3 A, AEC-Q101, SOT-89	SOT-89
R1, R17	2	1.00k	ERJ-P06F1001V	Panasonic	RES, 1.00 k, 1%, 0.25 W, 0805	0805

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Table 7. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
R2, R18	2	10.0k	CRCW080510K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.125 W, 0805	0805
R3, R19	2	1.00Meg	CRCW08051M00FKEA	Vishay-Dale	RES, 1.00 M, 1%, 0.125 W, 0805	0805
R4, R5, R20, R21	4	100	CRCW0402100RFKED	Vishay-Dale	RES, 100, 1%, 0.063 W, 0402	0402
R6, R22, R61	3	10	CRCW080510R0JNEA	Vishay-Dale	RES, 10, 5%, 0.125 W, 0805	0805
R7, R9, R11, R23, R25, R27	6	12	CRCW080512R0JNEA	Vishay-Dale	RES, 12, 5%, 0.125 W, 0805	0805
R8, R10, R12, R14, R15, R16, R24, R26, R28, R30, R31, R34	12	1.20	CRCW12061R20FKEA	Vishay-Dale	RES, 1.20, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206
R13, R29, R63, R64	4	10.0k	RC0603FR-0710KL	Yageo America	RES, 10.0 k, 1%, 0.1 W, 0603	0603
R32, R67	2	10.0k	RMCF0402FT10K0	Stackpole Electronics Inc	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R33, R48, R52	3	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
R35, R65	2	0	MCR18EZHJ000	Rohm	RES, 0, 5%, 0.25 W, 1206	1206
R36, R37, R38, R39, R40, R41, R42, R43, R44	9	1.00Meg	CRCW12061M00FKEA	Vishay-Dale	RES, 1.00 M, 1%, 0.25 W, 1206	1206
R45	1	49.9k	CRCW0402249K9FKED	Vishay-Dale	RES, 49.9 k, 1%, 0.063 W, 0402	0402
R46	1	1.21k	CRCW04021K21FKED	Vishay-Dale	RES, 1.21 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R47	1	523k	CRCW0402523KFKED	Vishay-Dale	RES, 523 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R49, R50, R51, R54, R58, R59, R62, R66	8	10.0	CRCW040210R0FKED	Vishay-Dale	RES, 10.0, 1%, 0.063 W, 0402	0402
R53	1	10.5k	CRCW040210K5FKED	Vishay-Dale	RES, 10.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R55, R60	2	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R56	1	40.2k	CRCW040240K2FKED	Vishay-Dale	RES, 40.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
R57	1	100k	RMCF0402FT100K	Stackpole Electronics Inc	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
T1, T3	2	50uH	750342879	Wurth Elektronik	Transformer, 50 uH, SMT	9.14x8mm
T2, T4	2	340uH	750313734	Wurth Elektronik	Transformer, 340 uH, TH	8x9.14mm
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14	14		0508-0-00-15-00-00-03-0	Mill-Max	PCB Pin, 20mil Dia, Gold, TH	PCB Pin, 20mil Dia, TH
U1, U4	2		ISO5852SDWR	Texas Instruments	5.7 kVrms Split O/P, Reinforced Isolated IGBT Gate Driver, DW0016B (SOIC-16)	DW0016B
U2, U3, U5, U6	4		SN6505BDBVR	Texas Instruments	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)	DBV0006A
U7, U10	2		SN74AHC1G08QDBVRQ1	Texas Instruments	Automotive Catalog Single 2-Input Positive-AND Gate, DBV0005A, LARGE T&R	DBV0005A
U8, U11	2		AMC1301DWVR	Texas Instruments	Precision +/-250-mV Input, 3-us Delay, Reinforced Isolated Amplifier, DWV0008A (SOIC-8)	DWV0008A
U9	1		TPS3700QDDCRQ1	Texas Instruments	Automotive, High-Voltage (18V) Window Comparator with Over- and Undervoltage Detection, DDC0006A (SOT-23-T-6)	DDC0006A
U12	1		TPS70950DBVR	Texas Instruments	150-mA, 30-V, Ultra-Low IQ, Wide Input Low-Dropout Regulator with Reverse Current Protection, DBV0005A (SOT-23-5)	DBV0005A

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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