# 12-Bit, 500MSPS ADC

## ISLA212P50

The ISLA212P50 is a 12-bit, 500MSPS analog-to-digital converter designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process. The ISLA212P50 is part of a pin-compatible portfolio of 12 to 16-bit A/Ds with maximum sample rates ranging from 130MSPS to 500MSPS.

The device utilizes two time-interleaved 250MSPS unit ADCs to achieve the ultimate sample rate of 500MSPS. A single 500MHz conversion clock is presented to the converter, and all interleave clocking is managed internally. The proprietary Intersil Interleave Engine (I2E) performs automatic correction of offset, gain, and sample time mismatches between the unit ADCs to optimize performance.

A serial peripheral interface (SPI) port allows for extensive configurability of the A/D. The SPI also controls the interleave correction circuitry, allowing the system to issue offline and continuous calibration commands as well as configure many dynamic parameters.

Digital output data is presented in selectable LVDS or CMOS formats. The ISLA212P50 is available in a 72 Ld QFN package with an exposed paddle. Operating from a 1.8V supply, performance is specified over the full industrial temperature range (-40°C to +85°C).

## Key Specifications

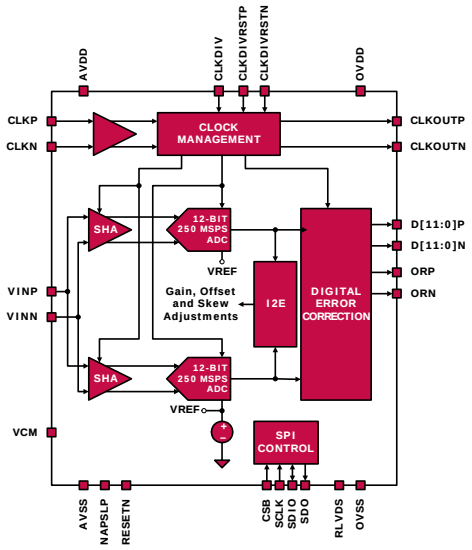
- SNR @ 500MSPS
  - = 70.3dBFS $f_{IN}$ = 30MHz
  - = 68.7dBFS $f_{IN}$ = 363MHz
- SFDR @ 500MSPS
  - = 84dBc $f_{IN}$ = 30MHz
  - = 76dBc $f_{IN}$ = 363MHz
- Total Power Consumption = 823mW @ 500MSPS

## Features

- Automatic Fine Interleave Correction Calibration
- Single Supply 1.8V Operation
- Clock Duty Cycle Stabilizer
- 75fs Clock Jitter
- 700MHz Bandwidth
- Programmable Built-in Test Patterns
- Multi-ADC Support
  - SPI Programmable Fine Gain and Offset Control
  - Support for Multiple ADC Synchronization
  - Optimized Output Timing
- Nap and Sleep Modes
  - 200µs Sleep Wake-up Time
- Data Output Clock
- DDR LVDS-Compatible or LVCMOS Outputs
- User-accessible Digital Temperature Monitor

## Applications

- Radar Array Processing
- Software Defined Radios
- Broadband Communications
- High-Performance Data Acquisition
- Communications Test Equipment




## Pin-Compatible Family

| MODEL | RESOLUTION | SPEED (MSPS) |
|---|---|---|
| ISLA216P25 | 16 | 250 |
| ISLA216P20 | 16 | 200 |
| ISLA216P13 | 16 | 130 |
| ISLA214P50 | 14 | 500 |
| ISLA214P25 | 14 | 250 |
| ISLA214P20 | 14 | 200 |
| ISLA214P13 | 14 | 130 |
| ISLA212P50 | 12 | 500 |
| ISLA212P25 | 12 | 250 |
| ISLA212P20 | 12 | 200 |
| ISLA212P13 | 12 | 130 |



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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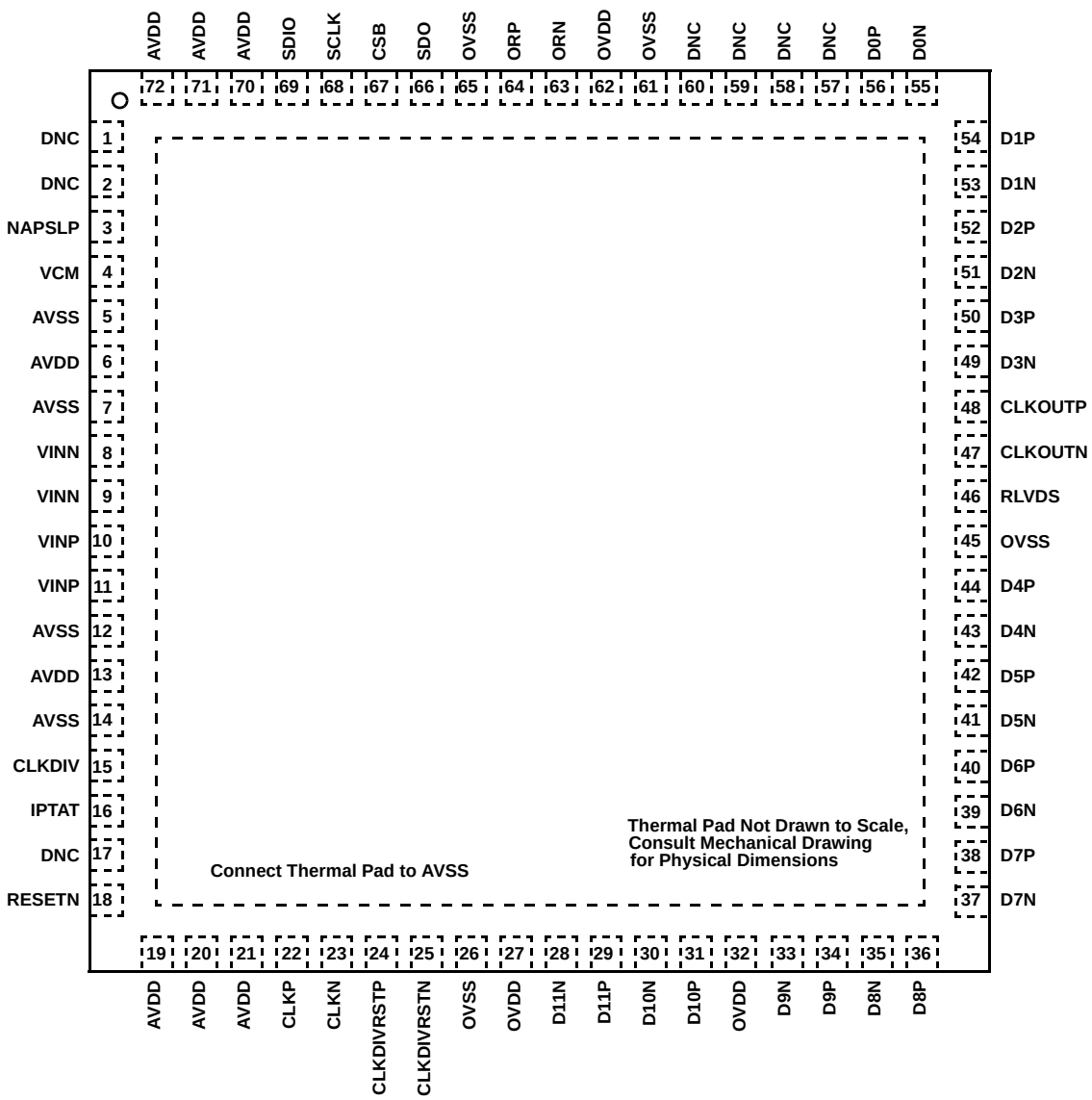
# Pin Configuration - LVDS MODE

ISLA212P50
(72 LD QFN)
TOP VIEW




# Pin Descriptions - 72 Ld QFN, LVDS Mode

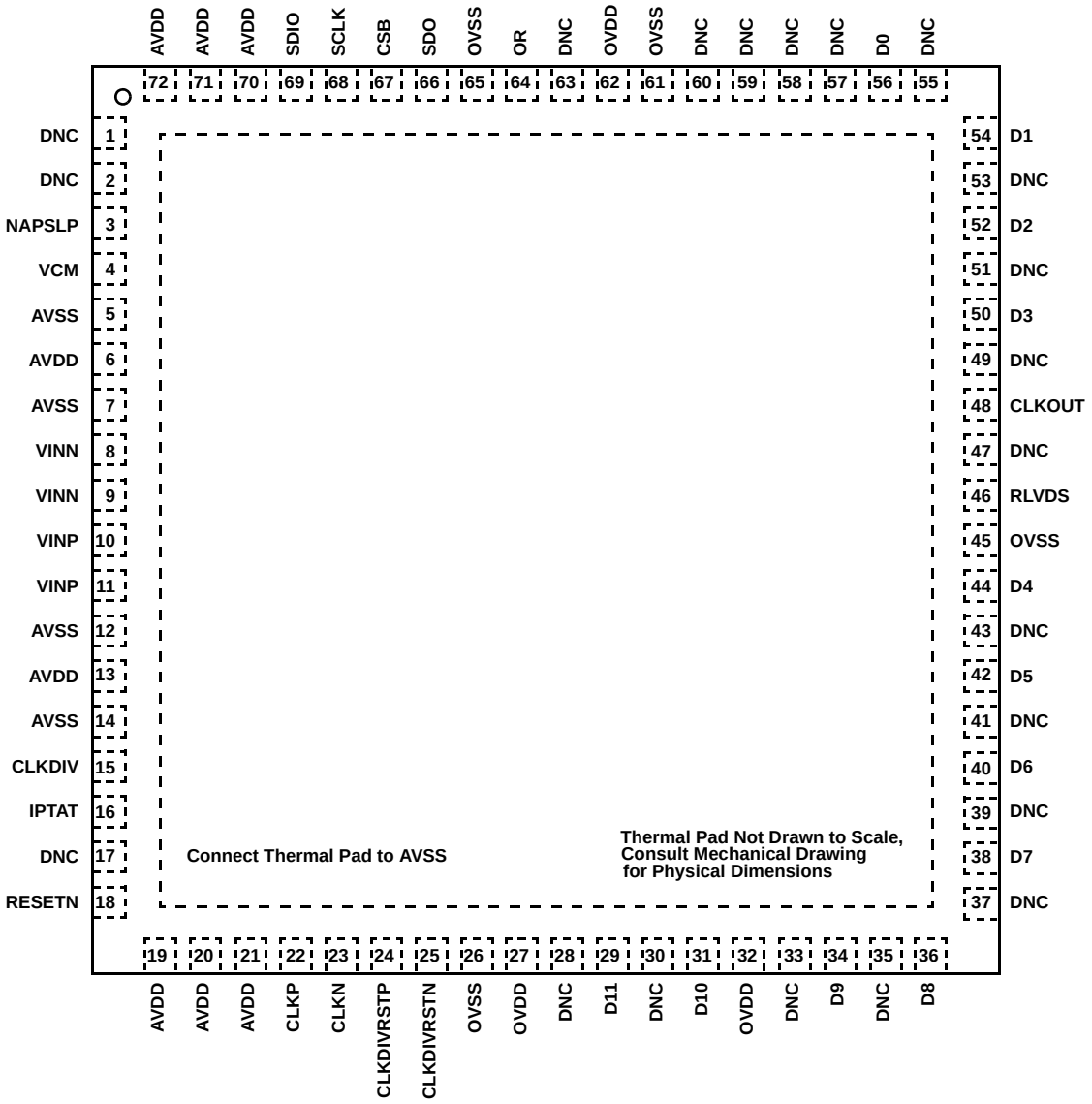
| PIN NUMBER | LVDS PIN NAME | LVDS PIN FUNCTION |
|---|---|---|
| 1, 2, 17, 57, 58, 59, 60 | DNC | Do Not Connect |
| 6, 13, 19, 20, 21, 70, 71, 72 | AVDD | 1.8V Analog Supply |
| 5, 7, 12, 14 | AVSS | Analog Ground |
| 27, 32, 62 | OVDD | 1.8V Output Supply |
| 26, 45, 61, 65 | OVSS | Output Ground |
| 3 | NAPSLP | Tri-Level Power Control (Nap, Sleep modes) |
| 4 | VCM | Common Mode Output |
| 8, 9 | VINN | Analog Input Negative |

## Pin Descriptions - 72 Ld QFN, LVDS Mode (Continued)

| PIN NUMBER | LVDS PIN NAME | LVDS PIN FUNCTION |
|---|---|---|
| 10, 11 | VINP | Analog Input Positive |
| 15 | CLKDIV | Tri-Level Clock Divider Control |
| 16 | IPTAT | Temperature Monitor (Output current proportional to absolute temperature) |
| 18 | RESETN | Power On Reset (Active Low) |
| 22, 23 | CLKP, CLKN | Clock Input True, Complement |
| 24, 25 | CLKDIVRSTP, CLKDIVRSTN | Synchronous Clock Divider Reset True, Complement |
| 28, 29 | D11N, D11P | LVDS Bit 11 (MSB) Output Complement, True |
| 30, 31 | D10N, D10P | LVDS Bit 10 Output Complement, True |
| 33, 34 | D9N, D9P | LVDS Bit 9 Output Complement, True |
| 35, 36 | D8N, D8P | LVDS Bit 8 Output Complement, True |
| 37, 38 | D7N, D7P | LVDS Bit 7 Output Complement, True |
| 39, 40 | D6N, D6P | LVDS Bit 6 Output Complement, True |
| 41, 42 | D5N, D5P | LVDS Bit 5 Output Complement, True |
| 43, 44 | D4N, D4P | LVDS Bit 4 Output Complement, True |
| 46 | RLVDS | LVDS Bias Resistor (connect to OVSS with 1% 10kΩ) |
| 47, 48 | CLKOUTN, CLKOUTP | LVDS Clock Output Complement, True |
| 49, 50 | D3N, D3P | LVDS Bit 3 Output Complement, True |
| 51, 52 | D2N, D2P | LVDS Bit 2 Output Complement, True |
| 53, 54 | D1N, D1P | LVDS Bit 1 Output Complement, True |
| 55, 56 | D0N, D0P | LVDS Bit 0 (LSB) Output Complement, True |
| 63, 64 | ORN, ORP | LVDS Over Range Complement, True |
| 66 | SDO | SPI Serial Data Output |
| 67 | CSB | SPI Chip Select (active low) |
| 68 | SCLK | SPI Clock |
| 69 | SDIO | SPI Serial Data Input/Output |
| Exposed Paddle | AVSS | Analog Ground |

# Pin Configuration - CMOS MODE

ISLA212P50
(72 LD QFN)
TOP VIEW




# Pin Descriptions - 72 Ld QFN, CMOS Mode

| PIN NUMBER | CMOS PIN NAME | CMOS PIN FUNCTION |
|---|---|---|
| 1, 2, 17, 28, 30, 33, 35, 37, 39, 41, 43, 47, 49, 51, 53, 55, 57, 58, 59, 60, 63 | DNC | Do Not Connect |
| 6, 13, 19, 20, 21, 70, 71, 72 | AVDD | 1.8V Analog Supply |
| 5, 7, 12, 14 | AVSS | Analog Ground |
| 27, 32, 62 | OVDD | 1.8V Output Supply |
| 26, 45, 61, 65 | OVSS | Output Ground |
| 3 | NAPSLP | Tri-Level Power Control (Nap, Sleep modes) |
| 4 | VCM | Common Mode Output |

## Pin Descriptions - 72 Ld QFN, CMOS Mode (Continued)

| PIN NUMBER | CMOS PIN NAME | CMOS PIN FUNCTION |
|---|---|---|
| 8, 9 | VINN | Analog Input Negative |
| 10, 11 | VINP | Analog Input Positive |
| 15 | CLKDIV | Tri-Level Clock Divider Control |
| 16 | IPTAT | Temperature Monitor (Output current proportional to absolute temperature) |
| 18 | RESETN | Power On Reset (Active Low) |
| 22, 23 | CLKP, CLKN | Clock Input True, Complement |
| 24, 25 | CLKDIVRSTP, CLKDIVRSTN | Synchronous Clock Divider Reset True, Complement |
| 29 | D11 | CMOS Bit 11 (MSB) Output |
| 31 | D10 | CMOS Bit 10 Output |
| 34 | D9 | CMOS Bit 9 Output |
| 36 | D8 | CMOS Bit 8 Output |
| 38 | D7 | CMOS Bit 7 Output |
| 40 | D6 | CMOS Bit 6 Output |
| 42 | D5 | CMOS Bit 5 Output |
| 44 | D4 | CMOS Bit 4 Output |
| 46 | RLVDS | LVDS Bias Resistor (connect to OVSS with 1% 10kΩ) |
| 48 | CLKOUT | CMOS Clock Output |
| 50 | D3 | CMOS Bit 3 Output |
| 52 | D2 | CMOS Bit 2 Output |
| 54 | D1 | CMOS Bit 1 Output |
| 56 | D0 | CMOS Bit 0 (LSB) Output |
| 64 | OR | CMOS Over Range |
| 66 | SDO | SPI Serial Data Output |
| 67 | CSB | SPI Chip Select (active low) |
| 68 | SCLK | SPI Clock |
| 69 | SDIO | SPI Serial Data Input/Output |
| Exposed Paddle | AVSS | Analog Ground |

# Ordering Information

| PART NUMBER (Notes 1, 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISLA212P50IRZ | ISLA212P50 IRZ | -40 to +85 | 72 Ld QFN | L72.10x10E |
| ISLA214P50IR72EV1Z | 14-bit 500MSPS ADC Evaluation Board (This 14-bit ADC evaluation board can be configured for 12-bit testing.) | | | |

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate–e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA212P50. For more information on MSL please see Tech Brief TB363.

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## Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
Latchup (Tested per JESD-78C; Class 2, Level A . . . . . 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 72 Ld QFN (Notes 3, 4) . . . . . | 23 | 0.9 |

Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Temperature . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

3. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, $T_A$ = -40°C to +85°C (typical specifications at +25°C), $A_{IN}$ = -1dBFS, $f_{SAMPLE}$ = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | SYMBOL | CONDITIONS | ISLA212P50 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN (Note 5) | TYP | MAX (Note 5) | |
| **DC SPECIFICATIONS (Note 6)** | | | | | | |
| **Analog Input** | | | | | | |
| Full-Scale Analog Input Range | $V_{FS}$ | Differential | **1.95** | 2.0 | **2.15** | $V_{P-P}$ |
| Input Resistance | $R_{IN}$ | Differential | | 300 | | Ω |
| Input Capacitance | $C_{IN}$ | Differential | | 9 | | pF |
| Full Scale Range Temp. Drift | $A_{VTC}$ | Full Temp | | 160 | | ppm/°C |
| Input Offset Voltage | $V_{OS}$ | | **-5.0** | -1.3 | **5.0** | mV |
| Common-Mode Output Voltage | $V_{CM}$ | | | 0.94 | | V |
| Common-Mode Input Current (per pin) | $I_{CM}$ | | | 2.6 | | µA/MSPS |
| **Clock Inputs** | | | | | | |
| Inputs Common Mode Voltage | | | | 0.9 | | V |
| CLKP, CLKN Input Swing | | | | 1.8 | | V |
| **Power Requirements** | | | | | | |
| 1.8V Analog Supply Voltage | AVDD | | **1.7** | 1.8 | **1.9** | V |
| 1.8V Digital Supply Voltage | OVDD | | **1.7** | 1.8 | **1.9** | V |
| 1.8V Analog Supply Current | $I_{AVDD}$ | | | 372 | **391** | mA |
| 1.8V Digital Supply Current (Note 6) | $I_{OVDD}$ | 3mA LVDS, (I2E powered down, Fs/4 Filter powered down) | | 85 | **95** | mA |
| Power Supply Rejection Ratio | PSRR | 30MHz, 45mVP-P signal on AVDD | | 60 | | dB |

**Electrical Specifications** All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, $T_A$ = -40°C to +85°C (typical specifications at +25°C), $A_{IN}$ = -1dBFS, $f_{SAMPLE}$ = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | ISLA212P50 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN (Note 5) | TYP | MAX (Note 5) | |
| **Total Power Dissipation** | | | | | | |
| Normal Mode | $P_D$ | 2mA LVDS, (I2E powered down, Fs/4 Filter powered down) | | 809 | | mW |
| | | 3mA LVDS, (I2E powered down, Fs/4 Filter powered down) | | 823 | **875** | mW |
| | | 3mA LVDS, (I2E on, Fs/4 Filter off) | | 858 | | mW |
| | | 3mA LVDS, (I2E on, Fs/4 Filter on) | | 892 | **943** | mW |
| Nap Mode | $P_D$ | | | 89 | **104** | mW |
| Sleep Mode | $P_D$ | CSB at logic high | | 7 | **19** | mW |
| Nap/Sleep Mode Wakeup Time | | Sample Clock Running | | 200 | | µs |
| **AC SPECIFICATIONS** | | | | | | |
| Differential Nonlinearity | DNL | $f_{IN}$ = 105MHz No Missing Codes | **-0.7** | ±0.16 | **0.7** | LSB |
| Integral Nonlinearity | INL | fin = 105MHz | **-1.8** | ±0.7 | **1.8** | LSB |
| Minimum Conversion Rate (Note 7) | $f_S$ MIN | | | | **80** | MSPS |
| Maximum Conversion Rate | $f_S$ MAX | | **500** | | | MSPS |
| Signal-to-Noise Ratio (Note 8) | SNR | $f_{IN}$ = 30MHz | | 70.3 | | dBFS |
| | | $f_{IN}$ = 105MHz | 68.0 | 70.3 | | dBFS |
| | | $f_{IN}$ = 190MHz | | 69.8 | | dBFS |
| | | $f_{IN}$ = 363MHz | | 68.7 | | dBFS |
| | | $f_{IN}$ = 461MHz | | 68.1 | | dBFS |
| | | $f_{IN}$ = 605MHz | | 66.9 | | dBFS |
| Signal-to-Noise and Distortion (Note 8) | SINAD | $f_{IN}$ = 30MHz | | 69.6 | | dBFS |
| | | $f_{IN}$ = 105MHz | 67.5 | 69.6 | | dBFS |
| | | $f_{IN}$ = 190MHz | | 68.8 | | dBFS |
| | | $f_{IN}$ = 363MHz | | 68.1 | | dBFS |
| | | $f_{IN}$ = 461MHz | | 66.1 | | dBFS |
| | | $f_{IN}$ = 605MHz | | 62.4 | | dBFS |
| Effective Number of Bits (Note 8) | ENOB | $f_{IN}$ = 30MHz | | 11.27 | | Bits |
| | | $f_{IN}$ = 105MHz | 10.92 | 11.27 | | Bits |
| | | $f_{IN}$ = 190MHz | | 11.14 | | Bits |
| | | $f_{IN}$ = 363MHz | | 11.02 | | Bits |
| | | $f_{IN}$ = 461MHz | | 10.69 | | Bits |
| | | $f_{IN}$ = 605MHz | | 10.07 | | Bits |

## Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, $T_A$ = -40°C to +85°C (typical specifications at +25°C), $A_{IN}$ = -1dBFS, $f_{SAMPLE}$ = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | ISLA212P50 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN (Note 5) | TYP | MAX (Note 5) | |
| Spurious-Free Dynamic Range (Note 8) | SFDR | $f_{IN}$ = 30MHz | | 84 | | dBc |
| | | $f_{IN}$ = 105MHz | 72 | 82 | | dBc |
| | | $f_{IN}$ = 190MHz | | 78 | | dBc |
| | | $f_{IN}$ = 363MHz | | 76 | | dBc |
| | | $f_{IN}$ = 461MHz | | 66 | | dBc |
| | | $f_{IN}$ = 605MHz | | 61 | | dBc |
| Spurious-Free Dynamic Range Excluding H2,H3 (Note 8) | SFDRX23 | $f_{IN}$ = 30MHz | | 88 | | dBc |
| | | $f_{IN}$ = 105MHz | | 89 | | dBc |
| | | $f_{IN}$ = 190MHz | | 88 | | dBc |
| | | $f_{IN}$ = 363MHz | | 83 | | dBc |
| | | $f_{IN}$ = 461MHz | | 84 | | dBc |
| | | $f_{IN}$ = 605MHz | | 77 | | dBc |
| Intermodulation Distortion | IMD | $f_{IN}$ = 70MHz | | 88 | | dBFS |
| | | $f_{IN}$ = 170MHz | | 96 | | dBFS |
| Word Error Rate | WER | | | $10^{-12}$ | | |
| Full Power Bandwidth | FPBW | | | 700 | | MHz |

NOTES:

5. Compliance to datasheet limits is assured by one of the following methods: production test, characterization and/or design.
6. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. $I_{OVDD}$ specifications apply for 10pF load on each digital output.
7. The DLL Range setting must be changed for low-speed operation.
8. Minimum specification guaranteed when calibrated at +85°C.

## Digital Specifications

**Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| **INPUTS** (Note 9) | | | | | | |
| Input Current High (RESETN) | $I_{IH}$ | $V_{IN}$ = 1.8V | **0** | 1 | **10** | µA |
| Input Current Low (RESETN) | $I_{IL}$ | $V_{IN}$ = 0V | **-25** | -12 | **-8** | µA |
| Input Current High (SDIO) | $I_{IH}$ | $V_{IN}$ = 1.8V | | 4 | **12** | µA |
| Input Current Low (SDIO) | $I_{IL}$ | $V_{IN}$ = 0V | **-600** | -415 | **-300** | µA |
| Input Current High (CSB) | $I_{IH}$ | $V_{IN}$ = 1.8V | **40** | 58 | **75** | µA |
| Input Current Low (CSB) | $I_{IL}$ | $V_{IN}$ = 0V | | 5 | **10** | µA |
| Input Current High (CLKDIV) | $I_{IH}$ | | **16** | 25 | **34** | µA |
| Input Current Low (CLKDIV) | $I_{IL}$ | | **-34** | -25 | **-16** | µA |
| Input Voltage High (SDIO, RESETN) | $V_{IH}$ | | **1.17** | | | V |
| Input Voltage Low (SDIO, RESETN) | $V_{IL}$ | | | | **.63** | V |
| Input Capacitance | $C_{DI}$ | | | 4 | | pF |
| **LVDS INPUTS (CLKDIVRSTP, CLKDIVRSTN)** | | | | | | |
| Input Common Mode Range | $V_{ICM}$ | | **825** | | **1575** | mV |
| Input Differential Swing (peak to peak, single-ended) | $V_{ID}$ | | **250** | | **450** | mV |

## Digital Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| CLKDIVRSTP Input Pull-down Resistance | $R_{Ipd}$ | | | 100 | | kΩ |
| CLKDIVRSTN Input Pull-up Resistance | $R_{Ipu}$ | | | 100 | | kΩ |
| **LVDS OUTPUTS** | | | | | | |
| Differential Output Voltage (Note 10) | $V_T$ | 3mA Mode | | 612 | | $mV_{P-P}$ |
| Output Offset Voltage | $V_{OS}$ | 3mA Mode | **1120** | 1150 | **1200** | mV |
| Output Rise Time | $t_R$ | | | 240 | | ps |
| Output Fall Time | $t_F$ | | | 240 | | ps |
| **CMOS OUTPUTS** | | | | | | |
| Voltage Output High | $V_{OH}$ | $I_{OH}$ = -500µA | **OVDD - 0.3** | OVDD - 0.1 | | V |
| Voltage Output Low | $V_{OL}$ | $I_{OL}$ = 1mA | | 0.1 | **0.3** | V |
| Output Rise Time | $t_R$ | | | 1.8 | | ns |
| Output Fall Time | $t_F$ | | | 1.4 | | ns |

NOTES:

9. The Tri-Level Inputs internal switching thresholds are approximately. 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.

10. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.

## I2E Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C.

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| Offset Mismatch-induced Spurious Power | | No I2E Calibration performed | | -65 | | dBFS |
| | | Active Run state enabled | | -70 | | dBFS |
| I2E Settling Times | I2Epost_t | Calibration settling time for Active Run state | | | **1000** | ms |
| Minimum Duration of Valid Analog Input | $t_{TE}$ | Allow one I2E iteration of Offset, Gain and Phase correction | | | **100** | µs |
| Largest Interleave Spur | | $f_{IN}$ = 10MHz to 240MHz, Active Run State enabled, in Track Mode | | -99 | | dBc |
| | | $f_{IN}$ = 10MHz to 240MHz, Active Run State enabled and previously settled, in Hold Mode | **-75** | -80 | | dBc |
| | | $f_{IN}$ = 260MHz to 490MHz, Active Run State enabled, in Track Mode | | -99 | | dBc |
| | | $f_{IN}$ = 260MHz to 490MHz, Active Run State enabled and previously settled, in Hold Mode | | -75 | | dBc |
| Total Interleave Spurious Power | | Active Run State enabled, in Track Mode, $f_{IN}$ is a broadband signal in the 1st Nyquist zone | | -85 | | dBc |
| | | Active Run State enabled, in Track Mode, $f_{IN}$ is a broadband signal in the 2nd Nyquist zone | | -75 | | dBc |
| Sample Time Mismatch Between Unit ADCs | | Active Run State enabled, in Track Mode | | 25 | | fs |
| Gain Mismatch Between Unit ADCs | | | | 0.01 | | %FS |
| Offset Mismatch Between Unit ADCs | | | | 1 | | mV |

# Timing Diagrams

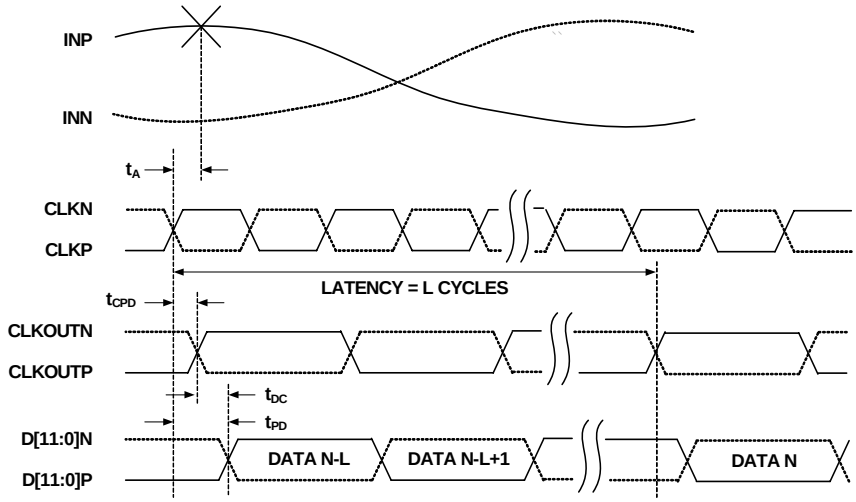



FIGURE 1A. LVDS

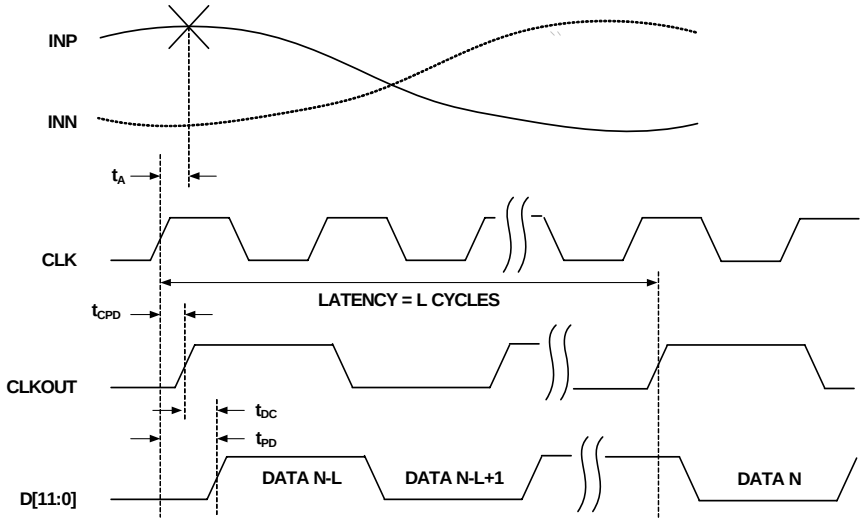



FIGURE 1B. CMOS

FIGURE 1. TIMING DIAGRAMS

## Switching Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C.

| PARAMETER | CONDITION | SYMBOL | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| **ADC OUTPUT** | | | | | | |
| Aperture Delay | | $t_A$ | | 114 | | ps |
| RMS Aperture Jitter | | $j_A$ | | 75 | | fs |
| Input Clock to Output Clock Propagation Delay | AVDD, OVDD = 1.7V to 1.9V, $T_A$ = -40°C to +85°C | $t_{CPD}$ | **1.65** | 2.4 | **3** | ns |
| | AVDD, OVDD = 1.8V, $T_A$ = +25°C | $t_{CPD}$ | 1.9 | 2.3 | 2.75 | ns |
| Relative Input Clock to Output Clock Propagation Delay (Note 13) | AVDD, OVDD = 1.7V to 1.9V, $T_A$ = -40°C to +85°C | $dt_{CPD}$ | **-450** | | **450** | ps |
| Input Clock to Data Propagation Delay | | $t_{PD}$ | **1.65** | 2.4 | **3.5** | ns |
| Output Clock to Data Propagation Delay, LVDS Mode | Rising/Falling Edge | $t_{DC}$ | **-0.1** | 0.16 | **0.5** | ns |
| Output Clock to Data Propagation Delay, CMOS Mode | Rising/Falling Edge | $t_{DC}$ | **-0.1** | 0.2 | **0.65** | ns |
| Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP) | | $t_{RSTS}$ | **0.4** | 0.06 | | ns |
| Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP) | | $t_{RSTH}$ | | 0.02 | **0.35** | ns |
| Synchronous Clock Divider Reset Recovery Time | DLL recovery time after Synchronous Reset | $t_{RSTRT}$ | | 52 | | µs |
| Latency (Pipeline Delay) | | L | | 20 | | cycles |
| Overvoltage Recovery | | $t_{OVR}$ | | 2 | | cycles |
| **SPI INTERFACE (Notes 11, 12)** | | | | | | |
| SCLK Period | Write Operation | $t_{CLK}$ | **32** | | | cycles |
| | Read Operation | $t_{CLK}$ | **32** | | | cycles |
| CSB↓ to SCLK↑ Setup Time | Read or Write | $t_S$ | **56** | | | cycles |
| CSB↑ after SCLK↑ Hold Time | Write | $t_H$ | **10** | | | cycles |
| CSB↑ after SCLK↓ Hold Time | Read | $t_{HR}$ | **32** | | | cycles |
| Data Valid to SCLK↑ Setup Time | Write | $t_{DS}$ | **12** | | | cycles |
| Data Valid after SCLK↑ Hold Time | Read or Write | $t_{DH}$ | | | **8** | cycles |
| Data Valid after SCLK↓ Time | Read | $t_{DVR}$ | | | **10** | cycles |

NOTES:

11. SPI Interface timing is directly proportional to the ADC sample period ($t_S$). Values above reflect multiples of a 2ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
12. The SPI may operate asynchronously with respect to the ADC sample clock.
13. The relative propagation delay is the difference in propagation time between any two devices that are matched in temperature and voltage, and is specified over the full operating temperature and voltage range.

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = 500MSPS.

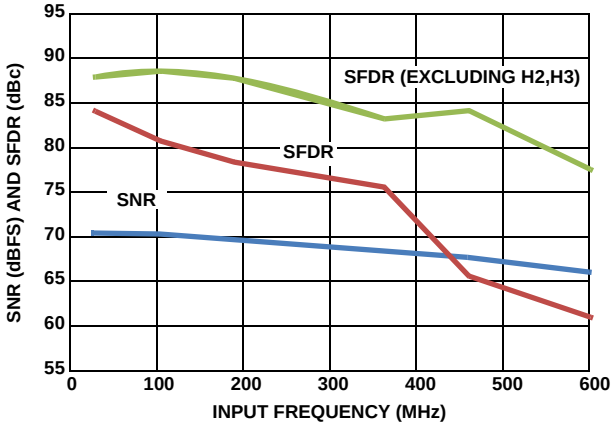



FIGURE 2. SNR AND SFDR vs $f_{IN}$

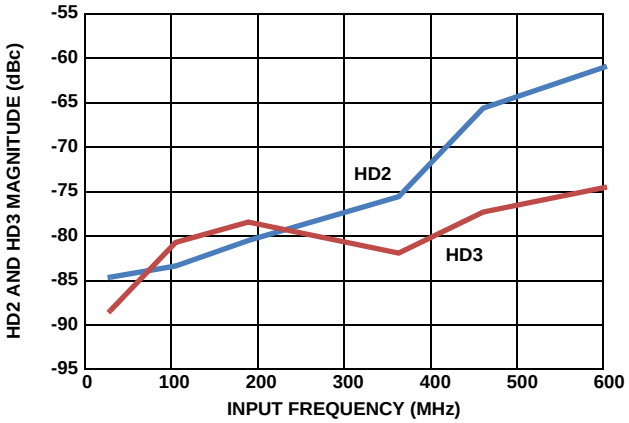



FIGURE 3. HD2 AND HD3 vs $f_{IN}$

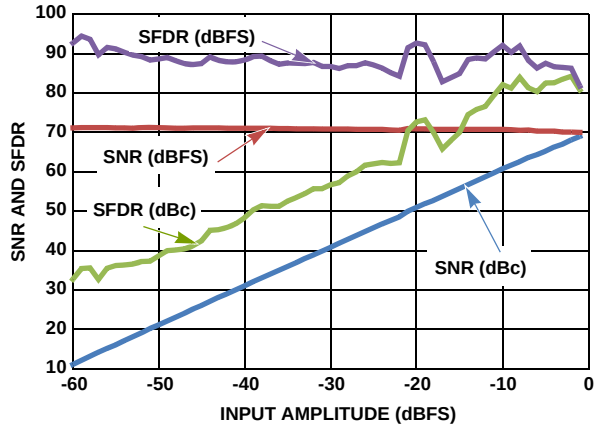



FIGURE 4. SNR AND SFDR vs $A_{IN}$

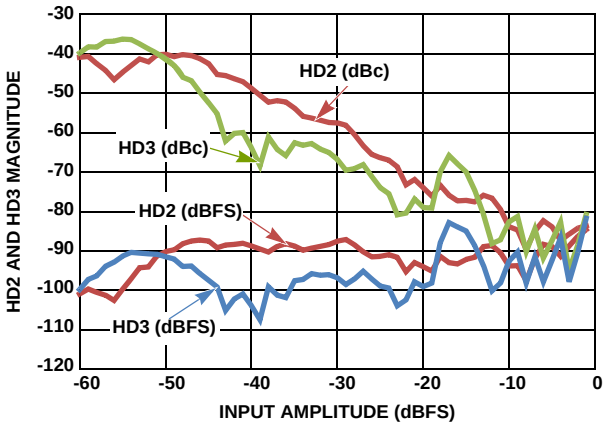



FIGURE 5. HD2 AND HD3 vs $A_{IN}$

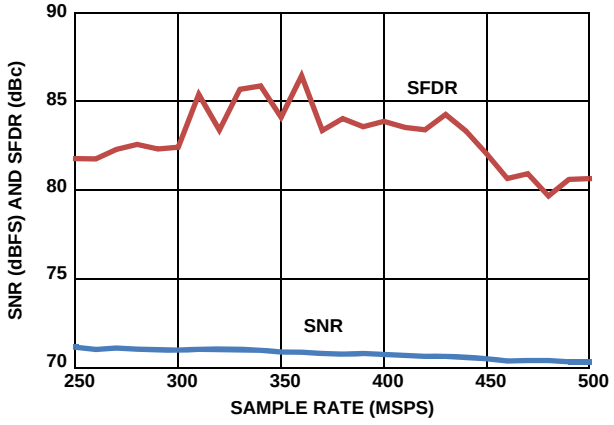



FIGURE 6. SNR AND SFDR vs $f_{SAMPLE}$

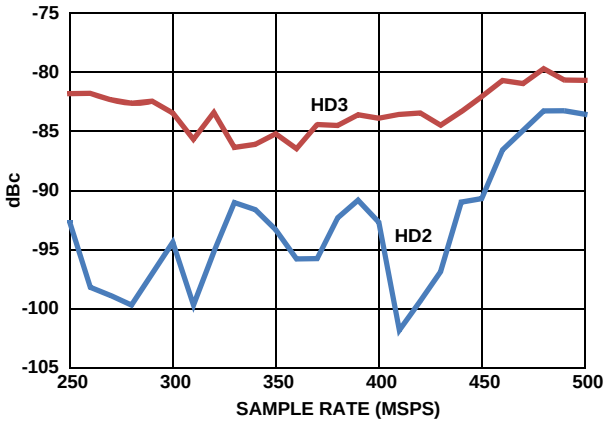



FIGURE 7. HD2 AND HD3 vs $f_{SAMPLE}$

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = 500MSPS. **(Continued)**

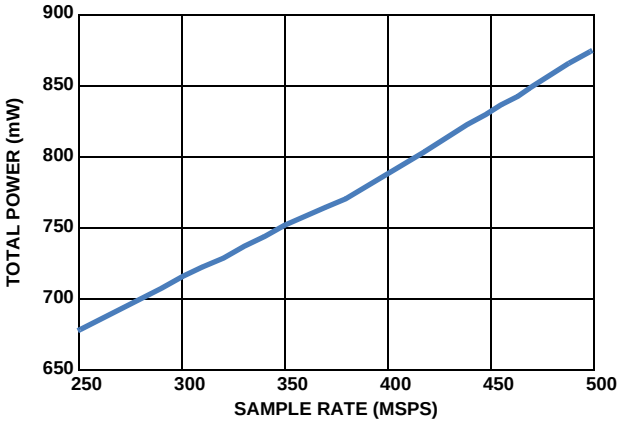



FIGURE 8. POWER vs $f_{SAMPLE}$ IN 3mA LVDS MODE

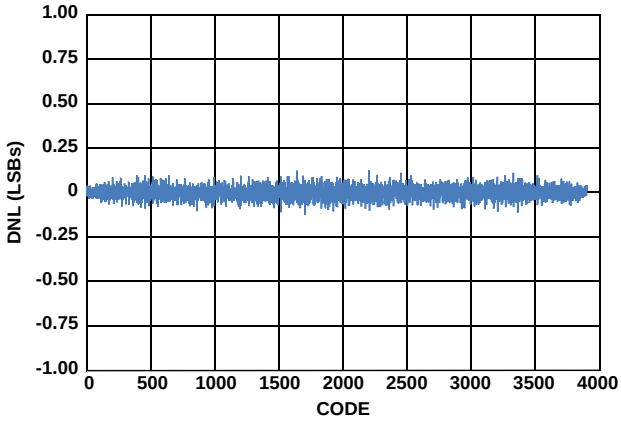



FIGURE 9. DIFFERENTIAL NONLINEARITY

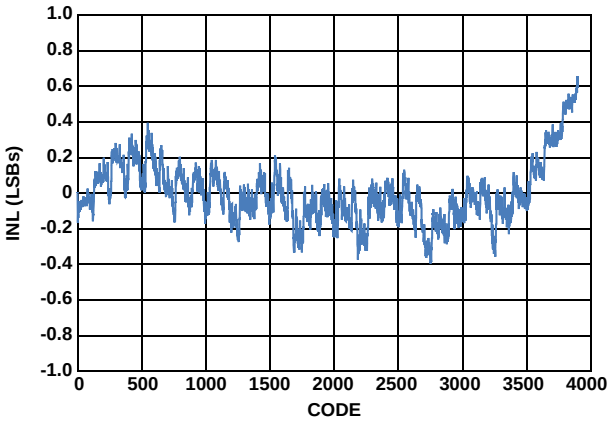



FIGURE 10. INTEGRAL NONLINEARITY

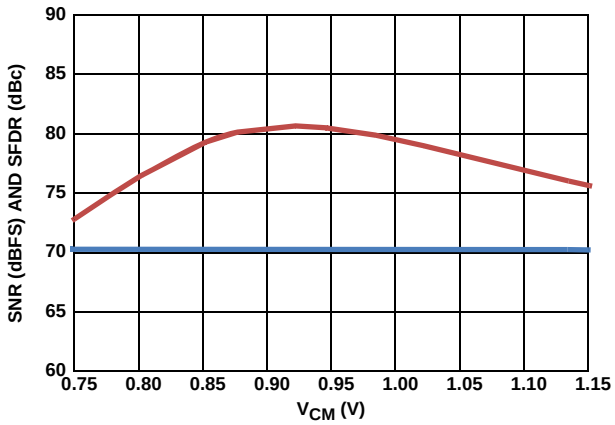



FIGURE 11. SNR AND SFDR vs $V_{CM}$

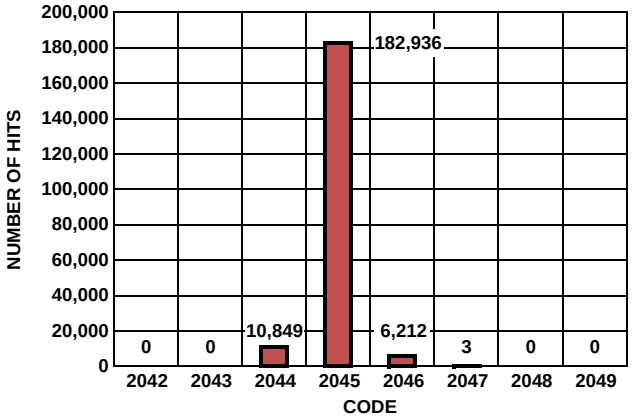



FIGURE 12. NOISE HISTOGRAM

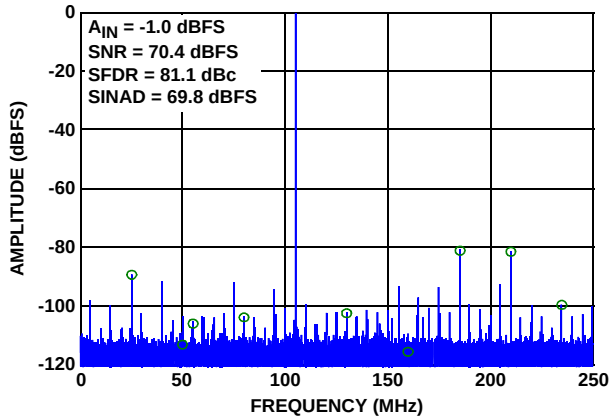



FIGURE 13. SINGLE-TONE SPECTRUM @ 105MHz

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = 500MSPS. **(Continued)**

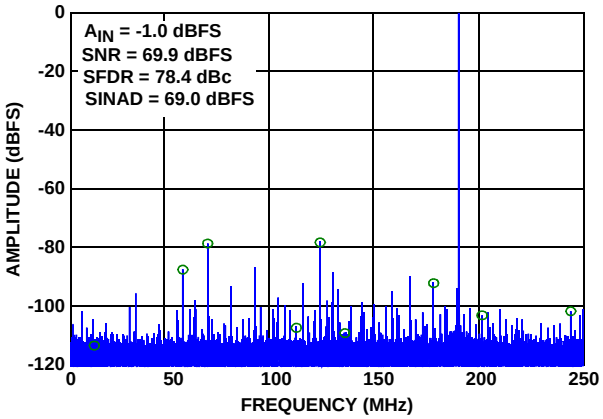



FIGURE 14. SINGLE-TONE SPECTRUM @ 190MHz

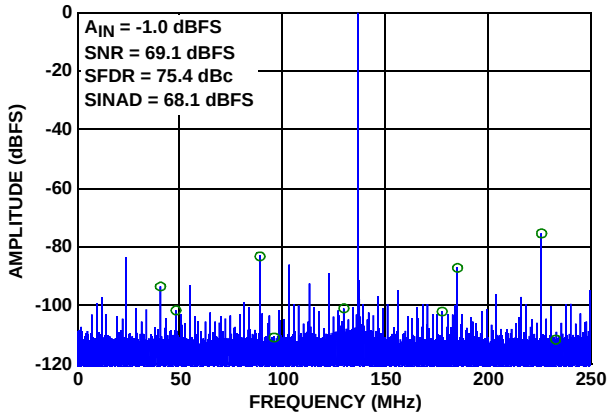



FIGURE 15. SINGLE-TONE SPECTRUM @ 363MHz

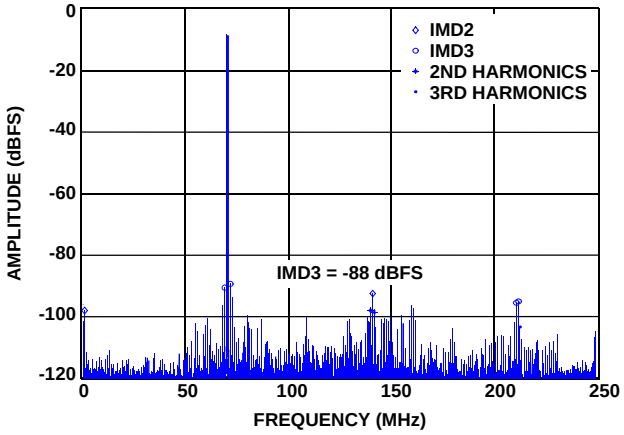



FIGURE 16. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz -7dBFS)

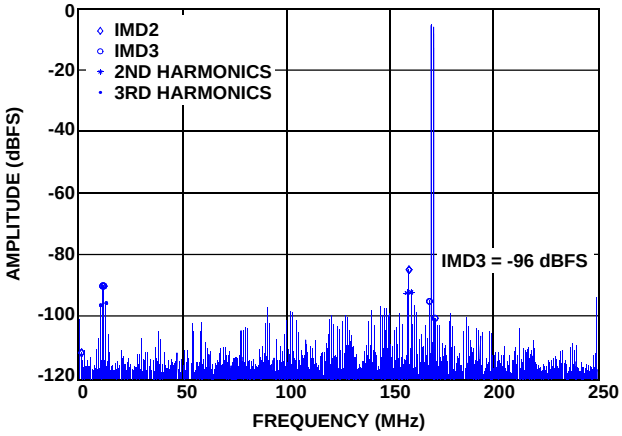



FIGURE 17. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz -7dBFS)

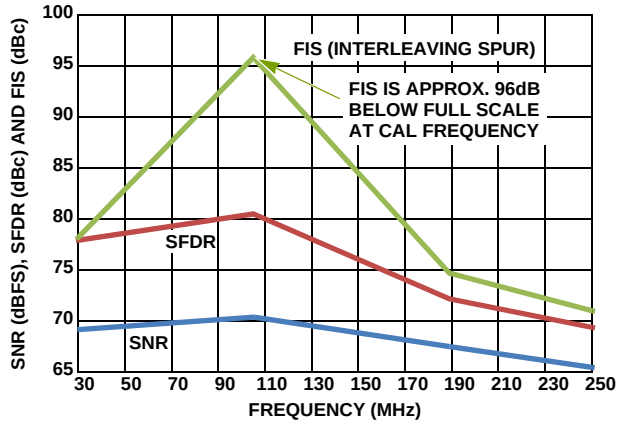



FIGURE 18. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 105MHZ

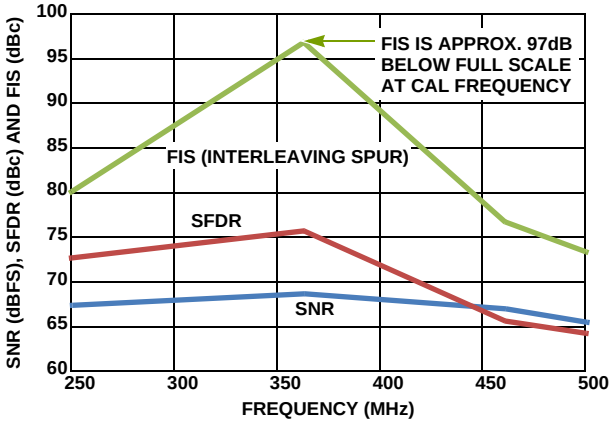



FIGURE 19. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 363MHZ

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, $T_A$ = +25°C, $A_{IN}$ = -1dBFS, $f_{IN}$ = 105MHz, $f_{SAMPLE}$ = 500MSPS. **(Continued)**

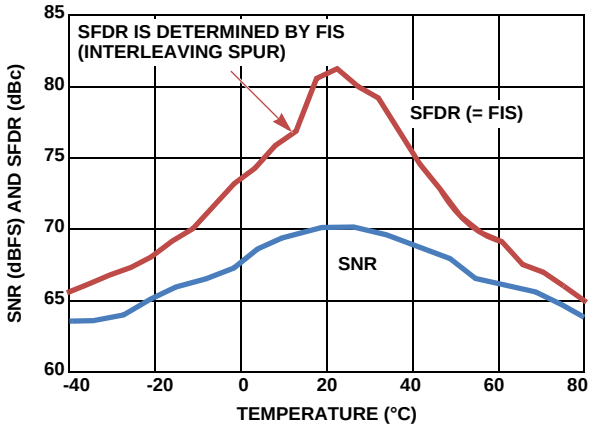



FIGURE 20. TEMPERATURE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT +25°C, $F_{IN}$ = 105MHZ

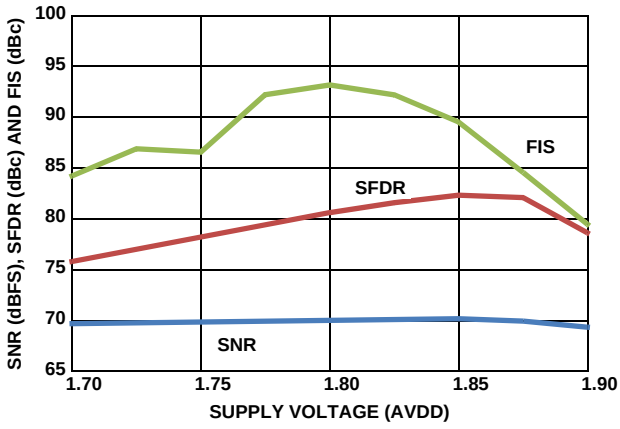



FIGURE 21. ANALOG SUPPLY VOLTAGE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 1.8V, $F_{IN}$ = 105MHZ

# Theory of Operation

## Functional Description

The ISLA212P50 is based upon a 12-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (see Figure 22). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied, resulting in a total latency of 20 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The device contains two core A/D converters with carefully matched transfer characteristics. The cores are clocked on alternate clock edges, resulting in a doubling of the sample rate.

Time–interleaved A/D systems can exhibit non–ideal artifacts in the frequency domain if the individual core A/D characteristics are not well matched. Gain, offset and timing skew mismatches are of primary concern.

The Intersil Interleave Engine (I2E) performs automatic interleave calibration for the offset, gain, and sample time skew mismatch between the core A/Ds. The I2E circuitry also adjusts in real-time for temperature and voltage variations.

Residual gain and sample time skew mismatch result in fundamental image spurs at $f_{NYQUIST} \pm f_{IN}$. Offset mismatches create spurs at DC and multiples of $f_{NYQUIST}$.

## Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 23. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. The data outputs output 0xCCCC during calibration; this can also be used to determine calibration status.

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is de-asserted. At 250MSPS the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

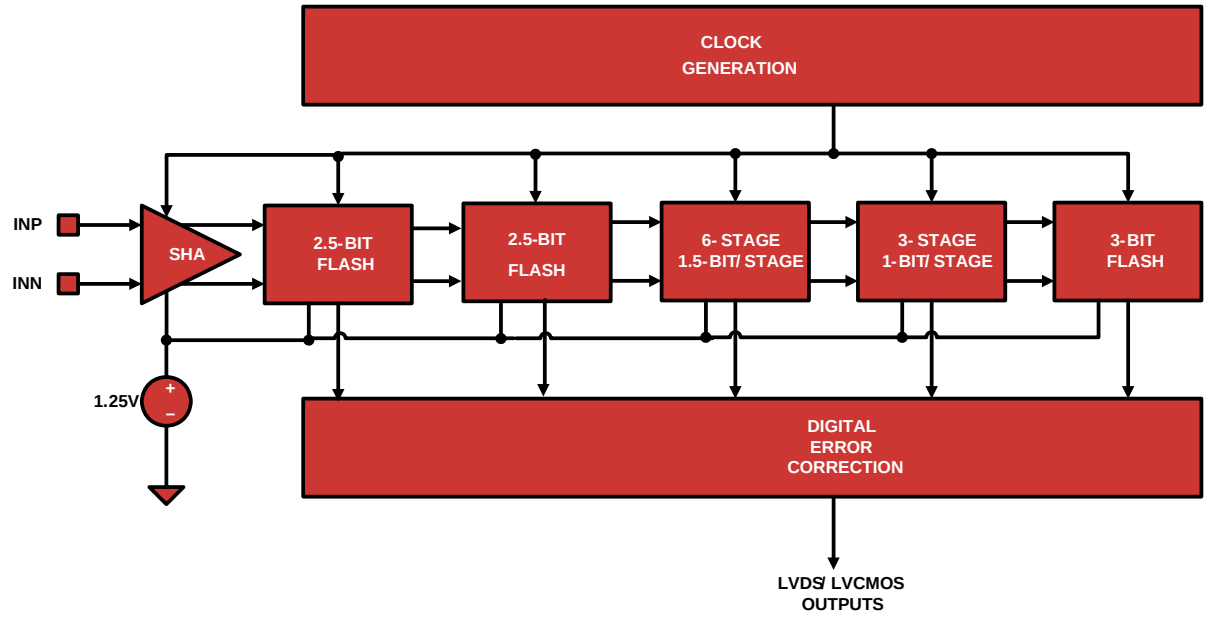



FIGURE 22. A/D CORE BLOCK DIAGRAM

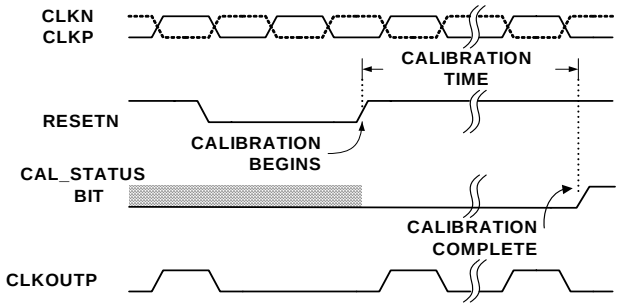



FIGURE 23. CALIBRATION TIMING

## User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA212P50 changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the A/D under the environmental conditions at which it will operate.

A supply voltage variation of less than 100mV will generally result in an SNR change of less than 0.5dBFS and SFDR change of less than 3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of less than 0.5dBFS and an SFDR change of less than 3dBc.

Figures 24 through 26 show the effect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. Applications working across the full temperature range can use the on-chip calibration feature to maximize performance when large temperature variations are expected.

## Temperature Calibration

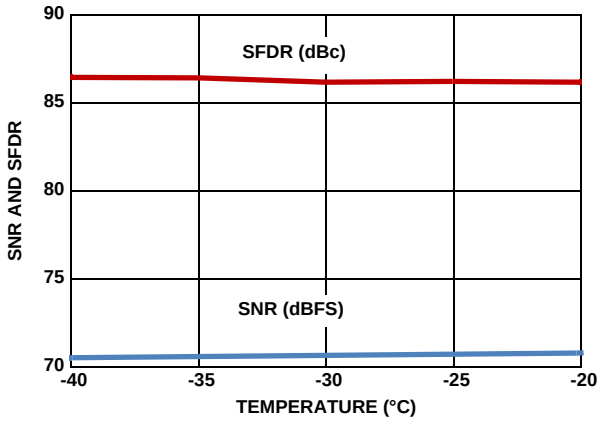



FIGURE 24. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE,DEVICE CALIBRATED AT -40°C, 500MSPS OPERATION, $f_{IN}$ = 105MHz

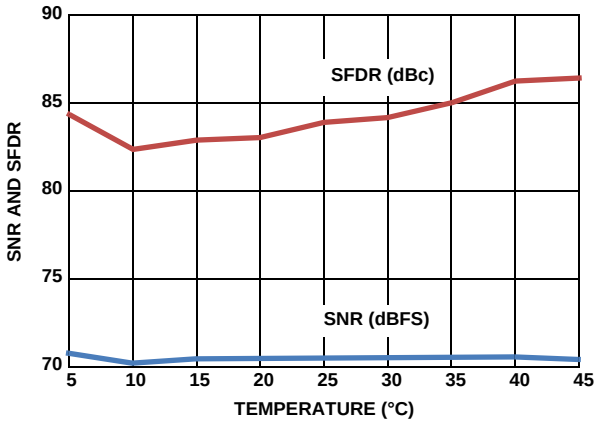



FIGURE 25. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, 500MSPS OPERATION, $f_{IN}$ = 105MHz

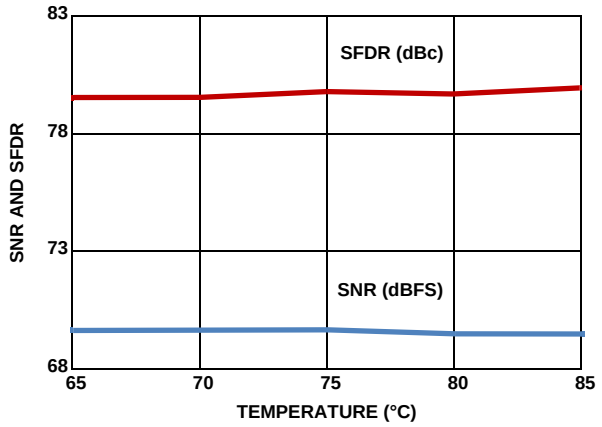



FIGURE 26. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, 500MSPS OPERATION, $f_{IN}$ = 105MHz

### Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage of 0.94V as shown in Figure 27.

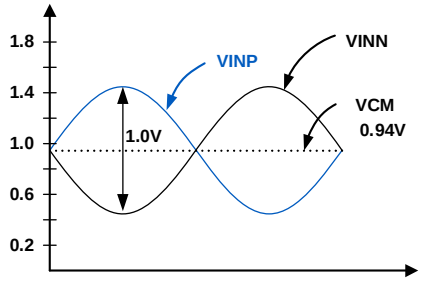



FIGURE 27. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 28 through 30. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 28 and 29.

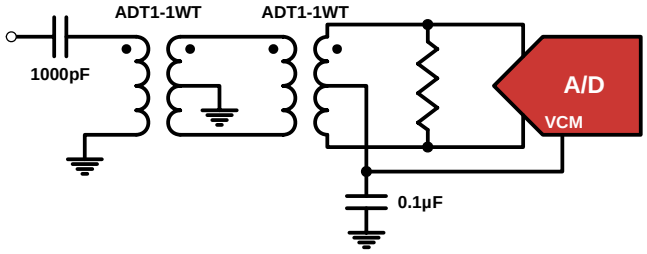



FIGURE 28. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

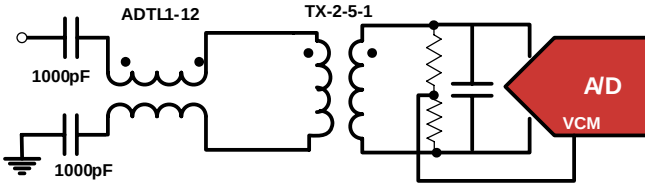



FIGURE 29. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA212P50 is 300Ω.

The SHA design uses a switched capacitor input stage (see Figure 43 on page 34), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the

next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

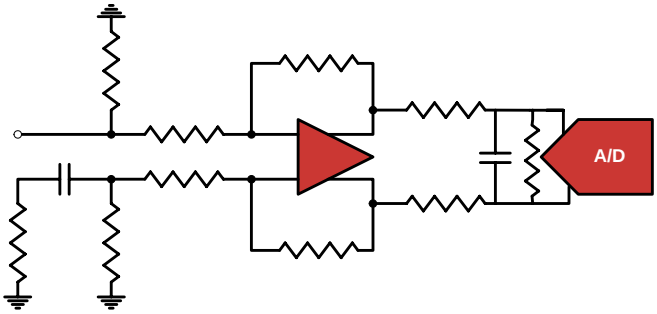



FIGURE 30. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 30, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552xx differential amplifier family can also be used in certain AC applications with minimal performance degradation. Contact the factory for more information.

## Clock Input

The clock input circuit is a differential pair (see Figure 44). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 31. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

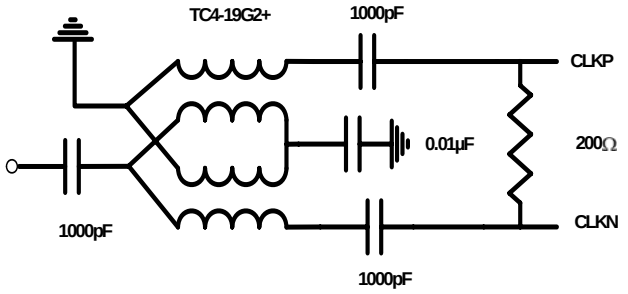



FIGURE 31. RECOMMENDED CLOCK DRIVE

A selectable 2x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs. The Phase Slip feature can be used as an alternative to using the CLKDIVRST pins to synchronize ADCs in a multiple ADC system.

TABLE 1. CLKDIV PIN SETTINGS

| CLKDIV PIN | DIVIDE RATIO |
|---|---|
| AVSS | 2 |
| Float | 1 |
| AVDD | Not Allowed |

## Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter ($t_J$) and SNR is shown in Equation 1 and is illustrated in Figure 32.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

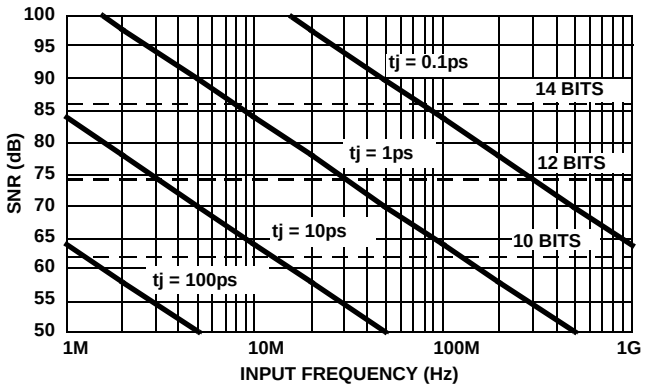



FIGURE 32. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure1A. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

## Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

## Digital Outputs

Output data is available as a parallel bus in LVDS-compatible (default) or CMOS modes. In either case, the data is presented in double data rate (DDR) format. Figure 1 shows the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA(default) or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should

experiment to determine if performance degradation is observed.

The output mode can be controlled through the SPI port, by writing to address 0x73, see “Serial Peripheral Interface” on page 25.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

## Power Dissipation

The power dissipated by the ISLA212P50 is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

## Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation to less than 104mW while Sleep mode reduces power dissipation to less than 19mW.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 500MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2.

TABLE 2. NAPSLP PIN SETTINGS

| NAPSLP PIN | MODE |
|---|---|
| AVSS | Normal |
| Float | Sleep |
| AVDD | Nap |

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in “Serial Peripheral Interface” on page 25.

## Data Format

Output data can be presented in three formats: two’s complement (default), Gray code and offset binary. The data format can also be controlled through the SPI port, by writing to address 0x73. Details on this are contained in “Serial Peripheral Interface” on page 25.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two’s complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 33 shows this operation.

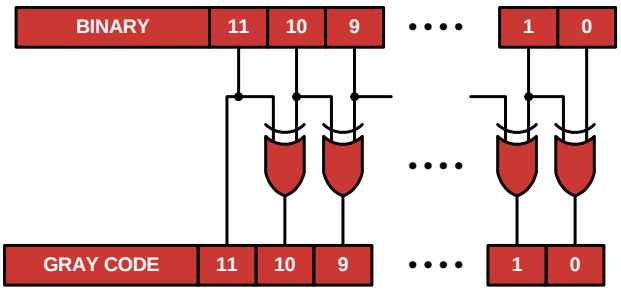
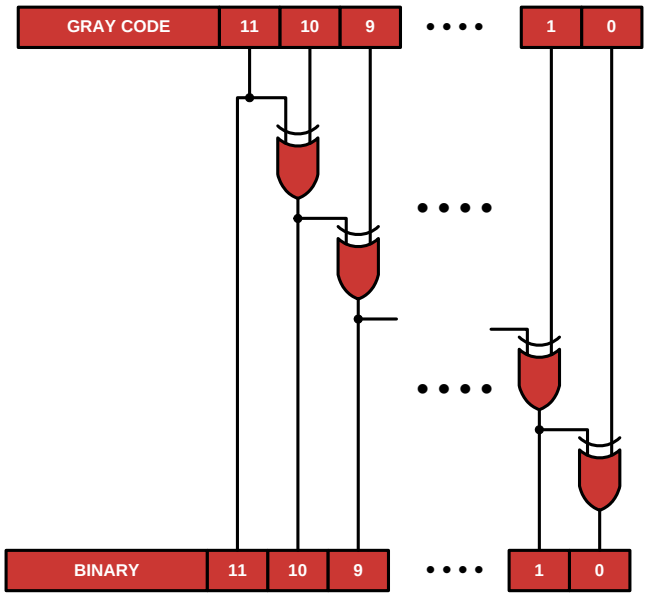



FIGURE 33. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 34.




Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

| INPUT VOLTAGE | OFFSET BINARY | TWO’S COMPLEMENT | GRAY CODE |
|---|---|---|---|
| –Full Scale | 0000 0000 0000 | 1000 0000 0000 | 0000 0000 0000 |
| –Full Scale + 1LSB | 0000 0000 0001 | 1000 0000 0001 | 0000 0000 0001 |
| Mid–Scale | 1000 0000 0000 | 0000 0000 0000 | 1100 0000 0000 |
| +Full Scale – 1LSB | 1111 1111 1110 | 0111 1111 1110 | 1000 0000 0001 |
| +Full Scale | 1111 1111 1111 | 0111 1111 1111 | 1000 0000 0000 |

# I2E Requirements and Restrictions

## Overview

I2E is a blind and background capable algorithm, designed to transparently eliminate interleaving artifacts. This circuitry eliminates interleave artifacts due to offset, gain, and sample time

mismatches between unit A/Ds, and across supply voltage and temperature variations in real-time.

Differences in the offset, gain, and sample times of time-interleaved A/Ds create artifacts in the digital outputs. Each of these artifacts creates a unique signature that may be detectable in the captured samples. The I2E algorithm optimizes performance by detecting error signatures and adjusting each unit A/D using minimal additional power.

I2E calibration is off by default at power-up. The I2E algorithm can be put in Active Run state via SPI. When the I2E algorithm is in Active Run state, it detects and corrects for offset, gain, and sample time mismatches in real time (see Track Mode description under "Active Run State" on page 22). However, certain analog input characteristics can obscure the estimation of these mismatches. The I2E algorithm is capable of detecting these obscuring analog input characteristics, and as long as they are present I2E will stop updating the correction in real time. Effectively, this freezes the current correction circuitry to the last known-good state (see Hold Mode description under "Active Run State" on page 22). Once the analog input signal stops obscuring the interleaved artifacts, the I2E algorithm will automatically start correcting for mismatch in real time again.

## Active Run State

During the Active Run state the I2E algorithm actively suppresses artifacts due to interleaving based on statistics in the digitized data. I2E has two modes of operation in this state (described in the following), dynamically chosen in real-time by the algorithm based on the statistics of the analog input signal.

1. Track Mode refers to the default state of the algorithm, when all artifacts due to interleaving are actively being eliminated. To be in Track Mode the analog input signal to the device must adhere to the following requirements:

- Possess total power greater than -20dBFS, integrated from 1MHz to Nyquist but excluding signal energy in a 100kHz band centered at $f_S/4$

The criteria above assumes 500MSPS operation; the frequency bands should be scaled proportionally for lower sample rates. Note that the effect of excluding energy in the 100kHz band around of $f_S/4$ exists in every Nyquist zone. This band generalizes to the form ($N*f_S/4$ - 50kHz) to ($N*f_S/4$ + 50kHz), where N is any odd integer. An input signal that violates these criteria briefly (approximately 10µs), before and after which it meets this criteria, will not impact system performance.

The algorithm must be in Track Mode for approximately one second (defined as I2Epost_t on "I2E Specifications" on page 11) after power-up before the specifications apply. Once this requirement has been met, the specifications of the device will continue to be met while I2E remains in Track Mode, even in the presence of temperature and supply voltage changes.

2. Hold Mode refers to the state of the I2E algorithm when the analog input signal does not meet the requirements specified above. If the algorithm detects that the signal no longer meets the criteria, it automatically enters Hold Mode. In Hold Mode, the I2E circuitry freezes the adjustment values based on the most recent set of valid input conditions. However, in Hold Mode, the I2E circuitry will not correct for new changes in interleave artifacts induced by supply voltage and temperature changes. The I2E circuitry will remain in Hold Mode until such time as the analog input signal meets the requirements for Track Mode.

## Power Meter

The power meter calculates the average power of the analog input, and determines if it's within range to allow operation in Track Mode. Both AC RMS and total RMS power are calculated, and there are separate SPI programmable thresholds and hysteresis values for each.

## FS/4 Filter (Notch)

A digital filter removes the signal energy in a 100kHz band around $f_S/4$ before the I2E circuitry uses these samples for estimating offset, gain, and sample time mismatches (data samples produced by the A/D are unaffected by this filtering). This allows the I2E algorithm to continue in Active Run state while in the presence of a large amount of input energy near the $f_S/4$ frequency. This filter can be powered down if it's known that the signal characteristics won't violate the restrictions. Powering down the FS/4 filter will reduce power consumption by approximately 30mW.

## Nyquist Zones

The I2E circuitry allows the use of any one Nyquist zone without configuration, but requires the use of only one Nyquist zone. Inputs that switch dynamically between Nyquist zones will cause poor performance for the I2E circuitry. For example, I2E will function properly for a particular application that has $f_S$ = 500MSPS and uses the 1$^{st}$ Nyquist zone (0MHz to 250MHz). I2E will also function properly for an application that uses $f_S$ = 500MSPS and the 2$^{nd}$ Nyquist zone (250MHz to 500MHz). I2E will not function properly for an application that uses $f_S$ = 500MSPS, and input frequency bands from 150MHz to 210MHz and 250MHz to 290MHz simultaneously. There is no need to configure the I2E algorithm to use a particular Nyquist zone, but no dynamic switching between Nyquist zones is permitted while I2E is running.

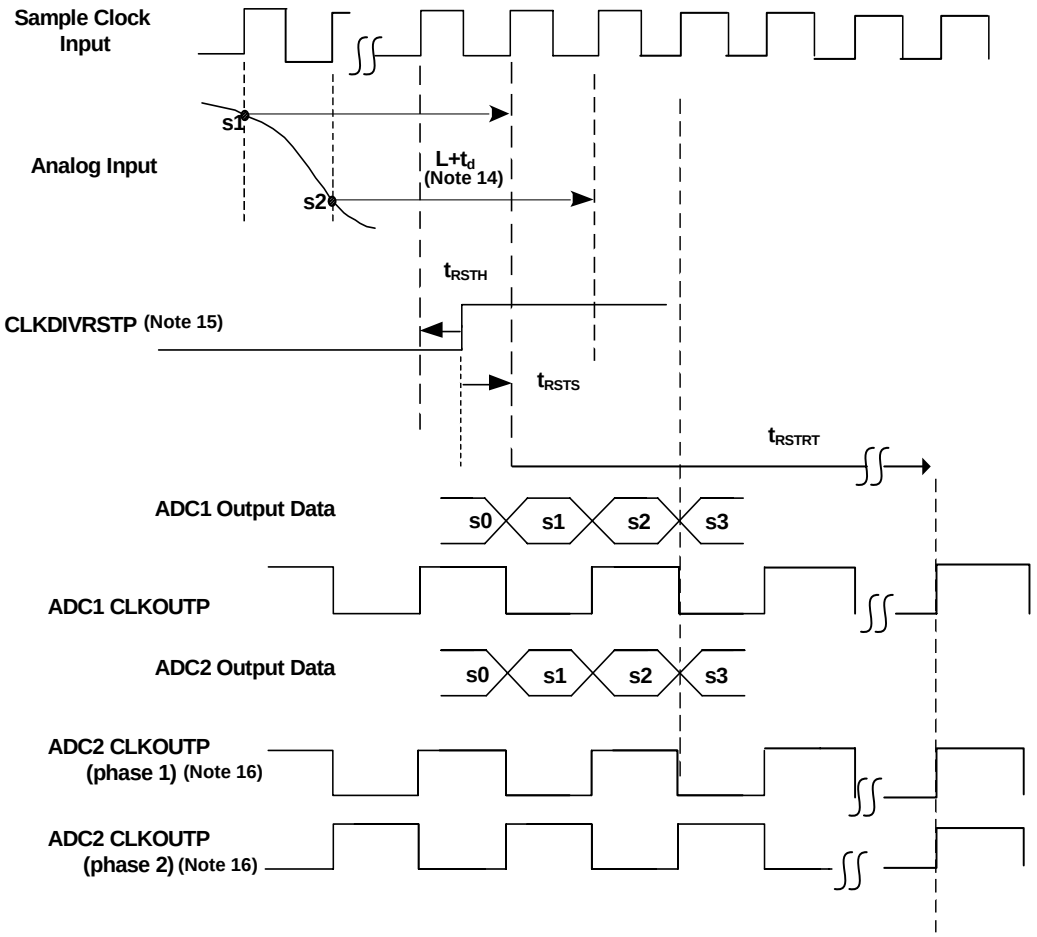
## Configurability and Communication

I2E can respond to status queries, be turned on and turned off, and generally configured via SPI programmable registers. Configuring of I2E is generally unnecessary unless the application cannot meet the requirements of Track Mode on or after power up. Parameters that can be adjusted and read back include FS/4 filter threshold and status, Power Meter threshold and status, and initial values for the offset, gain, and sample time values to use when I2E starts.

# Clock Divider Synchronous Reset

An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data. This clock is at half the frequency of the sample clock, and the absolute phase of the output clocks for multiple A/Ds is indeterminate. This feature allows the phase of multiple A/Ds to be synchronized (refer to Figure 35), which greatly simplifies data capture in systems employing multiple A/Ds.

The reset signal must be well-timed with respect to the sample clock (see "Switching Specifications" Table on page 13).




NOTES:

14. Delay equals fixed pipeline latency (L cycles) plus fixed analog propagation delay, $t_d$
15. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge. CLKDIVRSTN is not shown, but must be driven, and is the complement of CLKDIVRSTP.
16. Either Output Clock Phase (phase 1 or phase 2) equally likely prior to synchronization.

FIGURE 35. SYNCHRONOUS RESET OPERATION

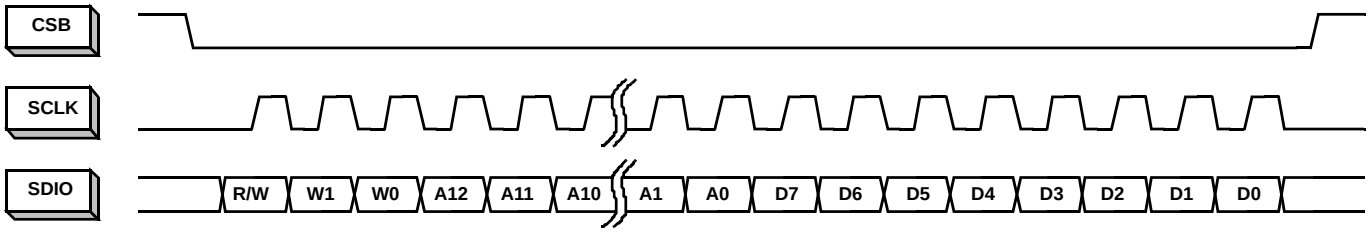



FIGURE 36. MSB-FIRST ADDRESSING

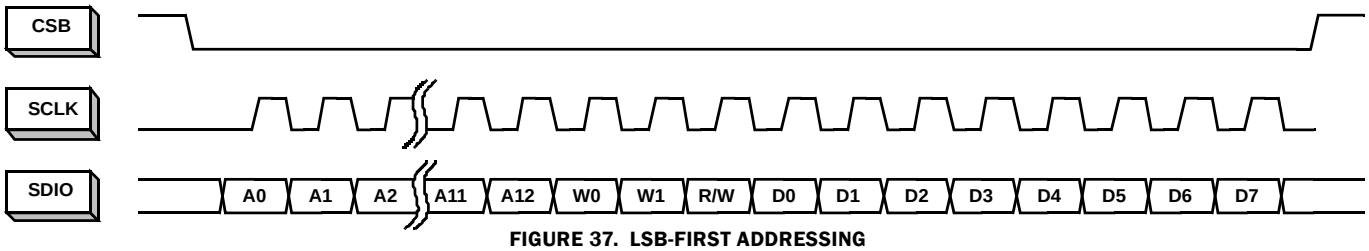
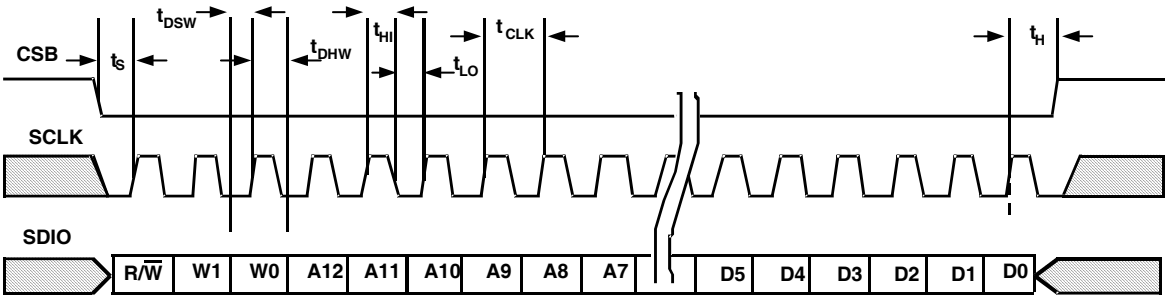



FIGURE 37. LSB-FIRST ADDRESSING




SPI WRITE

FIGURE 38. SPI WRITE

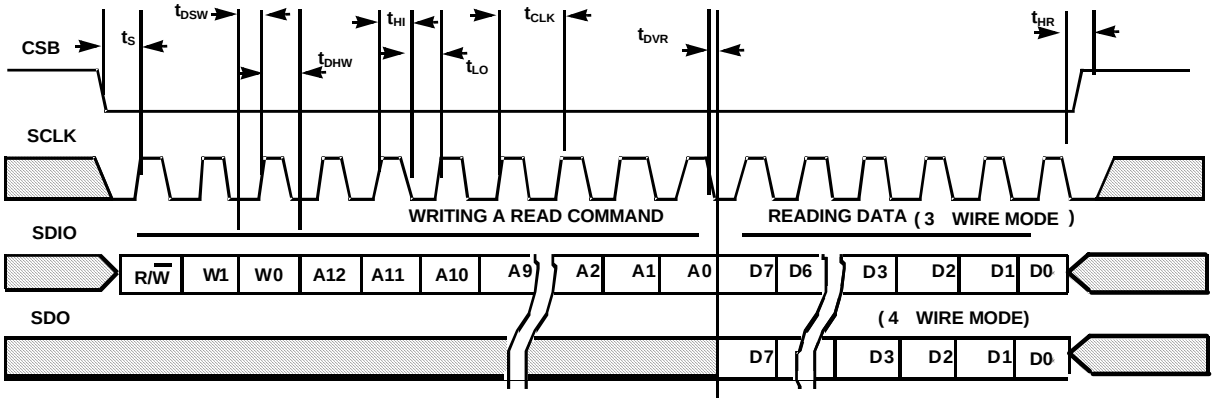



FIGURE 39. SPI READ

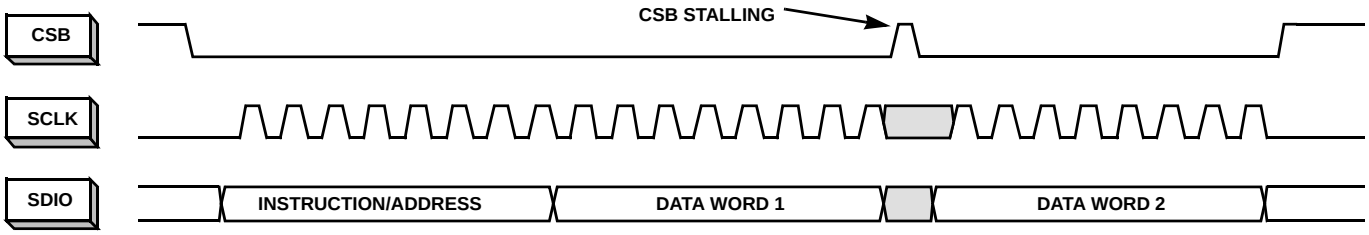



FIGURE 40. 2-BYTE TRANSFER

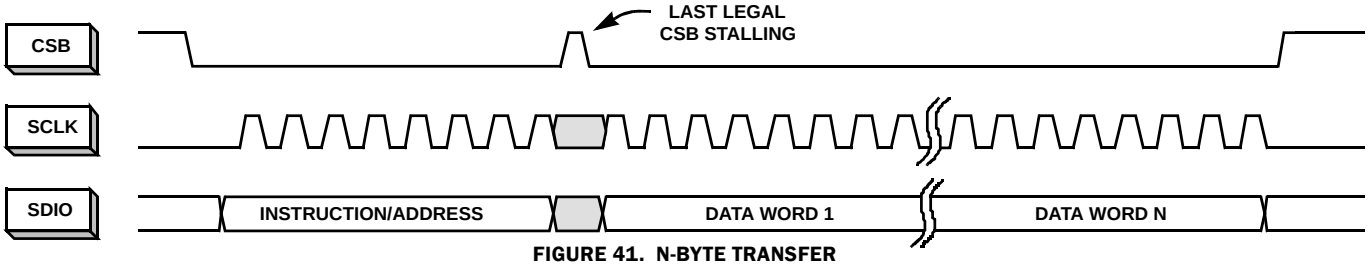



FIGURE 41. N-BYTE TRANSFER

# Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the A/D sample rate ($f_{SAMPLE}$) divided by 32 for both write operations and read operations. At $f_{SAMPLE}$ = 500MHz, maximum SCLK is 15.63MHz for writing and read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

## SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA212P50 functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 36 and 37 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it is decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 4). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 38, and timing values are given in “Switching Specifications on page 13.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the A/D (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 4. BYTE TRANSFER SELECTION

| [W1:W0] | BYTES TRANSFERRED |
|---|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 4 or more |

Figures 40 and 41 on page 24 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

## SPI Configuration

### ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

**Bit 7** SDO Active

**Bit 6** LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

**Bit 5** Soft Reset

Setting this bit high resets all SPI registers to default values.

**Bit 4** Reserved

This bit should always be set high.

**Bits 3:0** These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

### ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. Setting the burst_end address determines the end of the transfer; during a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

**Bits 7:0** Burst End Address

This register value determines the ending address of the burst data.

## Device Information

### ADDRESS 0X08: CHIP_ID

### ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

## Device Configuration/Control

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Intersil A/D products.

### ADDRESS 0X20: OFFSET_COARSE_ADC0

### ADDRESS 0X21: OFFSET_FINE_ADC0

The input offset of the A/D core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 5. The data format is twos complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 5. OFFSET ADJUSTMENTS

| PARAMETER | 0x20[7:0] COARSE OFFSET | 0x21[7:0] FINE OFFSET |
|---|---|---|
| Steps | 255 | 255 |
| –Full Scale (0x00) | -133LSB (-47mV) | -5LSB (-1.75mV) |
| Mid–Scale (0x80) | 0.0LSB (0.0mV) | 0.0LSB |
| +Full Scale (0xFF) | +133LSB (+47mV) | +5LSB (+1.75mV) |
| Nominal Step Size | 1.04LSB (0.37mV) | 0.04LSB (0.014mV) |

### ADDRESS 0X22: GAIN_COARSE__ADC0

### ADDRESS 0X23: GAIN_MEDIUM_ADC0

### ADDRESS 0X24: GAIN_FINE_ADC0

Gain of the A/D core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. (‘0011’ ≅ -4.2% and ‘1100’ ≅ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 23h and 24h.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 6. COARSE GAIN ADJUSTMENT

| 0x22[3:0] core 0 0x26[3:0] core 1 | NOMINAL COARSE GAIN ADJUST (%) |
|---|---|
| Bit3 | +2.8 |
| Bit2 | +1.4 |
| Bit1 | -2.8 |
| Bit0 | -1.4 |

TABLE 7. MEDIUM AND FINE GAIN ADJUSTMENTS

| PARAMETER | 0x23[7:0] MEDIUM GAIN | 0x24[7:0] FINE GAIN |
|---|---|---|
| Steps | 256 | 256 |
| –Full Scale (0x00) | -2% | -0.20% |
| Mid–Scale (0x80) | 0.00% | 0.00% |
| +Full Scale (0xFF) | +2% | +0.2% |
| Nominal Step Size | 0.016% | 0.0016% |

### ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to“Nap/Sleep” on page 21). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

TABLE 8. POWER-DOWN CONTROL

| VALUE | 0x25[2:0] POWER DOWN MODE |
|---|---|
| 000 | Pin Control |
| 001 | Normal Operation |
| 010 | Nap Mode |
| 100 | Sleep Mode |

### ADDRESS 0X26: OFFSET_COARSE_ADC1

### ADDRESS 0X27: OFFSET_FINE_ADC1

The input offset of A/D core#1 can be adjusted in fine and coarse steps in the same way that offset for core#0 can be adjusted. Both adjustments are made via an 8-bit word as detailed in Table 5. The data format is two’s complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

### ADDRESS 0X28: GAIN_COARSE__ADC1

### ADDRESS 0X29: GAIN_MEDIUM_ADC1

### ADDRESS 0X2A: GAIN_FINE_ADC1

Gain of A/D core #1 can be adjusted in coarse, medium and fine steps in the same way that core #0 can be adjusted. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2.

### ADDRESS 0X30: I2E STATUS

The I2E general status register.

Bits 0 and 1 indicate if the I2E circuitry is in Active Run or Hold state. The state of the I2E circuitry is dependent on the analog input signal itself. If the input signal obscures the interleave mismatched artifacts such that I2E cannot estimate the mismatch, the algorithm will dynamically enter the Hold state. For example, a DC mid-scale input to the A/D does not contain sufficient information to estimate the gain and sample time skew mismatches, and thus the I2E algorithm will enter the Hold state. In the Hold state, the analog adjustments for interleave correction will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

**Bit 0:** 0 = I2E has not detected a low power condition. 1 = I2E has detected a low power condition, and the analog adjustments for interleave correction are frozen.

**Bit 1:** 0 = I2E has not detected a low AC power condition. 1 = I2E has detected a low AC power condition, and I2E will continue to correct with best known information but will not update its interleave correction adjustments until the input signal achieves sufficient AC RMS power.

**Bit 2:** When first started, the I2E algorithm can take a significant amount of time to settle (~1s), dependent on the characteristics of the analog input signal. 0 = I2E is still settling, 1 = I2E has completed settling.

### ADDRESS 0X31: I2E CONTROL

The I2E general control register. This register can be written while I2E is running to control various parameters.

**Bit 0:** 0 = turn I2E off, 1= turn I2E on

**Bit 1:** 0 = no action, 1 = freeze I2E, leaving all settings in the current state. Subsequently writing a 0 to this bit will allow I2E to continue from the state it was left in.

**Bit 2-4:** Disable any of the interleave adjustments of offset, gain, or sample time skew

**Bit 5:** 0 = bypass notch (fs/4) filter, 1 = use notch filter on incoming data before estimating interleave mismatch terms

### ADDRESS 0X32: I2E STATIC CONTROL

The I2E general static control register. This register must be written prior to turning I2E on for the settings to take effect.

**Bit 1-4:** Reserved, always set to 0

**Bit 5:** 0 = normal operation, 1 = skip coarse adjustment of the offset, gain, and sample time skew analog controls when I2E is first turned on. This bit would typically be used if optimal analog adjustment values for offset, gain, and sample time skew have been preloaded in order to have the I2E algorithm converge more quickly.

The system gain of the pair of interleaved core A/Ds can be set by programming the medium and fine gain of the reference A/D before turning I2E on. In this case, I2E will adjust the non-reference A/D's gain to match the reference A/D's gain.

**Bit 7:** Reserved, always set to 0

### ADDRESS 0X4A: I2E POWER DOWN

This register provides the capability to completely power down the I2E algorithm and the Notch (fs/4) filter. This would typically be done to conserve power.

**BIT 0:** Power down the I2E Algorithm

**BIT 1:** Power down the Notch (fs/4) Filter

### ADDRESS 0X50-0X55: I2E FREEZE THRESHOLDS

This group of registers provides programming access to configure I2E's dynamic freeze control. As with any interleave mismatch correction algorithm making estimates of the interleave mismatch errors using the digitized application input signal, there are certain characteristics of the input signal that can obscure the mismatch estimates. For example, a DC input to the A/D contains no information about the sample time skew mismatch between the core A/Ds, and thus should not be used by the I2E algorithm to update its sample time skew estimate. Under such circumstances, I2E enters Hold state. In the Hold state, the analog adjustments will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

These registers allow the programming of the thresholds of the meters used to determine the quality of the input signal. This can be used by the application to optimize I2E's behavior based on knowledge of the input signal. For example, if a specific application had an input signal that was typically 30dB down from full scale, and was primarily concerned about analog performance of the A/D at this input power, lowering the RMS power threshold would allow I2E to continue tracking with this input power level, thus allowing it to track over voltage and temperature changes.

#### 0x50 (LSBs), 0x51 (MSBs) RMS Power Threshold

This 16-bit quantity is the RMS power threshold at which I2E will enter Hold state. The RMS power of the analog input is calculated continuously by I2E on incoming data.

Only the upper 12 bits of the ADC sample outputs are used in the averaging process for comparison to the power threshold registers. A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. As an example, if the application wanted to set this threshold to trigger near the RMS analog input of a -20dBFS sinusoidal input, the calculation to determine this register's value would be:

$$RMS_{codes} = \frac{\sqrt{2}}{2} \times 10^{\left(\frac{-20}{20}\right)} \times 2^{12} \cong (290)codes \quad \text{(EQ. 2)}$$

$$hex(((290))^2) = 0x14884_{TruncateMSBandLSBhexdigit} = \mathbf{0}x1488 \quad \text{(EQ. 3)}$$

Therefore, programming 0x1488 into these two registers will cause I2E to freeze when the signal being digitized has less RMS power than a -20dBFS sinusoid.

The default value of this register is 0x1000, causing I2E to freeze when the input amplitude is less than -21.2 dBFS.

The freezing of I2E by the RMS power meter threshold affects the gain and sample time skew interleave mismatch estimates, but not the offset mismatch estimate.

#### 0x52 RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the RMS input power must achieve ³ threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

### 0X53(LSBS), 0X54(MSBS) AC RMS POWER THRESHOLD

Similar to RMS power threshold, there must be sufficient AC RMS power (or dV/dt) of the input signal to measure sample time skew mismatch for an arbitrary input. This is clear from observing the effect when a high voltage (and therefore large RMS value) DC input is applied to the A/D input. Without sufficient dV/dt in the input signal, no information about the sample time skew between the core A/Ds can be determined from the digitized samples. The AC RMS Power Meter is implemented as a high-passed (via DSP) RMS power meter.

The required algorithm is documented as follows.

1. Write the MSBs of the 16-bit quantity to SPI Address 0x54
2. Write the LSBs of the 16-bit quantity to SPI Address 0x53

Only the upper 12 bits of the ADC sample outputs are used in the averaging process for comparison to the power threshold registers. A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. The calculation methodology to set this register is identical to the description in the RMS power threshold description.

The freezing of I2E when the AC RMS power meter threshold is not met affects the sample time skew interleave mismatch estimate, but not the offset or gain mismatch estimates.

#### 0x55 AC RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the AC RMS input power must achieve threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

## Address 0x60-0x64: I2E initialization

These registers provide access to the initialization values for each of offset, gain, and sample time skew that I2E programs into the target core A/D before adjusting to minimize interleave mismatch. They can be used by the system to, for example, reduce the convergence time of the I2E algorithm by programming in the optimal values before turning I2E on. In this case, I2E only needs to adjust for temperature and voltage-induced changes since the optimal values were recorded.

## Global Device Configuration/Control

### ADDRESS 0X70: SKEW_DIFF

The value in the skew_diff register adjusts the timing skew between the two A/D cores. The nominal range and resolution of this adjustment are given in Table 9. The default value of this register after power-up is 80h.

TABLE 9. DIFFERENTIAL SKEW ADJUSTMENT

| PARAMETER | 0x70[7:0] DIFFERENTIAL SKEW |
|---|---|
| Steps | 256 |
| –Full Scale (0x00) | -6.5ps |
| Mid–Scale (0x80) | 0.0ps |
| +Full Scale (0xFF) | +6.5ps |
| Nominal Step Size | 51fs |

### ADDRESS 0X71: PHASE_SLIP

The output data clock is generated by dividing down the A/D input sample clock. Some systems with multiple A/Ds can more easily latch the data from each A/D by controlling the phase of the output data clock. This control is accomplished through the use of the phase_slip SPI feature, which allows the rising edge of the output data clock to be advanced by one input clock period, as shown in the Figure 42. Execution of a phase_slip command is accomplished by first writing a '0' to bit 0 at address 0x71, followed by writing a '1' to bit 0 at address 0x71.

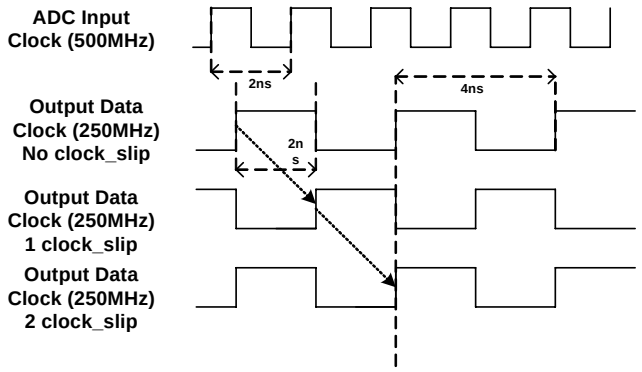



FIGURE 42. PHASE SLIP

### ADDRESS 0X72: CLOCK_DIVIDE

The ISLA212P50 has a selectable clock divider that can be set to divide by two or one (no division). By default, the tri-level CLKDIV pin selects the divisor This functionality can be overridden and controlled through the SPI, as shown in Table 10. This register is not changed by a Soft Reset.

TABLE 10. CLOCK DIVIDER SELECTION

| VALUE | 0x72[2:0] CLOCK DIVIDER |
|---|---|
| 000 | Pin Control |
| 001 | Divide by 1 |
| 010 | Divide by 2 |
| other | Not Allowed |

### ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The ISLA212P50 can present output data in two physical formats: LVDS (default) or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (default, 3mA or low (2mA).

Data can be coded in three possible formats: two's complement (default), Gray code or offset binary. See Table 12.

This register is not changed by a Soft Reset.

TABLE 11. OUTPUT MODE CONTROL

| VALUE | 0x73[7:5] OUTPUT MODE |
|---|---|
| 000 | LVDS 3mA (Default) |
| 001 | LVDS 2mA |
| 100 | LVCMOS |

TABLE 12. OUTPUT FORMAT CONTROL

| VALUE | 0x73[2:0] OUTPUT FORMAT |
|---|---|
| 000 | Two's Complement (Default) |
| 010 | Gray Code |
| 100 | Offset Binary |

## ADDRESS 0X74: OUTPUT_MODE_B

**Bit 6** DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. Table 13 shows the allowable sample rate ranges for the slow and fast settings. Note that Bit 4 at 0x74 is reserved and must not change value. A user writing to Bit 6 should first read 0x74 to determine proper value to write back to Bit 4 when writing to 0x74.

TABLE 13. DLL RANGES

| DLL RANGE | MIN | MAX | UNIT |
|---|---|---|---|
| Slow | 80 | 200 | MSPS |
| Fast | 160 | 500 | MSPS |

## ADDRESS 0XB6: CALIBRATION STATUS

The LSB at address 0xB6 can be read to determine calibration status. The bit is '0' during calibration and goes to a logic '1' when calibration is complete.This register is unique in that it can be read after POR at calibration, unlike the other registers on chip, which can't be read until calibration is complete.

## DEVICE TEST

The ISLA212P50 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A user can pick from preset built-in patterns by writing to the output test mode field [7:4] at C0h or user defined patterns by writing to the user test mode field [2:0] at C0h. The user defined patterns should be loaded at address space C1 through D0, see the "SPI Memory Map" on page 31 for more detail. The predefined patterns are shown in Table 14. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

## ADDRESS 0XC0: TEST_IO

**Bits 7:4** Output Test Mode

These bits set the test mode according to table below. Other values are reserved.User test patterns loaded at 0xC1 through 0xD0 are also available by writing '1000' to [7:4] at 0xC0 and a pattern depth value to [2:0] at 0xC0. See the memory map.

**Bits 2:0** User Test Mode

The three LSBs in this register determine the test pattern in combination with registers 0xC1 through 0xD0. Refer to the SPI Memory Map on page 31.

TABLE 14. OUTPUT TEST MODES

| VALUE | 0xC0[7:4] OUTPUT TEST MODE | WORD 1 | WORD 2 |
|---|---|---|---|
| 0000 | Off | | |
| 0001 | Midscale | 0x8000 | N/A |
| 0010 | Positive Full-Scale | 0xFFFF | N/A |
| 0011 | Negative Full-Scale | 0x0000 | N/A |
| 0100 | Checkerboard (DDR) | | |
| 0101 | Reserved | N/A | N/A |
| 0110 | Reserved | N/A | N/A |
| 0111 | All on/off (DDR) | | |
| 1000 | User Pattern | user_patt1 | user_patt2 |
| 1001 | Reserved | N/A | N/A |
| 1010 | Ramp | N/A | N/A |

## ADDRESS 0XC1: USER_PATT1_LSB

## ADDRESS 0XC2: USER_PATT1_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 1.

## ADDRESS 0XC3: USER_PATT2_LSB

## ADDRESS 0XC4: USER_PATT2_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 2

## ADDRESS 0XC5: USER_PATT3_LSB

## ADDRESS 0XC6: USER_PATT3_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 3

## ADDRESS 0XC7: USER_PATT4_LSB

## ADDRESS 0XC8: USER_PATT4_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 4.

## ADDRESS 0XC9: USER_PATT5_LSB

## ADDRESS 0XCA: USER_PATT5_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 5.

#### ADDRESS 0XCB: USER_PATT6_LSB

#### ADDRESS 0XCC: USER_PATT6_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 6

#### ADDRESS 0XCD: USER_PATT7_LSB

#### ADDRESS 0XCE: USER_PATT7_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 7.

#### ADDRESS 0XCF: USER_PATT8_LSB

#### ADDRESS 0XD0: USER_PATT8_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 8

### Digital Temperature Sensor

#### ADDRESS 0X4B: TEMP_COUNTER_HIGH

Bits [2:0] of this register hold the 3 MSBs of the 11-bit temperature code.

Bit [7] of this register indicates a valid temperature_counter read was performed. A logic '1' indicates a valid read.

#### ADDRESS 0X4C: TEMP_COUNTER_LOW

Bits [7:0] of this register hold the lower 8 LSBs of the 11-bit temperature code.

#### ADDRESS 0X4D: TEMP_COUNTER_CONTROL

Bit [7] Measurement mode select bit, set to '1' for recommended PTAT mode. '0' (default) is IPTAT mode and is less accurate and not recommended.

Bit [6] Temperature counter enable bit. Set to '1' to enable.

Bit [5] Temperature counter power down bit. Set to '1' to power down temperature counter.

Bit [4] Temperature counter reset bit. Set to '1' to reset count.

Bit [3:1] Three bit frequency divider field. Sets temperature counter update rate. Update rate is proportional to ADC sample clock rate and divide ratio. A '101' updates the temp counter every ~ 66µs (for 250Msps). Faster updates rates result in lower precision.

Bit [0] Select sampler bit. Set to '0'.

This set of registers provides digital access to an PTAT or IPTAT-based temperature sensor, allowing the system to estimate the temperature of the die, allowing easy access to information that can be used to decide when to recalibrate the A/D as needed.

The nominal transfer function of the temperature counter is Codes (in decimal) = 0.56*T(°C) + 618. This corresponds to approximately a 65 LSB increase from -40°C to +85°C. The accuracy of the sensor is approximately ±20% for both slope and starting code offset.

A typical temperature measurement can occur as follows:

1. Write '0xCA' to address 0x4D - enable temp counter, divide = '101'
2. Wait >= 132uS (at 250Msps) - longer wait time ensures the sensor completes one valid cycle.
3. Write '0x20' to address 0x4D - power-down, disable temp counter - recommended between measurements. This ensures that the output does not change between MSB and LSB reads.
4. Read address 0x4B (MSBs)
5. Read address 0x4C (LSBs)
6. Record temp code value
7. Write '0x20' to address 0x4D - power-down, disable temp counter

Contact the factory for more information if needed.

# SPI Memory Map

| | Addr. (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SPI Config/Control | 00 | port_config | SDO Active | LSB First | Soft Reset | | | Mirror (bit5) | Mirror (bit6) | Mirror (bit7) | 00h |
| | 01 | Reserved | Reserved | | | | | | | | |
| | 02 | burst_end | Burst end address [7:0] | | | | | | | | 00h |
| | 03-07 | Reserved | Reserved | | | | | | | | |
| DUT Info | 08 | chip_id | Chip ID # | | | | | | | | Read only |
| | 09 | chip_version | Chip Version # | | | | | | | | Read only |
| | 0A-0F | Reserved | Reserved | | | | | | | | |
| Device Config/Control | 10-1F | Reserved | Reserved | | | | | | | | |
| | 20 | offset_coarse_adc0 | Coarse Offset | | | | | | | | cal. value |
| | 21 | offset_fine_adc0 | Fine Offset | | | | | | | | cal. value |
| | 22 | gain_coarse_adc0 | Reserved | | | | Coarse Gain | | | | cal. value |
| | 23 | gain_medium_adc0 | Medium Gain | | | | | | | | cal. value |
| | 24 | gain_fine_adc0 | Fine Gain | | | | | | | | cal. value |
| | 25 | modes_adc0 | Reserved | | | | | Power Down Mode ADC0 [2:0]<br>000 = Pin Control<br>001 = Normal Operation<br>010 = Nap<br>100 = Sleep<br>Other codes = Reserved | | | 00h<br>NOT reset by Soft Reset |
| | 26 | offset_coarse_adc1 | Coarse Offset | | | | | | | | cal. value |
| | 27 | offset_fine_adc1 | Fine Offset | | | | | | | | cal. value |
| | 28 | gain_coarse_adc1 | Reserved | | | | Coarse Gain | | | | cal. value |
| | 29 | gain_medium_adc1 | Medium Gain | | | | | | | | cal. value |
| | 2A | gain_fine_adc1 | Fine Gain | | | | | | | | cal. value |
| | 2B | modes_adc1 | Reserved | | | | | Power Down Mode ADC1 [2:0]<br>000 = Pin Control<br>001 = Normal Operation<br>010 = Nap<br>100 = Sleep<br>Other codes = Reserved | | | 00h<br>NOT reset by Soft Reset |
| | 2C-2F | Reserved | Reserved | | | | | | | | |
| I2E Control and Status | 30 | I2E_status | | | | Reserved | | I2E Settled | Low AC RMS Power | Low RMS Power | Read only |
| | 31 | I2E_control | | | Enable Notch (fs/4) Filter | Disable Offset | Disable Gain | Disable Skew | Freeze | Run | 20h |
| | 32 | I2E_static_control | Reserved must be set to 0 | | Skip coarse adj. | Reserved, must be set to 0 | | | | Should be set to 1 | 01h |
| | 33-49 | Reserved | Reserved | | | | | | | | |
| | 4A | I2E_power_down | | | | | | | Notch (fs/4) Filter Power Down | I2E Power Down | 03h |
| | 4B | temp_counter_high | | | | | | Temp Counter [10:8] | | | Read only |
| | 4C | temp_counter_low | Temp Counter [7:0] | | | | | | | | Read only |
| | 4D | temp_counter_control | | Enable | PD | Reset | Divider [2:0] | | | Select | 00h |
| | 4E-4F | Reserved | Reserved | | | | | | | | |
| | 50 | I2E_rms_power_threshold_lsb | RMS Power Threshold, LSBs [7:0] | | | | | | | | 00h |

## SPI Memory Map (Continued)

| | Addr. (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| I2E Control and Status | 51 | I2E_rms_power_threshold_msb | RMS Power Threshold, MSBs [15:8] | | | | | | | | 10h |
| | 52 | I2E_rms_hysteresis | RMS Power Hysteresis | | | | | | | | FFh |
| | 53 | I2E_ac_rms_power_threshold_lsb | AC Power Threshold, LSBs, [7:0] | | | | | | | | 50h |
| | 54 | I2E_ac_rms_power_threshold_msb | AC Power Threshold, MSBs, [15:8] | | | | | | | | 00h |
| | 55 | I2E_ac_rms_hysteresis | AC RMS Power Hysteresis | | | | | | | | 10h |
| | 56-5F | Reserved | Reserved | | | | | | | | |
| | 60 | coarse_offset_init | Coarse Offset Initialization value | | | | | | | | 80h |
| | 61 | fine_offset_init | Fine Offset Initialization value | | | | | | | | 80h |
| | 62 | medium_gain_init | Medium Gain Initialization value | | | | | | | | 80h |
| | 63 | fine_gain_init | Fine Gain Initialization value | | | | | | | | 80h |
| | 64 | sample_time_skew_init | Sample Time Skew Initialization value | | | | | | | | 80h |
| | 65-6F | Reserved | Reserved | | | | | | | | |
| DeviceConfig/Control | 70 | skew_diff | Differential Skew | | | | | | | | 80h |
| | 71 | phase_slip | Reserved | | | | | | | Next Clock Edge | 00h |
| | 72 | clock_divide | | | | | | Clock Divide [2:0]<br>000 = Pin Control<br>001 = divide by 1<br>010 = divide by 2<br>Other codes = Reserved | | | 00h<br>NOT reset by Soft Reset |
| | 73 | output_mode_A | Output Mode [7:5]<br>000 =LVDS 3mA (Default)<br>001 = LVDS 2mA<br>100 = LVCMOS<br>Other codes = Reserved | | | | | Output Format [2:0]<br>000 = Two's Complement (Default)<br>010 = Gray Code<br>100 = Offset Binary<br>Other codes = Reserved | | | 00h<br>NOT reset by Soft Reset |
| | 74 | output_mode_B | | DLL Range<br>0 = Fast<br>1 = Slow<br>(Default = '0') | | Reserved | | | | | 00h<br>NOT reset by Soft Reset |
| | 75-BF | Reserved | Reserved | | | | | | | | |
| | A4 | dll_ctrl_upper_adc0 | Consult Factory | | | | | | | | cal. value |
| | A5 | dll_ctrl_lower_adc0 | Consult Factory | | | | | | | | cal. value |
| | A6 | dll_status_upper_adc0 | Consult Factory | | | | | | | | Read only |
| | A7 | dll_status_lower_adc0 | Consult Factory | | | | | | | | Read only |
| | A8 | dll_ctrl_upper_adc1 | Consult Factory | | | | | | | | cal. value |
| | A9 | dll_ctrl_lower_adc1 | Consult Factory | | | | | | | | cal. value |
| | AA | dll_status_upper_adc1 | Consult Factory | | | | | | | | Read only |
| | AB | dll_status_lower_adc1 | Consult Factory | | | | | | | | Read only |
| | AC-B5 | Reserved | Reserved | | | | | | | | |
| | B6 | Cal_Status | Reserved | | | | | | | Calibration Done | Read only |
| | B7-BF | Reserved | Reserved | | | | | | | | |

## SPI Memory Map (Continued)

| | Addr. (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Device Test | C0 | test_io | Output Test Mode (DDR) [7:4]<br>0 = Off (Note 14)<br>1 = Midscale Short<br>2 = +FS Short<br>3 = -FS Short<br>4 = Checker Board output - 0xAAAA, 0x5555 DDR<br>5 = Reserved<br>6 = Reserved<br>7 = 0xFFFF,0x0000 all on pattern, DDR Word Toggle<br>8 = User Pattern (1 to 8 deep, DDR, MSB justified)<br>9 = Reserved<br>10 = Ramp<br>11-15 = Reserved | | | | | User Test Mode(DDR) [2:0]<br>0 = cycle pattern 1 through 2<br>1 = cycle pattern 1 through 4<br>2 = cycle pattern 1 through 6<br>3 = cycle pattern 1 through 8<br>4-7 =NA | | | 00h |
| | C1 | user_patt1_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | C2 | user_patt1_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | C3 | user_patt2_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | C4 | user_patt2_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | C5 | user_patt3_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | C6 | user_patt3_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | C7 | user_patt4_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | C8 | user_patt4_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | C9 | user_patt5_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | CA | user_patt5_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | CB | user_patt6_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | CC | user_patt6_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | CD | user_patt7_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | CE | user_patt7_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | CF | user_patt8_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h |
| | D0 | user_patt8_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h |
| | D1-FD | Reserved | Reserved | | | | | | | | |
| | FE | VRAM_latch_enable | Reserved | | | | | | | LE<br>Active high | 00h |
| | FF | Reserved | | | | | | | | | |

NOTE:

14. During Calibration xCCCC (MSB justified) is presented at the output data bus, toggling on the LSB (and higher) data bits occurs at completion of calibration. This behavior can be used as an option to monitoring Over range to determine calibration state.

## Equivalent Circuits

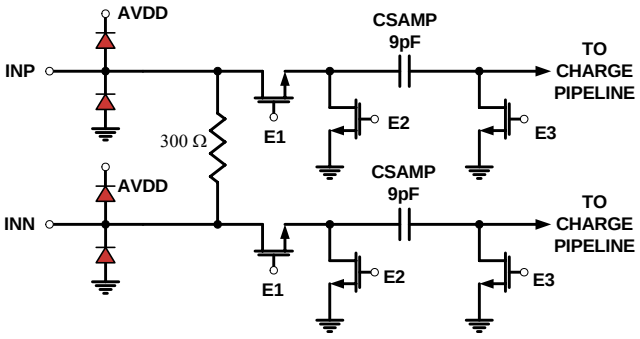



FIGURE 43. ANALOG INPUTS

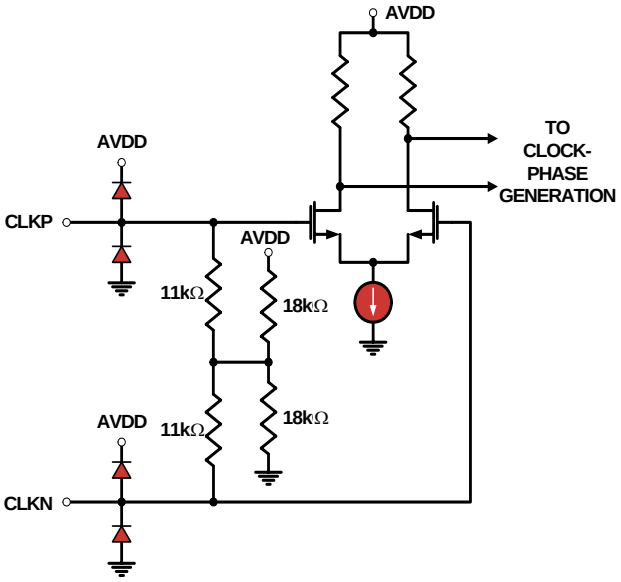



FIGURE 44. CLOCK INPUTS

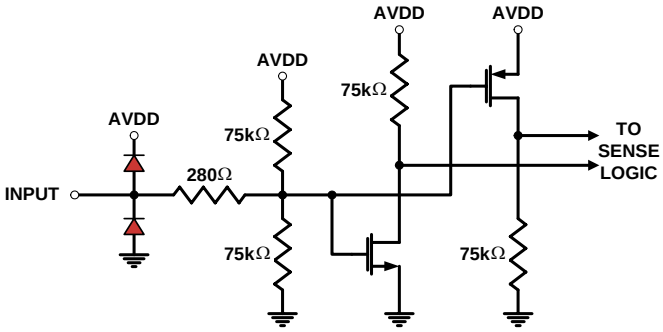



FIGURE 45. TRI-LEVEL DIGITAL INPUTS

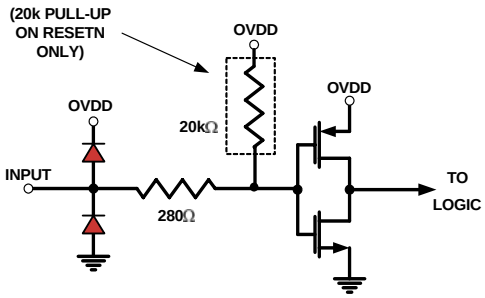



FIGURE 46. DIGITAL INPUTS

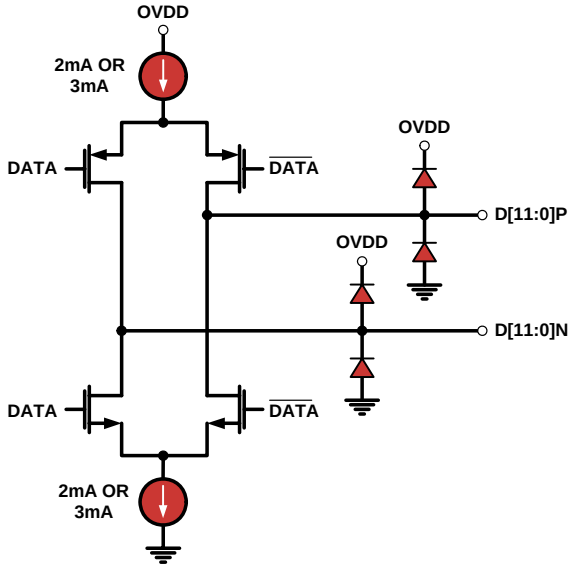



FIGURE 47. LVDS OUTPUTS

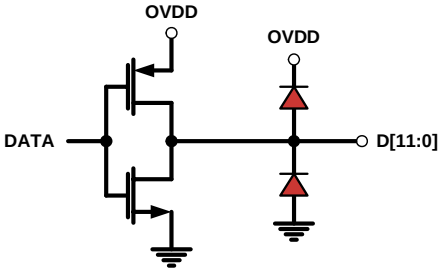



FIGURE 48. CMOS OUTPUTS

## Equivalent Circuits (Continued)

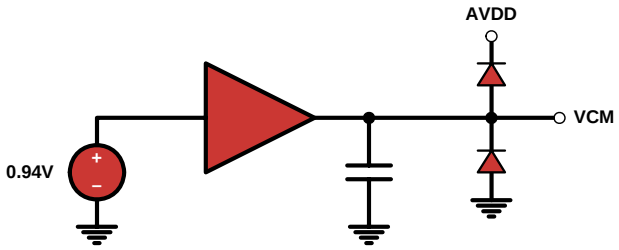



FIGURE 49. VCM_OUT OUTPUT

# A/D Evaluation Platform

Intersil offers an A/D Evaluation platform which can be used to evaluate any of Intersil's high speed A/D products. The platform consists of a FPGA based data capture motherboard and a family of A/D daughtercards. This USB based platform allows a user to quickly evaluate the A/D's performance at a user's specific application frequency requirements. More information is available at http://www.intersil.com/converters/adc_eval_platform/

# Layout Considerations

## Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

## Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

## Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

## Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

## LVDS Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power-plane breaks with signal traces.

## LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

## Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal A/D performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

# Definitions

**Analog Input Bandwidth** is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

**Aperture Delay or Sampling Delay** is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

**Aperture Jitter** is the RMS variation in aperture delay for a set of samples.

**Clock Duty Cycle** is the ratio of the time the clock wave is at logic high to the total time of one clock period.

**Differential Non-Linearity (DNL)** is the deviation of any code width from an ideal 1 LSB step.

**Effective Number of Bits (ENOB)** is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

**Gain Error** is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage less 2 LSB. It is typically expressed in percent.

**I2E** The Intersil Interleave Engine. This highly configurable circuitry performs estimates of offset, gain, and sample time

skew mismatches between the core converters, and updates analog adjustments for each to minimize interleave spurs.

**Integral Non-Linearity (INL)** is the maximum deviation of the A/D's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Least Significant Bit (LSB)** is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

**Missing Codes** are output codes that are skipped and will never appear at the A/D output. These codes cannot be reached with any input value.

**Most Significant Bit (MSB)** is the bit that has the largest value or weight.

**Pipeline Delay** is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

**Power Supply Rejection Ratio (PSRR)** is the ratio of the observed magnitude of a spur in the A/D FFT, caused by an AC signal superimposed on the power supply voltage.

**Signal to Noise-and-Distortion (SINAD)** is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

**Signal-to-Noise Ratio** (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

**Spurious-Free-Dynamic Range (SFDR)** is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| 5/25/11 | FN7843.1 | Initial Release to Web |

# Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISLA212P50

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

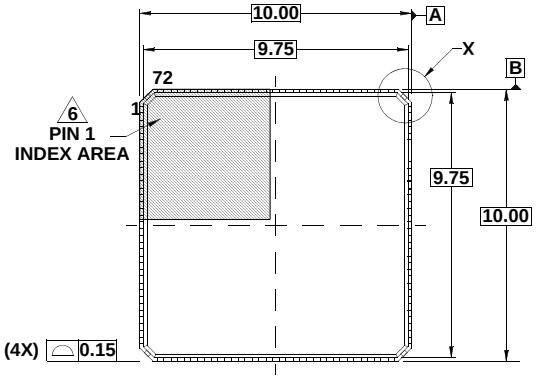
*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see www.intersil.com

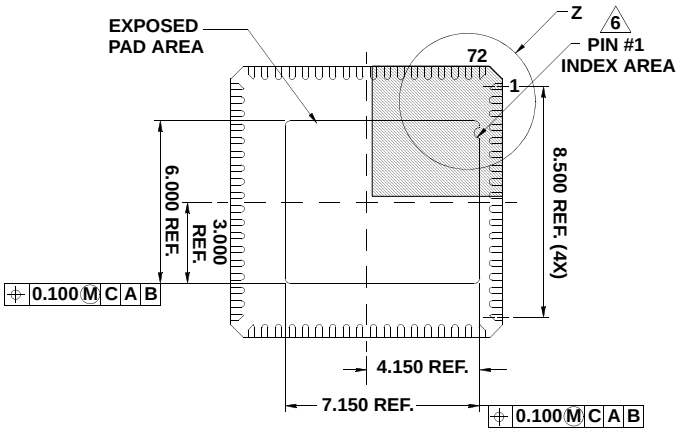
# Package Outline Drawing

## L72.10x10E

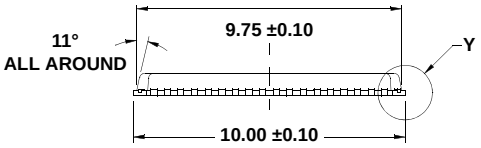
**72 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 0, 11/09**



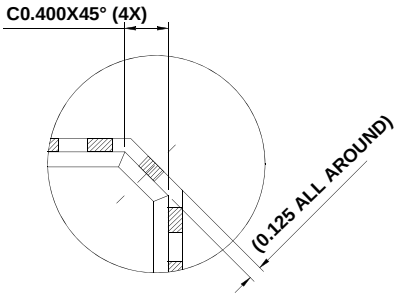

TOP VIEW



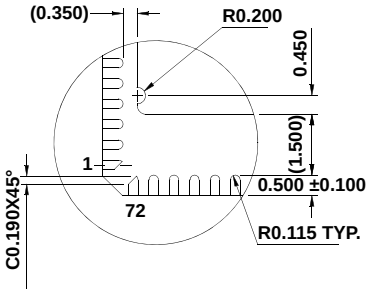

BOTTOM VIEW



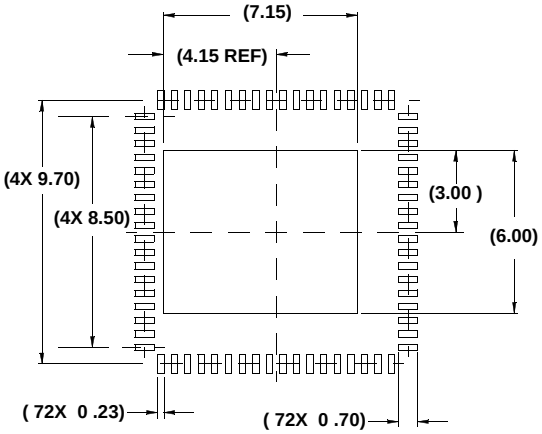

SIDE VIEW



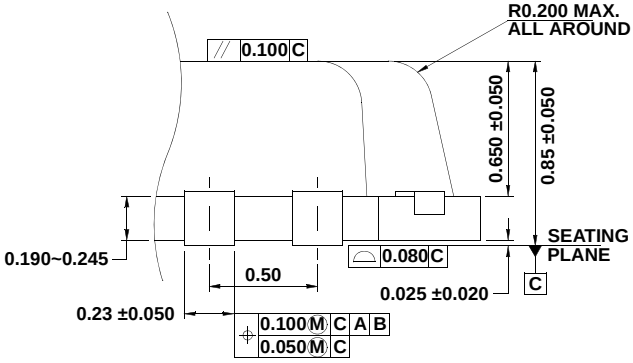

DETAIL "X"




DETAIL "Z"




TYPICAL RECOMMENDED LAND PATTERN




DETAIL "Y"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ANSI Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.10
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. Package outline compliant to JESD-M0220.