Low Input Voltage and High Efficiency, Synchronous Boost Converter with 1.3A Switch

ISL9113A

The ISL9113A provides a power supply solution for devices powered by three-cell alkaline, NiCd, NiMH, or one-cell Li-Ion/Li-Polymer batteries. It offers either a fixed 5V or an adjustable output option for USB-OTG or portable HDMI applications. The device is guaranteed to supply 500mA from a 3V input and 5V output, and has a typical 1.3A peak current limit. High 1.8MHz switching frequency allows for the use of tiny, low-profile inductors, and ceramic capacitors to minimize the size of the overall solution.

The ISL9113A is an internally compensated, fully integrated synchronous converter optimized for efficiency with minimal external components. At light load, the device enters Skip mode and consumes only 20µA of quiescent current, resulting in higher efficiency at light loads and maximum battery life.

The device is available in an 8 Ld DFN package.

Related Literature

- For a full list of related documents, visit our website
  - ISL9113A product page

Features

- Up to 95% efficiency at typical operating conditions
- Input voltage range: 0.8V to 4.7V
- Output current: Up to 500mA (V_{BAT} = 3.0V, V_{OUT} = 5.0V)
- Low quiescent current: 20µA (typical)
- Logic control shutdown (I_Q < 1µA)
- 1.2V EN high logic
- Output disconnect during shutdown
- Skip mode under light-load condition
- Undervoltage lockout
- Fault protection: OVP, OTP, short-circuit
- 8 Ld 2mmx2mm DFN Package

Applications

- Products including portable HDMI and USB-OTG
- Smartphones
- Tablet and mobile internet devices

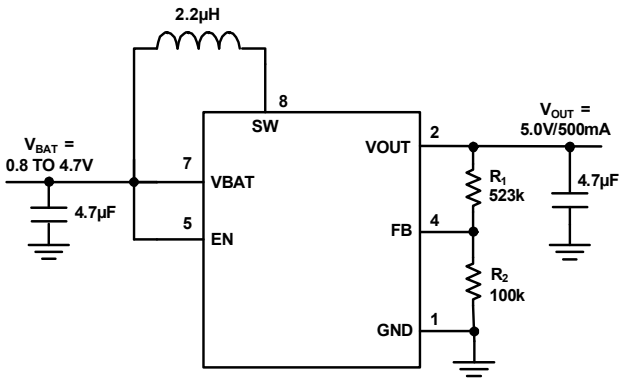


FIGURE 1. TYPICAL APPLICATION

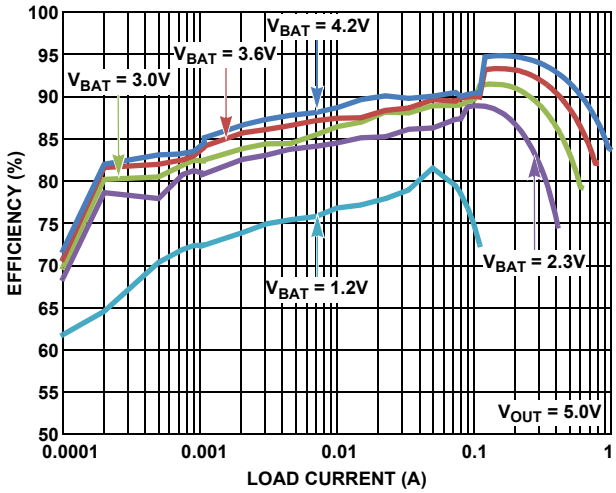


FIGURE 2. EFFICIENCY

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram

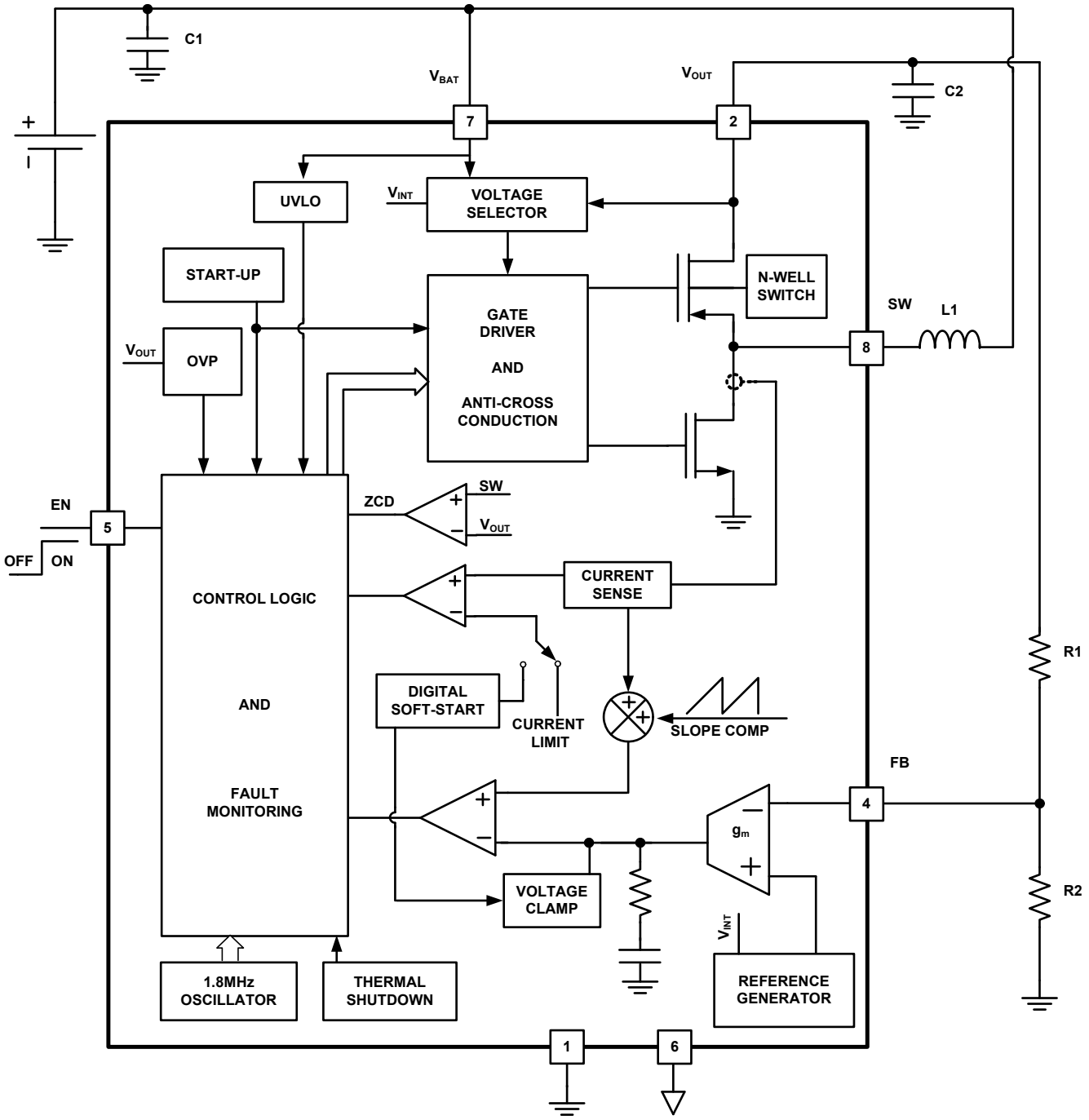
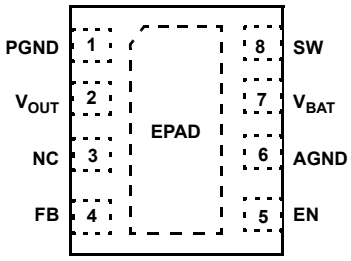


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL9113A
(8 LD DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	PGND	Power ground
2	V_{OUT}	Device output
3	NC	No connection
4	FB	Feedback pin of the converter. Connect voltage divider resistors between V_{OUT}, FB, and GND for desired output.
5	EN	The EN pin is an active-HIGH logic input for enabling the device. When asserted HIGH, the boost function begins. When asserted LOW, the device is completely disabled, and current is blocked from flowing from the SW pin to the output, and vice versa. This pin should be tied either HIGH to enable the device, or LOW to disable the device.
6	AGND	Analog ground
7	V_{BAT}	Device input supply from a battery. Connect a 4.7µF ceramic capacitor to the power ground.
8	SW	The SW pin is the switching node of the power converter. Connect one terminal of the inductor to the SW pin and the other to power input.
	EPAD	The exposed pad must be connected to PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the system GND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL9113AIRAZ-T	3AA	Adjustable	-40 to +85	6k	8 Ld DFN	L8.2x2D
ISL9113AIRAZ-EVZ	Evaluation Board for ISL9113AIRAZ-T					

NOTES:

1. Refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see device information page for ISL9113A. For more information on MSL see Tech Brief TB363.

Absolute Maximum Ratings

V_{BAT}, EN, V_{OUT} . . . . . -0.3V to 6.5V
SW Voltage
DC . . . . . -0.5V to 6.5V
Pulse <10ns . . . . . -0.5V to 8.0V
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 3kV
(Other ESD specifications should meet Level 1 requirement)
Latch-Up (Tested per JESD78; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 4, 5)	80	15

Junction Temperature Range . . . . . -40°C to+125°C
Operating Temperature Range . . . . . -40°C to+85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{BAT} (After start-up) . . . . . 0.8V to 4.7V
V_{OUT} . . . . . (V_{BAT} + 0.2V) to 5.2V
Ambient Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC} the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{BAT} = 3.0V, V_{OUT} = 5.0V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Start-Up Voltage	V_{MIN}	V_{EN} = V_{BAT}, R_{LOAD} = 50Ω		0.75	**0.90**	V
Input Undervoltage Lockout	V_{UVLO}	V_{EN} = V_{BAT}, R_{LOAD} = 50Ω	**0.66**	0.70	**0.76**	V
Feedback Voltage	V_{FB}		**784**	800	**816**	mV
Output Voltage	V_{OUT}	V_{BAT} = 2.8V	**3.0**		**5.2**	V
Feedback Pin Input Current		V_{FB} = 0.8V			**100**	nA
Quiescent Current from V_{OUT}	I_{Q1}	V_{BAT} = V_{EN} = 1.2V, no load (Note 7)		20	**45**	µA
Shutdown Current from V_{BAT}	I_{SD}	V_{EN} = 0V, V_{BAT} = 1.2V, V_O = 0		0.5	**2.8**	µA
Leakage Current at SW Pin		V_{EN} = 0V, V_{BAT} = 4.7V, V_O = 0			**1.0**	µA
N-Channel MOSFET ON-Resistance				0.20		Ω
P-Channel MOSFET ON-Resistance				0.35		Ω
N-Channel MOSFET Peak Current Limit	I_{PK}		**1.1**	1.3	**1.5**	A
Maximum Duty Cycle	D_{MAX}		**82**	87.5		%
PWM Switching Frequency	F_{OSC}		**1.5**	1.8	**2.0**	MHz
EN Logic High		2.5V < V_{BAT} < 4.7V	**1.2**			V
		V_{BAT} < 2.5V	**0.48*V_{BAT}**			V
EN Logic Low		2.5V < V_{BAT} < 4.7V			**0.35**	V
		V_{BAT} < 2.5V			**0.14*V_{BAT}**	V
Soft Start-Up Time		C_{OUT} = 4.7µF, L = 2.2µH		0.2	**1**	ms
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	I_{LOAD} = 0 to 50mA	**-1.5**		**+1.5**	%
Line Regulation		V_{BAT} = 3.0V to 3.6V, I_{LOAD} = 1mA	**-1.0**		**+1.0**	%
Output Overvoltage Protection Threshold				5.9		V
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
7. I_{Q1} is measured at V_{OUT} and multiplied by V_{OUT}/V_{BAT}; thus, the equivalent input quiescent current is calculated.

Detailed Description

Current Mode PWM Operation

The control scheme of the device is based on the peak current mode control and the control loop is compensated internally. The peak current of the N-channel MOSFET switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical current limit is set to 1.3A.

The control circuit includes a ramp generator, slope compensator, error amplifier, and a PWM comparator (see "Block Diagram" on page 2). The ramp signal is derived from the inductor current. This ramp signal is then compared to the error amplifier output to generate the PWM gating signals for driving both N-channel and P-channel MOSFETs. The PWM operation is initialized by the clock from the internal oscillator (typical 1.8MHz). The N-channel MOSFET is turned ON at the beginning of a PWM cycle, the P-channel MOSFET remains OFF, and the current starts ramping up. When the sum of the ramp and the slope compensator output reaches the error amplifier output voltage, the PWM comparator outputs a signal to turn OFF the N-channel MOSFET. Here, both MOSFETs remain OFF during the dead-time interval. Next, the P-channel MOSFET is turned ON and remains ON until the end of this PWM cycle. During this time, the inductor current ramps down until the next clock. At this point, following a short dead time, the N-channel MOSFET is again turned ON, repeating as previously described.

Skip Mode Operation

The boost converter is capable of operating in two different modes. When the inductor current is sensed to cross zero for eight consecutive times, the converter enters Skip mode. In Skip mode, each pulse cycle is still synchronized by the PWM clock. The N-channel MOSFET is turned ON at the rising edge of the clock and turned OFF when the inductor peak current reaches typically 25% of the current limit. Then, the P-channel MOSFET is turned ON, and it stays ON until its current goes to zero. Subsequently, both N-channel and P-channel MOSFETs are turned OFF until the next clock cycle starts, at which time the N-channel MOSFET is turned ON again. When V_{OUT} is 1.5% higher than the nominal output voltage, the N-channel MOSFET is immediately turned OFF, and the P-channel MOSFET is turned ON until the inductor current goes to zero. The N-channel MOSFET resumes operation when V_{FB} falls back to its nominal value, repeating the previous operation. The converter returns to 1.8MHz PWM mode operation when V_{FB} drops 1.5% below its nominal voltage.

Given the Skip mode algorithm incorporated in the ISL9113A, the average value of the output voltage is approximately 0.75% higher than the nominal output voltage under PWM operation. This positive offset improves the load transient response when switching from Skip mode to PWM mode operation. The ripple on the output voltage is typically $1.5\% * V_{OUT}$ (nominal) when input voltage is sufficiently lower than output voltage, and it increases as the input voltage approaches the output voltage.

Synchronous Rectifier

The ISL9113A integrates one N-channel MOSFET and one P-channel MOSFET to realize a synchronous boost converter.

Because the commonly used discrete Schottky rectifier is replaced with the low $r_{DS(ON)}$ P-channel MOSFET, the power conversion efficiency reaches a value above 90%. Since a typical step-up converter has a conduction path from the input to the output via the body diode of the P-channel MOSFET, a special circuit (see "Block Diagram" on page 2) is used to reverse the polarity of the P-channel body diode when the device is shut down. Thus, this configuration completely disconnects the load from the input during shutdown of the converter. The benefit of this feature is that the battery will not be completely depleted during shutdown of the converter. No additional components are needed to disconnect the battery from the output of the converter.

Soft-Start

The soft start-up duration is the time between the device being enabled and V_{OUT} rising to within 3% of target voltage. When the device is enabled, the start-up cycle starts with a linear phase. During the linear phase, the rectifying switch is turned ON in a current limited configuration, delivering about 350mA, until the output capacitor is charged to approximately 90% of the input voltage. At this point, PWM operation begins in Boost mode. If the output voltage is below 2.3V, PWM switching is done at a fixed duty-cycle of 75% until the output voltage reaches 2.3V. When the output voltage exceeds 2.3V, the closed-loop current mode PWM loop overrides the duty cycle until the output voltage is regulated. Peak inductor current is ramped to the final value (typically 1.3A) during the soft-start period to limit inrush current from the input source. Fault monitoring begins approximately 2ms after the device is enabled.

Over-Temperature Protection (OTP)

The device offers over-temperature protection. A temperature sensor circuit is integrated and monitors the internal IC temperature. Once the temperature exceeds the preset threshold (typically +150°C), the IC shuts down immediately. The OTP has a typical hysteresis of +25°C. When the device temperature decreases by this, the device starts operating.

Printed Circuit Board Layout Recommendations

The ISL9113A is a high-frequency, switching boost converter. Accordingly, the converter has fast voltage change and high switching current that may cause EMI and stability issues if the layout is not done properly. Therefore, careful layout is critical to minimize the trace inductance and reduce the area of the power loop.

Power components, such as input capacitor, inductor, and output capacitor, should be placed close to the device. Board traces that carry high switching current should be routed wide and short. A solid power ground plane is important for EMI suppression.

The switching node (SW pin) of the converter and the traces connected to this pin are very noisy. Noise sensitive traces, such as the FB trace, should be kept away from SW node. The voltage divider should be placed close to the FB pin to prevent noise pickup. Figure 4 on page 6 shows the recommended PCB layout.

In the 8 Ld DFN package, the heat generated in the device is mainly dissipated through the thermal pad. Maximizing the

copper area connected to the thermal pad is preferable. It is recommended to add at least four vias within the pad to the GND plane for the best thermal relief.

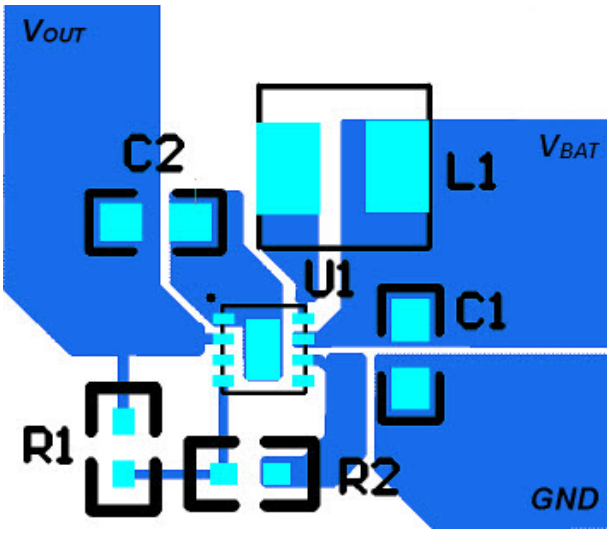


FIGURE 4. RECOMMENDED PCB LAYOUT

Output Voltage Setting Resistor Selection

Resistors R_1 and R_2, shown in the "Block Diagram" on page 2, can be used to set the desired output voltage values using Equation 1:

$$V_{OUT} = V_{FB} \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

where V_{FB} is the internal FB reference voltage (0.8V typical). The current flowing through the divider resistors is calculated as $V_{OUT}/(R_1 + R_2)$. Large resistance is recommended to minimize current into the divider, and thus improve the total efficiency of the converter. R_1 and R_2 should be placed close to the FB pin of the device to prevent noise pickup.

Inductor Selection

An inductor with core material suitable for high-frequency applications (e.g., ferrite) is desirable to minimize core loss and improve efficiency. The inductor should have a low ESR to reduce copper loss. Moreover, the inductor saturation current should be higher than the maximum peak current of the device; i.e., 1.5A.

The device is designed to operate with an inductor value of 2.2µH to provide stable operation across the range of load, input, and output voltages. Stable mode switching between PWM and Skip mode operation is guaranteed at this inductor value. Table 1 shows recommended inductors.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	PART NUMBER	DIMENSIONS - W x L x H (mm)
Murata	LQH32PN2R2NN0L	3.2 x 2.5 x 1.7 (maximum)
Toko	1239AS-H-2R2M	2.5 x 2.0 x 1.2 (maximum)
	1286AS-H-2R2M	2.0 x 1.6 x 1.2 (maximum)
TDK	TFM201610A-2R2M	2.0 x 1.6 x 1.0 (maximum)
Cyntec	PSE25201B-2R2MS	2.0 x 1.6 x 1.2 (maximum)

Capacitor Selection

INPUT CAPACITOR

A minimum of a 4.7µF ceramic capacitor is recommended to provide stable operation under typical operating conditions. For input voltage less than 1.0V application, an additional 4.7µF ceramic capacitor is recommended for better noise filtering and EMI suppression. The input capacitor should be placed close to the input pin, GND pin, and the non-switching terminal of the inductor.

OUTPUT CAPACITOR

For the output capacitor, a ceramic capacitor with small ESR is recommended to minimize output voltage ripple. A typical 4.7µF should be used to provide stable operation at different typical operating conditions. The output capacitor should be placed close to the output pin and GND pin of the device. Table 2 shows the recommended capacitors.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

TABLE 3. FAULT DETECTION AND RESPONSE

FAULT CONDITION	DETECTION DETAILS	ACTION
Low Battery Voltage	V_{BAT} < 0.7V	Shut down until V_{EN} or V_{BAT} is cycled.
V_{OUT} Out of Regulation	V_{OUT} is 10% below the target output voltage	Shut down only if V_{BAT} and V_{OUT} fall below 2.1V. Device automatically restarts after 200ms.
Short-Circuit	V_{OUT} falls below V_{BAT}	Shut down immediately. Device automatically restarts after 200ms.
Over-Temperature Protection	Die temperature is > +150°C	Switching stops. Device automatically restarts when temperature decreases to +125°C.
Output Overvoltage Protection	V_{OUT} > 5.9V	Switching stops until EN pin is toggled or power is cycled.

Typical Characteristics

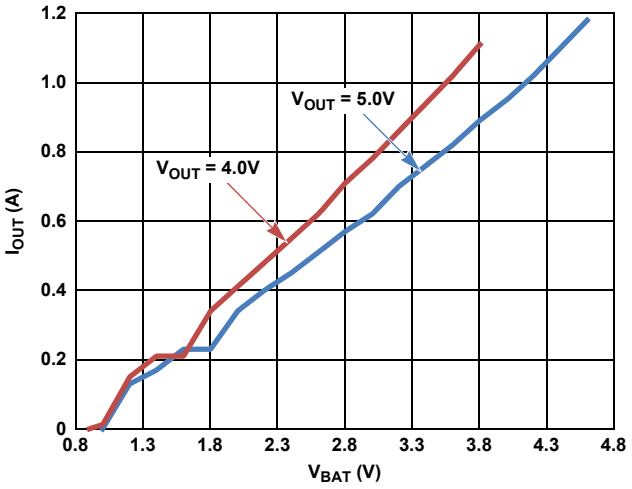


FIGURE 5. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

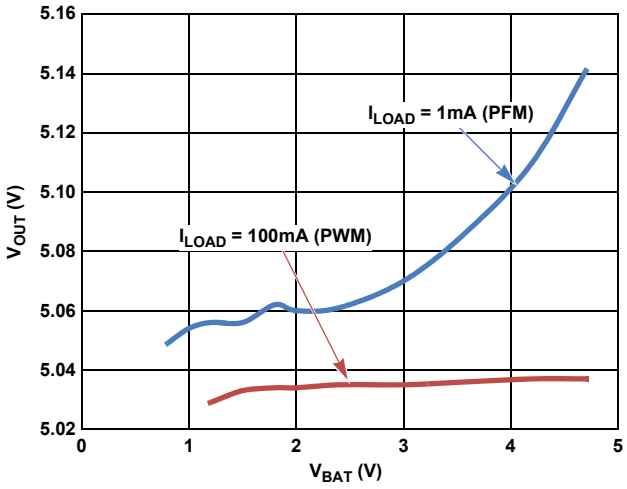


FIGURE 6. LINE REGULATION, V_{OUT} = 5V

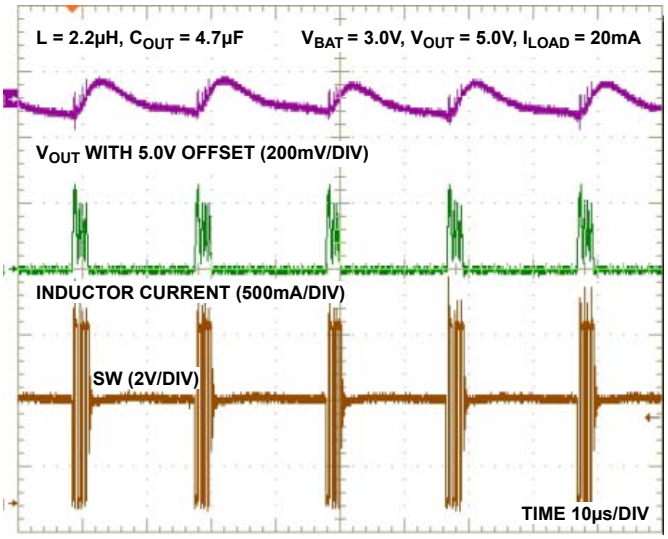


FIGURE 7. PULSE SKIP MODE WAVEFORM

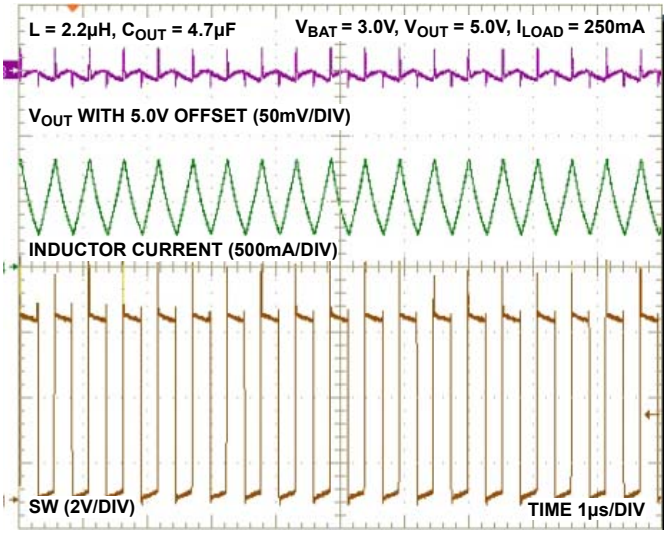


FIGURE 8. PWM WAVEFORM

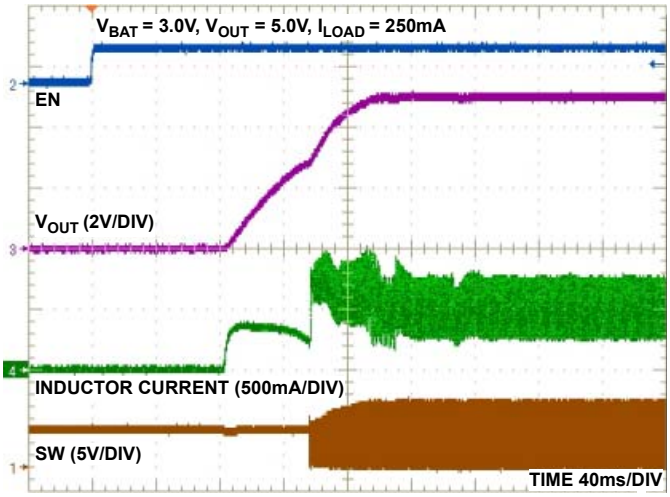


FIGURE 9. START-UP AFTER ENABLE (I_{LOAD} = 250mA)

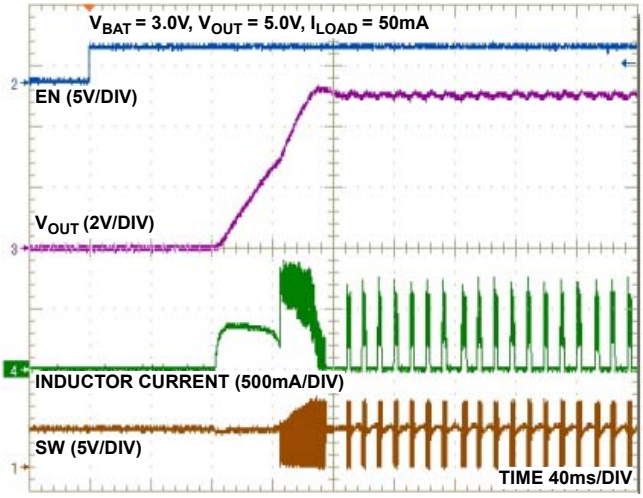


FIGURE 10. START-UP AFTER ENABLE (I_{LOAD} = 50mA)

Typical Characteristics (Continued)

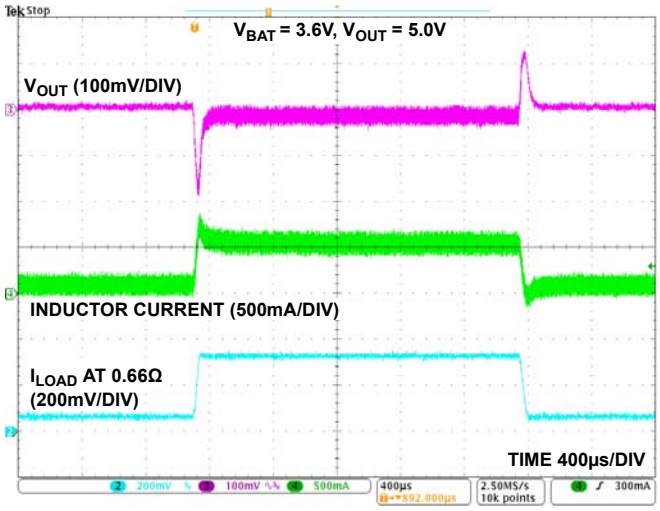


FIGURE 11. LOAD TRANSIENT RESPONSE (100mA TO 500mA)

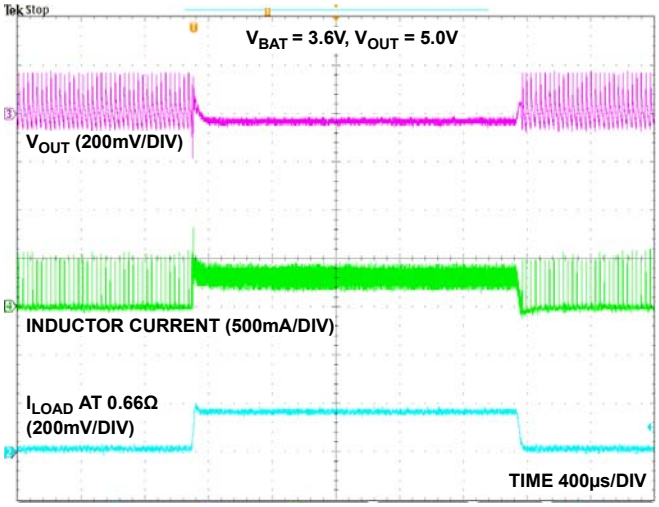


FIGURE 12. LOAD TRANSIENT RESPONSE (20mA TO 250mA)

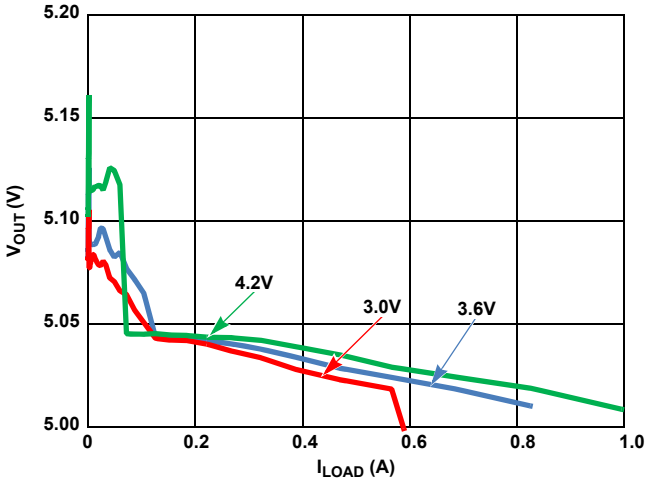


FIGURE 13. LOAD REGULATION

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 4, 2017	FN8620.1	On page 1: Figure 1, improved diagram to make it more readable. Updated Related Literature section to new standard. On page 10, updated POD from rev 0 to rev 1. Changes: Tiebar Note 5 updated From: "Tiebar shown (if present) is a non-functional feature." To: "Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)."
December 19, 2013	FN8620.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

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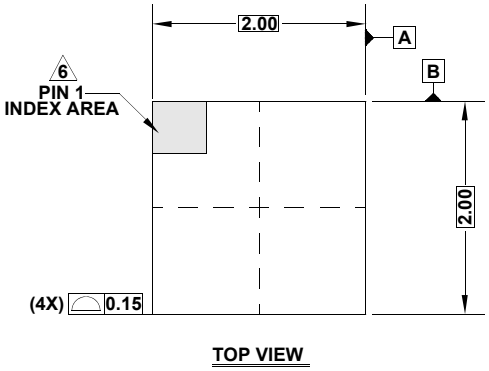
Package Outline Drawing

For the most recent package outline drawing, see L8.2x2D.

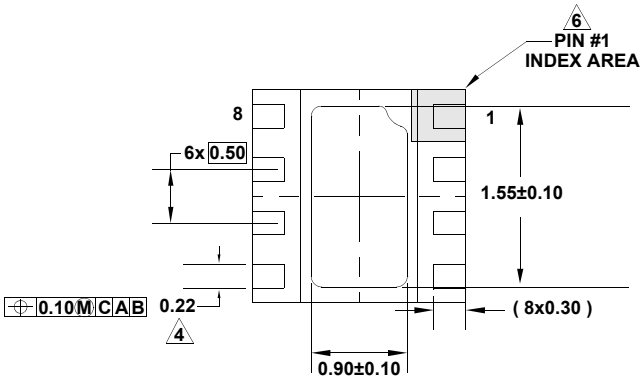
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

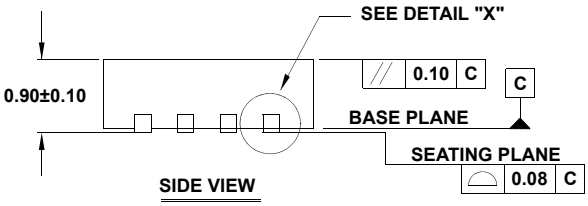
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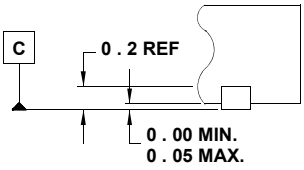
TOP VIEW



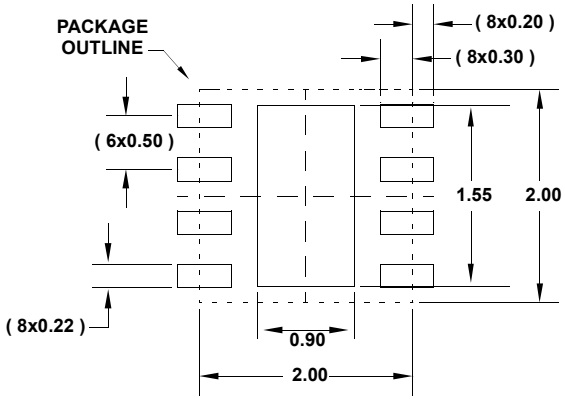
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.