ISL89410, ISL89411, ISL89412

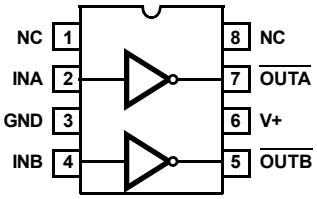
High Speed, Dual Channel Power MOSFET Drivers

FN6798
Rev 2.00
October 16, 2015

The ISL89410, ISL89411, ISL89412 ICs are similar to the EL7202, EL7212, EL7222 series but with greater VDD ratings. These are very high speed matched dual drivers capable of delivering peak currents of 2.0A into highly capacitive loads. The high speed performance is achieved by means of a proprietary “Turbo-Driver” circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10-fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

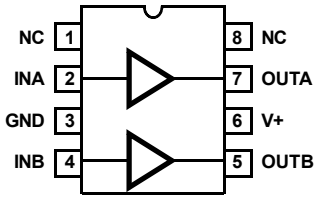
Pinouts

ISL89411
(8 LD PDIP, SOIC)
TOP VIEW



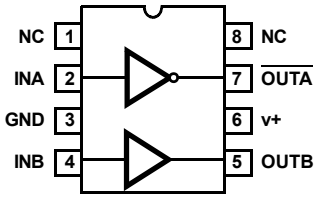
INVERTING DRIVERS

ISL89410
(8 LD PDIP, SOIC)
TOP VIEW



NON-INVERTING DRIVERS

ISL89412
(8 LD PDIP, SOIC)
TOP VIEW



COMPLEMENTARY DRIVERS

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Features

- Industry Standard Driver Replacement
- Improved Response Times
- Matched Rise and Fall Times
- Reduced Clock Skew
- Low Output Impedance
- Low Input Capacitance
- High Noise Immunity
- Improved Clocking Rate
- Low Supply Current
- Wide Operating Voltage Range
- Pb-Free Available (RoHS compliant)

Applications

- Clock/line Drivers
- CCD Drivers
- Ultra-Sound Transducer Drivers
- Power MOSFET Drivers
- Switch Mode Power Supplies
- Class D Switching Amplifiers
- Ultrasonic and RF Generators
- Pulsed Circuits

Pin Descriptions

SYMBOL	PIN DESCRIPTIONS
V_+	Power voltage from 4.5V to 18V.
GND	Power voltage return
INA, INB	Logic inputs.
$\overline{\text{OUTA}}$ OUTA	Non-inverted ouput for ISL89410. Inverted output for ISL89411 and ISL89412.
$\overline{\text{OUTB}}$ OUTB	Non-inverted output for ISL89410 and ISL89412. Inverted output for ISL89411.
NC	These pins must be left unconnected.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL89410IPZ (Note) **(No longer available, recommended replacement: ISL89410IBZ)**	89410 IPZ	-40 to +85	8 Ld PDIP** (Pb-free)	E8.3

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL89410IBZ (Note)	89410 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
ISL89410IBZ-T13* (Note)	89410 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	M8.15E
ISL89411IPZ (Note)	ISL 89411IPZ	-40 to +85	8 Ld PDIP** (Pb-free)	E8.3
ISL89411IBZ (Note)	89411 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
ISL89411IBZ-T13* (Note)	89411 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	M8.15E
ISL89412IPZ **(No longer available, recommended replacement: ISL89412IBZ)**	89412 IPZ	-40 to +85	8 Ld PDIP** (Pb-free)	E8.3
ISL89412IBZ (Note)	89412 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
ISL89412IBZ-T13* (Note)	89412 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	M8.15E

*Please refer to TB347 for details on reel specifications.

**Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply (V+ to GND) 19.0V
Input Pins . . . . . -0.3V to +0.3V above V+
Combined Peak Output Current 4A

Maximum Recommended Operating Conditions

Recommended Operating V+ Range . . . . . 4.5V to 18.0V
Input Pins . . . . . 0V to V+

Thermal Information

Operating Junction Temperature . . . . . +125°C
Power Dissipation
8 Ld SOIC 570mW
8 Ld PDIP* 1050mW
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

T_A = +25°C, V = 18V unless otherwise specified; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IH}	Logic “1” Input Voltage		2.4			V
I_{IH}	Logic “1” Input Current	@V+		0.1	10	µA
V_{IL}	Logic “0” Input Voltage				0.8	V
I_{IL}	Logic “0” Input Current	@0V		0.1	10	µA
V_{HVS}	Input Hysteresis			0.3		V
OUTPUT						
R_{OH}	Pull-Up Resistance	I_{OUT} = -100mA		3	6	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100mA		4	6	Ω
I_{PK}	Peak Output Current	Source		2		A
		Sink		2		A
I_{DC}	Continuous Output Current	Source/Sink	100			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs High/ISL89410		4.5	7.5	mA
		Inputs High/ISL89411		1	2.5	mA
		Inputs High/ISL89412		2.5	5.0	mA
V_S	Operating Voltage		4.5		18	V

AC Electrical Specifications

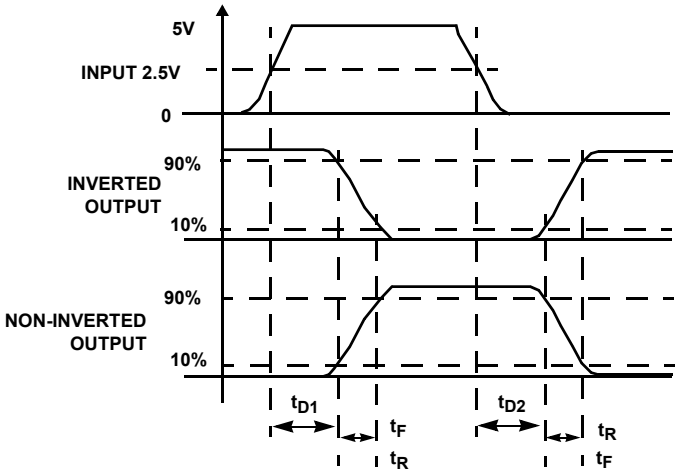
T_A = +25°C, V = 18V unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_R	Rise Time (Note 1)	C_L = 500pF		7.5		ns
		C_L = 1000pF		10	20	ns
t_F	Fall Time (Note 1)	C_L = 500pF		10		ns
		C_L = 1000pF		13	20	ns
t_{D1}	Turn-On Delay Time (Note 1)	See “Timing Table” on page 4		18	25	ns
t_{D2}	Turn-Off Delay Time (Note 1)	See“Timing Table” on page 4		20	25	ns

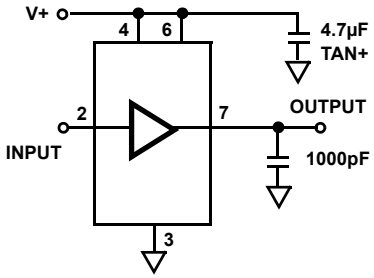
NOTE:

1. Limits established by characterization and are not production tested.

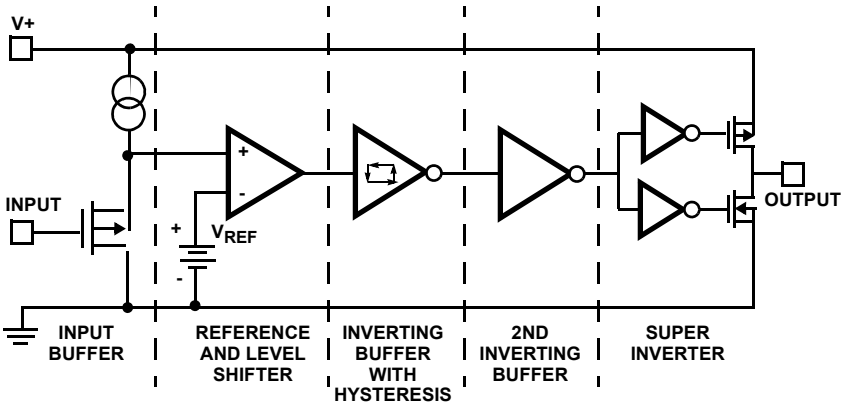
Timing Table



Standard Test Configuration



Simplified Schematic



Typical Performance Curves

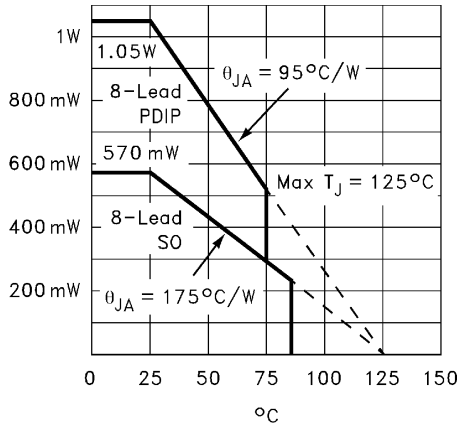


FIGURE 1. MAX POWER/DERATING CURVES

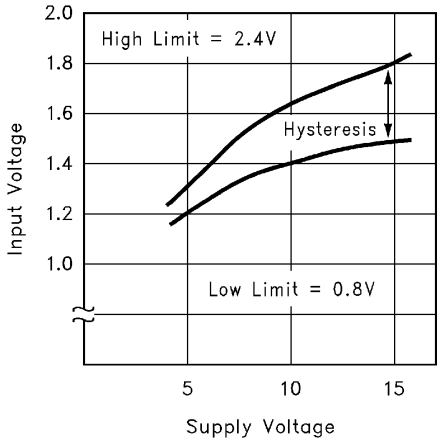


FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

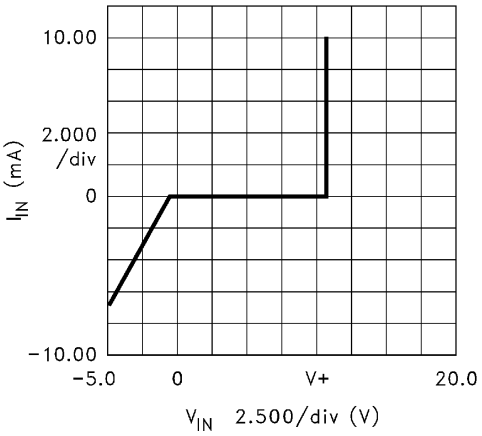


FIGURE 3. INPUT CURRENT vs VOLTAGE

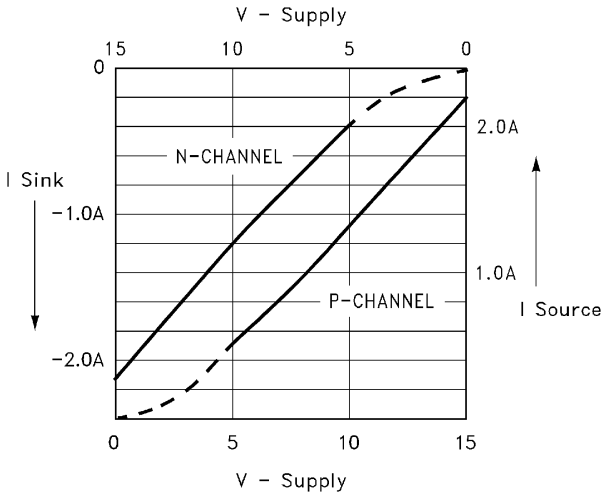
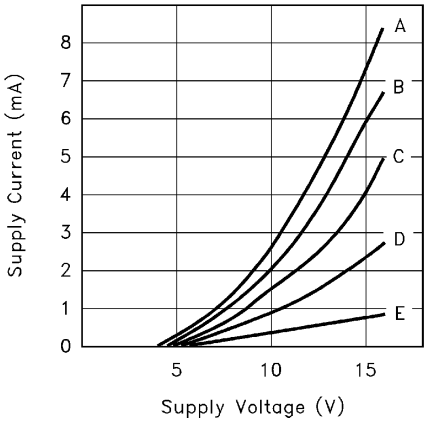


FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE



CASE:

Device	Input Level	Curve
ISL89410	GND	A
	GND, V+	B
	V+	C
ISL89411	GND	C
	GND, V+	D
	V+	E
ISL89412	GND	B
	GND, V+	C
	V+	D

FIGURE 5. QUIESCENT SUPPLY CURRENT

Typical Performance Curves (Continued)

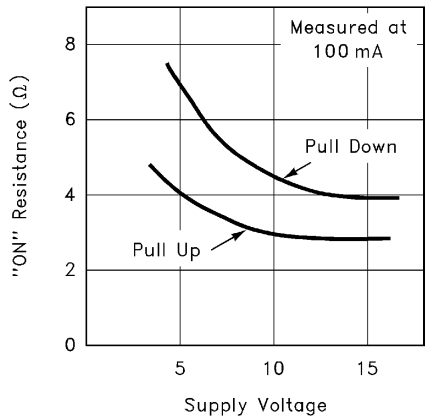


FIGURE 6. "ON" RESISTANCE vs SUPPLY VOLTAGE

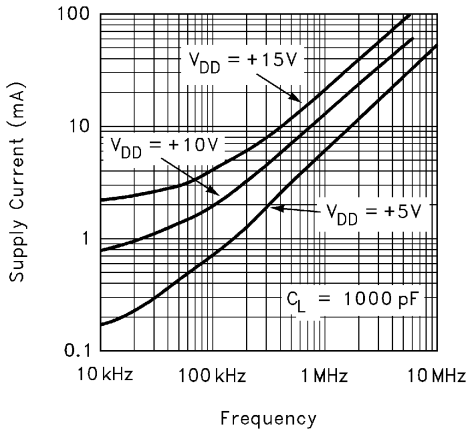


FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY

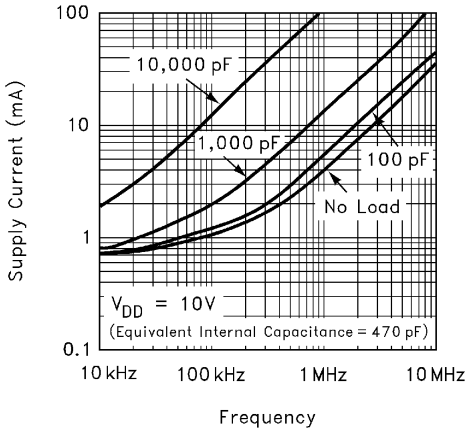


FIGURE 8. AVERAGE SUPPLY CURRENT vs CAPACITIVE LOAD

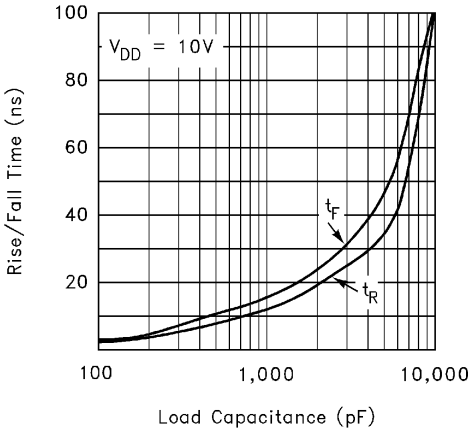


FIGURE 9. RISE/FALL TIME vs LOAD

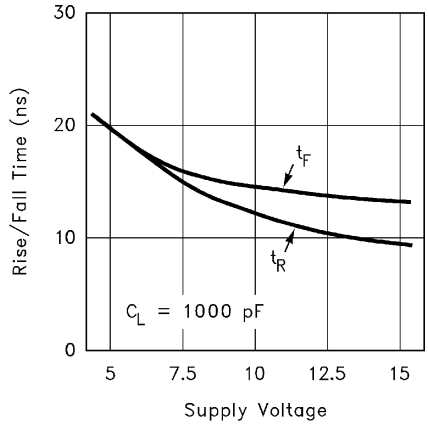


FIGURE 10. RISE/FALL TIME vs SUPPLY VOLTAGE

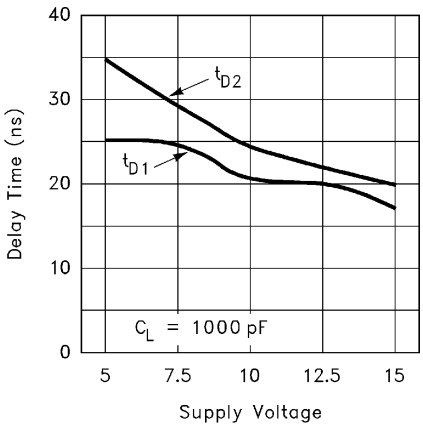


FIGURE 11. PROPAGATION DELAY vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

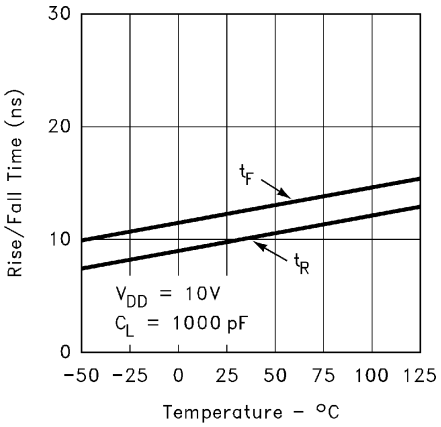


FIGURE 12. RISE/FALL TIME vs TEMPERATURE

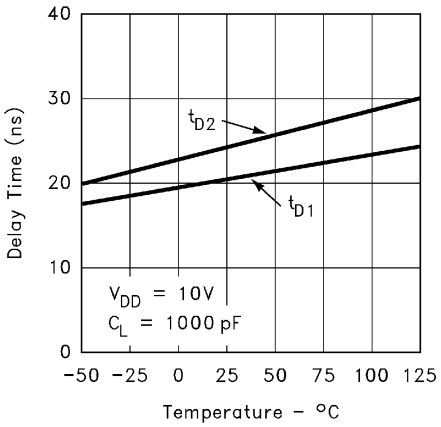
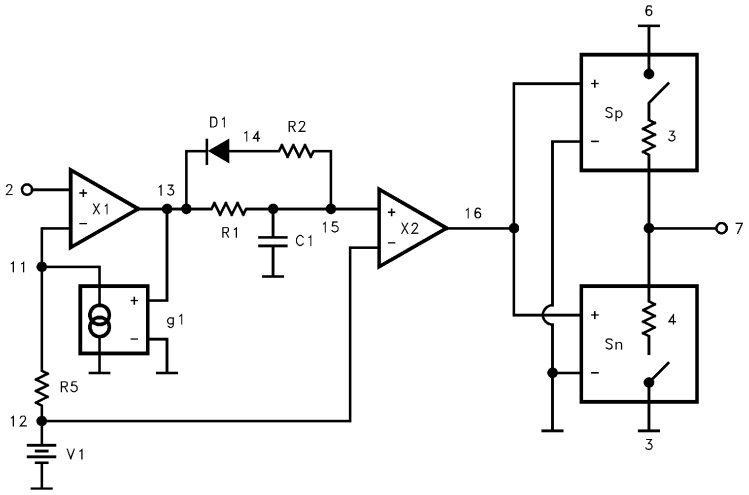


FIGURE 13. DELAY vs TEMPERATURE

ISL89411 Macro Model



**** ISL89411 Model ****

```
*                    input
*                    |     gnd
*                    |     |     Vsupply
*                    |     |     |     Vout
.subckt M89411 2     3     6     7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938µ
.model dmod d
.model spmod vswitch ron3 roff2meg von1 voff1.5
.model snmod vswitch ron4 roff2meg von3 voff2
.ends M89411
```

```
.subckt comp1 out inp inm vss
e1 out vss table { (v(inp) v(inm))* 5000}   (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
```

Application Guidelines

It is important to minimize inductance to the power FET by keeping the output drive current loop as short as possible. Also, the decoupling capacitor, Cq, should be a high quality ceramic capacitor with a Q that should be a least 10x the gate Q of the power FET. A ground plane under this circuit is also recommended.

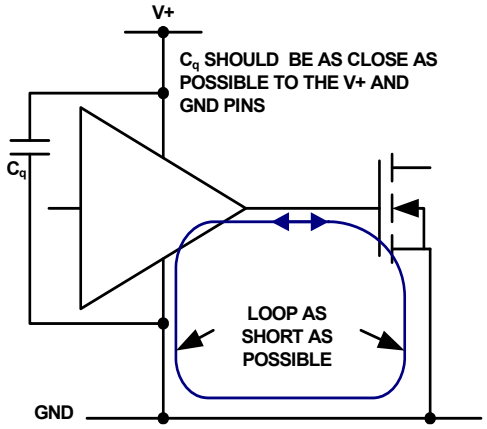


FIGURE 14. RECOMMENDED LAYOUT METHODS

In applications where it is difficult to place the driver very close to the power FET (which may result with excessive parasitic inductance), it then may be necessary to add an external gate resistor to dampen the inductive ring. If this resistor must be too large in value to be effective, then as an alternative, Schottky diodes can be added to clamp the ring voltage to V+ or GND.

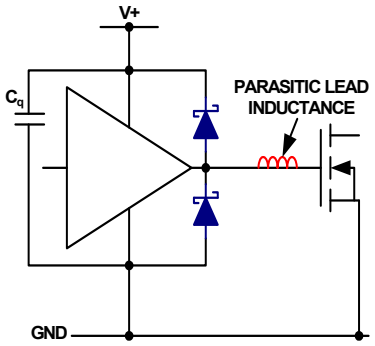


FIGURE 15. SUGGESTED CONFIGURATION FOR DRIVING INDUCTIVE LOADS

Where high supply voltage operation is required (15V to 18V), input signals with a minimum of 3.3V input drive is suggested and a minimum rise/fall time of 100ns. This is recommended to minimize the internal bias current power dissipation.

Excessive power dissipation in the driver can result when driving highly capacitive FET gates at high frequencies. These gate power losses are defined by Equation 1:

$$P = 2 \bullet Q_C \bullet V_{gs} \bullet f_{SW} \quad \text{(EQ. 1)}$$

where:

P = Power
Q_C = Charge of the Power FET at V_{gs}
V_{gs} = Gate drive voltage (V+)
f_{SW} = switching Frequency

Adding a gate resistor to the output of the driver will transfer some of the driver dissipation to the resistor. Another possible solution is to lower the gate driver voltage which also lowers Q_C.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 16, 2015	FN6798.2	Updated Ordering Information Table on page 1. Added Revision History and About Intersil sections. Updated POD MDP0027 to M8.15E.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

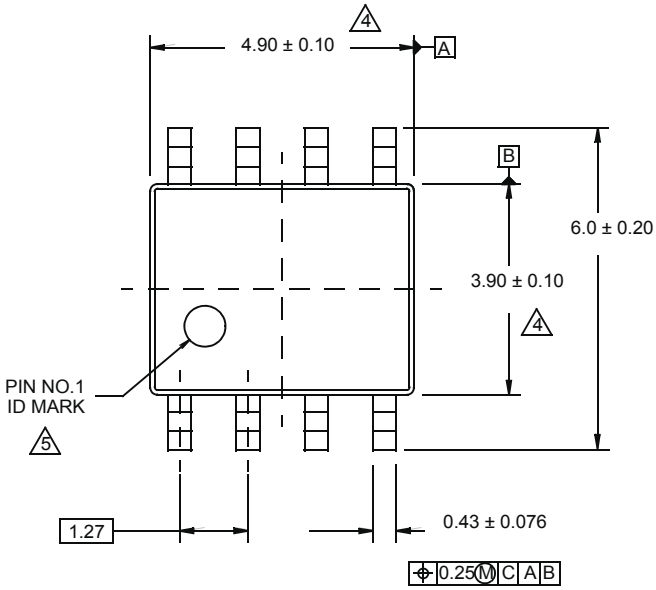
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

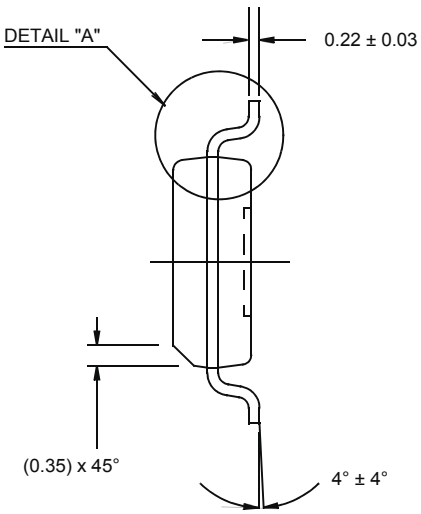
Package Outline Drawing

M8.15E

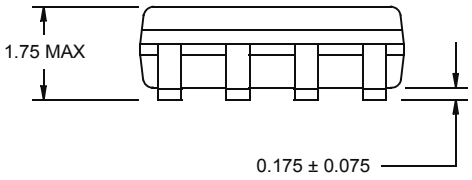
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



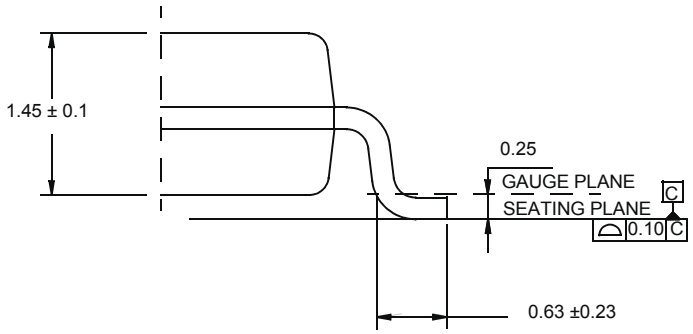
TOP VIEW



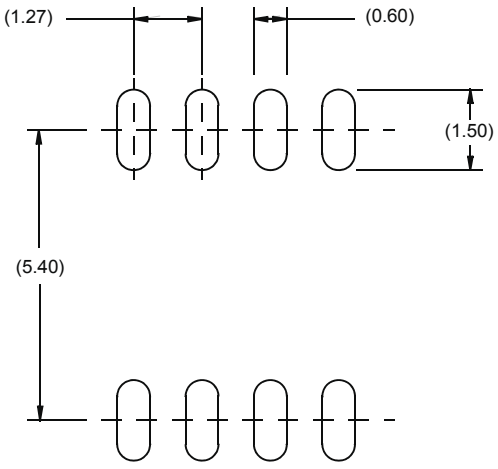
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"

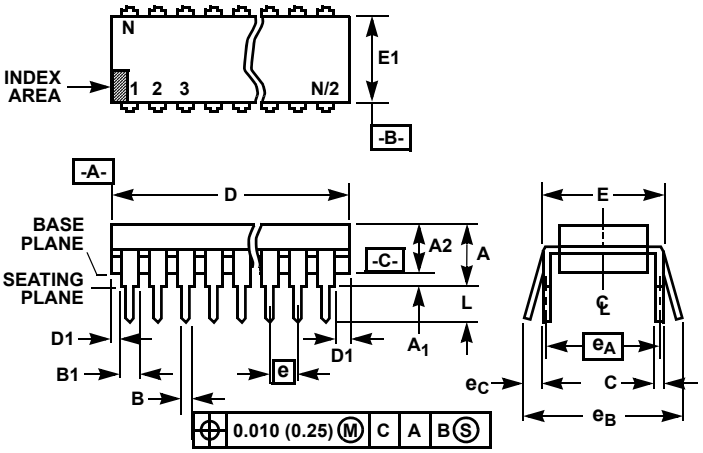


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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