5V, 30Mbps, RS-485/RS-422 Transceiver

The Intersil ISL81485 is a BiCMOS, 5V powered, single transceiver that meets both the RS-485 and RS-422 standards for balanced communication, and features a larger output voltage and higher data rate to benefit high speed applications.

Unlike competitive devices, this Intersil transceiver is specified for 10% tolerance supplies (4.5V to 5.5V), and it delivers a much larger worst case differential output voltage (2.0V compared to the typical 1.5V) over the full supply range. The increased output voltage translates into longer reach, or better data integrity, at the 30Mbps data rate.

This device presents a “1 unit load” to the RS-485 bus, which allows up to 32 transceivers on the network.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

Driver (Tx) outputs are short circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL81485IB (81485IB)	-40 to 85	8 Ld SOIC	M8.15
ISL81485IB-T (81485IB)	-40 to 85	8 Ld SOIC (Tape and Reel)	M8.15
ISL81485IU (1485)	-40 to 85	8 Ld MSOP	M8.118
ISL81485IU-T (1485)	-40 to 85	8 Ld MSOP (Tape and Reel)	M8.118

Features

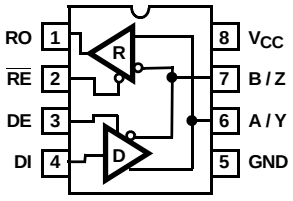
- Specified for 10% Tolerance Supplies
- High Data Rates. . . . . up to 30Mbps
- Large Differential Output Voltage. . . . 2.0V(min.) into 54Ω
- Drop-In Replacement for the ADM1485
- One Unit Load Allows up to 32 Devices on the Bus
- Low Quiescent Current 800μA
- -7V to +12V Common Mode Input Voltage Range
- Three State Rx and Tx Outputs
- 15ns (Max) Propagation Delays, 5ns (Max) Skew
- Operates from a Single +5V Supply (10% Tolerance)
- Current Limiting and Thermal Shutdown for driver Overload Protection

Applications

- SCSI “Fast 20” Drivers and Receivers
- Factory Automation
- Field Bus Networks
- Security Networks
- Building Environmental Control Systems
- Industrial/Process Control Networks

Pinout

ISL81485 (SOIC, MSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright © Intersil Americas Inc. 2003. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

Truth Table

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B / Z	A / Y
X	1	1	0	1
X	1	0	1	0
X	0	X	High-Z	High-Z

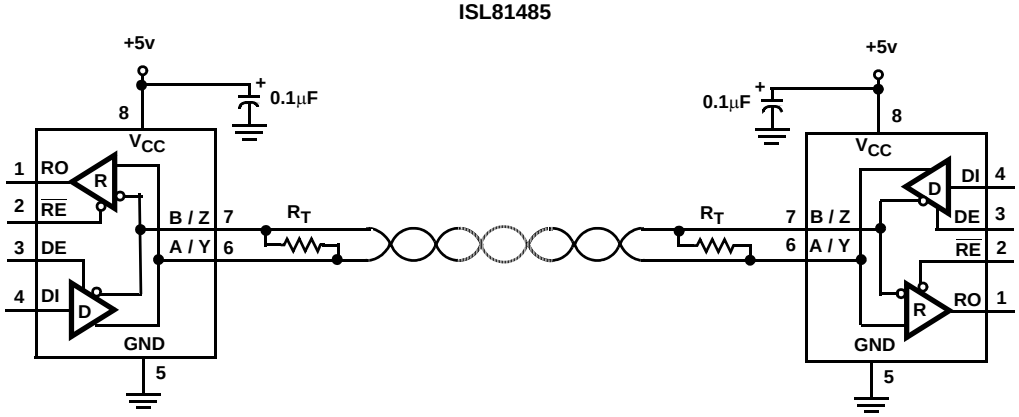
Truth Table

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs Open	1
1	X	X	High-Z

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A > B by at least 0.2V, RO is high; If A < B by 0.2V or more, RO is low; RO = High if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	RS-485/422 level, noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
B/Z	RS-485/422 level, inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
V_{CC}	System power supply input (4.5V to 5.5V).

Typical Operating Circuit



Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.5V to 7V
Input / Output Voltages
A/Y, B/Z . . . . . -8V to +12.5V
RO . . . . . -0.5V to (V_{CC} +0.5V)
Short Circuit Duration
Y, Z. . . . . Continuous

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{O}C/W)
8 Ld SOIC Package	105
8 Ld MSOP Package	140

Maximum Junction Temperature (Plastic Package) . . . . . 150^{O}C
Maximum Storage Temperature Range . . . . . -65^{O}C to 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{O}C
(Lead Tips Only)

Operating Conditions

Temperature Range
ISL81485IX. . . . . -40^{O}C to 85^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = 25^{O}C, Note 2

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (^{O}C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R = 50Ω (RS-422) (Figure 1A)		Full	2.5	3	-	V
		R = 27Ω (RS-485) (Figure 1A)		Full	2	2.5	5	V
		R_D = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 1B)		Full	1.5	-	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω (Figure 1A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω (Figure 1A)		Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω (Figure 1A)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	-1	-	1	µA
Input Current (A/Y, B/Z) (Note 5)	I_{IN2}	DE = 0V, V_{CC} = 0V or 4.5 to 5.5V	V_{IN} = 12V	Full	-	-	1	mA
			V_{IN} = -7V	Full	-0.8	-	-	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	40	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	4	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-	-	±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	12	-	-	kΩ
No-Load Supply Current, Note 3	I_{CC}	DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	1	2.2	mA
			DE = 0V	Full	-	0.8	1	mA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 4)		Full	60	-	250	mA

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = 25°C, Note 2 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Receiver Short-Circuit Current	I_{OSR}	$0V \le V_O \le V_{CC}$	Full	7	-	85	mA
SWITCHING CHARACTERISTICS							
Driver Input to Output Prop Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	2	9	15	ns
Driver Prop Delay Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	1	5	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	5	15	ns
Driver Enable to Output High	t_{ZH}	C_L = 50pF, SW = GND (Figure 3)	Full	-	9	25	ns
Driver Enable to Output Low	t_{ZL}	C_L = 50pF, SW = V_{CC} (Figure 3)	Full	-	9	25	ns
Matched Enable Switching $\lvert t_{AZH} - t_{BZL} \rvert$ or $\lvert t_{BZH} - t_{AZL} \rvert$	Δt_{EN}	(Figure 3)	Full	-	1	3	ns
Driver Disable from Output High	t_{HZ}	C_L = 50pF, SW = GND (Figure 3)	Full	-	9	25	ns
Driver Disable from Output Low	t_{LZ}	C_L = 50pF, SW = V_{CC} (Figure 3)	Full	-	9	25	ns
Matched Disable Switching $\lvert t_{AHZ} - t_{BLZ} \rvert$ or $\lvert t_{BHZ} - t_{ALZ} \rvert$	Δt_{DIS}	(Figure 3)	Full	-	2	5	ns
Driver Maximum Data Rate	f_{MAXD}	$\lvert V_{OD} \rvert \ge 1.5V$ (Figure 4)	Full	30	-	-	Mbps
Receiver Input to Output Prop Delay	t_{PLH}, t_{PHL}	(Figure 5)	Full	8	17	30	ns
Receiver Prop Delay Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 5)	Full	-	1	5	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND (Figure 6)	Full	-	7	20	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	7	20	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND (Figure 6)	Full	-	7	20	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	7	20	ns
Receiver Maximum Data Rate	f_{MAXR}	C_L = 15pF, $V_{ID} \ge 1.5V$, RO t_H and $t_L \ge$ 20ns	Full	30	-	-	Mbps

NOTES:

2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
3. Supply current specification is valid for loaded drivers when DE = 0V.
4. Applies to peak current. See “Typical Performance Curves” for more information.
5. Devices meeting these limits are denoted as “1 unit load (UL)” transceivers. The RS-485 standard allows up to 32 Unit Loads on the bus, so a 1UL transceiver permits > 32 devices on the bus.

Test Circuits and Waveforms

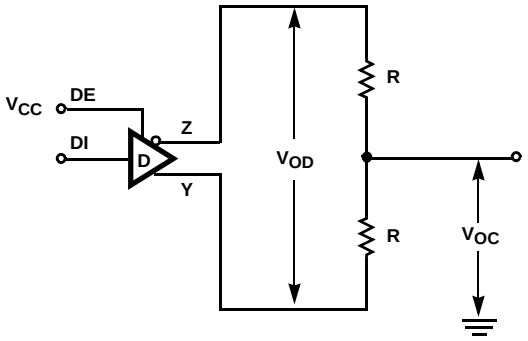


FIGURE 1A. V_{OD} AND V_{OC}

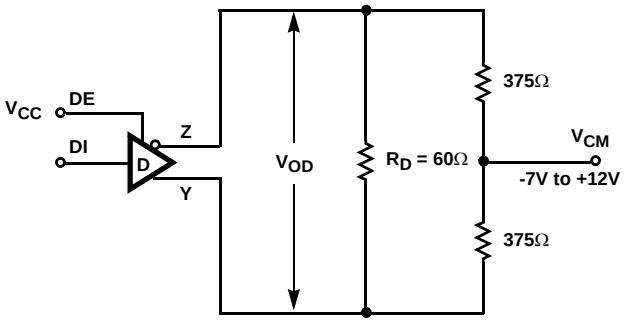


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

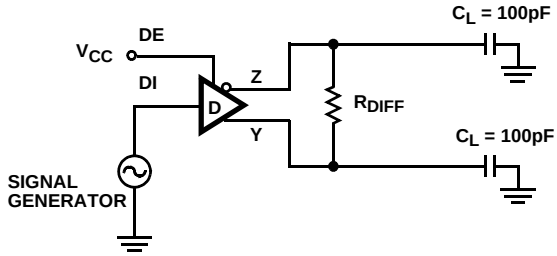
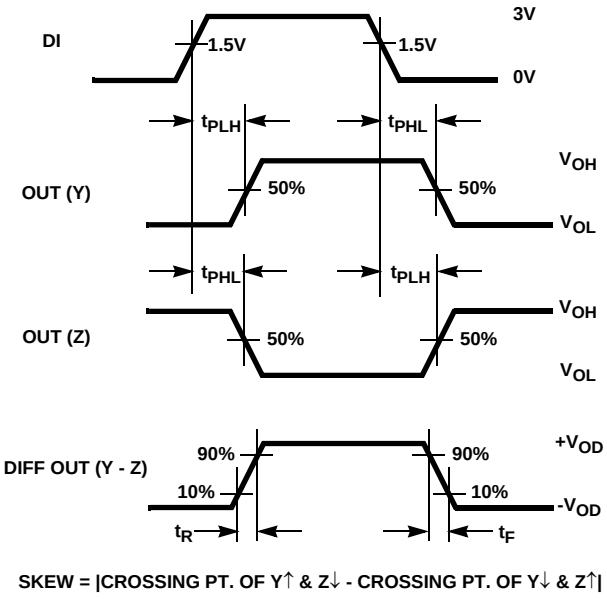


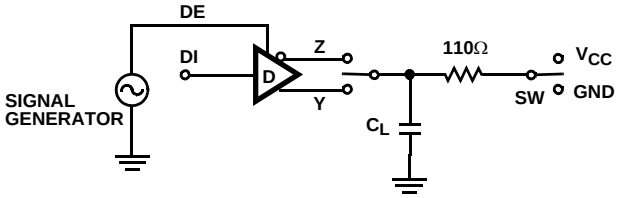
FIGURE 2A. TEST CIRCUIT



SKEW = |CROSSING PT. OF Y↑ & Z↓ - CROSSING PT. OF Y↓ & Z↑|

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y / Z	X	1 / 0	GND	50
t_{LZ}	Y / Z	X	0 / 1	V_{CC}	50
t_{ZH}	Y / Z	X	1 / 0	GND	50
t_{ZL}	Y / Z	X	0 / 1	V_{CC}	50

FIGURE 3A. TEST CIRCUIT

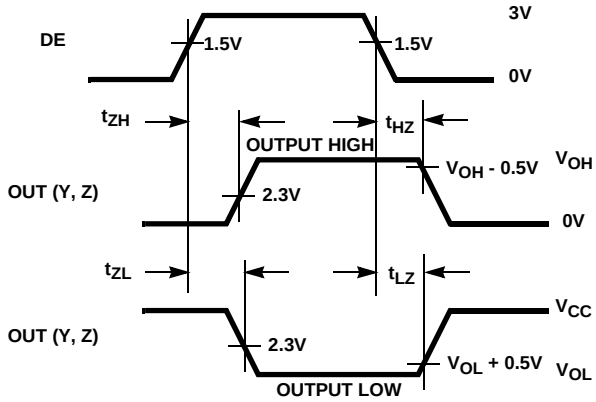


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

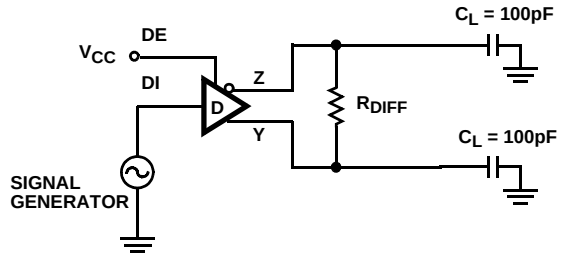


FIGURE 4A. TEST CIRCUIT

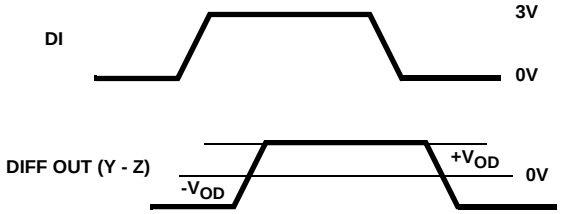


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

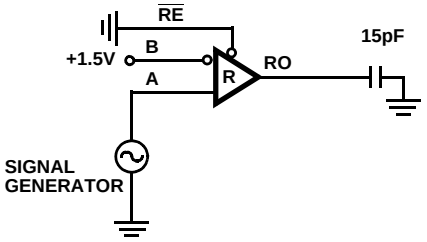


FIGURE 5A. TEST CIRCUIT

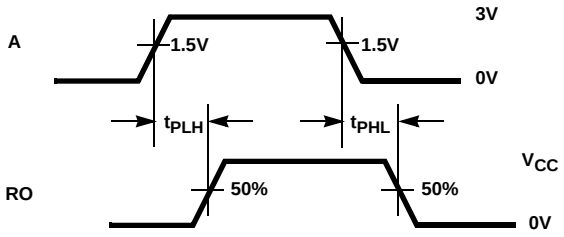
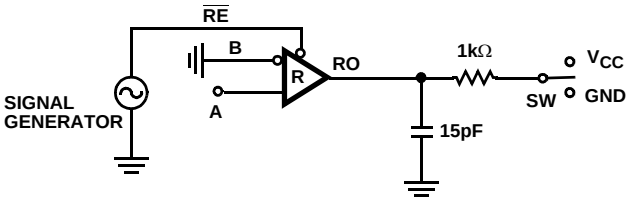


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH}	0	+1.5V	GND
t_{ZL}	0	-1.5V	V_{CC}

FIGURE 6A. TEST CIRCUIT

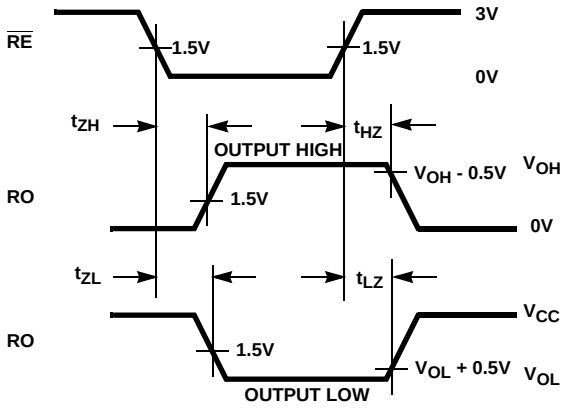


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 spec requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

This device utilizes a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is ±200mV, as required by the RS422 and RS-485 specifications.

Receiver input resistance surpasses the RS-422 spec of 4kΩ, and meets the RS-485 "Unit Load" requirement of 12kΩ minimum, thereby allowing up to 32 devices on a bus.

Receiver inputs function with common mode voltages as great as 7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks, or industrial applications, where induced voltages are a definite concern.

The receiver includes a "fail-safe if open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

The receiver easily meets the data rate supported by the driver, and receiver outputs are three-statable via the active low $\overline{RE}$ input.

Driver Features

The RS-485, RS-422 driver is a differential output device that delivers at least 2V across a 54Ω load (RS-485), and at least 2.5V across a 100Ω load (RS-422) even with V_{CC} = 4.5V. The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

The driver is three-statable via the active high DE input.

Outputs of the driver are not slew rate limited, so faster output transition times allow data rates of at least 30Mbps.

Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 30Mbps usually are limited to lengths of a couple hundred feet, but the larger differential output voltage of this transceiver allows that distance to be pushed past 350'. Figure 7 illustrates the 30Mbps performance of the ISL81485 driving 350' of CAT5 cable, terminated in 120Ω at both the driver and receiver ends. As shown, the differential signal (A-B) delivered to the receiver inputs at the end of the cable is still greater than 1.5V (i.e., 7.5 times the required Rx sensitivity). Thus, even longer cables can be driven if lower noise margins are acceptable.

Twisted pair is the cable of choice for RS-485, RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative, when using a 30Mbps device, to minimize reflections. In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 spec requires that drivers survive worst case bus contentions undamaged. The ISL81485 meets this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 spec, even at the common mode voltage range extremes.

In the event of a major short circuit condition, the device also includes a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically reenable after the die temperature drops about 15 degrees. If the contention persists, the thermal shutdown/reenable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Typical Performance Curves V_{CC} = 5V, T_A = 25°C; Unless Otherwise Specified

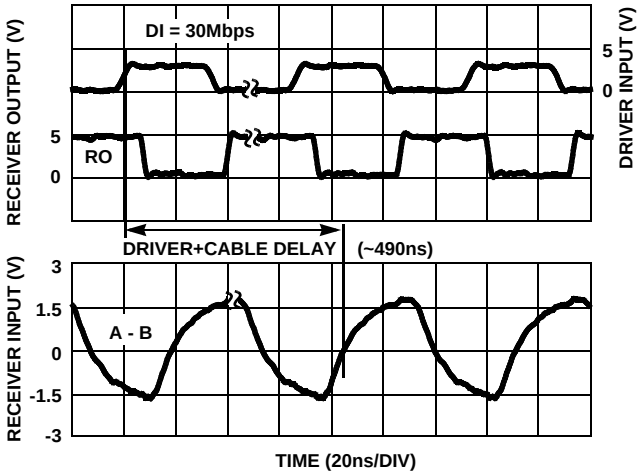


FIGURE 7. DRIVER AND RECEIVER WAVEFORMS DRIVING 350 FEET (107 METERS) OF CAT5 CABLE (DOUBLE TERMINATED WITH 120Ω)

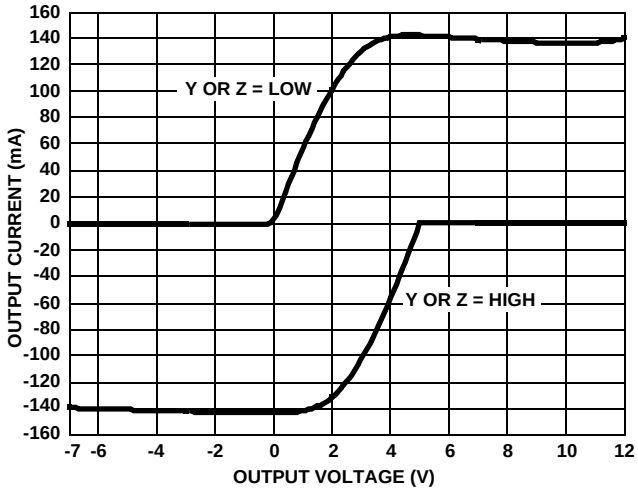


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

Typical Performance Curves V_{CC} = 5V, T_A = 25°C; Unless Otherwise Specified **(Continued)**

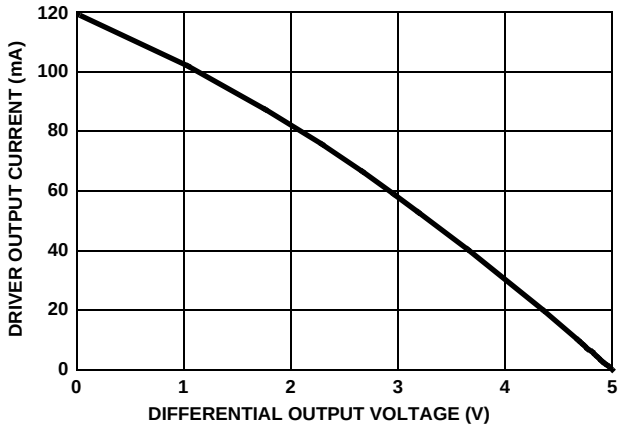


FIGURE 9. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

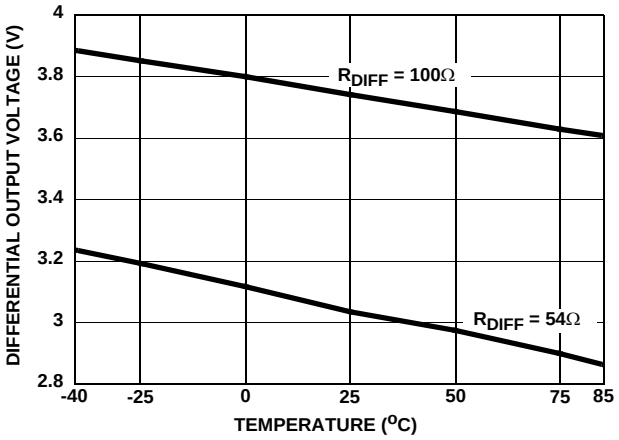


FIGURE 10. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

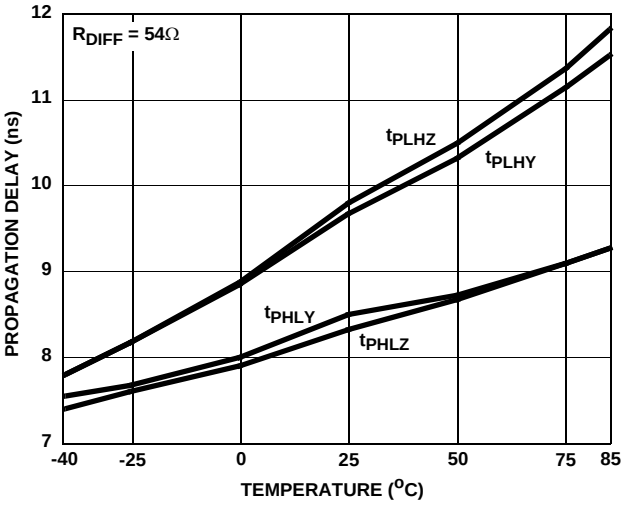


FIGURE 11. DRIVER PROPAGATION DELAY vs TEMPERATURE

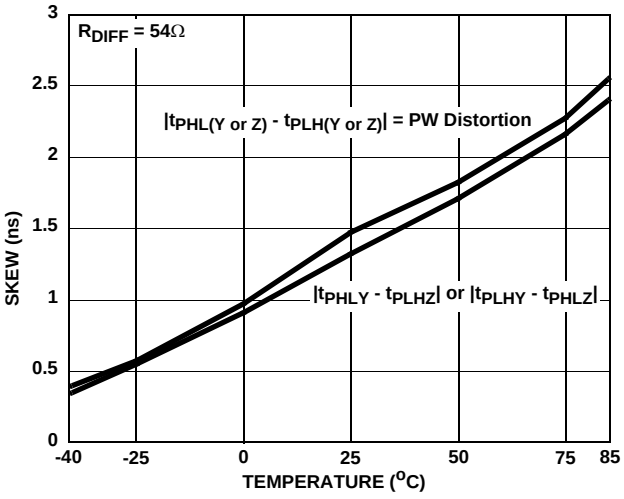


FIGURE 12. DRIVER SKEW AND PULSE DISTORTION vs TEMPERATURE

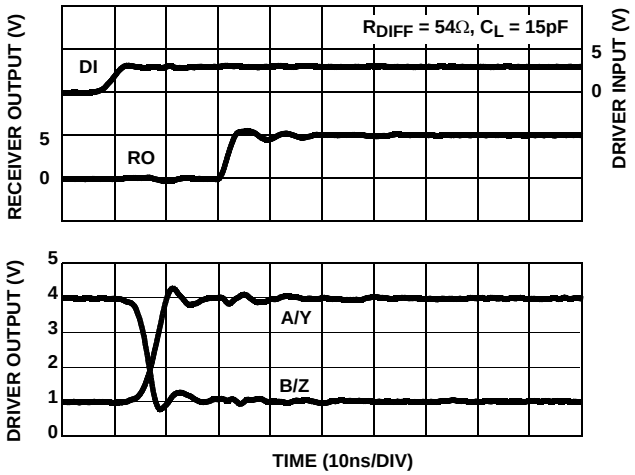


FIGURE 13. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

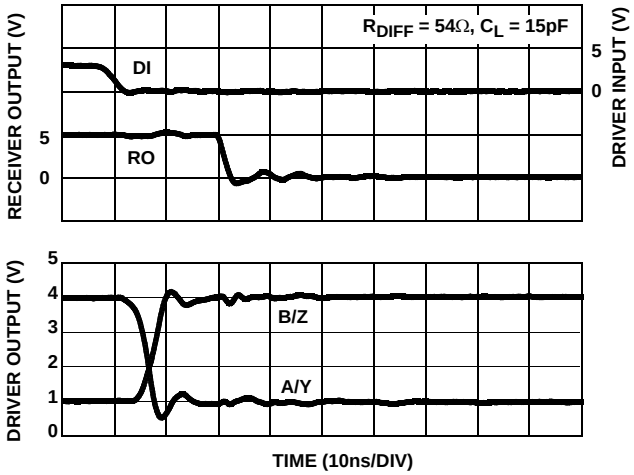


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

Typical Performance Curves V_{CC} = 5V, T_A = 25°C; Unless Otherwise Specified **(Continued)**

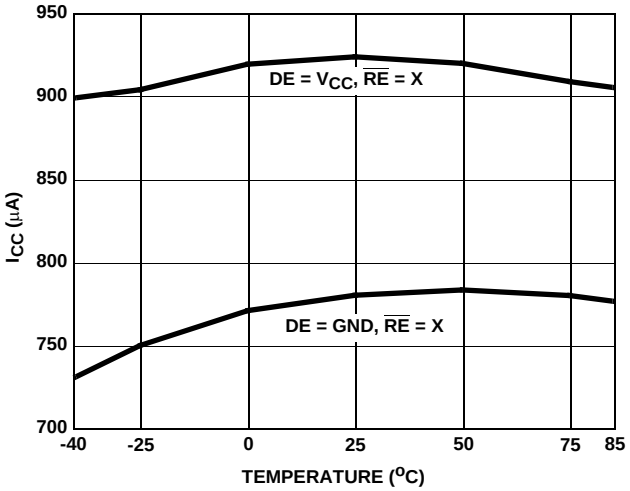


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

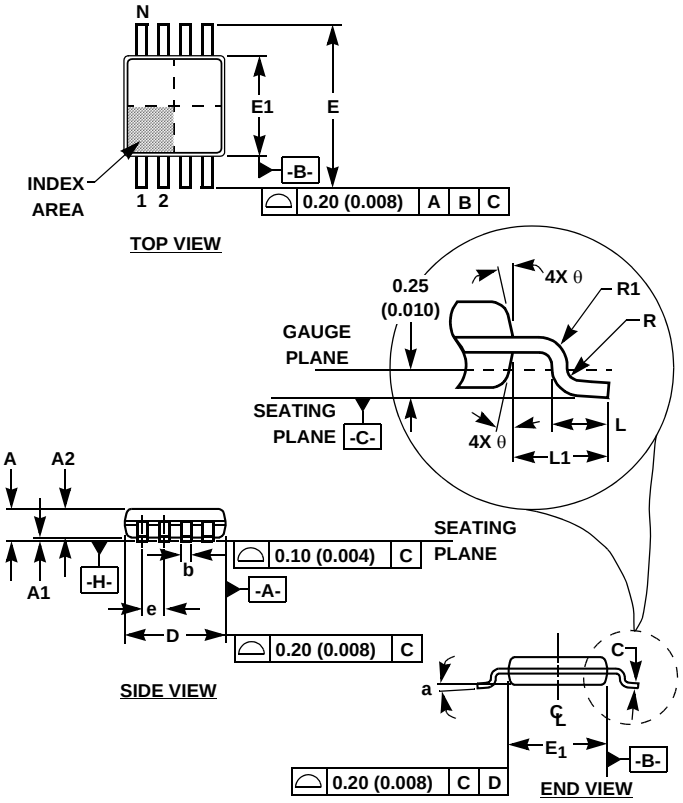
TRANSISTOR COUNT:

528

PROCESS:

Si Gate BiCMOS

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

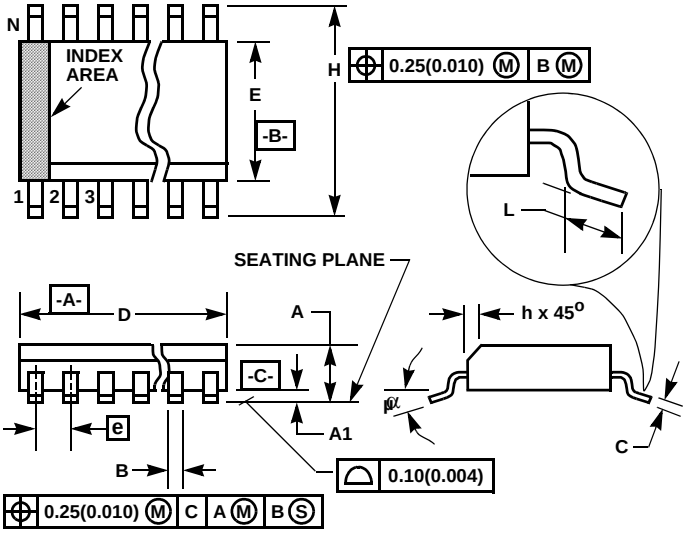
M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com