ISL80121-5

1A Ultra Low Dropout Linear Regulator with Programmable Current Limiting

FN7713
Rev 6.00
March 21, 2016

The ISL80121-5 is a low dropout voltage, single output LDO with programmable current limiting. The ISL80121-5 operates from input voltages of 5V to 6V with a nominal output voltage of 5V. Other custom voltage options are available upon request.

A submicron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value. The programmable current limiting improves system reliability of end applications. An external capacitor on the soft-start pin provides an adjustable soft-starting ramp. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode.

This BiCMOS LDO will consume significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. Quiescent current is modestly compromised to achieve a very fast load transient response.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	PROGRAMMABLE I_{LIMIT}	I_{LIMIT} (DEFAULT)	ADJ or FIXED V_{OUT}
ISL80101-ADJ	No	1.75A	ADJ
ISL80101	No	1.75A	1.8V, 2.5V, 3.3V, 5.0V
ISL80101A	Yes	1.62A	ADJ
ISL80121-5	Yes	0.75A	5.0V

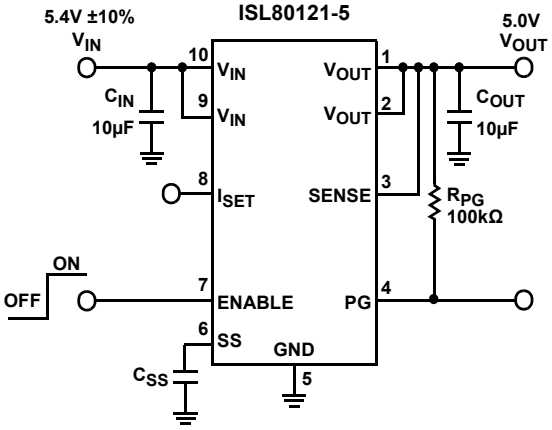
Features

- ±1.8% V_{OUT} accuracy guaranteed over line, load and T_J = -40°C to +125°C
- Very low 130mV dropout voltage
- High accuracy current limit programmable up to 1.75A
- Very fast transient response
- 210µV_{RMS} output noise
- Power-good output
- Programmable soft-start
- Over-temperature protection
- Small 10 Ld DFN package

Applications

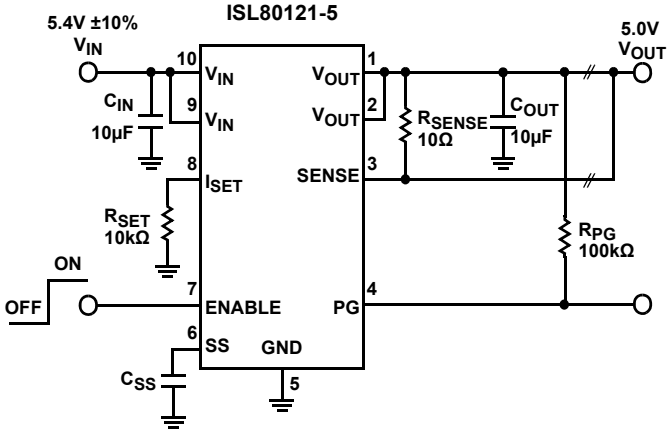
- USB devices
- Telecommunications and networking
- Medical equipment
- Instrumentation systems
- Routers and switchers
- Gaming

Typical Applications



I_{LIMIT} = 0.75A
(DEFAULT)

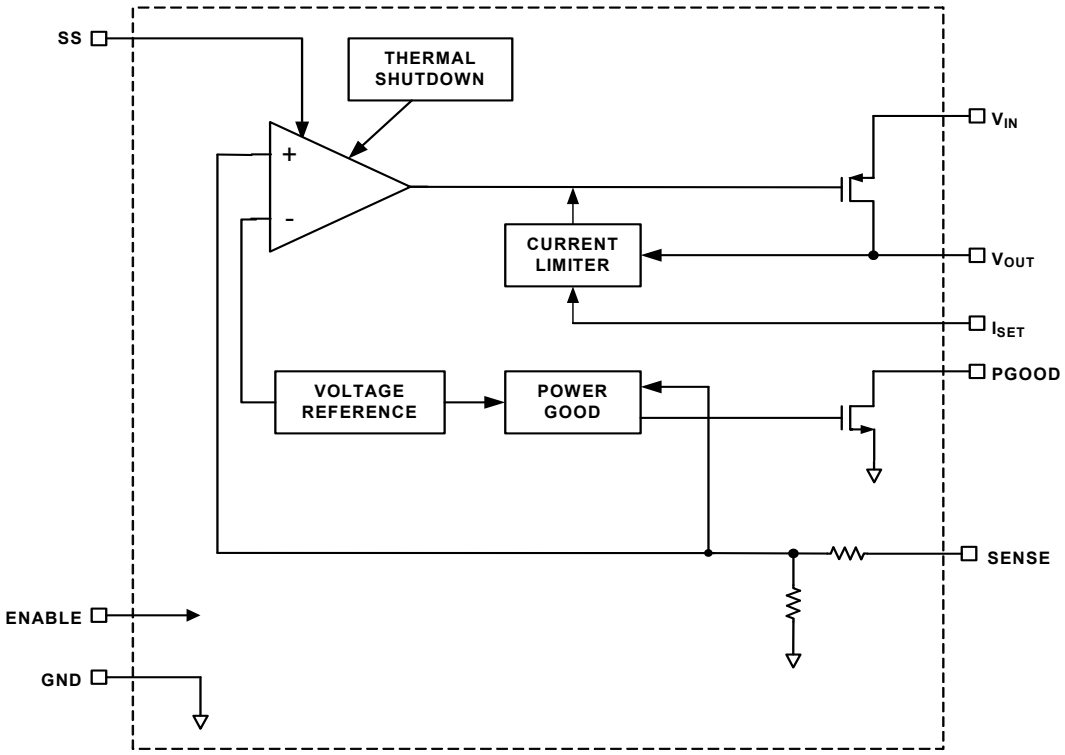
FIGURE 1.



$$I_{LIMIT} = 0.75 + \frac{2.9}{R_{SET}(k\Omega)}$$

FIGURE 2.

Block Diagram



Ordering Information

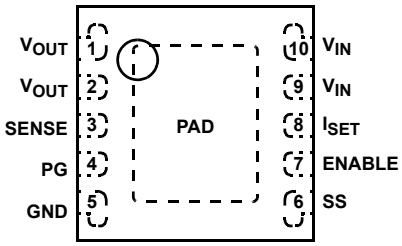
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} VOLTAGE	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG DWG. #
ISL80121IR50Z	DZAD	5.0V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80121-5EVAL2Z	Evaluation Board				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL80121-5. For more information on MSL, please see Technical Brief TB363.

Pin Configuration

ISL80121-5
(10 LD 3x3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Output voltage. A minimum 10µF X5R/X7R output capacitor is required for stability. See "External Capacitor Requirements" on page 9 for more details.
3	SENSE	Remote voltage sense for internally fixed V_{OUT} options. Parasitic resistance between the V_{OUT} pin and the load causes small voltage drops, which degrade V_{OUT} accuracy. For applications that require a stiff V_{OUT}, connect the sense pin to the load.
4	PG	V_{OUT} in regulation signal. Logic low indicates V_{OUT} is not in regulation, and must be grounded if not used.
5	GND	Ground.
6	SS	External capacitor adjusts inrush current.
7	ENABLE	V_{IN}-independent chip enable. TTL and CMOS compatible.
8	I_{SET}	Current limit setting. Current limit is 0.75A when this pin is left floating. This default value can be increased by tying R_{SET} to GND, or decreased by tying R_{SET} to V_{IN}. See "Programmable Current Limit" on page 8 for more details. Do not short this pin to ground.
9, 10	V_{IN}	Input supply. A minimum of 10µF X5R/X7R input capacitor is required for stability. See "External Capacitor Requirements" on page 9 for more details.
-	EPAD	EPAD at ground potential. Soldering it directly to GND plane is required for thermal considerations. See "Power Dissipation and Thermals" on page 9 for more details.

Absolute Maximum Ratings (Note 6)

V_{IN} Relative to GND . . . . . -0.3V to +6.5V
V_{OUT} Relative to GND . . . . . -0.3V to +6.5V
PG, ENABLE, SENSE, SS, I_{SET}
Relative to GND . . . . . -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114) 2.5kV
Machine Model (Tested per JESD22-A115). 250V
Latch-up (Tested per JESD78) . . . . . ±100mA at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 4, 5)	48	7

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions (Note 7)

Junction Temperature Range (T_J) . . . . . -40°C to +125°C
V_{IN} Relative to GND . . . . . 5V to 6V
I_{SET} in Normal Operation . . . . . ≤500mV
SENSE in Normal Operation . . . . . V_{OUT}
PG Sink Current 10mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
7. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: V_{IN} = 5.4V, V_{OUT} = 5.0V, T_J = +25°C, I_{LOAD} = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 8 and Tech Brief TB379.

Boldface limits apply across the operating temperature range, -40°C to +125°C. Pulse load techniques used by ATE to ensure T_J = T_A defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	5.4V < V_{IN} < 6V; 0A < I_{LOAD} < 1A	**-1.8**		**1.8**	%
DC Input Line Regulation	(V_{OUT} low line - V_{OUT} high line)/V_{OUT} low line	5.4V < V_{IN} < 6V, V_{OUT} = 5V	**-1**		**1**	%
DC Output Load Regulation	(V_{OUT} no load - V_{OUT} high load)/V_{OUT} no load	0A < I_{LOAD} < 1A	**-1**		**1**	%
Ground Pin Current	I_Q	I_{LOAD} = 0A, 5.4V < V_{IN} < 6V		3	**5**	mA
		I_{LOAD} = 1A, 5.4V < V_{IN} < 6V		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE = 0.2V, V_{IN} = 6V		0.2	**12**	µA
Dropout Voltage (Note 9)	V_{DO}	I_{LOAD} = 1A, V_{SENSE} = 0V		90	**130**	mV
Output Current Limit	I_{LIMIT}	5.4V < V_{IN} < 6V, I_{SET} is floating	**0.66**	0.75	**0.84**	A
		5.4V < V_{IN} < 6V, R_{SET} = 19.33kΩ		0.9		A
Thermal Shutdown Temperature	TSD	5.4V < V_{IN} < 6V		160		°C
Thermal Shutdown Hysteresis	TSDn	5.4V < V_{IN} < 6V		30		°C

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: V_{IN} = 5.4V, V_{OUT} = 5.0V, T_J = +25°C, I_{LOAD} = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 8 and Tech Brief TB379.

Boldface limits apply across the operating temperature range, -40°C to +125°C. Pulse load techniques used by ATE to ensure T_J = T_A defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD} = 1A		40		dB
		f = 1kHz, I_{LOAD} = 100mA		40		dB
Output Noise Voltage		I_{LOAD} = 10mA, BW = 10Hz < f < 100kHz		210		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold	$V_{EN(HIGH)}$	5.4V < V_{IN} < 6V	**0.5**	0.8	**1.0**	V
Hysteresis	$V_{EN(HYS)}$	5.4V < V_{IN} < 6V	**10**	80	**200**	mV
ENABLE Pin Turn-on Delay	t_{EN}	C_{OUT} = 10µF, I_{LOAD} = 1A		100		µs
ENABLE Pin Leakage Current		V_{IN} = 6V, ENABLE = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
Reset Pull-down Current	I_{PD}	ENABLE = 0V, SS = 1V	**0.5**	1	**1.3**	mA
Soft-start Charge Current	I_{CHG}		**-3.3**	-2	**-0.8**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	84	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		I_{SINK} = 500µA		47	**100**	mV
PG Flag Leakage Current		V_{IN} = 6V, PG = 6V		0.05	**1**	µA

NOTES:

8. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
9. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the output is below its nominal regulation.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 5.4V, V_{OUT} = 5.0V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

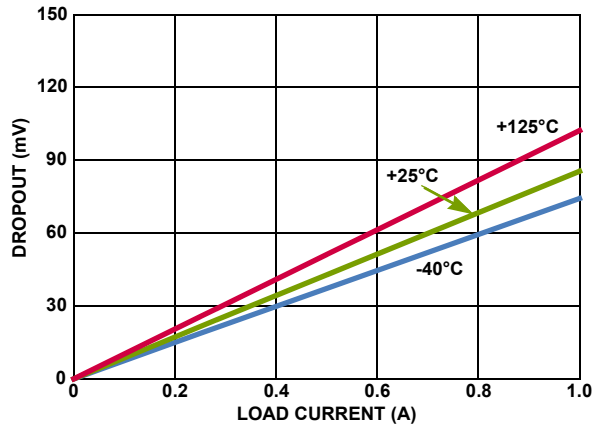


FIGURE 3. DROPOUT VOLTAGE vs LOAD

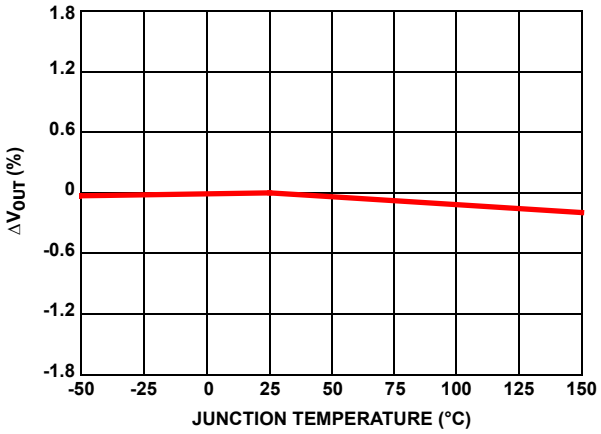


FIGURE 4. OUTPUT VOLTAGE vs TEMPERATURE

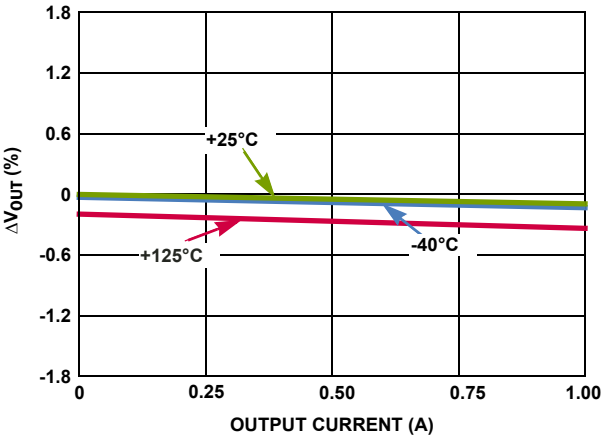


FIGURE 5. OUTPUT VOLTAGE vs OUTPUT CURRENT

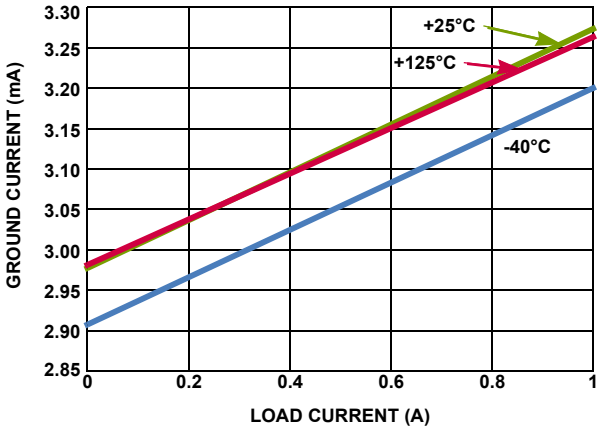


FIGURE 6. GROUND CURRENT vs LOAD CURRENT

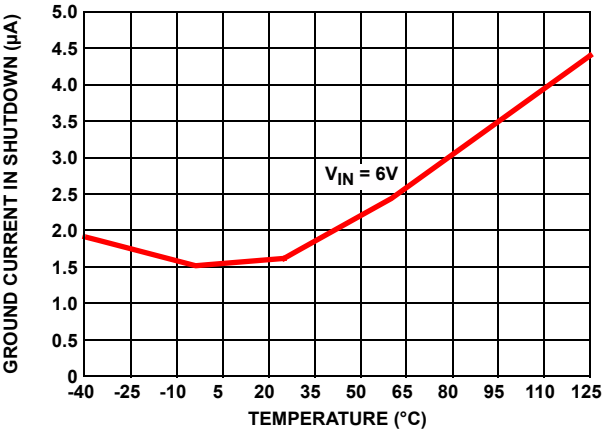


FIGURE 7. GROUND CURRENT IN SHUTDOWN vs TEMPERATURE

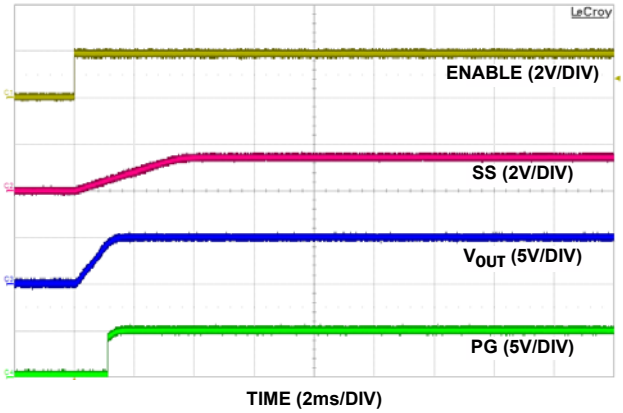


FIGURE 8. ENABLE START-UP

Typical Operating Performance

Unless otherwise noted: V_{IN} = 5.4V, V_{OUT} = 5.0V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

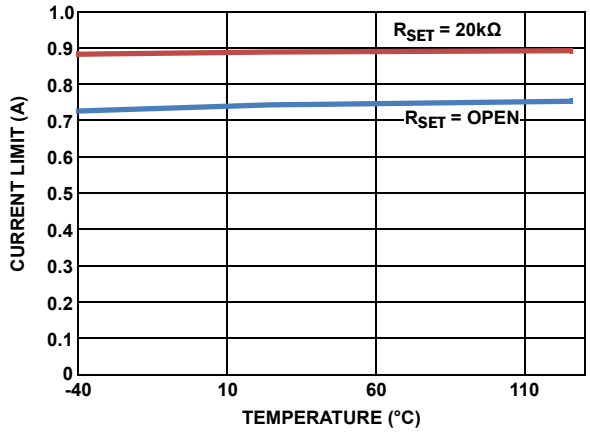


FIGURE 9. CURRENT LIMIT vs TEMPERATURE

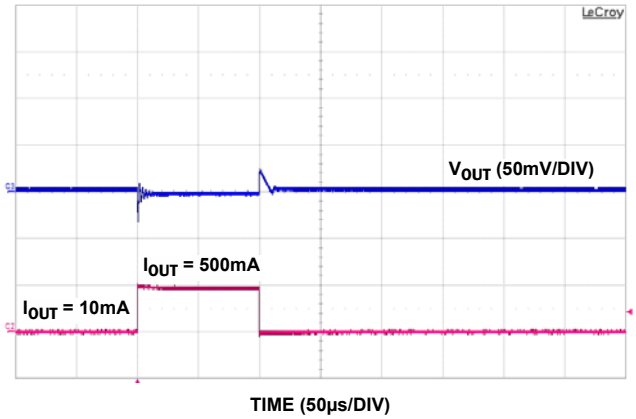


FIGURE 10. LOAD TRANSIENT RESPONSE

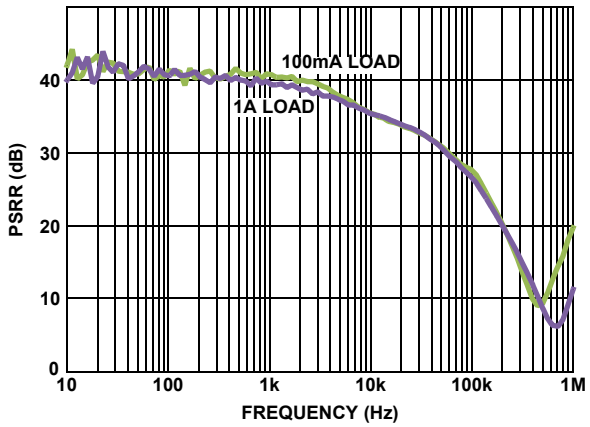


FIGURE 11. PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

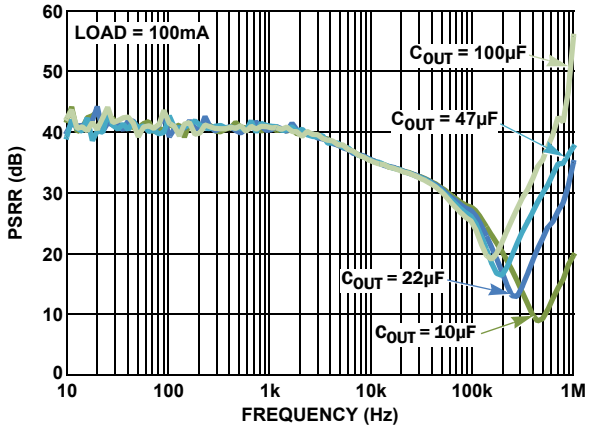


FIGURE 12. PSRR vs FREQUENCY FOR VARIOUS OUTPUT CAPACITORS (I_{OUT} = 100mA)

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Functional Description

Input Voltage Requirements

The ISL80121-5 is optimized for 5V output, and can operate from input voltages of 5V to 6V. Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The generous dropout specification of this family of LDOs allows applications to design for a level of efficiency.

Programmable Current Limit

The ISL80121-5 protects against overcurrent due to short-circuit and overload conditions applied to the output. When this happens, the LDO performs as a constant current source. If the short-circuit or overload condition is removed, the output returns to normal voltage regulation operation.

The current limit is set at 0.75A by default when the I_{SET} pin is left floating.

This limit can be increased by tying a resistor R_{SET} from the I_{SET} pin to ground. The current limit is determined by R_{SET} as shown in Equation 1:

$$I_{LIMIT} = 0.75 + \frac{2.9}{R_{SET(k\Omega)}} \quad \text{(EQ. 1)}$$

Figure 13 shows the relationship between R_{SET} and the current limit when the R_{SET} is tied from I_{SET} pin to GND. Do not short this pin to ground. Increasing the current limit past 1.75A may cause damage to the part and is highly discouraged.

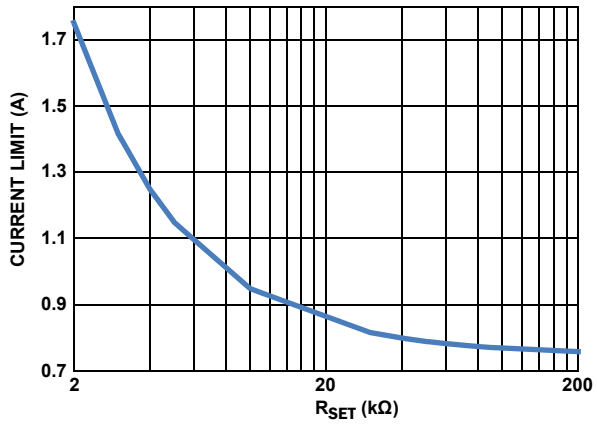

FIGURE 13. INCREASING I_{LIMIT} (R_{SET} TO GND)

The current limit can be decreased from the 0.75A default by tying R_{SET} from the I_{SET} pin to V_{IN}. The current limit is then determined by both R_{SET} and V_{IN} following Equation 2:

$$I_{LIMIT} = 0.75 - \frac{2.9 \times (2 \times V_{IN} - 1)}{R_{SET(k\Omega)}} \quad \text{(EQ. 2)}$$

Figure 14 shows the relationship between R_{SET} and the current limit when R_{SET} is tied from the I_{SET} pin to V_{IN} for V_{IN} = 5.4V.

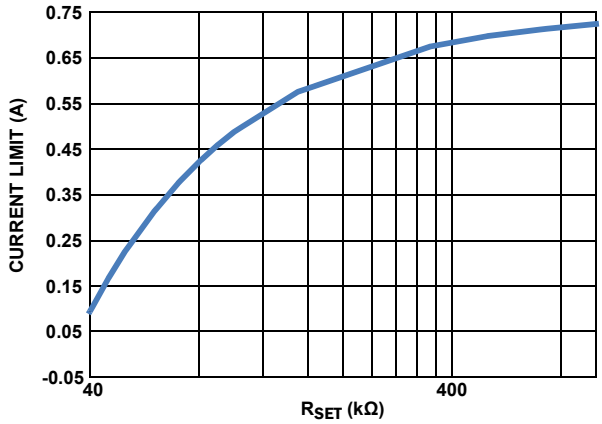

FIGURE 14. DECREASING I_{SET} (R_{SET} TO V_{IN})

Enable Operation

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. An internal pull-up or pull-down resistor to change these values is available upon request. As a result, this pin must not be left floating and should be tied to V_{IN} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open-drain outputs to control the ENABLE pin. The ENABLE pin may be connected directly to V_{IN} for applications with outputs that are always on.

Power-good Operation

PG is a logic output that indicates the status of V_{OUT}. The PG flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PG pin requires an external pull-up resistor typically connected to the V_{OUT} pin. The PG pin should not be pulled up to a voltage source greater than V_{IN}. PG goes low when the output voltage drops below 84% of the nominal output voltage, the current limit faults, or the input voltage is too low. For applications not using this feature, connect this pin to ground.

Soft-start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up this C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 3:

$$t_{start} = \frac{(C_{SS} x 0.5)}{2\mu A} \quad \text{(EQ. 3)}$$

Equation 4 determines the C_{SS} required for a specific start-up inrush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired inrush current.

$$C_{SS} = \frac{(V_{OUT} x C_{OUT} x 2\mu A)}{I_{INRUSH} x 0.5V} \quad \text{(EQ. 4)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL80121-5 applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 10µF X5R/X7R is used for local bypass on V_{OUT}. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very low ESR multilayer ceramic capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age and temperature. X7R and X5R dieletric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions (Note 7)" on page 4. The power dissipation can be calculated by using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 5)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 6:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 6)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 5, is less than the maximum allowable power dissipation $P_{D\,(MAX)}$.

The DFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane). Figure 15 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

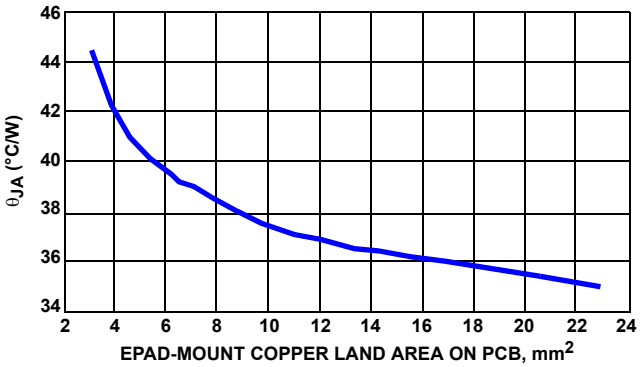

FIGURE 15. 3mm x 3mm 10 LD DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

The power level and the thermal impedance of the package (+48°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

General Power PAD Design Considerations

Figure 16 shows the recommended use of vias on the thermal pad to remove heat from the IC. This typical array populates the thermal pad footprint with vias spaced three times the radius distance from the center of each via. Small via size is advisable, but not to the extent that solder reflow becomes difficult.

All vias should be connected to the pad potential, with low thermal resistance for efficient heat transfer. Complete connection of the plated through-hole to each plane is important. It is not recommended to use "thermal relief" patterns to connect the vias.

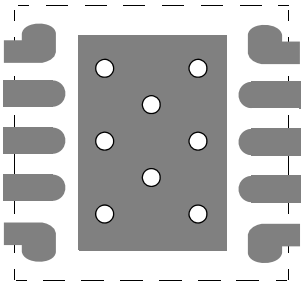

FIGURE 16. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 21, 2016	FN7713.6	On page 1 -Under Features, changed “Very low 130mV dropout voltage at V_{IN} = 5V” to “Very low 130mV dropout voltage”. -Updated Figures 1 and 2 by removing ±1.8%. -Updated “Block Diagram” on page 2. -On page 4, updated latch-up condition from +85C to +125C. -In Electrical Specifications table updated the following: -Heading -DC Output Voltage Accuracy Test Condition -DC Input Line Regulation Spec/Symbol/Test Condition -DC Output Load Regulation Spec/Symbol -Ground Pin Current Test Condition -Dropout Voltage Test Condition -Output Current Limit Test Condition -Thermal Shutdown Temperature Test Condition -Thermal Shutdown Hysteresis Test Condition -Turn-on Threshold Test Condition/Spec Changed Minimum spec from “0.3” to “0.5” -Hysteresis Test Condition -Updated y-Axis and title of Figure 7 on page 6. -Updated Y-Axis labels and titles of Figures 11 and 12 on page 7. -Removed “that can accommodate profiles smaller than the TO220/263” from last sentence of paragraph under “Input Voltage Requirements” on page 8. -Removed “current limit tripping, and VIN” from first sentence under “Power-good Operation” on page 8. -Removed “PG functions during shutdown, but not during thermal shutdown.” from “Power-good Operation” on page 8. -Replaced Products section with About Intersil section. -Updated POD to the latest revision changes are listed below: -Rev.7 to Rev. 8 “Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter)” -Rev. 8 to Rev. 9, “Added missing dimension 0.415 in Typical Recommended land pattern”. -Rev. 9 to Rev. 10 “Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins. POD was corrected in land pattern to show correct dimension markings” -Rev. 10 to Rev. 11 “Tiebar Note 4 updated, From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).”
June 22, 2012	FN7713.5	1. Changed POD L10.3X3 on page 12 to latest revision from 6 to 7. Change POD is as follows: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metalized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly. 2. “Input Voltage Requirements” on page 8 changed input voltages from “2.2V” to “5V” 3. Page 1: On 3rd paragraphs first sentence “CMOS” changed to “BiCMOS”. 4. Page1: 1st paragraph sentence changed from: “This LDO operates from input voltages of 2.2V to 6V. The ISL80121-5 has a nominal output voltage of 5V”. T0: “The ISL80121-5 operates from input voltages of 5V to 6V with a nominal output voltage of 5V”. 5. Page 2: Removed Note in Ordering Information: “The 1.5V, 3.3V and 5V fixed output voltages will be released in the future. Please contact Intersil Marketing for more details”. 6. Page 4: Recommended Operation Conditions “V_{In} relative to GND changed from 2.2V to 6V to 5V to 6V” 7. Page 4: Recommended Operation Conditions Removed “V_{out} Range line 800mV T0 5V”
September 29, 2011	FN7713.4	Table 1 on page 1 updated to include more information on Intersil's 1A LDO portfolio.
April 22, 2011	FN7713.3	In Figure 10 on page 7, corrected label from “V_{OUT} (50V/DIV)." to “V_{OUT} (50mV/DIV)." In “DC Output Voltage Accuracy” on page 4, corrected the MAX value from -1.8 to +1.8.

Revision History

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DATE	REVISION	CHANGE
February 24, 2011	FN7713.2	1. page 1, paragraph 2, “The programmable current limiting improves system reliability of applications” changed to “The programmable current limiting improves system reliability of end applications.” 2. page 1, Features, “Programmable Soft-starting” changed to “Programmable Soft-Start” 3. Made subbing consistent throughout document. 4. page 3, EPAD Description “directly to GND plane is optional.” Changed to “directly to GND plane is required for thermal considerations. See “Power Dissipation and Thermals” on page 9 for more details.” 5. page 5, Removed Notes in Electrical Spec Table, which read:”Minimum capacitor of 10µF X5R/X7R on V_{IN} and V_{OUT} required for stability.” and “If the current limit for inrush current is acceptable in application, do not use this feature. Used only when large bulk capacitance required on V_{OUT} for application.” 6. page 5, Electrical Specifications, PG Pin Characteristics, V_{out} PG Flag Threshold a.Typical "85" changed to “84” %V_{out} 7. page 9, after Thermal Fault Protection section a.Added “General Power PAD Design Considerations” section with Figure 14. 8. All PGOOD changed to PG throughout. 9. Changed Theta Ja from 51C/W to 48C/W. 1.page 1, Features a."200µVrms Output Noise” changed to “210 µVrms Output Noise” 2.page 1, Typical Applications, right side figure a.Resize "V_{OUT}" (pin2) and “SENSE” (pin3) 3.page 8, Equation 4 a.Extra parenthesis ")" removed page 1 Before Features added Table of Key Differences. page 2 Block Diagram - Removed “ADJ Voltage Version” and left the “Sense” Connection. page 3 Pin Number 8, description, 2nd sentence: “Current limit is 0.75mA...” changed to “Current limit is 0.75A...” page 5 Electrical Specifications, AC Characteristics, Input Supply Ripple Rejection Test conditions and Typical values changed from “f = 1kHz, ILOAD = 1A, f = 120Hz, ILOAD = 1A” TO “f = 1kHz, ILOAD = 1A, f = 1kHz, ILOAD = 100mA” page 6, Figure 5 - X-axis label changed from “Output Current (mA)" to “Output Current (A) page 8, Figure 14 - a.Figure label change. “IN” in "V_{IN}" was subscripted.
December 6, 2010	FN7713.1	1. In “Block Diagram” on page 2: a. Added “ADJ adjustable voltage version” Pin. Added “fixed voltage version” to “SENSE” pin 2. On page 4: “Ground Pin Current” Test Conditions a. Replaced "V_{OUT}+0.4V" with "2.2V" on both lines
December 2, 2010	FN7713.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

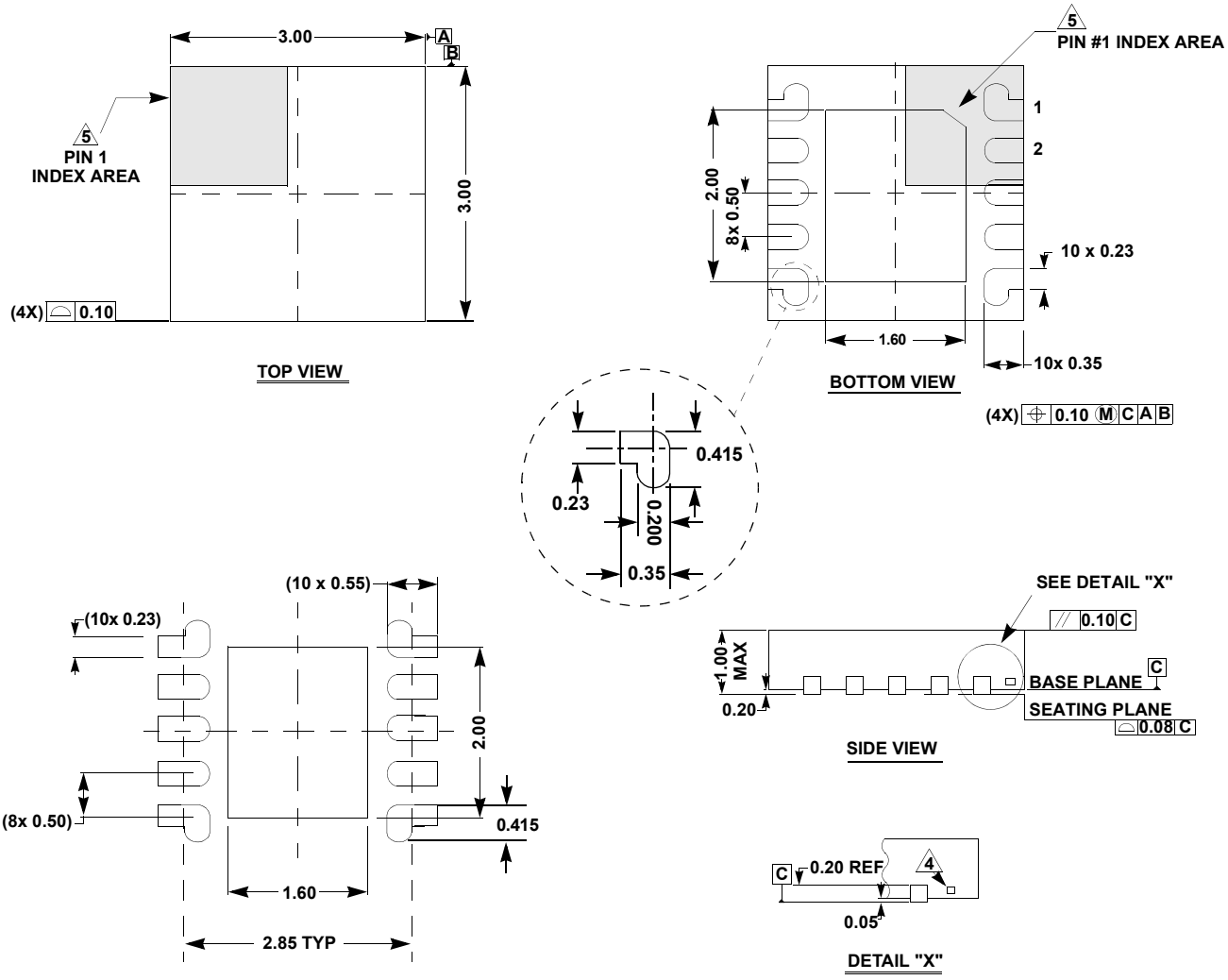
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)
Rev 11, 3/15



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.