Improved Industry Standard Single-Ended Current Mode PWM Controller

The ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845 family of adjustable frequency, low power, pulse width modulating (PWM) current mode controllers is designed for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection.

This advanced BiCMOS design is pin compatible with the industry standard 384x family of controllers and offers significantly improved performance. Features include low operating current, 60μA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL6840	7.0	100%
ISL6841	7.0	50%
ISL6842	14.4V	100%
ISL6843	8.4V	100%
ISL6844	14.4V	50%
ISL6845	8.4V	50%

Features

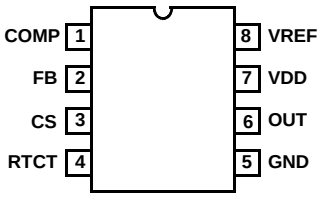
- 1A MOSFET gate driver
- 60μA startup current, 100μA maximum
- 25ns propagation delay current sense to output
- Fast transient response with peak current mode control
- Adjustable switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Trimmed timing capacitor discharge current for accurate deadtime/maximum duty cycle control
- High bandwidth error amplifier
- Tight tolerance voltage reference over line, load, and temperature
- Tight tolerance current limit threshold
- Pb-free plus anneal available (RoHS Compliant)

Applications

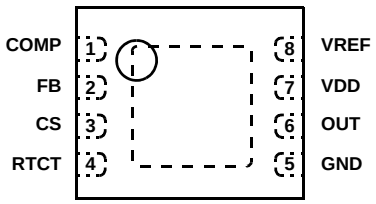
- Telecom and Datacom Power
- Wireless Base Station Power
- File Server Power
- Industrial Power Systems
- PC Power Supplies
- Isolated Buck and Flyback Regulators
- Boost Regulators

Pinout

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845
8 LD SOIC, MSOP
TOP VIEW



8 LD DFN
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6840IB*	ISL 6840IB	-40 to +105	8 Ld SOIC	M8.15
ISL6840IBZ* (See Note)	6840 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6840IU*	6840	-40 to +105	8 Ld MSOP	M8.118
ISL6840IUZ* (See Note)	6840Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6841IB*	ISL 6841IB	-40 to +105	8 Ld SOIC	M8.15
ISL6841IBZ* (See Note)	6841 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6841IU*	6841	-40 to +105	8 Ld MSOP	M8.118
ISL6841IUZ* (See Note)	6841Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6842IB*	ISL 6842IB	-40 to +105	8 Ld SOIC	M8.15
ISL6842IBZ* (See Note)	6842 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6842IU*	6842	-40 to +105	8 Ld MSOP	M8.118
ISL6842IUZ* (See Note)	6842Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6843IB*	ISL 6843IB	-40 to +105	8 Ld SOIC	M8.15
ISL6843IBZ* (See Note)	6843 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6843IU*	6843	-40 to +105	8 Ld MSOP	M8.118
ISL6843IUZ* (See Note)	6843Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6844IB*	ISL 6844IB	-40 to +105	8 Ld SOIC	M8.15
ISL6844IBZ* (See Note)	6844 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6844IU*	6844	-40 to +105	8 Ld MSOP	M8.118
ISL6844IUZ (See Note)	6844Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6845IB*	ISL 6845IB	-40 to +105	8 Ld SOIC	M8.15
ISL6845IBZ* (See Note)	6845 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6845IU*	6845	-40 to +105	8 Ld MSOP	M8.118
ISL6845IUZ* (See Note)	6845Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118

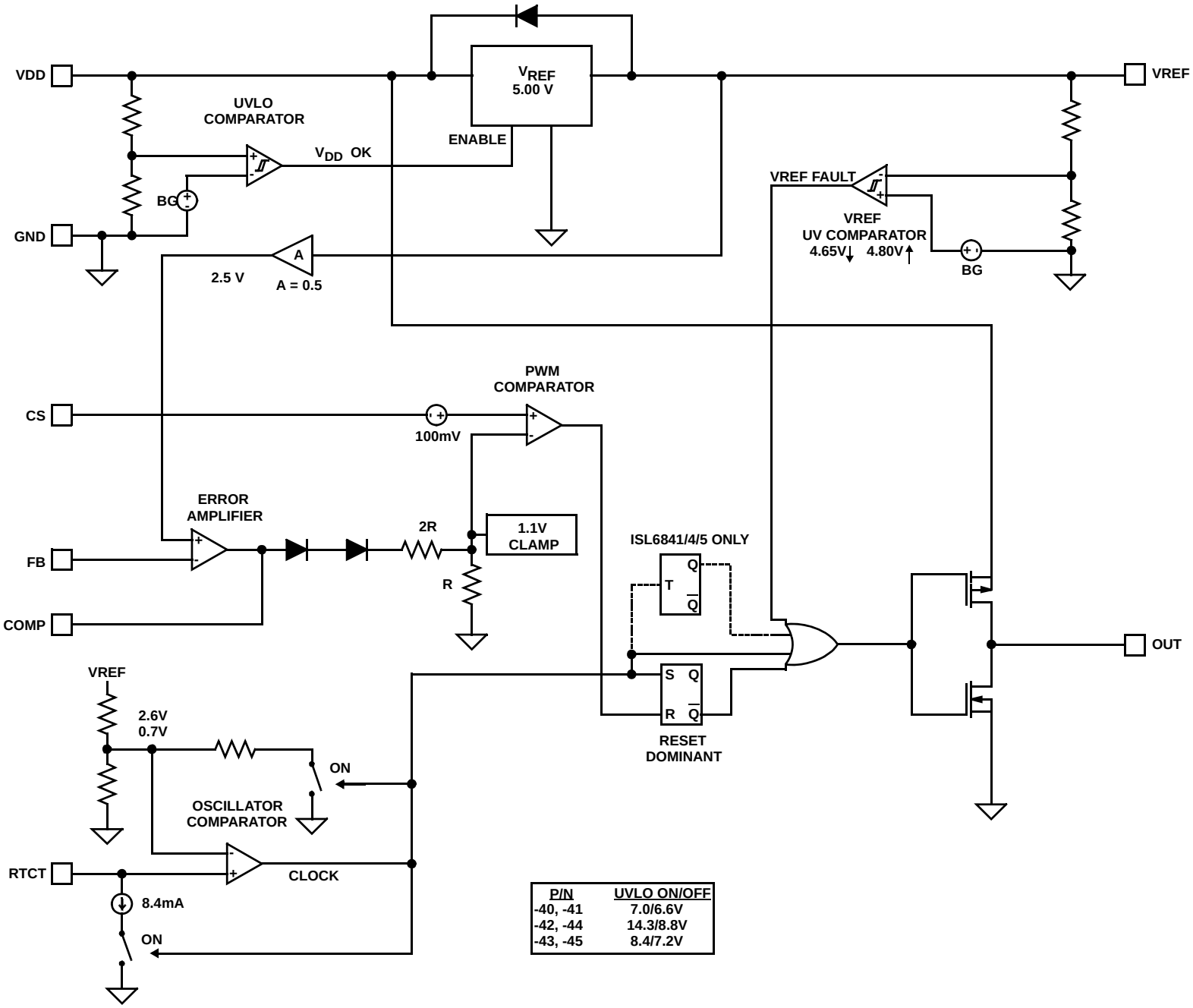
Ordering Information (Continued)

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6840IRZ-T† (See Note)	40Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6841IRZ-T† (See Note)	41Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6842IRZ-T (See Note)	42Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6843IRZ-T (See Note)	43Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6844IRZ-T† (See Note)	44Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6845IRZ-T (See Note)	45Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3

*Add -T to part number for Tape and Reel packaging.
†Contact Factory for Availability

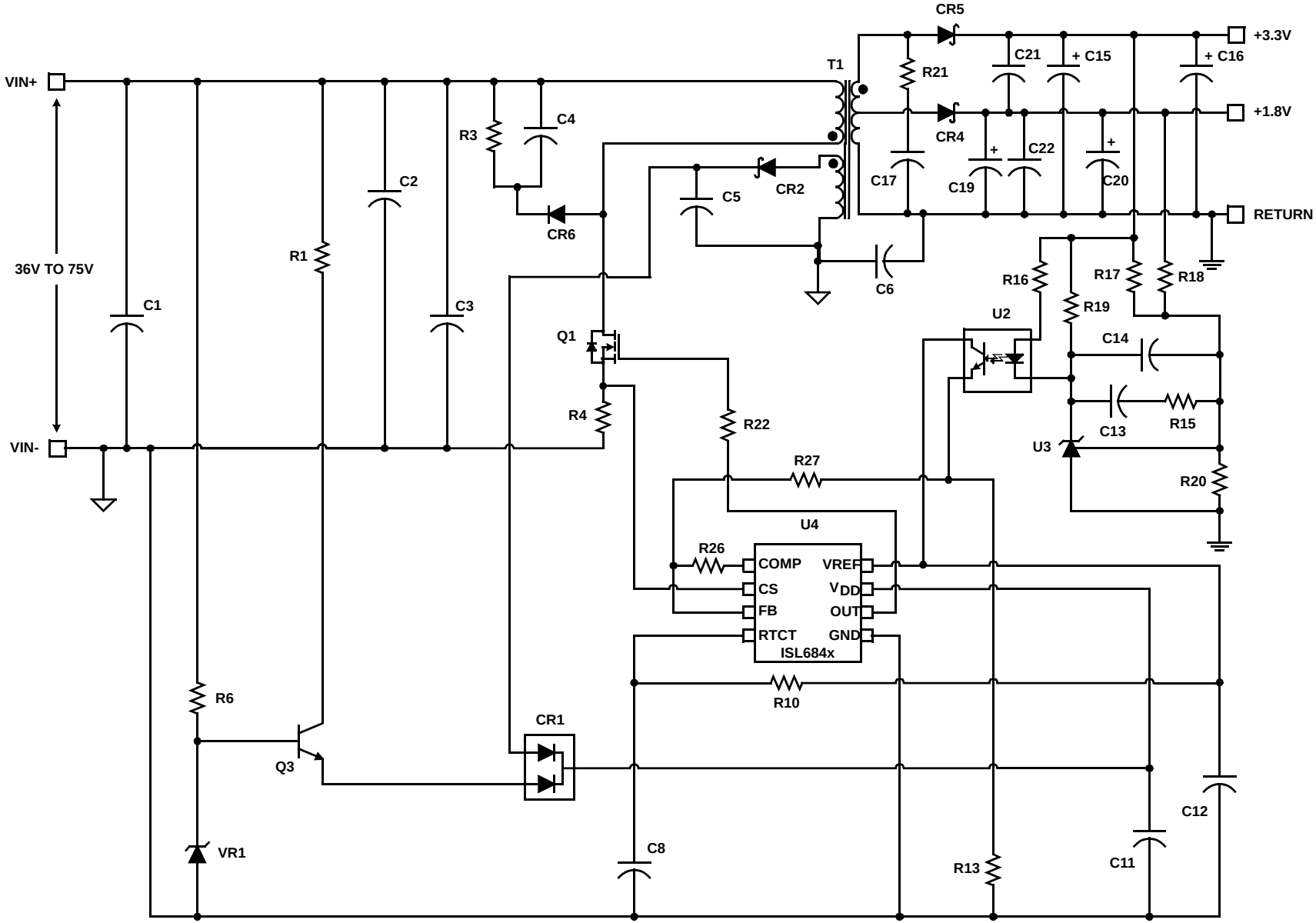
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Block Diagram

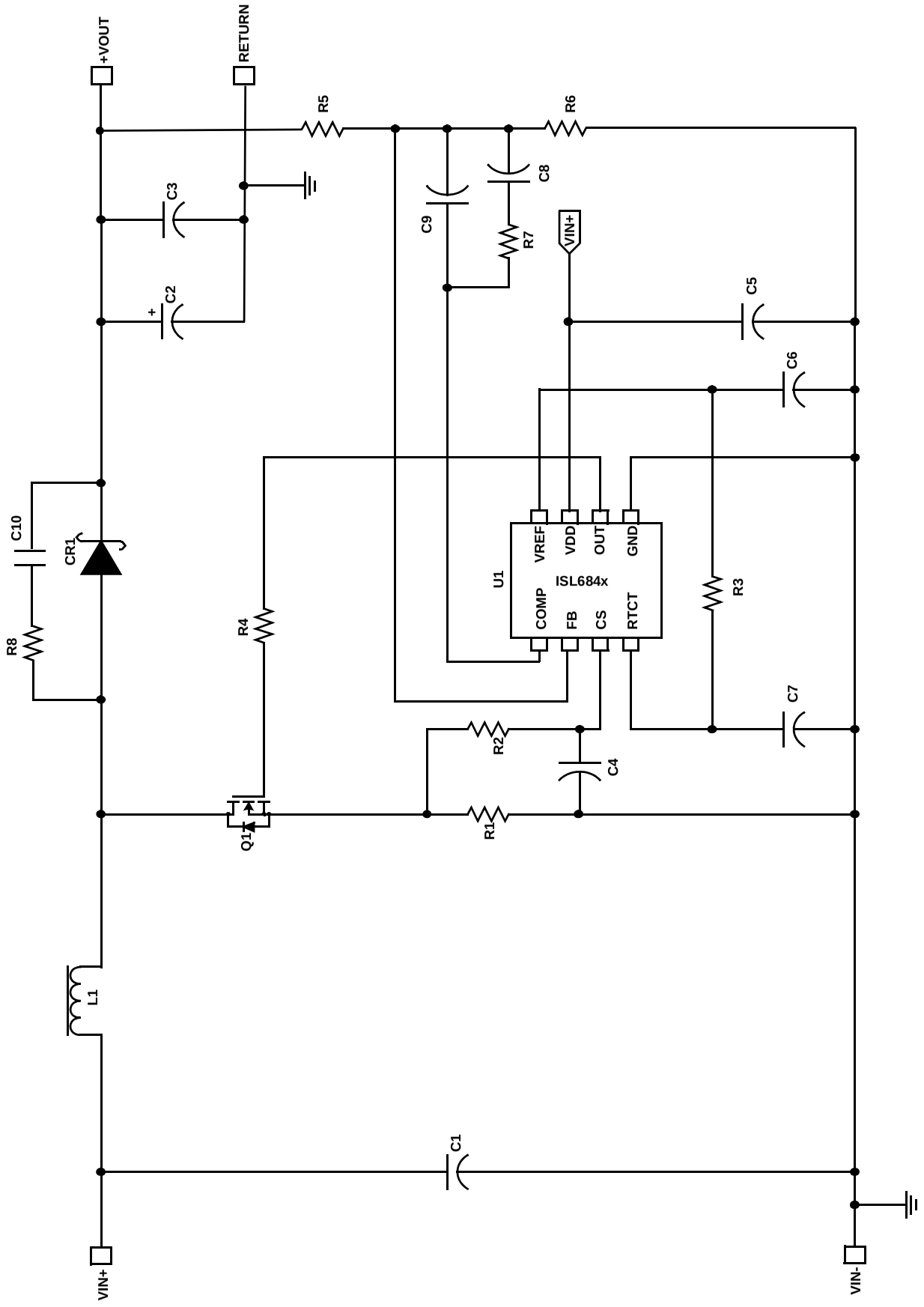


P/N	UVLO ON/OFF
-40, -41	7.0/6.6V
-42, -44	14.3/8.8V
-43, -45	8.4/7.2V

Typical Application - 48V Input Dual Output Flyback



Typical Application - Boost Converter



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUT . . . . . GND - 0.3V to V_{DD} + 0.3V
Signal Pins . . . . . GND - 0.3V to 6.0V
Peak GATE Current 1A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2000V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . . 1000V

Operating Conditions

Temperature Range
ISL684xIx . . . . . -40°C to +105°C
Supply Voltage Range (Typical, Note 3)
ISL6840, ISL6841. . . . . 7.5V to 14V
ISL6843, ISL6845. . . . . 9V to 16V
ISL6842, ISL6844. . . . . 15V to 18V

Thermal Information

Thermal Resistance (Typical, Note 1,)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Note 2).	77	6
SOIC Package	100	N/A
MSOP Package	130	N/A

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC- Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

+150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Constantly operated at +150°C may shorten the life of the part.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 3 and page 4. V_{DD} = 15V (Note 7), Rt = 10kΩ, Ct = 3.3nF, T_A = -40 to +105°C (Note 4), Typical values are at T_A = +25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold (ISL6840, ISL6841)		6.5	7.0	7.5	V
START Threshold (ISL6843, ISL6845)		7.8	8.4	9.0	V
START Threshold (ISL6842, ISL6844)		13.3	14.3	15.3	V
STOP Threshold (ISL6840, ISL6841)		6.1	6.6	6.9	V
STOP Threshold (ISL6843, ISL6845)		6.7	7.2	7.7	V
STOP Threshold (ISL6842, ISL6844)		8.0	8.8	9.6	V
Hysteresis (ISL6840, ISL6841)		-	0.4	-	V
Hysteresis (ISL6843, ISL6845)		-	0.8	-	V
Hysteresis (ISL6842, ISL6844)		-	5.4	-	V
Startup Current, I_{DD}	V_{DD} < START Threshold	-	60	100	µA
Operating Current, I_{DD}	(Note 5)	-	3.3	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	5.5	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	4.925	5.000	5.050	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 6)	-	5	-	mV
Fault Voltage		4.40	4.65	4.85	V
VREF Good Voltage		4.60	4.80	VREF - 0.05	V
Hysteresis		50	165	250	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 3 and page 4. V_{DD} = 15V (Note 7), Rt = 10kΩ, Ct = 3.3nF, T_A = -40 to +105°C (Note 4), Typical values are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1.0	µA
CS Offset Voltage	V_{CS} = 0V (Note 6)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 6)	0.80	1.15	1.30	V
Input Signal, Maximum		0.91	0.97	1.03	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V (Note 6)	2.5	3.0	3.5	V/V
CS to OUT Delay	(Note 6)	-	25	40	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 6)	60	90	-	dB
Unity Gain Bandwidth	(Note 6)	3.5	5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.475	2.514	2.55	V
FB Input Bias Current	V_{FB} = 0V	-1.0	-0.2	1.0	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	1.0	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	-0.4	-	-	mA
COMP VOH	V_{FB} = 2.3V	4.80	-	VREF	V
COMP VOL	V_{FB} = 2.7V	0.4	-	1.0	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 6)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_J = +25°C	49	52	55	kHz
Frequency Variation with V_{DD}	T = +25°C $(f_{18V} - f_{12V})/f_{12V}$	-	0.2	1.0	%
Temperature Stability	(Note 6)	-	-	5	%
Amplitude, Peak to Peak		-	1.9	-	V
RTCT Discharge Voltage		-	0.7	-	V
Discharge Current	RTCT = 2.0V	7.2	8.4	9.5	mA
OUTPUT					
Gate VOH	V_{DD} to OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate VOL	OUT toGND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 6)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 6)	-	20	40	ns
Fall Time	C_{OUT} = 1nF (Note 6)	-	20	40	ns
PWM					
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	94	96	-	%
	ISL6841, ISL6844, ISL6845	47	48	-	%
Minimum Duty Cycle	ISL6840, ISL6842, ISL6843	-	-	0	%
	ISL6841, ISL6844, ISL6845	-	-	0	%

NOTES:

4. Specifications at -40°C although guaranteed, are not 100% tested in production.
5. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
6. These parameters, although guaranteed, are not 100% tested in production.
7. Adjust V_{DD} above the start threshold and then lower to 15V.

Typical Performance Curves

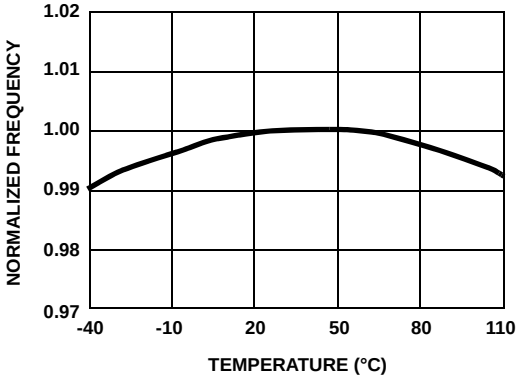


FIGURE 1. FREQUENCY vs TEMPERATURE

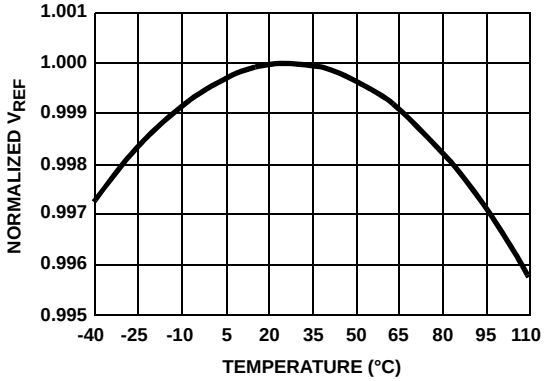


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

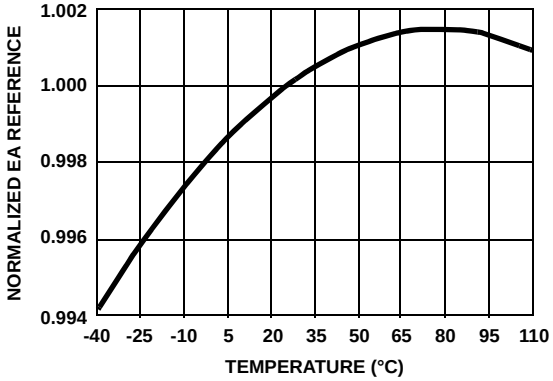


FIGURE 3. EA REFERENCE vs TEMPERATURE

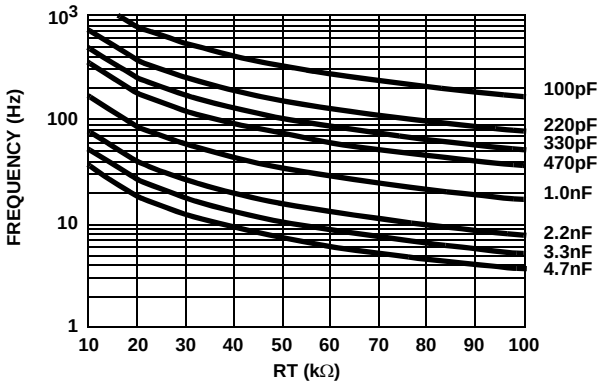


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, Dmax, can be calculated from Equations 1, 2, 3 and 4:

$$t_C \approx 0.583 \bullet RT \bullet CT \quad \text{(EQ. 1)}$$

$$t_D \approx -RT \bullet CT \bullet \ln\left(\frac{0.0083 \bullet RT - 4.3}{0.0083 \bullet RT - 2.4}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(t_C + t_D) \quad \text{(EQ. 3)}$$

$$D = t_C \bullet f \quad \text{(EQ. 4)}$$

Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

VDD - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the

average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated in Equation 5:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the VDD and GND pins as possible.

VREF - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

Functional Description

Features

The ISL684x current mode PWMs make an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL684x controllers have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

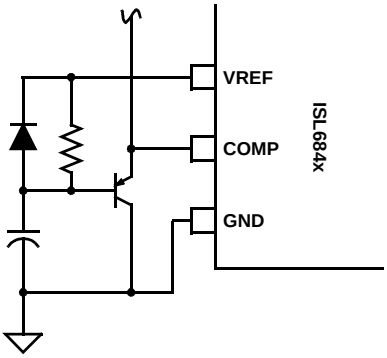


FIGURE 5. SOFT-START

Gate Drive

The ISL684x are capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. Adding excessive slope compensation, however, results in a control loop that behaves more as a voltage mode controller than as current mode controller.

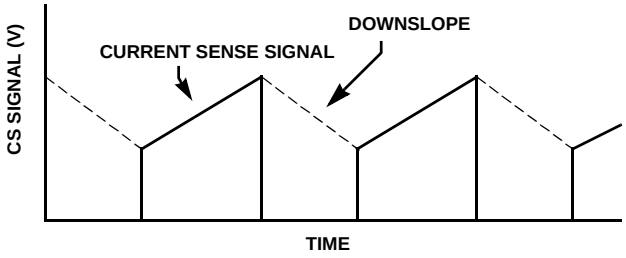


FIGURE 6. CURRENT SENSE DOWNSLOPE

Slope compensation may added to the CS signal in the following manner.

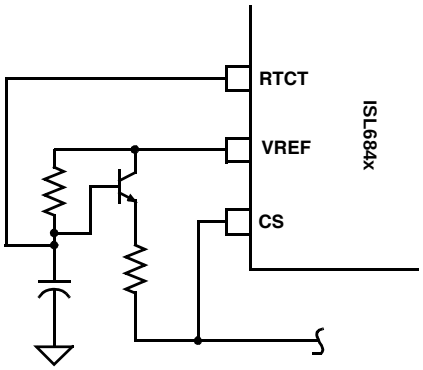


FIGURE 7. SLOPE COMPENSATION

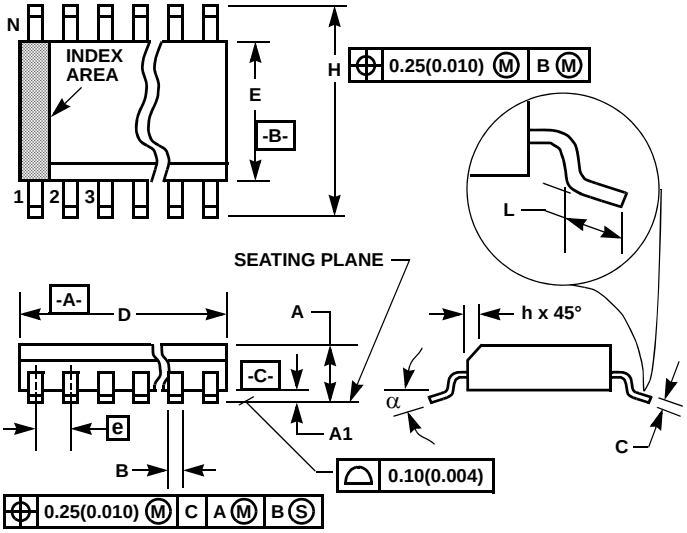
Fault Conditions

A Fault condition occurs if VREF falls below 4.65V. When a Fault is detected OUT is disabled. When VREF exceeds 4.80V, the Fault condition clears, and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

Small Outline Plastic Packages (SOIC)



NOTES:

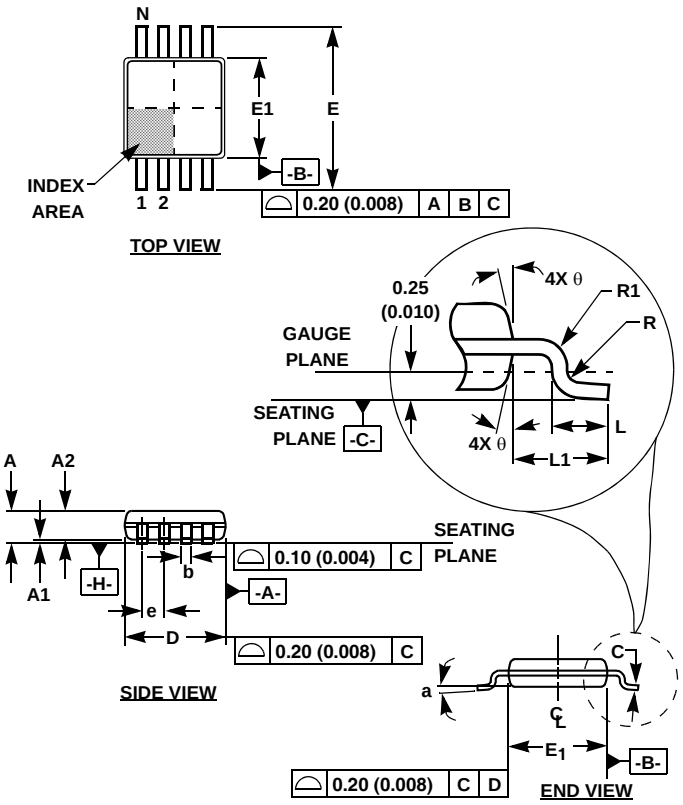
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

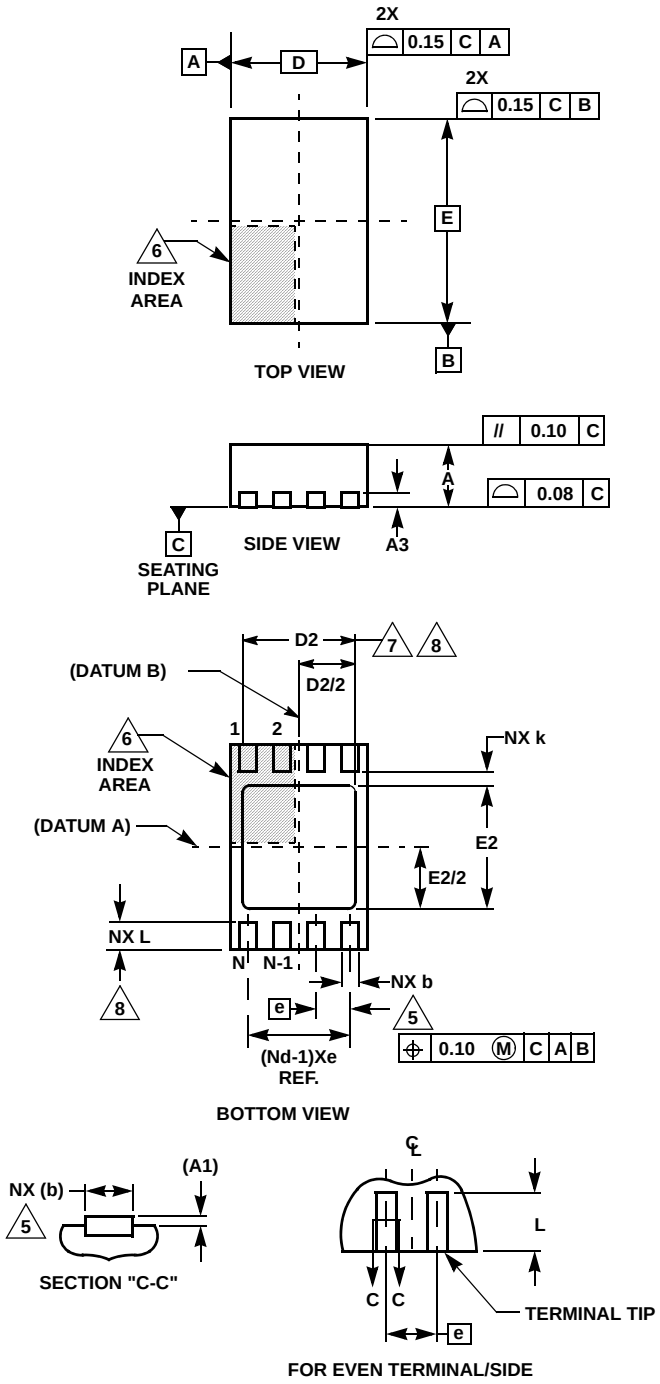
M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

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