Data Sheet | July 25, 2005 | FN9159.4

Advanced Synchronous Rectified Buck MOSFET Drivers with Pre-POR OVP

The ISL6612A and ISL6613A are high frequency MOSFET drivers specifically designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. These drivers combined with HIP63xx or ISL65xx Multi-Phase Buck PWM controllers and N-Channel MOSFETs form complete core-voltage regulator solutions for advanced microprocessors.

The ISL6612A drives the upper gate to 12V, while the lower gate can be independently driven over a range from 5V to 12V. The ISL6613A drives both upper and lower gates over a range of 5V to 12V. This drive-voltage provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

An advanced adaptive zero shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize the dead time. These products add an overvoltage protection feature operational before VCC exceeds its turn-on threshold, at which the PHASE node is connected to the gate of the low side MOSFET (LGATE). The output voltage of the converter is then limited by the threshold of the low side MOSFET, which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial startup.

These drivers also feature a three-state PWM input which, working together with Intersil's multi-phase PWM controllers, prevents a negative transient on the output voltage when the output is shut down. This feature eliminates the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

Features

- Pin-to-pin Compatible with HIP6601 SOIC family
- Dual MOSFET Drives for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-Through Protection
  - Body Diode Detection
  - Auto-zero of $r_{DS(ON)}$ Conduction Offset Effect
- Adjustable Gate Voltage (5V to 12V) for Optimal Efficiency
- 36V Internal Bootstrap Schottky Diode
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency (up to 2MHz)
  - 3A Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- Three-State PWM Input for Output Stage Shutdown
- Three-State PWM Input Hysteresis for Applications With Power Sequencing Requirement
- Pre-POR Overvoltage Protection
- VCC Undervoltage Protection
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- Dual Flat No-Lead (DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Core Regulators for Intel® and AMD® Microprocessors
- High Current DC-DC Converters
- High Frequency and High Efficiency VRM and VRD

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Technical Briefs TB400 and TB417 for Power Train Design, Layout Guidelines, and Feedback Compensation Design

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER**	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6612ACB	0 to 85	8 Ld SOIC	M8.15
ISL6612ACB-T	8 Ld SOIC Tape and Reel		M8.15
ISL6612ACBZ*	0 to 85	8 Ld SOIC (Pb-Free)	M8.15
ISL6612ACBZ-T*	8 Ld SOIC Tape and Reel (Pb-Free)		M8.15
ISL6612ACBZA*	0 to 85	8 Ld SOIC (Pb-Free)	M8.15
ISL6612ACBZA-T*	8 Ld SOIC Tape and Reel (Pb-Free)		M8.15
ISL6612ACR	0 to 85	10 Ld 3x3 DFN	L10.3x3
ISL6612ACR-T	10 Ld 3x3 DFN Tape and Reel		L10.3x3
ISL6612ACRZ*	0 to 85	10 Ld 3x3 DFN (Pb-Free)	L10.3x3
ISL6612ACRZ-T*	10 Ld 3x3 DFN Tape and Reel (Pb-Free)		L10.3x3
ISL6612AECB	0 to 85	8 Ld EPSOIC	M8.15B
ISL6612AECB-T	8 Ld EPSOIC Tape and Reel		M8.15B
ISL6612AECBZ*	0 to 85	8 Ld EPSOIC (Pb-Free)	M8.15B
ISL6612AECBZ-T*	8 Ld EPSOIC Tape and Reel (Pb-Free)		M8.15B
ISL6612AEIB	-40 to +85	8 Ld EPSOIC	M8.15B
ISL6612AEIB-T	8 Ld EPSOIC Tape and Reel		M8.15B
ISL6612AEIBZ*	-40 to +85	8 Ld EPSOIC (Pb-Free)	M8.15B
ISL6612AEIBZ-T*	8 Ld EPSOIC Tape and Reel (Pb-Free)		M8.15B
ISL6612AIB	-40 to +85	8 Ld SOIC	M8.15
ISL6612AIB-T	8 Ld SOIC Tape and Reel		M8.15
ISL6612AIBZ*	-40 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6612AIBZ*-T	8 Ld SOIC Tape and Reel (Pb-free)		M8.15
ISL6612AIR	-40 to +85	10 Ld 3x3 DFN	L10.3x3
ISL6612AIR-T	10 Ld 3x3 DFN Tape and Reel		L10.3x3
ISL6612AIRZ*	-40 to +85	10 Ld 3x3 DFN (Pb-Free)	L10.3x3
ISL6612AIRZ-T*	10 Ld 3x3 DFN Tape and Reel (Pb-Free)		L10.3x3
ISL6613ACB	0 to 85	8 Ld SOIC	M8.15
ISL6613ACB-T	8 Ld SOIC Tape and Reel		M8.15

Ordering Information (Continued)

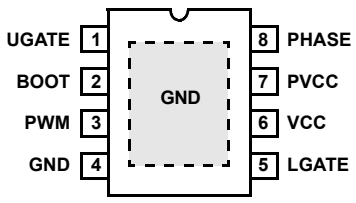
PART NUMBER**	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6613ACBZ*	0 to 85	8 Ld SOIC (Pb-Free)	M8.15
ISL6613ACBZ-T*	8 Ld SOIC Tape and Reel (Pb-Free)		M8.15
ISL6613AECB	0 to 85	8 Ld EPSOIC	M8.15B
ISL6613AECB-T	8 Ld EPSOIC Tape and Reel		M8.15B
ISL6613AECBZ*	0 to 85	8 Ld EPSOIC (Pb-Free)	M8.15B
ISL6613AECBZ-T*	8 Ld EPSOIC Tape and Reel (Pb-Free)		M8.15B
ISL6613AEIB	-40 to +85	8 Ld EPSOIC	M8.15B
ISL6613AEIB-T	8 Ld EPSOIC Tape and Reel		M8.15B
ISL6613AEIBZ*	-40 to +85	8 Ld EPSOIC (Pb-Free)	M8.15B
ISL6613AEIBZ-T*	8 Ld EPSOIC Tape and Reel (Pb-Free)		M8.15B
ISL6613ACR	0 to 85	10 Ld 3x3 DFN	L10.3x3
ISL6613ACR-T	10 Ld 3x3 DFN Tape and Reel		L10.3x3
ISL6613ACRZ*	0 to 85	10 Ld 3x3 DFN (Pb-Free)	L10.3x3
ISL6613ACRZ-T*	10 Ld 3x3 DFN Tape and Reel (Pb-Free)		L10.3x3
ISL6613AIB	-40 to +85	8 Ld SOIC	M8.15
ISL6613AIB-T	8 Ld SOIC Tape and Reel		M8.15
ISL6613AIBZ*	-40 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6613AIBZ*-T	8 Ld SOIC Tape and Reel (Pb-free)		M8.15
ISL6613AIR	-40 to +85	10 Ld 3x3 DFN	L10.3x3
ISL6613AIR-T	10 Ld 3x3 DFN Tape and Reel		L10.3x3
ISL6613AIRZ*	-40 to +85	10 Ld 3x3 DFN (Pb-Free)	L10.3x3
ISL6613AIRZ-T*	10 Ld 3x3 DFN Tape and Reel (Pb-Free)		L10.3x3

*Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

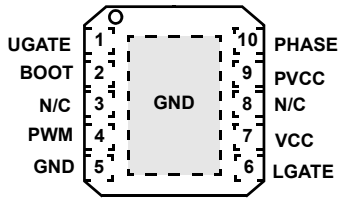
Check website for availability.

Pinouts

ISL6612ACB, ISL6612AIB, ISL6613ACB, ISL6613AIB (SOIC)
ISL6612AECB, ISL6612AEIB, ISL6613AECB, ISL6613AEIB (EPSOIC)
TOP VIEW

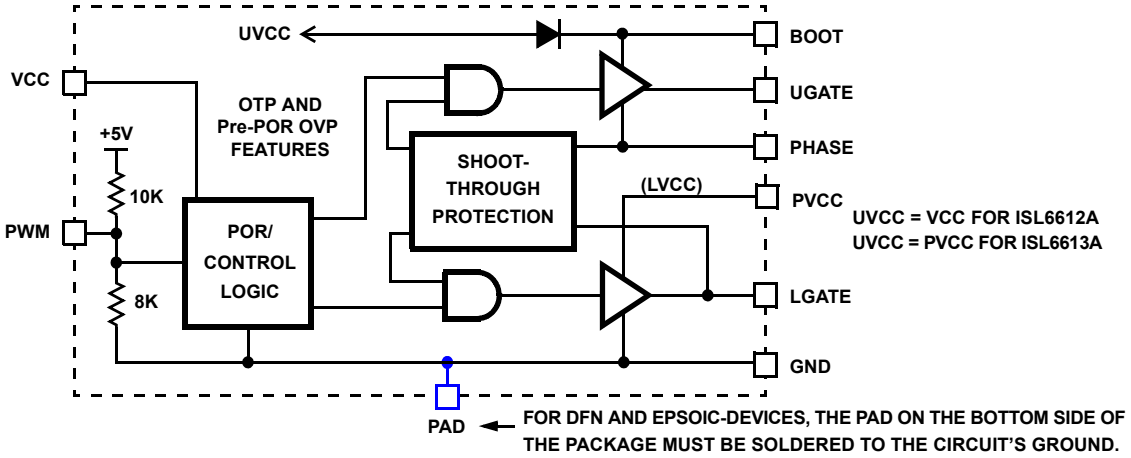


ISL6612ACR, ISL6612AIR, ISL6613ACR, ISL6613AIR (10L 3X3 DFN)
TOP VIEW

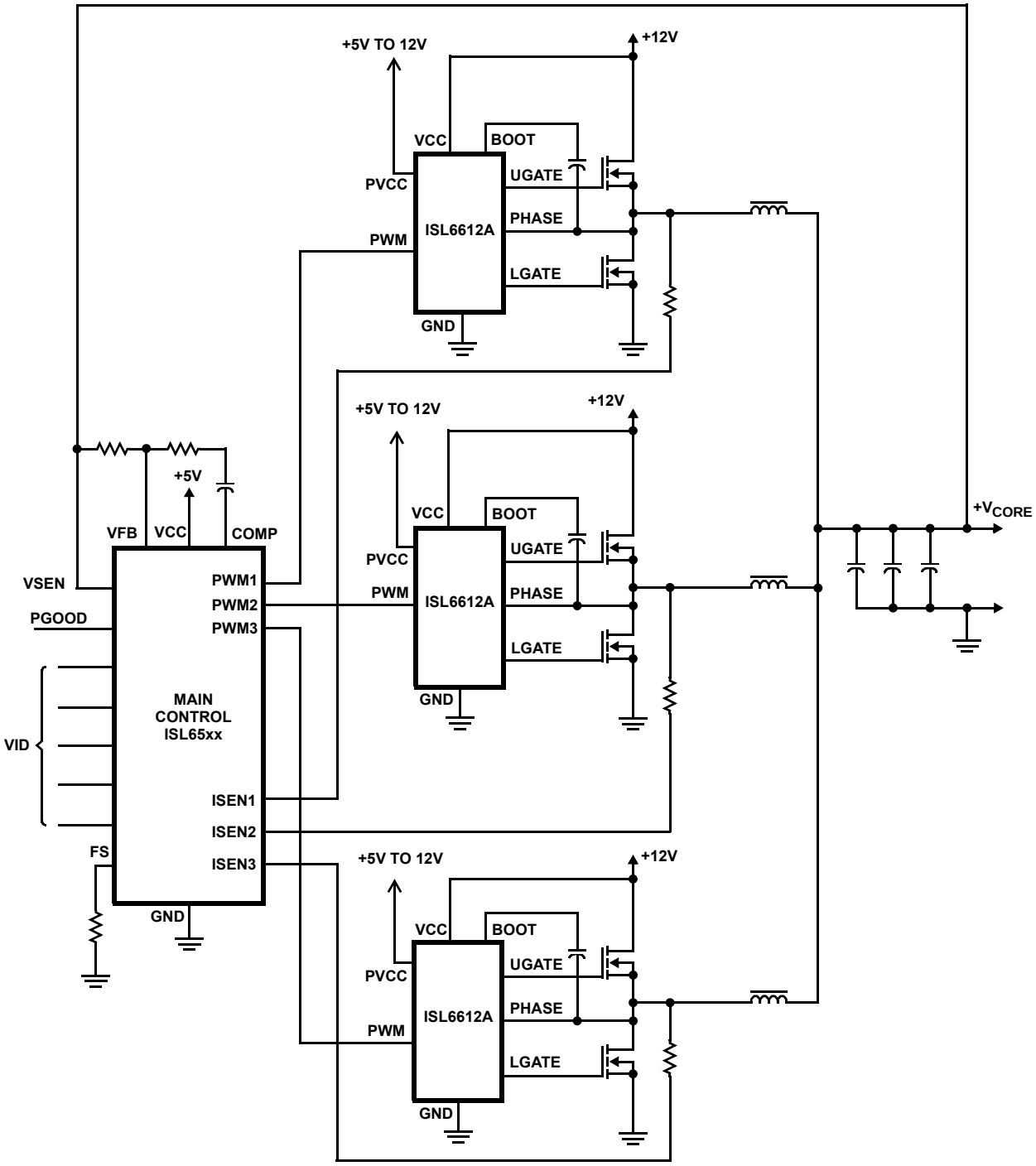


Block Diagram

ISL6612A AND ISL6613A



Typical Application - 3 Channel Converter Using ISL65xx and ISL6612A Gate Drivers



Absolute Maximum Ratings

Supply Voltage (VCC) 15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) 36V
Input Voltage (V_{PWM}) . . . . . GND - 0.3V to 7V
UGATE . . . . . V_{PHASE} - 0.3V_{DC} to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
LGATE . . . . . GND - 0.3V_{DC} to V_{PVCC} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{PVCC} + 0.3V
PHASE . . . . . GND - 0.3V_{DC} to 15V_{DC}
GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT-GND}$<36V)
ESD Rating
Human Body Model . . . . . Class I JEDEC STD

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Maximum Operating Junction Temperature . . . . . 125°C
Supply Voltage, VCC . . . . . 12V ±10%
Supply Voltage Range, PVCC . . . . . 5V to 12V ±10%

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	100	N/A
EPSOIC Package (Notes 2, 3)	50	7
DFN Package (Notes 2, 3)	48	7

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	ISL6612A, f_{PWM} = 300kHz, V_{VCC} =12V	-	7.2	-	mA
		ISL6613A, f_{PWM} = 300kHz, V_{VCC} =12V	-	4.5	-	mA
	I_{VCC}	ISL6612A, f_{PWM} = 1MHz, V_{VCC} = 12V	-	11	-	mA
		ISL6613A, f_{PWM} = 1MHz, V_{VCC} = 12V	-	5	-	mA
Gate Drive Bias Current	I_{PVCC}	ISL6612A, f_{PWM} = 300kHz, V_{PVCC} = 12V	-	2.5	-	mA
		ISL6613A, f_{PWM} = 300kHz, V_{PVCC} = 12V	-	5.2	-	mA
	I_{PVCC}	ISL6612A, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	7	-	mA
		ISL6613A, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	13	-	mA
POWER-ON RESET AND ENABLE						
VCC Rising Threshold		T_A = 0°C to 85°C	9.35	9.80	10.00	V
VCC Rising Threshold		T_A = -40°C to 85°C	8.35	9.80	10.00	V
VCC Falling Threshold		T_A = 0°C to 85°C	7.35	7.60	8.00	V
VCC Falling Threshold		T_A = -40°C to 85°C	6.35	7.60	8.00	V
PWM INPUT (See Timing Diagram on Page 7)						
Input Current	I_{PWM}	V_{PWM} = 5V	-	450	-	µA
		V_{PWM} = 0V	-	-400	-	µA
PWM Rising Threshold		VCC = 12V	-	3.00	-	V
PWM Falling Threshold		VCC = 12V	-	2.00	-	V
Typical Three-State Shutdown Window		VCC = 12V	1.80	-	2.40	V
Three-State Lower Gate Falling Threshold		VCC = 12V	-	1.50	-	V
Three-State Lower Gate Rising Threshold		VCC = 12V	-	1.00	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Three-State Upper Gate Rising Threshold		VCC = 12V	-	3.20	-	V
Three-State Upper Gate Falling Threshold		VCC = 12V	-	2.60	-	V
Shutdown Holdoff Time	t_{TSSHD}		-	245	-	ns
UGATE Rise Time	t_{RU}	V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time	t_{RL}	V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time	t_{FU}	V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t_{FL}	V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Propagation Delay (Note 4)	t_{PDHU}	V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Propagation Delay (Note 4)	t_{PDHL}	V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
UGATE Turn-Off Propagation Delay (Note 4)	t_{PDLU}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LGATE Turn-Off Propagation Delay (Note 4)	t_{PDLL}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LG/UG Three-State Propagation Delay (Note 4)	t_{PDTS}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
OUTPUT (Note 4)						
Upper Drive Source Current	I_{U_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	1.25	-	A
Upper Drive Source Impedance	R_{U_SOURCE}	150mA Source Current	1.25	2.0	3.0	Ω
Upper Drive Sink Current	I_{U_SINK}	V_{PVCC} = 12V, 3nF Load	-	2	-	A
Upper Drive Transition Sink Impedance	$R_{U_SINK_TR}$	70ns With Respect To PWM Falling	-	1.3	2.2	Ω
Upper Drive DC Sink Impedance	$R_{U_SINK_DC}$	150mA Source Current	0.9	1.65	3.0	Ω
Lower Drive Source Current	I_{L_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	2	-	A
Lower Drive Source Impedance	R_{L_SOURCE}	150mA Source Current	0.85	1.25	2.2	Ω
Lower Drive Sink Current	I_{L_SINK}	V_{PVCC} = 12V, 3nF Load	-	3	-	A
Lower Drive Sink Impedance	R_{L_SINK}	150mA Sink Current	0.60	0.80	1.35	Ω

NOTE:

4. Guaranteed by design. Not 100% tested in production.

Functional Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
SOIC	DFN		
1	1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
-	3, 8	N/C	No Connection.
3	4	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
4	5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	7	VCC	Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
7	9	PVCC	This pin supplies power to both upper and lower gate drives in ISL6613A; only the lower gate drive in ISL6612A. Its operating range is +5V to 12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
9	11	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Description

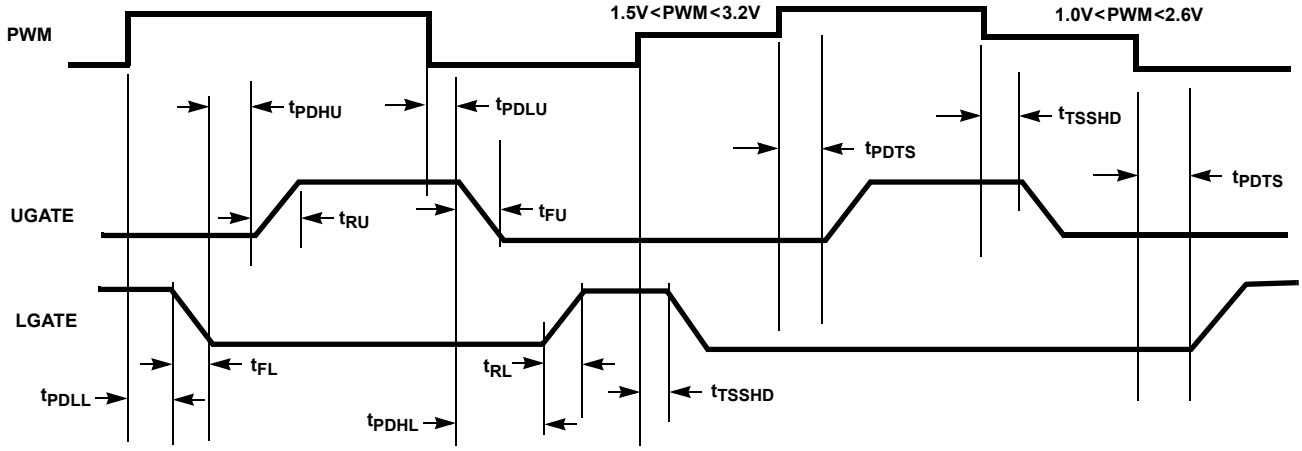


FIGURE 1. TIMING DIAGRAM

Operation

Designed for versatility and speed, the ISL6612A and ISL6613A MOSFET drivers control both high-side and low-side N-Channel FETs of a half-bridge power train from one externally provided PWM signal.

Prior to VCC exceeding its POR level, the Pre-POR overvoltage protection function is activated during initial startup; the upper gate (UGATE) is held low and the lower gate (LGATE), controlled by the Pre-POR overvoltage protection circuits, is connected to the PHASE. Once the VCC voltage surpasses the VCC Rising Threshold (See Electrical Specifications), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the PHASE voltage and determines the upper gate delay time [t_{PDHU}]. This prevents both the lower and upper MOSFETs from conducting simultaneously. Once this delay period is complete, the upper gate drive begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM results in the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, t_{PDHL}. The PHASE voltage and the UGATE voltage are monitored, and the lower gate is allowed to rise after PHASE drops below a level or the voltage of UGATE to PHASE reaches a level depending upon the current direction (See next section for details). The lower gate then rises [t_{RL}], turning on the lower MOSFET.

thresholds outlined in the ELECTRICAL SPECIFICATIONS

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

These drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFETs' body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.2V/+0.8V trip point for a forward/reverse current, at which time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing from false detection of the -0.2V phase level during $r_{DS(ON}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. During the phase detection, the disturbance of LGATE's falling transition on the PHASE node is blanked out to prevent falsely tripping. Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

Three-State PWM Input

A unique feature of these drivers and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling

determine when the lower and upper gates are enabled.

This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

In addition, more than 400mV hysteresis also incorporates into the three-state shutdown window to eliminate PWM input oscillations due to the capacitive load seen by the PWM input through the body diode of the controller's PWM output when the power-up and/or power-down sequence of bias supplies of the driver and PWM controller are required.

Power-On Reset (POR) Function

During initial startup, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds 9.8V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the falling threshold of 7.6V (typically), operation of the driver is disabled.

Pre-POR Overvoltage Protection

Prior to VCC exceeding its POR level, the upper gate is held low and the lower gate is controlled by the overvoltage protection circuits during initial startup. The PHASE is connected to the gate of the low side MOSFET (LGATE), which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial startup. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

When VCC drops below its POR level, both gates pull low and the Pre-POR overvoltage protection circuits are not activated until VCC resets.

Internal Bootstrap Device

Both drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above UVCC + 5V and its capacitance value can be chosen from the following equation:

$$C_{BOOT_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT_CAP}} \quad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet UVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the data sheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 53nC for UVCC (i.e. PVCC in ISL6613A, VCC in ISL6612A) = 12V. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.267µF is required.

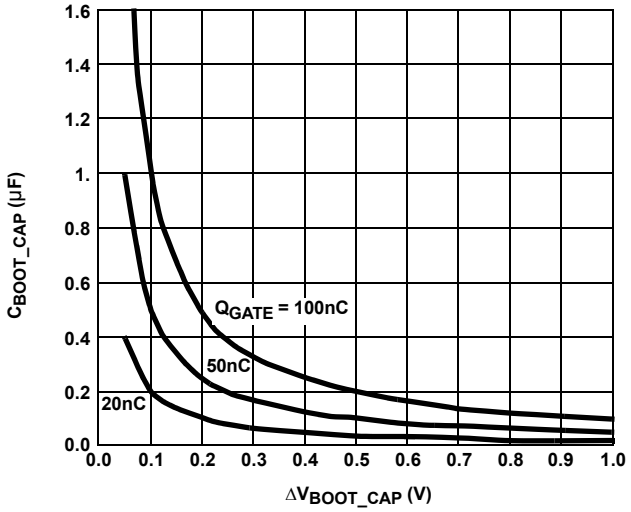


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6612A and ISL6613A provide the user flexibility in choosing the gate drive voltage for efficiency optimization. The ISL6612A upper gate drive is fixed to VCC [+12V], but the lower drive rail can range from 12V down to 5V depending on what voltage is applied to PVCC. The ISL6613A ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW at room temperature, while the power dissipation capacity in the EPSOIC and DFN packages, with an exposed heat escape pad, is more than 2W and 1.5W, respectively. Both EPSOIC and DFN packages are more suitable for high frequency applications. See Layout Considerations paragraph for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for

the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively,

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q \bullet VCC \quad \text{(EQ. 2)}$$

$$P_{Qg_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \quad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The I_Q*VCC product is the quiescent power of the driver without capacitive load and is typically 116mW at 300kHz.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg_Q1}}{2}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

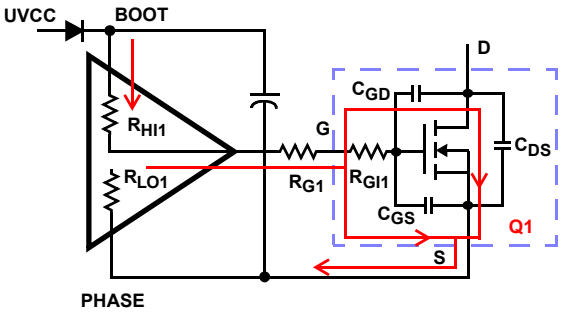


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

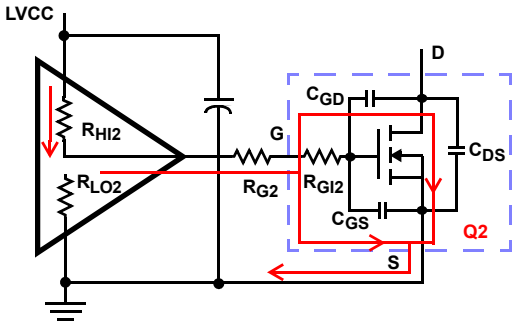


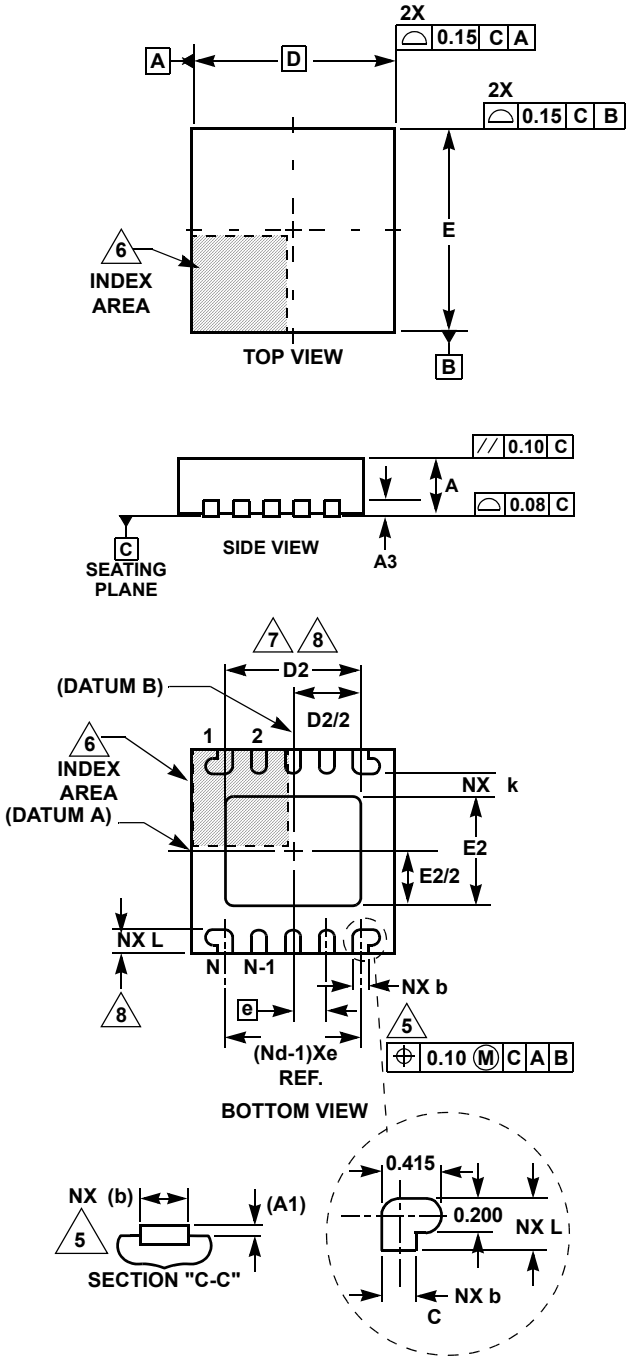
FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Layout Considerations

For heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Place each channel power component as close to each other as possible to reduce PCB copper losses and PCB parasitics: shortest distance between DRAINs of upper FETs and SOURCEs of lower FETs; shortest distance between DRAINs of lower FETs and the power ground. Thus, smaller amplitudes of positive and negative ringing are on the switching edges of the PHASE node. However, some space in between the power components is required for good airflow. The traces from the drivers to the FETs should be kept short and wide to reduce the inductance of the traces and to promote clean drive signals.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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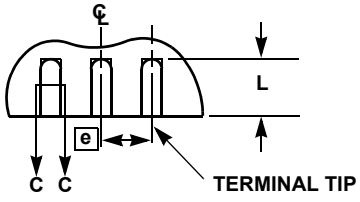
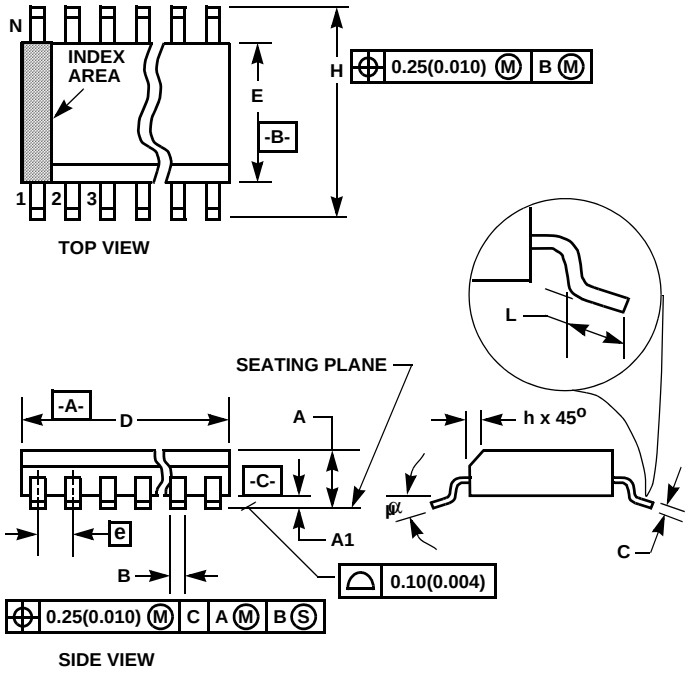
NOTES:

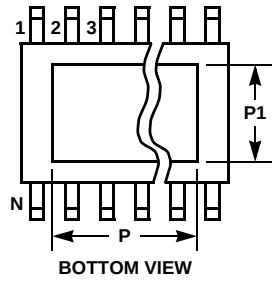
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Small Outline Exposed Pad Plastic Packages (EPSOIC)





M8.15B

8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.43	1.68	-
A1	0.001	0.005	0.03	0.13	-
B	0.0138	0.0192	0.35	0.49	9
C	0.0075	0.0098	0.19	0.25	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.31	3.39	4
e	0.050 BSC		1.27 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.64	6
N	8		8		7
α	0°	8°	0°	8°	-
P	-	0.094	-	2.387	11
P1	-	0.094	-	2.387	11

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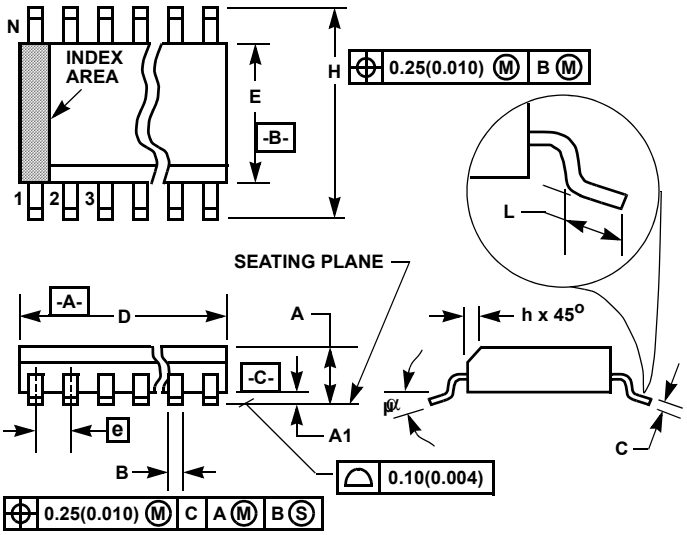
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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