Triple Output Regulator with Single Synchronous Buck and Dual LDO

The ISL6455 is a highly integrated triple output regulator which provides a single chip solution for FPGAs and wireless chipset power management. The device integrates an adjustable high efficiency synchronous buck regulator with two adjustable ultra low noise LDO regulators. Either the ISL6455 or ISL6455A can be selected based on whether 3.3V ±10% or 5V ±10% is required as an input voltage.

The synchronous current mode control PWM regulator with integrated N- Channel and P-Channel power MOSFET provides adjustable voltages based on external resistor setting. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz, allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The ISL6455 also has two LDO adjustable regulators using internal PMOS transistors as pass devices. LDO2 features ultra low noise typically below $30\mu V_{RMS}$ to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6455 also integrates a $\overline{\text{RESET}}$ function, which eliminates the need for additional RESET IC required in WLAN and other applications. The IC asserts a $\overline{\text{RESET}}$ signal whenever the V_{IN} supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after V_{IN} has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include overcurrent protection and thermal shutdown for all of the three outputs. High integration and the thin Quad Flat No-lead (QFN) package makes ISL6455 an ideal choice for powering FPGAs and small form factor wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

Ordering Information

PART NUMBER* (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6455IRZ	64 55IRZ	-40 to +85	24 Ld QFN	L24.4x4B
ISL6455AIRZ	64 55AIRZ	-40 to +85	24 Ld QFN	L24.4x4B

Add “-TK” or T5K suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Fully integrated synchronous buck regulator + dual LDO
- PWM output voltage adjustable.
  - 0.8V to 2.5V with ISL6455 (VIN = 3.3V)
  - 0.8V to 3.3V with ISL6455A (VIN = 5.0V)
- High output current. 600mA
- Dual LDO adjustable options
  - LDO1, 1.2V to Vin - 0.3V (3.3Vmax). 300mA
  - LDO2, 1.2V to Vin - 0.3V (3.3Vmax). 300mA
- Ultra-compact DC/DC converter design
- Stable with small ceramic output capacitors and no load
- High conversion efficiency
- Low shutdown supply current
- Low dropout voltage for LDOs
  - LDO1 . . . . . 150mV (typical) at 300mA
  - LDO2 . . . . . 150mV (typical) at 300mA
- Low output voltage noise
  - $<30\mu V_{RMS}$ (typical) for LDO2 (VCO supply)
- PG_LDO and PG_PWM (PWM and LDO) outputs
- Extensive circuit protection and monitoring features
  - PWM overvoltage protection
  - Overcurrent protection
  - Shutdown
  - Thermal shutdown
- Integrated $\overline{\text{RESET}}$ output for microprocessor reset
- Proven reference design for total WLAN system solution
- QFN package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale package footprint Improves PCB efficiency and is thinner in Profile
- Pb-free (RoHS compliant)

Applications

- WLAN cards
  - PCMCIA, Cardbus32, MiniPCI cards
  - Compact flash cards
- Hand-held instruments

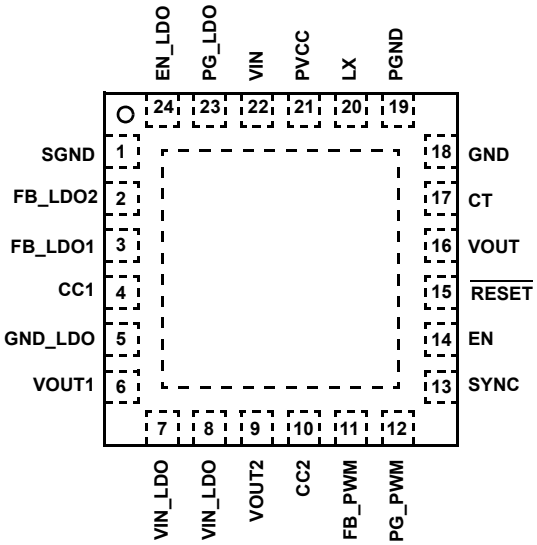
Related Literature

- TB363 - Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)
- TB389 - PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

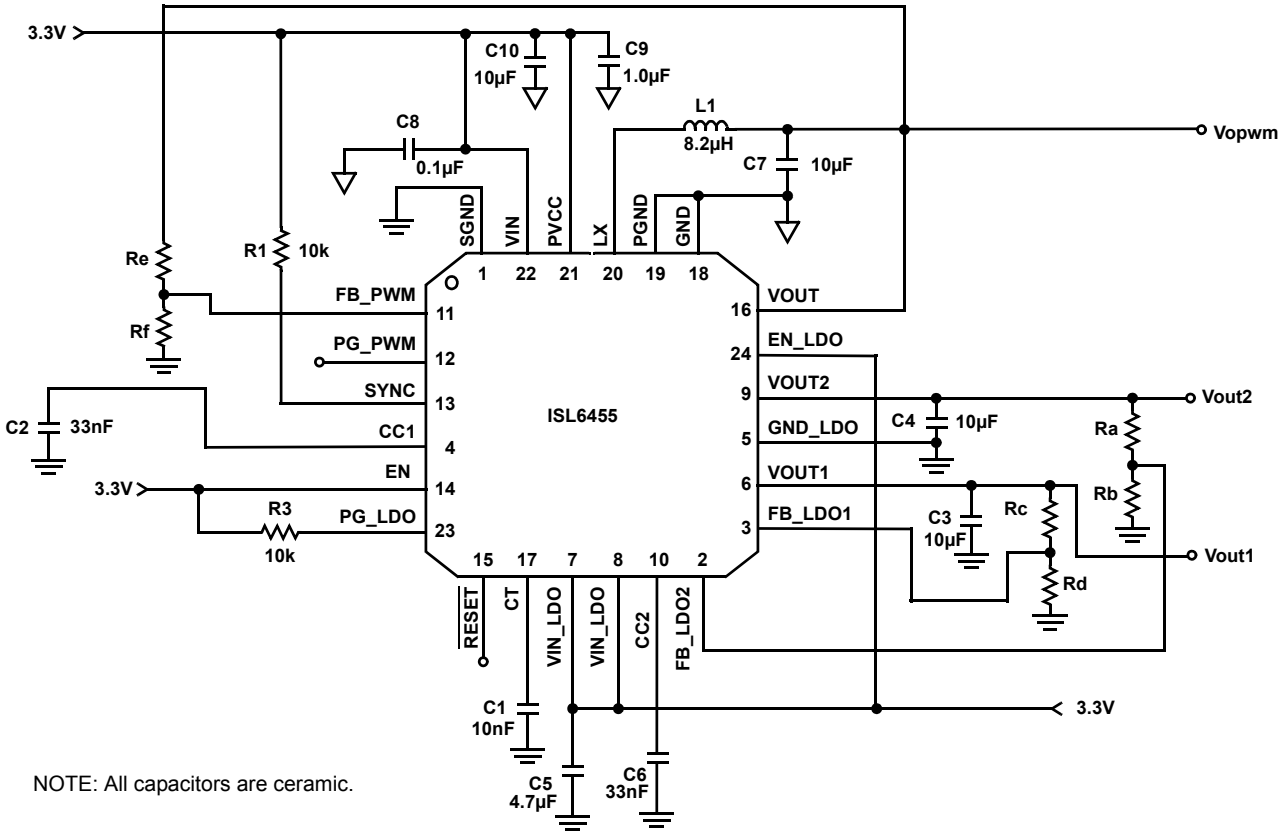
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pinout

ISL6455, ISL6455A (24 LD QFN)
TOP VIEW

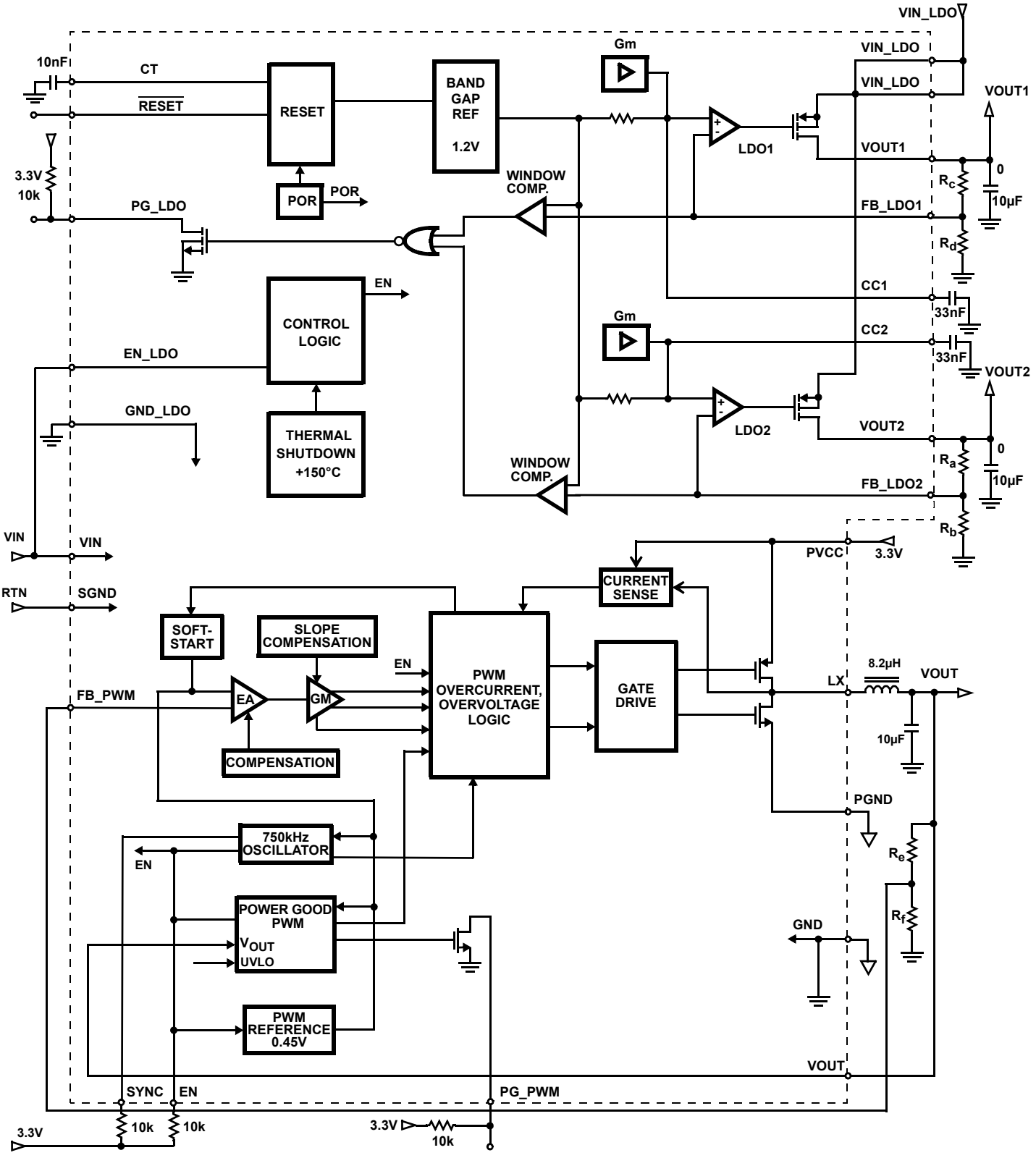


Typical Application Schematic



NOTE: All capacitors are ceramic.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{IN}, PV_{CC}, V_{IN}_LDO . . . . . GND -0.3V to +6.0V
Max Continuous Output Current 600mA

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN (Note 1)	42	6

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Range . . . . . -55°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = V_{IN}_LDO = PV_{CC} = 3.3V for ISL6455 and 5.0V for the ISL6455A, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = -40°C to +85° (Note 2), typical values are at T_A = +25°C.Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY					
VIN_PWM Supply Voltage Range	ISL6455	3.0	3.3	3.6	V
	ISL6455A	4.2	5.0	5.5	V
VIN_LDO Supply Voltage Range		3.0	-	5.5	V
Operating Supply Current (Note 4) for ISL6455	V_{IN} = V_{IN}_LDO = PV_{CC} = 3.3V f_{SW} = 750kHz, C_{OUT} = 10µF, I_L = 0mA	-	2.5	3.1	mA
Operating Supply Current (Note 4) for ISL6455A	V_{IN} = V_{IN}_LDO = PV_{CC} = 5.0V f_{SW} = 750kHz, C_{OUT} = 10µF, I_L = 0mA	-	3.5	4.5	mA
Shutdown Supply Current ISL6455 and ISL6455A	EN = EN_LDO = GND	-	5	10	µA
Input Bias Current (EN pin)	EN = EN_LDO = GND/V_{IN}	-1.5	1.0	1.5	µA
VIN_PWM UVLO Threshold for ISL6455	V_{TR}	2.55	2.65	2.71	V
	V_{TF}	2.51	2.56	2.61	V
VIN_PWM UVLO Threshold for ISL6455A	V_{TR}	3.94	4.05	4.13	V
	V_{TF}	3.78	3.89	3.97	V
VIN_LDO UVLO Threshold for ISL6455 and ISL6455A	V_{TR}	2.46	2.64	2.82	V
	V_{TF}	2.53	2.59	2.66	V
Thermal Shutdown Temperature (Note 6)	Rising Threshold	-	150	-	°C
Thermal Shutdown Hysteresis (Note 6)		-	20	-	°C
SYNCHRONOUS BUCK PWM REGULATOR					
Output Voltage	ISL6455	0.8	-	2.5	V
	ISL6455A	0.8	-	3.3	V
FB_PWM Initial Voltage Accuracy (Note 7)	V_{REF} = 0.45V, I_{OUT} = 3mA, T_A = -40°C to +85°C	-0.9	-	0.9	%
FB_PWM Line Regulation	I_O = 3mA, V_{IN} = PV_{CC} = 3.0V - 3.6V (ISL6455) or 4.2V - 5.5V (6455A)	-0.5	-	0.5	%
FB_PWM Load Regulation	I_O = 3mA to 500mA, V_{IN} = PV_{CC} = 3.0V - 3.6V (ISL6455) or 4.2V - 5.5V (ISL6455A)	-1.1	-	+1.1	%
Peak Output Current Limit		700mA	-	1300	mA
PMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	170	-	mΩ

Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = V_{IN}_LDO = PV_{CC} = 3.3V for ISL6455 and 5.0V for the ISL6455A, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = -40°C to +85° (Note 2), typical values are at T_A = +25°C.Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
NMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	50	-	mΩ
Efficiency	I_{OUT} = 200mA, V_{IN} = 3.3V, V_{OUT} = 1.8V	-	93	-	%
Soft-Start Time	4096 Clock Cycles @ 750kHz	-	5.5	-	ms
OSCILLATOR					
Oscillator Frequency	T_A = -40°C to +85°C	620	750	880	kHz
Frequency Synchronization Range (f_{SYNC})	Clock signal on SYNC pin	500	-	1000	kHz
SYNC High Level Input Voltage	As % of V_{IN}	70	-	-	%
SYNC Low Level Input Voltage	As % of V_{IN}	-	-	30	%
Sync Input Leakage Current	SYNC = GND or V_{IN}	-1.0	-	1.0	µA
Min Duty Cycle of External Clock Signal (Note 6)		-	20	-	%
Max Duty Cycle of External Clock Signal (Note 6)		-	80	-	%
PG_PWM					
Rising Threshold	1.2mA source/sink, FB_PWM vs 0.45V V_{REF}	+5.5	8.0	+10.5	%
Falling Threshold	FB_PWM vs 0.45V V_{REF}	-10.5	-8.0	-5.5	%
Leakage Current	PG_PWM = GND or V_{IN}	-	0.01	0.1	µA
LDO1 SPECIFICATIONS					
Output Voltage Range	VIN_VLDO > 3.0V	1.2	-	2.7	V
Output Voltage Range	VIN_VLDO > 3.6V	1.2	-	3.3	V
FB_LDO1 Voltage Accuracy (Note 7)	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (Note 6)	V_{IN} = 3.6V	300	-	-	mA
Output Current Limit (Note6)		350	420	600	mA
Dropout Voltage (Note 4)	I_{OUT} = 300mA	-	150	300	mV
FB_LDO1 Line Regulation	I_{OUT} = 10mA, VIN_LDO = 3.0-5.5V	-0.5	-	0.5	%/V
FB_LDO1 Load Regulation	I_{OUT} = 10mA to 300mA	-0.5	-	0.5	%
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µ2F	-	65	-	μV_{RMS}
	C_{OUT} = 10µF	-	60	-	μV_{RMS}
LDO2 SPECIFICATIONS					
Output Voltage Range	VIN_VLDO > 3.0V	1.2	-	2.7	V
Output Voltage Range	VIN_VLDO > 3.6V	1.2	-	3.3	V
FB_LDO2 Voltage Accuracy (Note 7)	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (Note 6)	V_{IN} = 3.6V	300	-	-	mA
Output Current Limit (Note 6)		350	420	600	mA
Dropout Voltage (Note 4)	I_{OUT} = 300mA	-	150	300	mV
FB_LDO2 Line Regulation	I_{OUT} = 10mA, VIN_LDO = 3.0V - 5.5V	-0.5	-	0.5	%/V
FB_LDO2 Load Regulation	I_{OUT} = 10mA to 300mA	-0.5	-	0.5	%

Electrical Specifications

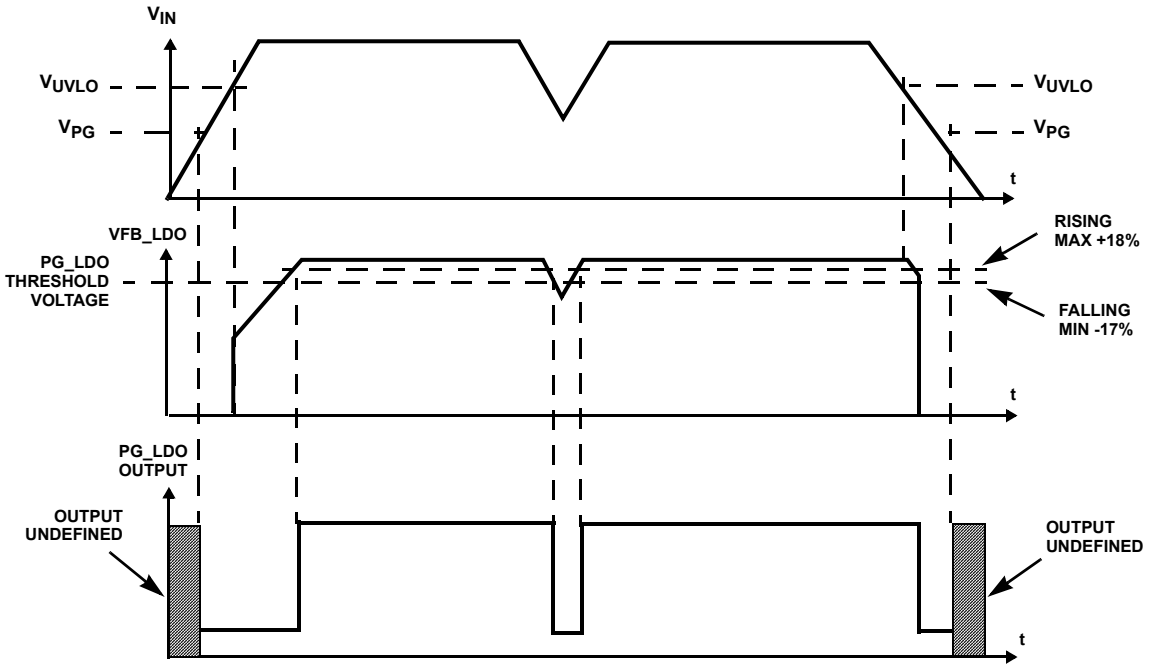
Recommended operating conditions unless otherwise noted. V_{IN} = $V_{IN_}$LDO = PV_{CC} = 3.3V for ISL6455 and 5.0V for the ISL6455A, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = -40°C to +85° (Note 2), typical values are at T_A = +25°C.Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	30	-	μV_{RMS}
	C_{OUT} = 10µF	-	20	-	μV_{RMS}
ENABLE (EN and (EN_LDO)					
EN High Level Input Voltage	As % of VIN	70	-	-	%
EN Low Level Input Voltage	As % of VIN	-	-	30	%
RESET BLOCK SPECIFICATIONS					
$\overline{\text{RESET}}$ (reset released)	ISL6455, ISOURCE = 500µA, VIN = 2.90V	0.8 x V_{CC}	-	-	V
$\overline{\text{RESET}}$ (reset asserted)	ISL6455, ISINK = 1.2mA, VIN = 2.50V	-	-	0.3	V
$\overline{\text{RESET}}$ Rising Threshold	ISL6455	2.71	2.77	2.84	V
$\overline{\text{RESET}}$ Falling Threshold	ISL6455	2.69	2.75	2.81	V
$\overline{\text{RESET}}$ (reset released)	ISL6455A, ISOURCE = 800µA, VIN = 4.70V	0.8 x V_{CC}	-	-	V
$\overline{\text{RESET}}$ (reset asserted)	ISL6455A, ISINK = 3.2mA, VIN = 4.10V	-	-	0.4	V
$\overline{\text{RESET}}$ Rising Threshold	ISL6455A	4.19	4.27	4.35	V
$\overline{\text{RESET}}$ Falling Threshold	ISL6455A	4.16	4.24	4.32	V
$\overline{\text{RESET}}$ Threshold Hysteresis	ISL6455	-	20	-	mV
$\overline{\text{RESET}}$ Threshold Hysteresis	ISL6455A	-	30	-	mV
$\overline{\text{RESET}}$ Active Timeout Period (Note 5)	C_T = 0.01µF	-	25	-	ms
POWER GOOD (PG_LDO)					
Minimum Input Voltage for Valid PG_LDO		-	1.2	-	V
PGOOD Threshold (Rising)	FB_LDO vs 1.184V VREF	+11	+15	+17	%
PGOOD Threshold (Falling)		-17	-15	-11	%
PGOOD Output Voltage Low	I_{OL} = 1.2mA	-	-	0.4	V
PGOOD Output Leakage Current	PG_LDO = GND or VIN	-	0.01	0.1	µA
PWM OUTPUT OVERVOLTAGE					
Overvoltage Threshold	FB_PWM vs 0.45V VREF	28	31	34	%

NOTES:

3. This is the V_{IN} current consumed when the device is active but not switching. Does not include gate drive current.
4. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 50mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
5. The RESET timeout period is linear with CT at the slope of 2.5ms/nF. Thus, at 10nF (0.01µF) the RESET time is 25ms; at 1000nF (0.1µF) the RESET time would be 250ms.
6. Limits established by characterization and are not production tested.
7. Add the external feedback resistor mismatch error to get initial V_{OUT} accuracy.

PG_LDO Timing Diagram



NOTE:

8. V_{PG} is the minimum input voltage for a valid PG_LDO.

Pin Descriptions

PVCC - Positive supply for the power (internal FET) stage of the PWM section.

SGND - Analog ground for the PWM. All internal control circuits are referenced to this pin.

EN - The PWM controller is enabled when this pin is HIGH, and disabled when the pin is pulled LOW. It is a CMOS logic-level input (referenced to V_{IN}).

V_{IN}_LDO - This is the input voltage pin for LDO1 and LDO2.

EN_LDO - LDO1 and LDO2 are enabled when this pin is HIGH, and disabled when the pin is pulled LOW. It is a CMOS logic-level input (referenced to V_{IN}).

CT - Timing capacitor pin to set the 25ms minimum pulse width for the $\overline{\text{RESET}}$ signal.

$\overline{\text{RESET}}$ - This pin is the output of the reset supervisory circuit, which monitors VIN_PWM. The IC asserts a $\overline{\text{RESET}}$ signal whenever the supply voltage drops below a preset threshold. It is kept asserted for a minimum of 25ms after V_{CC} (V_{IN}) has risen above the reset threshold. The output is push-pull. The device will continue to operate until V_{IN} drops below the UVLO threshold.

When EN = LOW then $\overline{\text{RESET}}$ = HIGH and the moment EN is made HIGH the RESET will pulse LOW for a period of 25ms minimum (VIN > Reset threshold). If VIN < reset threshold then it will switch low and stay low for a period of 25ms after VIN_PWM crosses the reset threshold.

PG_LDO - This is a high impedance open drain output that provides the status of both LDOs. When either of the outputs are out of regulation, PG_LDO goes LOW. Add a pull-up resistor approximately 10kΩ from PG_LDO to VIN.

CC1 - This is the compensation capacitor connection for LDO1. Connect a 0.033µF capacitor from CC1 to GND_LDO.

CC2 - This is the compensation capacitor connection for LDO2. Connect a 0.033µF capacitor from CC2 to GND_LDO.

V_{OUT2} - This pin is the output of LDO2. Bypass with a minimum 2.2µF, low ESR capacitor to GND_LDO for stable operation.

GND_LDO - Ground pin for LDO1 and LDO2.

V_{OUT1} - This pin is the output of LDO1. Bypass with a minimum 2.2µF, low ESR capacitor to GND_LDO for stable operation.

PGND - Power ground for the PWM controller stage.

V_{OUT} - This I/O pin senses the output voltage of the PWM converter for the purpose of detecting the over and undervoltage conditions.

PG_PWM - This pin is an active pull-down able to sink 1mA (min). This output is HIGH IMPEDANCE when V_{OUT} is within ±8% (typical). For pull-up, add a resistor approximately 10kΩ from PG_PWM to VIN

FB_LDO1 and FB_LDO2 - These pins are used to set the LDO output with the proper selection of resistors. i.e. Ra and Rb for LDO1 and Rc and Rd for LDO2. Resistors should be chosen to provide a minimum current of 200µA load for each LDO output.

LX - The LX pin is the switching node of synchronous buck converter, connected internally at the junction point of the upper MOSFET source and lower MOSFET drain. Connect this pin to the output inductor.

V_{IN} - This pin is the power supply for the PWM controller stage and must be closely decoupled to ground.

SYNC - This is the external clock synchronization input. The device can be synchronized to 500kHz to 1MHz switching frequency. If unused then it should be tied to GND or VCC

GND - Tie this pin to the ground plane with a low impedance, shortest possible path.

FB_PWM- This is used to set the value of the output voltage of the PWM with external resistors Re and Rf.

Functional Description

The ISL6455 is a 3-in-1 multi-output regulator designed for FPGA and wireless chipset power applications. The device integrates a single synchronous buck regulator with dual LDOs. The PWM output can be set by choosing appropriate values for Re and Rf. At a setting of 1.8V the synchronous buck regulator provides for an efficiency greater than 92%. The LDO1 can be set with resistor pair Rc and Rd. The LDO2 can be set with the resistor pair Ra and Rb. Undervoltage lock-out (UVLO) prevents the converter from turning on when the input voltage is less than 2.6V typical.

Additional blocks include output overcurrent protection, thermal sensor, PGOOD detectors, RESET function and shutdown logic.

Synchronous Buck Regulator

The synchronous buck regulator with integrated N-Channel and P-Channel power MOSFETs and external voltage setting resistors provides for adjustable voltages from the PWM. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The PWM architecture uses a peak current mode control scheme with internal slope compensation. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The error amplifier sets the threshold for the PWM comparator. The high side switch is turned off when the sensed inductor current reaches this threshold. After a minimum dead time preventing shoot through current, the low side N-Channel MOSFET will be turned on, and the current ramps down again. As the clock cycle is completed, the low side switch will be turned off and the next clock cycle starts.

The control loop is internally compensated reducing the amount of external components.

The switch current is internally sensed and the maximum peak current limit is 1300mA.

Synchronization

The typical operating frequency for the converter is 750kHz if no clock signal is applied to SYNC pin. It is possible to synchronize the converter to an external clock within a frequency range from 500kHz to 1MHz. The device automatically detects the rising edge of the first clock and will synchronize immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch-over will be initiated if no rising edge on the SYNC pin is detected for a duration of two internal 1.3µs clock cycles.

Soft-Start

As the EN (Enable) pin goes high, the soft-start function will generate an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high in-rush currents. The soft-start duration is typically 5.5ms with 750kHz switching frequency. When the soft-start is completed, the error amplifier will be connected directly to the internal voltage reference. The SYNC input is ignored during soft-start.

Enable PWM

Logic low on EN pin forces the PWM section into shutdown. In shutdown all the major blocks of the PWM including power switches, drivers, voltage reference, and oscillator are turned off.

Power Good (PG_PWM)

When chip is enabled, this output is asserted HIGH, when V_{OUT} is within 8% of V_{OPWM} value and active low outside this range. When the PWM is disabled, the output is active low.

Leave the PG_PWM pin unconnected when not used.

PWM Overvoltage and Overcurrent Protection

The PWM output current is sampled at the end of each PWM cycle. Should it exceed the overcurrent limit, a 4-bit up/down counter counts up two LSB. Should it not be in overcurrent, the counter counts down one LSB, (but the counter will not "rollover" or count below 0000). If > 33% of the PWM cycles go into overcurrent, the counter rapidly reaches count 1111 and the PWM output is shut down and the soft-start counter is reset. After 16 clocks the PWM, output is enabled and the SS cycle is started.

If V_{OUT} exceeds the overvoltage limit for 32 consecutive clock cycles, the PWM output is shut off and the SS counters reset. The chip waits for the output voltage to go below undervoltage (8% below nominal) then goes through two dummy soft-start cycles (PWM disabled for 2 SS cycles = 11ms) and then starts a normal soft-start cycle.

PG_LDO

PG_LDO is an open drain pulldown NMOS output that will sink 1mA at 0.4V maximum. It goes to the active low state if either LDO output is out of regulation by a value greater than 15%. When the LDO is disabled, the output is active low.

LDO Regulators

Each LDO consists of a 1.184V reference, error amplifier, MOSFET driver, P-Channel pass transistor, and dual-mode comparator. The voltage is set by means of two resistors: the Ra and Rb for LDO2 and Rc and Rd for LDO1. The 1.184V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference

to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower than the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output.

Internal P-Channel Pass Transistors

Both the LDO Regulators in ISL6455 feature a typical 0.5Ω $r_{DS(on)}$ P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6455 does not have these drawbacks.

Integrated RESET for MAC/Baseband Processors

The ISL6455 includes a microprocessor supervisory block. This block eliminates an extra RESET IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a $\overline{\text{RESET}}$ signal whenever the VIN_PWM supply voltage decreases below a preset threshold, and keeps it asserted for a programmable time period set by the external capacitor CT.

UVLO Reset threshold is always lower than the RESET threshold. This insures that as V_{IN} falls, the reset goes low before the LDOs and PWM are shut off.

Integrator Circuitry

Both ISL6455 LDO Regulators use external 33nF compensation capacitors for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

Shutdown

Driving the EN_LDO pin low will put LDO1 and LDO2 into the shutdown mode. Driving the EN pin low will put the PWM into shutdown mode. Pulling both the EN and EN_LDO pins low simultaneously, puts the ISL6455, ISL6455A in a shutdown mode, and supply current drops to 15µA typical.

Protection Features for the LDOs

Current Limit

The ISL6455 and ISL6455A monitor and control the pass transistor's gate voltage to limit the output current. The current limit for both LDO1 and LDO2 is 330mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6455, ISL6455A. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by +20°C, resulting in an intermittent output condition during continuous thermal overload. Thermal overload protection protects the ISL6455, ISL6455A against fault conditions. For continuous operation, the absolute maximum junction temperature rating of +150°C in not to be exceeded.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6455 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where:

$P1 = I_{OUT1} \times V_{OUT1} \times n$, n is the efficiency of the PWM

$P2 = I_{OUT2} (V_{IN} - V_{OUT2})$

$P3 = I_{OUT3} (V_{IN} - V_{OUT3})$

The maximum power dissipation is:

$P_{max} = (T_{jmax} - T_A)/\theta_{JA}$

Where T_{jmax} = +150°C, T_A = ambient temperature, and θ_{JA} is the thermal resistance from the junction to the surrounding environment.

The ISL6455, ISL6455A package feature an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Additionally, the ISL6455 and ISL6455A ground (GND_LDO and PGND) performs the dual function of providing an electrical connection to system ground and channeling heat away. Connect the exposed bottom pad direct to the GND_LDO ground plane.

Application Information

LDO Regulator Capacitor Selection and Regulator Stability

Capacitors are required at the ISL6455, ISL6455A LDO regulators' input and output for stable operation over the entire load range and the full temperature range. Use >1µF capacitor at the input of LDO regulators, V_{IN}_LDO pins. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provide better PSRR and line transient response. The input

capacitor must be located at a distance of not more than 0.5 inches from the V_{IN} pins of the IC and returned to a clean analog ground. Any good quality ceramic capacitor can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for both LDOs. The ISL6455 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 3.3µF, is recommended for V_{OUT1} for 300mA output current, and 3.3µF is recommended for V_{OUT2} at 300mA load current. There is no upper limit to the output capacitor value. A larger capacitor can reduce noise and improve load transient response, stability and PSRR. A higher value output capacitor (10µF) is recommended for LDO2 when used to power VCO circuitry in wireless chipsets. The output capacitor should be located very close to V_{OUT} pins to minimize impact of PC board inductances and the other end of the capacitor should be returned to a clean analog ground.

PWM Regulator Component Selection

INDUCTOR SELECTION

A 8.2µH typical output inductor is used with the ISL6455 and a 12µH typical with the ISL6455A PWM section. Values less than this may cause stability problems because of the internal compensation of the regulator. The important parameters of the inductor that need to be considered are the current rating of the inductor and the DC resistance of the inductor. The DC resistance of the inductor will influence directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency. In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current. (See Table 1).

TABLE 1. RECOMMENDED INDUCTORS

OUTPUT CURRENT	INDUCTOR VALUE	VENDOR PART NUMBER	COMMENTS
600mA	8.2µH	Coilcraft MSS6122-822MX	ISL6455
600mA	12µH	Coilcraft MSS6122-123MX	ISL6455A

OUTPUT CAPACITOR SELECTION

For the best performance, a low ESR output capacitor is needed. If an output capacitor is selected with an ESR value ≤120mΩ, its RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as shown in Equation 1:

$$I_{RMS(C)_O} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad \text{(EQ. 1)}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor as shown in Equation 2:

$$\Delta V_O = V_O \times \left(\frac{1 - \frac{V_O}{V_I}}{L \times f} \right) \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad \text{(EQ. 2)}$$

Where the highest output voltage ripple occurs at the highest input voltage.

TABLE 2. RECOMMENDED CAPACITORS

CAPACITOR VALUE	ESR/mΩ	VENDOR PART NUMBER	COMMENTS
10µF	<50	TDK C2012X5R0J106M	Ceramic

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10µF and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as shown in Equation 3:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I} \right)} \quad \text{(EQ. 3)}$$

The worst case RMS ripple current occurs at D = 0.5.

Ceramic capacitors show good performance because of their low ESR value, and because they are less sensitive to voltage transients, compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

Output Voltage Setting

The equations for the Output voltages are shown in Equation 4:

$$VOUT = \frac{0.45}{Rf}(Re + Rf)$$

$$VOUT1 = \frac{1.184}{Rb}(Ra + Rb) \quad \text{(EQ. 4)}$$

$$VOUT2 = \frac{1.184}{Rd}(Rc + Rd)$$

The output resistors should be selected so that the minimum output load is about 200µA.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design of ISL6455, ISL6455A based power supply due to the high switching frequency and low noise LDO implementations.

Allocate two board levels as ground planes, with many vias between them to create a low impedance, high-frequency plane. Tie all the device ground pins through multiple vias each to this ground plane, as close to the device as possible. Also tie the exposed pad on the bottom of the device to this ground plane.

Use wide and short traces for the high current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node to minimize the effects of ground noise.

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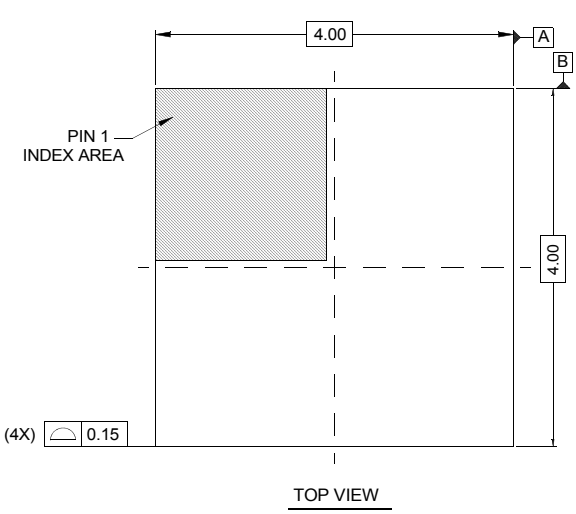
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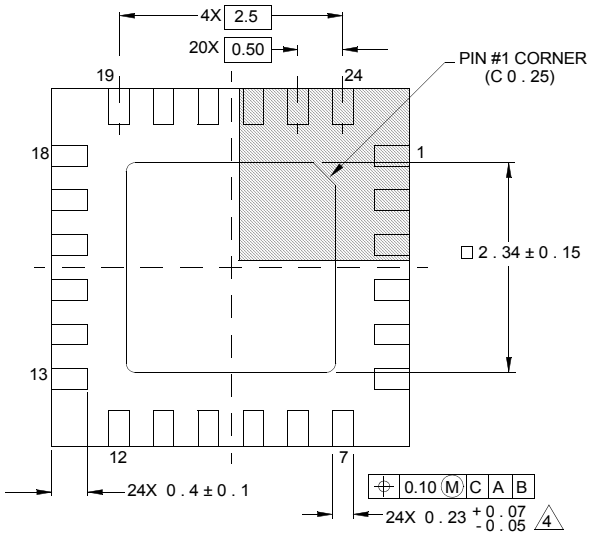
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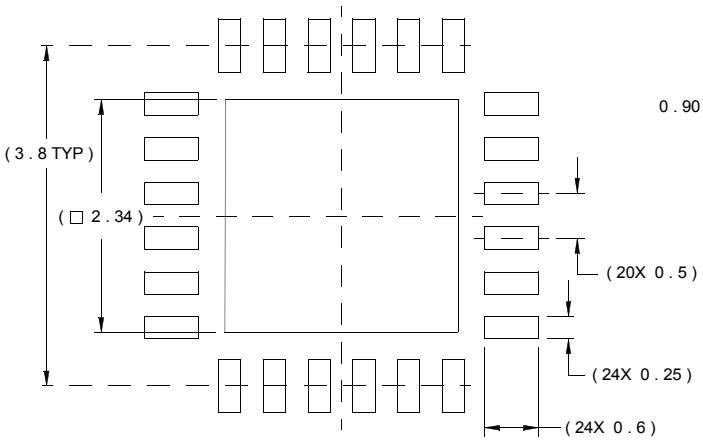
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



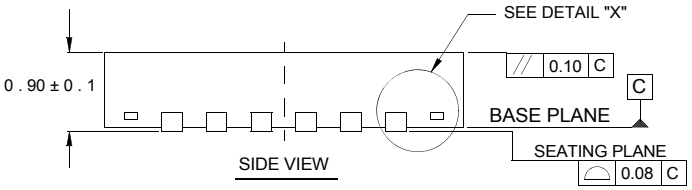
TOP VIEW



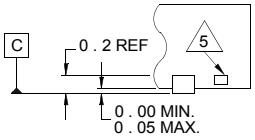
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.