NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL54050

ISL54047

Ultra Low ON-Resistance, High Off-Isolation, Single Supply, Diff SPST Analog Switch

FN6503
Rev 0.00
May 31, 2007

The Intersil ISL54047 device is a low ON-resistance, low voltage, high off-isolation, bidirectional, differential single-pole/single-throw (SPST) analog switch. It was designed to operate from a single +1.65V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low R_{ON} (0.44Ω) and fast switching speeds (t_{ON} = 40ns, t_{OFF} = 35ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply.

The ISL54047 has been designed with a T-switch architecture. This approach results in maximum off-isolation while retaining a low impedance signal path when switches are ON.

The device can be used as a low impedance bypass element for noisy amplifier circuits.

The ISL54047 has two normally open (NO) SPST switches that are controlled by a single logic control pin.

TABLE 1. FEATURES AT A GLANCE

	ISL54047
Number of Switches	2
SW	SPST
4.3V R_{ON}	0.44Ω
4.3V t_{ON}/t_{OFF}	40ns/35ns
3V R_{ON}	0.51Ω
3V t_{ON}/t_{OFF}	50ns/40ns
1.8V R_{ON}	0.98Ω
1.8V t_{ON}/t_{OFF}	70ns/65ns
Package	10 Ld 1.8 x 1.4 x 0.5mm μTQFN

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

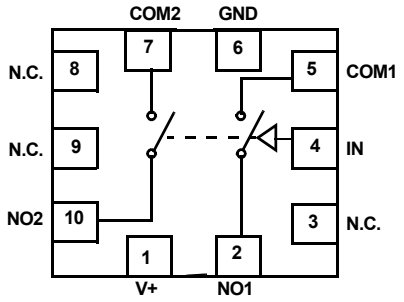
- T-Switch Architecture
- OFF-Isolation at 100kHz
  - Into 50Ω Load 102dB
  - Into 8Ω Load 118dB
- ON Resistance (R_{ON})
  - V+ = +4.3V 0.44Ω
  - V+ = +3.0V 0.51Ω
  - V+ = +1.8V 0.98Ω
- R_{ON} Matching Between Channels 0.04Ω
- R_{ON} Flatness Across Signal Range 0.07Ω
- Single Supply Operation . . . . . +1.65V to +4.5V
- Low Power Consumption (P_D) . . . . . <0.45μW
- Fast Switching Action (V+ = +4.3V)
  - t_{ON} 40ns
  - t_{OFF} 35ns
- ESD HBM Rating . . . . . >8kV
- 1.8V Logic Compatible (+3V supply)
- Low ICC Current when VinH is not at the V+ Raill
- Available in 10 lead 1.8 x 1.4 x 0.5mm μTQFN
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Battery powered, Handheld, and Portable Equipment
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

Pinout (Note 1)

ISL54047 (μTQFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	NO1, NO2
0	OFF
1	ON

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.65V to +4.5V)
GND	Ground Connection
IN	Digital Control Input
COMx	Analog Switch Common Pin
NOx	Analog Switch Normally Open Pin
N.C.	No Connect

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54047IRUZ-T	D	-40 to +85	10 Ld 1.8 x 1.4 x 0.5mm μTQFN Tape and Reel	L10.1.8x1.4A

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Absolute Maximum Ratings

V+ to GND . . . . . -0.5 to 5.5V
Input Voltages
NO, IN (Note 2) . . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
COM (Note 2). . . . . -0.5 to ((V+) + 0.5V)
Continuous Current NO, COM. . . . . ±300mA
Peak Current NO, COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating:
HBM . . . . . >8kV
MM . . . . . >500V
CDM. . . . . >1.4kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld μTQFN Package (Note 3)	143	61

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range. . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. Extended operation above the recommended operating conditions could result in decreased reliability. The Absolute Maximum Ratings are stress only ratings and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NOx, IN, or COMx pins exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} = 0V to V+, (See Figure 4)	25	-	0.45	-	Ω
		Full	-	0.55	-	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} = Voltage at max R_{ON}, (Note 7)	25	-	0.04	-	Ω
		Full	-	0.04	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, V_{NO} = 0V to V+, (Note 6)	25	-	0.07	-	Ω
		Full	-	0.08	-	Ω
NO OFF Leakage Current, $I_{NO(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, V_{NO} = 3V, 0.3V	25	-100	-	100	nA
		Full	-195	-	195	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, or V_{NO} = 0.3V, 3V, or Floating	25	-100	-	100	nA
		Full	-195	-	195	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} = 3.0V, R_L =50Ω, C_L = 35pF, (See Figure 1)	25	-	40	-	ns
		Full	-	50	-	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} = 3.0V, R_L =50Ω, C_L = 35pF, (See Figure 1)	25	-	35	-	ns
		Full	-	45	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 2V, R_G = 0Ω, (See Figure 2)	25	-	192	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 3)	25	-	102	-	dB
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$, (See Figure 3)	25	-	81	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$, (See Figure 5)	25	-	-95	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.01	-	%

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	46	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	233	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.65		4.5	V
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = 0V	25	-	-	0.1	µA
		Full	-	-	1	µA
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = V+	25	-	-	0.5	µA
		Full	-	-	1	µA
Positive Supply Current, I+	V+ = +4.2V, V_{IN} = 2.85V	25	-	-	12	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.6	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = 0V to V+, (See Figure 4)	25	-	0.55	0.6	Ω
		Full	-	-	0.8	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = Voltage at max R_{ON}, (Note 7)	25	-	0.05	0.07	Ω
		Full	-	-	0.08	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = 0V to V+, (Note 6)	25	-	0.1	0.15	Ω
		Full	-	-	0.15	Ω
NO OFF Leakage Current, $I_{NO(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} = 3V, 0.3V	25	-	0.9	-	nA
		Full	-	30	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} = 0.3V, 3V, or Floating	25	-	0.8	-	nA
		Full	-	30	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1)	25	-	50	-	ns
		Full	-	60	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1)	25	-	40	-	ns
		Full	-	50	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 1.5V, R_G = 0Ω, (See Figure 2)	25	-	115	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 3)	25	-	102	-	dB
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$, (See Figure 3)	25	-	81	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$, (See Figure 5)	25	-	-95	-	dB

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.016	-	%
NO Capacitance, C_{OFF}	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	48	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	236	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = +3.6V, V_{IN} = 0V or V+	25	-	0.01	-	µA
		Full	-	0.52	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.5	V
Input Voltage High, V_{INH}		25	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.8V Supply

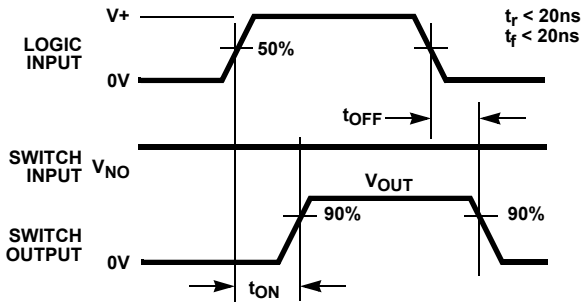
Test Conditions: V+ = +1.65V to +2V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.4V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.65V, I_{COM} = 100mA, V_{NO} = 0V to V+, (See Figure 4)	25	-	1.24	-	Ω
		Full	-	1.34	-	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.65V, V_{NO} = 1.0V, R_L =50Ω, C_L = 35pF, (See Figure 1)	25	-	70	-	ns
		Full	-	80	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.65V, V_{NO} = 1.0V, R_L =50Ω, C_L = 35pF, (See Figure 1)	25	-	65	-	ns
		Full	-	75	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 1V, R_G = 0Ω, (See Figure 2)	25	-	53	-	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	52	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	237	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.4	V
Input Voltage High, V_{INH}		25	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA

NOTES:

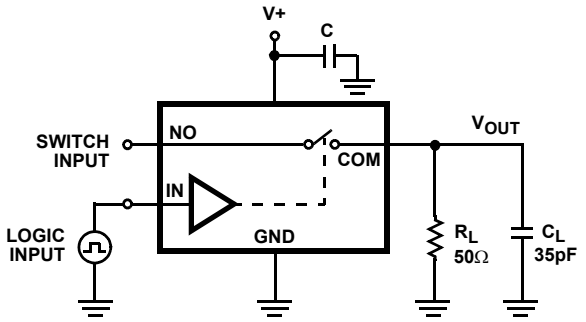
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
7. R_{ON} matching between channels is calculated by subtracting the channel with the highest max Ron value from the channel with lowest max Ron value, between NO1 and NO2.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

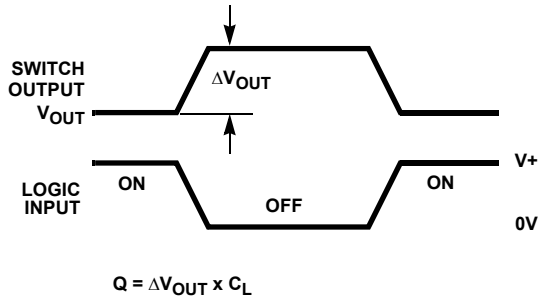


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO)} \frac{R_L}{R_L + R_{(ON)}}$$

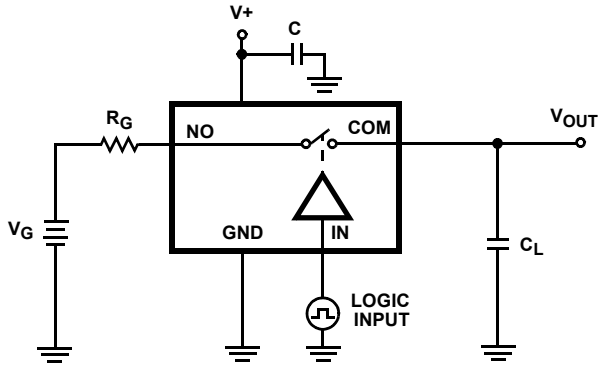
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

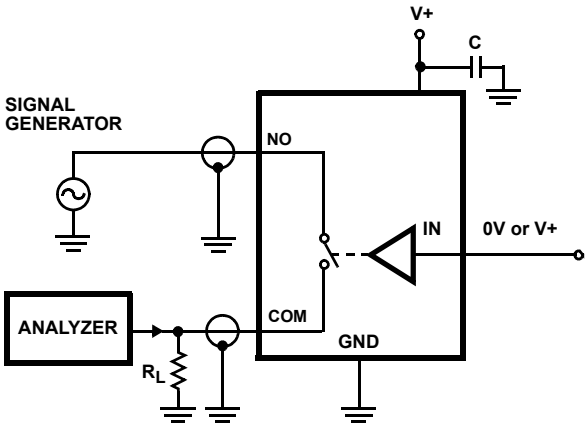
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

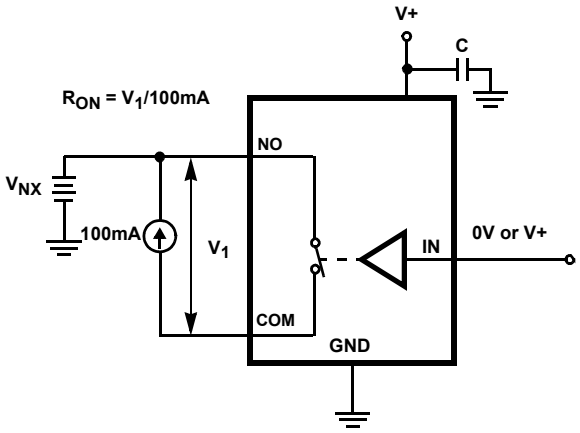
FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

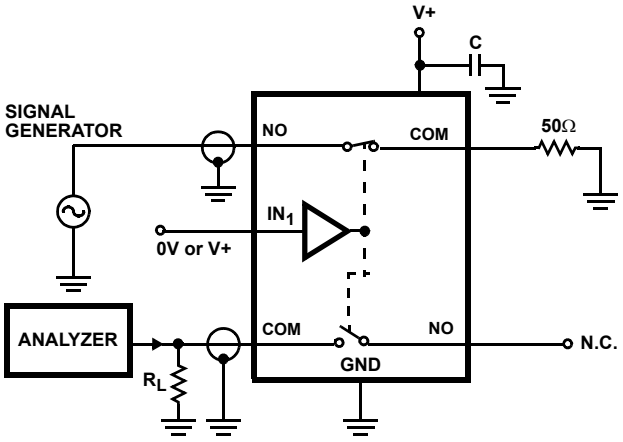
FIGURE 3. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

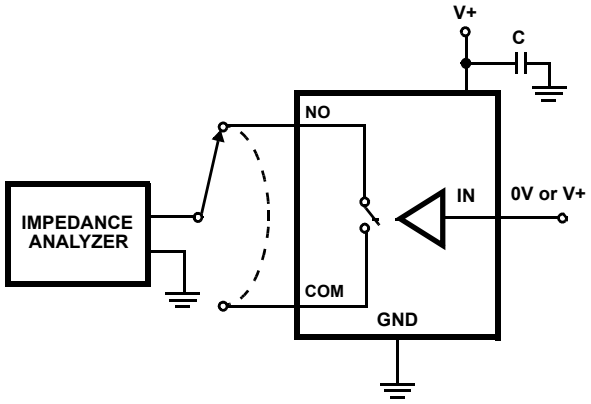
FIGURE 4. R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 5. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 6. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL54047 is a bidirectional, differential single pole/single throw (SPST) analog switch that offer precise switching capability from a single 1.65V to 4.5V supply with low on-resistance (0.44Ω) and high speed operation (t_{ON} = 40ns, t_{OFF} = 35ns). The devices are especially well suited for portable battery powered equipment due to their low operating supply voltage (1.65V), low power consumption (4.5µW max) and the tiny µTQFN package. The ultra low on-resistance and Ron flatness provide very low insertion loss and distortion to applications that require signal reproduction.

External V+ Series Resistor

For improved ESD and latch-up immunity Intersil recommends adding a 100Ω resistor in series with the V+ power supply pin of the ISL54047 IC (see Figure 7).

During an over-voltage transient event, such as occurs during system level IEC 61000 ESD testing, substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the V+ power supply to ground. This will result in a significant amount of current flow in the IC which can potentially create a latch-up state or permanently damage the IC. The external V+ resistor limits the current during this over-stress situation and has been found to prevent latch-up or destructive damage for many over voltage transient events.

Under normal operation the sub-microamp I_{DD} current of the IC produces an insignificant voltage drop across the 100Ω series resistor resulting in no impact to switch operation or performance.

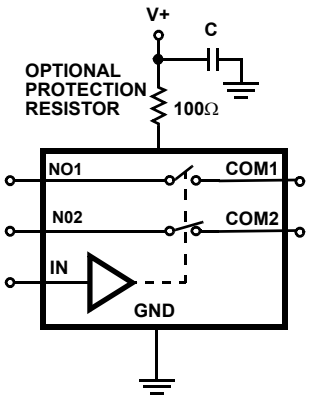


FIGURE 7. V+ SERIES RESISTOR FOR ENHANCED ESD AND LATCH-UP IMMUNITY

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 8). The resistor limits

the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch. Connecting schottky diodes to the signal pins as shown in Figure 8 will shunt the fault current to the supply or to ground thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

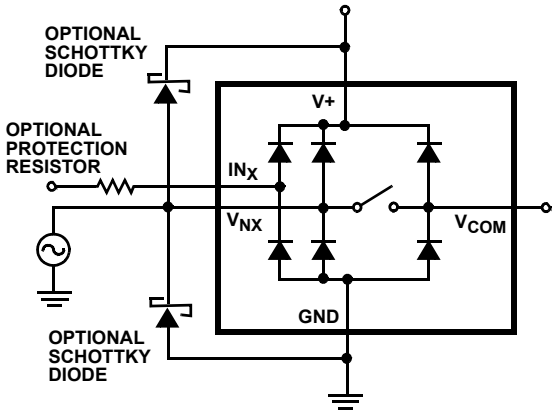


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL54047 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL54047 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the Electrical Specification Tables on page 5 and Typical Performance Curves on page 9 for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family are 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.7V to 4.5V (see Figure 18). At 2.7V the V_{IL} level is about 0.53V. This is still above the 1.8V CMOS guaranteed low output maximum level of 0.5V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

The ISL54047 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply the device draws only 12µA of current (see Figure 16 for VIN = 2.85V).

Frequency Performance

In 50Ω systems, the ISL54047 has a -3dB bandwidth of 27MHz (see Figure 21). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 22 details the high Off Isolation and Crosstalk rejection provided by this part. At 100kHz, Off Isolation is about 102dB in 50Ω systems, 118dB into 8Ω, and 124dB into 4Ω, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

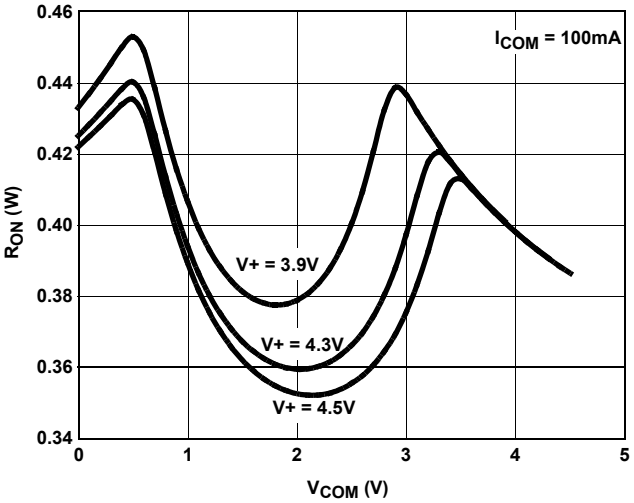


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

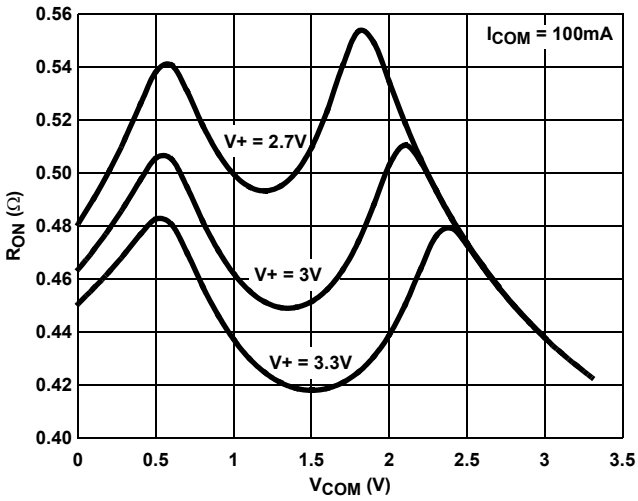


FIGURE 10. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

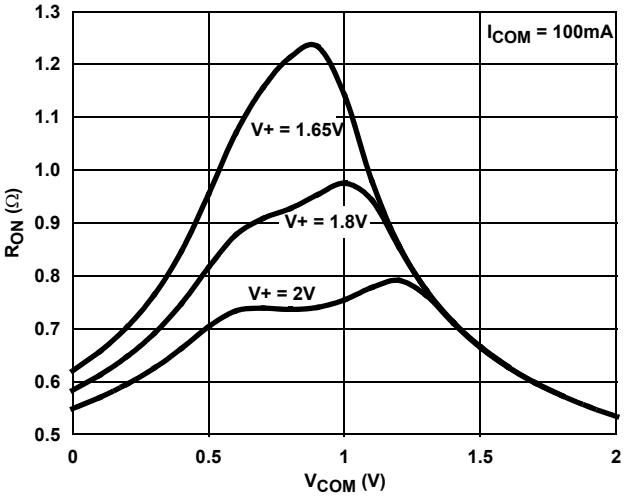


FIGURE 11. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

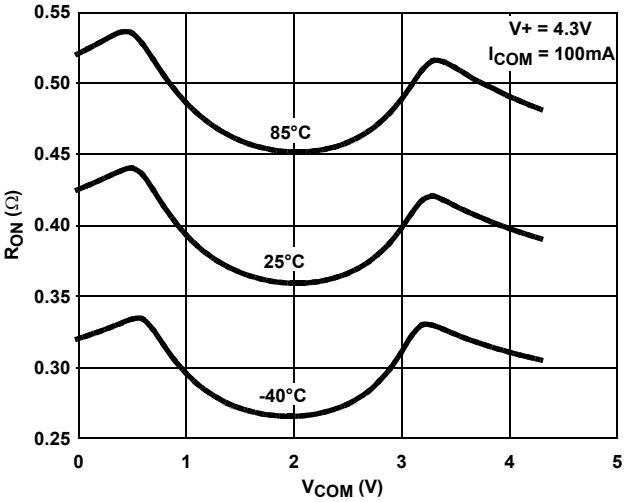


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

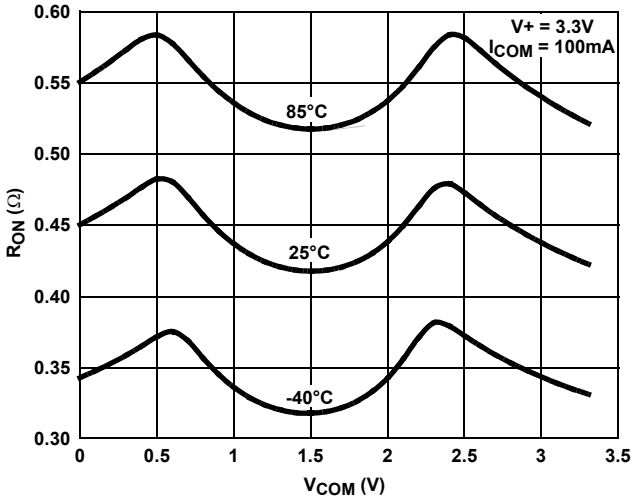


FIGURE 13. ON RESISTANCE vs SWITCH VOLTAGE

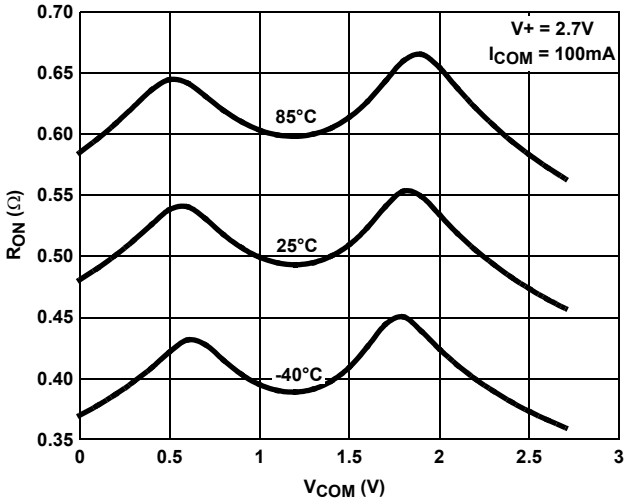


FIGURE 14. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

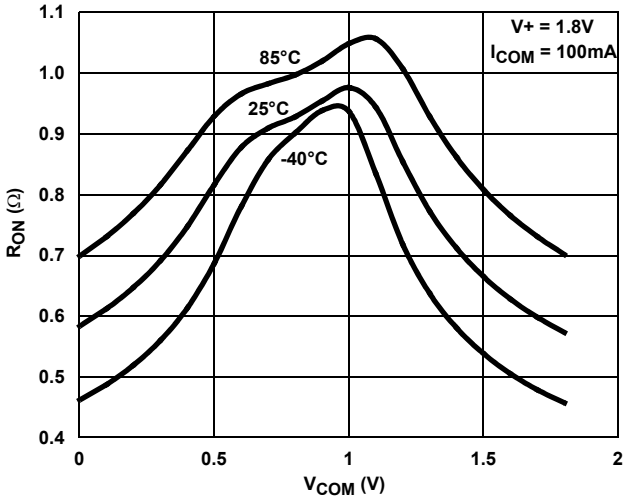


FIGURE 15. ON RESISTANCE vs SWITCH VOLTAGE

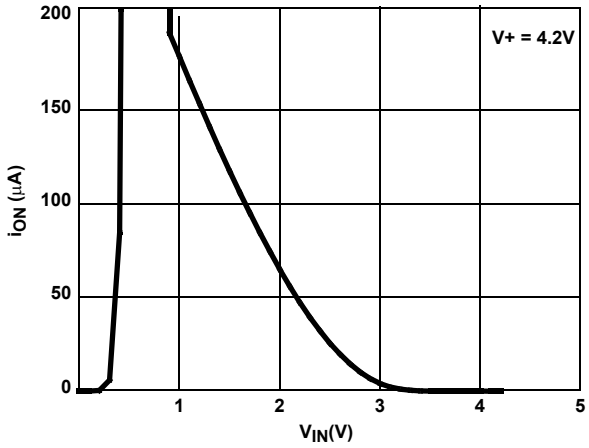


FIGURE 16. SUPPLY CURRENT vs VLOGIC VOLTAGE

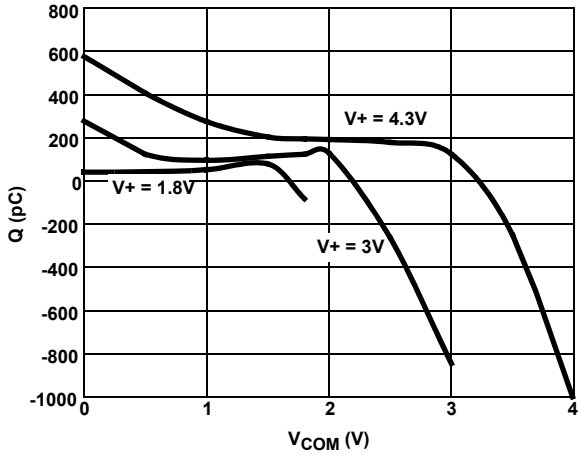


FIGURE 17. CHARGE INJECTION vs SWITCH VOLTAGE

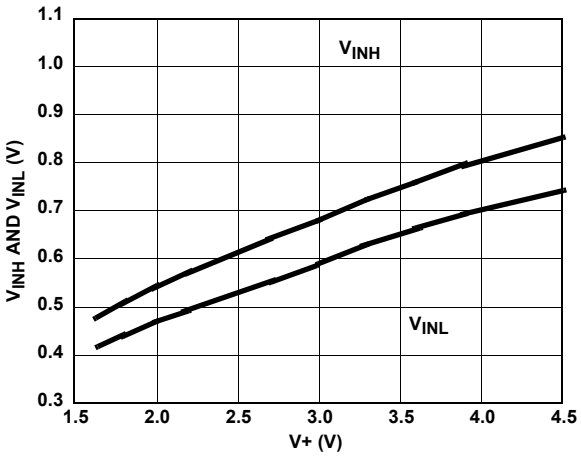


FIGURE 18. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

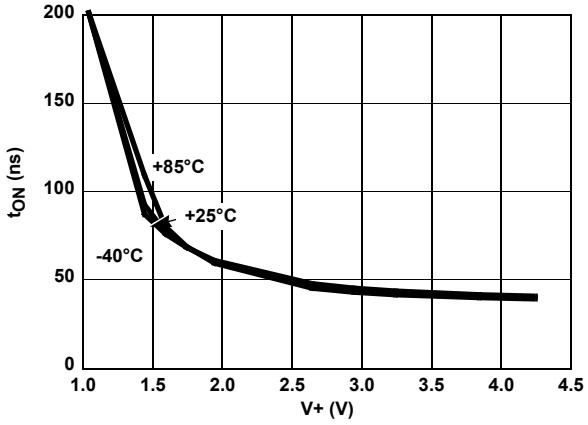


FIGURE 19. TURN-ON TIME vs SUPPLY VOLTAGE

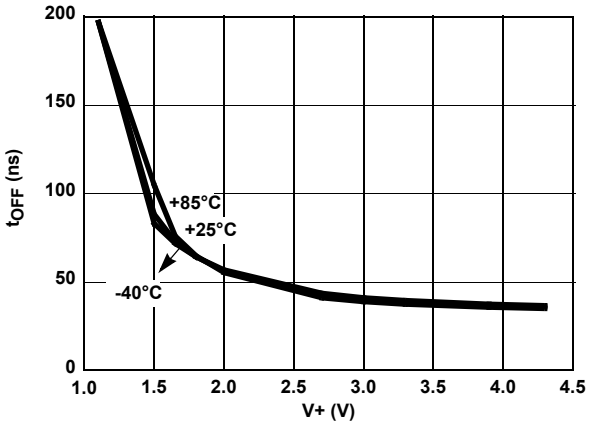


FIGURE 20. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

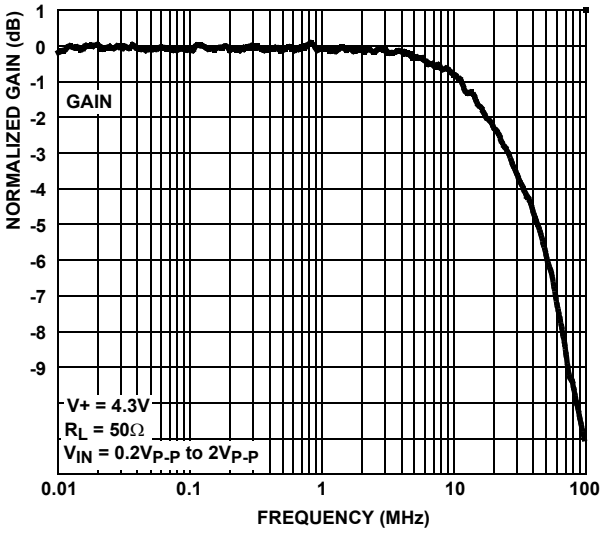


FIGURE 21. FREQUENCY RESPONSE

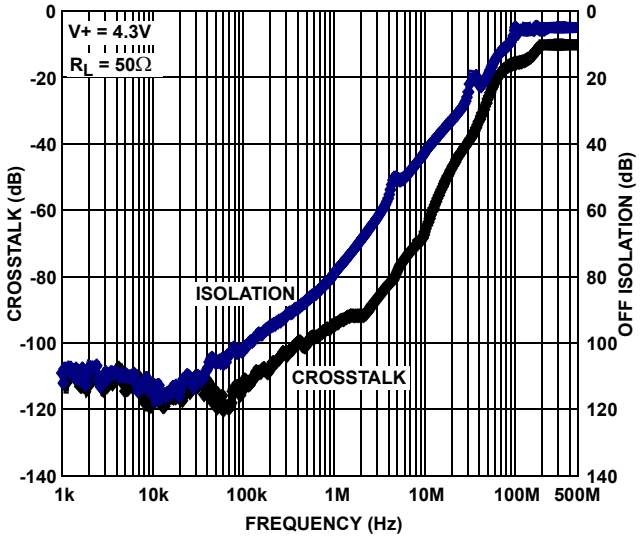


FIGURE 22. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

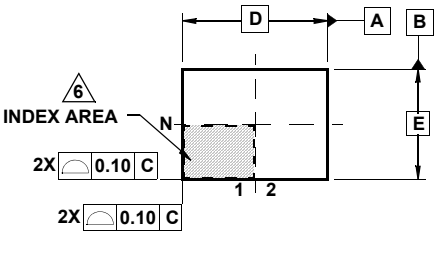
TRANSISTOR COUNT:

114

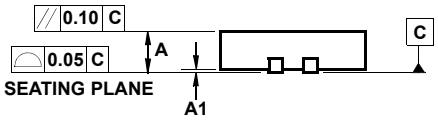
PROCESS:

Submicron CMOS

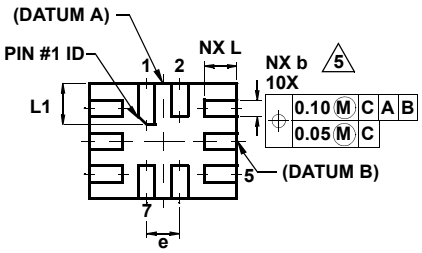
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



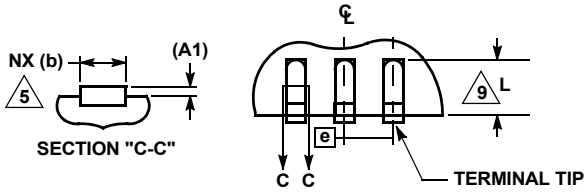
TOP VIEW



SIDE VIEW



BOTTOM VIEW



L10.1.8x1.4A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 or 0.15 REF		-
b	0.15	0.20	0.25	5, 9
D	1.75	1.80	1.85	-
E	1.35	1.40	1.45	-
e		0.40 BSC		-
L	0.35	0.40	0.45	9
L1	0.45	0.50	0.55	-
N		10		2
Nd		2		3
Ne		3		3
θ	0	-	12	4

Rev. 1 1/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
10. JEDEC Reference MO-255.

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