NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL29023

ISL29010

Light-to-Digital Output Sensor with High Sensitivity, Gain Selection, and I2C Interface

FN6414
Rev 1.00
November 11, 2011

The ISL29010 is an integrated light sensor with I^2C interface. It has an internal signed15-bit integrating type ADC designed based on the charge-balancing conversion technique. This ADC is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The lux range select feature allows the user to program the lux range for optimized counts/lux.

In normal operation, power consumption is typically 250µA. Furthermore, a power-down mode can be controlled by software via the I^2C interface, reducing power consumption to less than 1µA.

Designed to operate on supplies from 2.5V to 3.3V, the ISL29010 is specified for operation over the -40°C to +85°C ambient temperature range.

Ordering Information

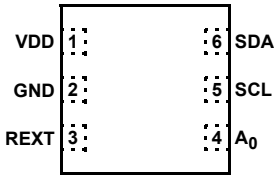
PART NUMBER (Notes 1, 2, 3)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL29010IROZ-T7	-40 to +85	6 Ld ODFN	L6.2x2.1
ISL29010IROZ-EVALZ	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL29010. For more information on MSL please see tech brief TB477.

Pinout

ISL29010
(6 LD ODFN)
TOP VIEW



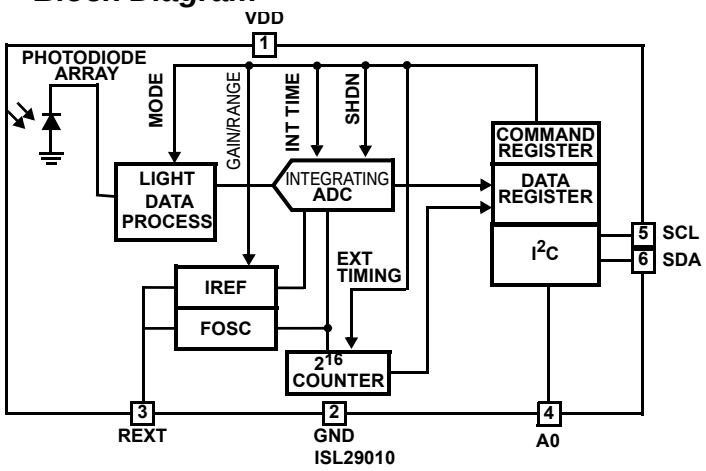
Features

- Range select via I^2C
  - Range 1 = 0 lux to 2,000 lux
  - Range 2 = 0 lux to 8,000 lux
  - Range 3 = 0 lux to 32,000 lux
  - Range 4 = 0 lux to 128,000 lux
- Human eye response (540nm peak sensitivity)
- Temperature compensated
- Signed 15-bit resolution
- Adjustable resolution: up to 20 counts per lux
- 1 bit I^2C address selection
- Simple output code, directly proportional to lux
- IR + UV rejection
- 50Hz/60Hz rejection
- 2.5V to 3.3V supply
- 6 Ld ODFN (2.1mmx2mm)
- Pb-free (RoHS compliant)
- Operating temperature range: -40°C to +85°C

Applications

- Display and keypad backlight dimming for
  - Mobile Devices: Smart phone, PDA, and GPS
  - Computing devices: Notebook PC, UMPC web pod
  - Consumer devices: LCD-TV, digital picture frame, and digital cameras
- Industrial and medical light sensing

Block Diagram



Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply Voltage between V_{DD} and GND 3.6V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.2V to 5.5V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
A0, REXT Pin Voltage . . . . . -0.2V to VDD
ESD Rating
Human Body Model 2kV
Machine Model 200V

Thermal Information

Thermal Resistance (Typical Note 4)	θ_{JA} (°C/W)
6 Ld ODFN	88

Maximum Die Temperature . . . . . +90°C
Storage Temperature . . . . . -40°C to +100°C
Operating Temperature . . . . . -40°C to +85°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ, unless otherwise specified, Internal Timing Mode operation (See “Principles of Operation” on page 3).

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
E_e	Detectable Input Light Intensity			0.5k to 10k		lux
V_{DD}	Power Supply Range		2.50		3.30	V
I_{DD}	Supply Current			0.25	0.33	mA
I_{DD1}	Supply Current Disabled	Software disabled		0.1	1	µA
$f_{OSC}1$	Internal Oscillator Frequency	Gain/Range = 1 or 2	308	342	377	kHz
$f_{OSC}2$	Internal Oscillator Frequency	Gain/Range = 3 or 4	616	684	754	kHz
f_{I2C}	I^2C Clock Rate Range			1 to 400		kHz
DATA0	Dark ADC Code	E = 0 lux, Gain/Range = 1		0	6	Counts
DATA1	Full-Scale ADC Code			32767		Counts
DATA2	Light Count Output	E = 300 lux, fluorescent light, Gain/Range = 1 (Note 5)	3300	4400	5500	Counts
DATA3	Light Count Output	E = 300 lux, fluorescent light, Gain/Range = 2 (Note 5)		1100		Counts
DATA4	Light Count Output	E = 300 lux, fluorescent light, Gain/Range = 3 (Note 5)		275		Counts
DATA5	Light Count Output	E = 300 lux, fluorescent light, Gain/Range = 4 (Note 5)		69		Counts
V_{REF}	Voltage of R_{EXT} Pin		0.490	0.515	0.540	V
V_{TL}	SCL ,SDA and A0 Threshold LO	(Note 6)		1.05		V
V_{TH}	SCL ,SDA and A0 Threshold HI	(Note 6)		1.95		V
I_{SDA}	SDA Current Sinking Capability		3	5		mA

NOTES:

5. Fluorescent light is substituted by a green LED during production.
6. The voltage threshold levels of the SDA and SCL pins are VDD dependent: V_{TL} = 0.35*V_{DD}. V_{TH} = 0.65*V_{DD}.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
1	VDD	Positive supply; connect this pin to a regulated 2.5V to 3.3V supply	
2	GND	Ground pin. The thermal pad is connected to the GND pin	
3	REXT	External resistor pin for ADC reference; connect this pin to ground through a (nominal) 100kΩ resistor with 1% tolerance	
4	A0	Bit 0 of I^2C address	
5	SCL	I^2C serial clock	The I^2C bus lines can pulled above VDD, 5.5V max.
6	SDA	I^2C serial data	

Principles of Operation

Photodiodes

The ISL29010 contains two photodiode arrays which convert light into current. Some diodes are sensitive to both visible and infrared light, while the others are only sensitive to infrared light. Using the infrared portion of the light as baseline, the visible light can be extracted. The spectral response vs wavelength is shown in Figure 6 in the “Typical Performance Curves” on page 9. After light is converted to current during the light data process, the current output is converted to digital by a single built-in integrating type signed 15-bit Analog-to-Digital Converter (ADC). An I^2C command reads the visible light intensity in counts.

The converter is a charge-balancing integrating type signed 15-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously. See “Integration Time or Conversion Time” on page 7 and “Noise Rejection” on page 8.

The built-in ADC offers user flexibility in integration time or conversion time. There are two timing modes: Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I^2C External Timing Mode commands. See External Timing Mode example. A good balancing act of integration time and resolution (depending on the application) is required for optimal results.

The ADC has four I^2C programmable range select to dynamically accommodate various lighting conditions. For very dim conditions, the ADC can be configured at its lowest range. For very bright conditions, the ADC can be configured at its highest range.

I^2C Interface

There are eight (8) 8-bit registers available inside the ISL29010. The command and control registers define the operation of the device. The command and control registers do not change until the registers are overwritten. There are two 8-bit registers that set the high and low interrupt thresholds. There are four 8-bit data Read Only registers, two bytes for the sensor reading and another two bytes for the timer counts. The data registers contain the ADC's latest digital output, and the number of clock cycles in the previous integration period.

The ISL29010 has a 7-bit I^2C interface slave address. The six most significant bits are hardwired internally as 100010 while the least significant bit A0 can be either connected to Ground or VDD to allow two possible addresses 1000100 or 1000101. When 1000100x or 1000101x with x as R or $\overline{W}$ is sent after the Start condition, this device compares the first seven bits of this byte to its address and matches.

Figure 1 shows a sample one-byte read. Figure 2 shows a sample one-byte write. Figure 3 shows a sync_I^2C timing diagram sample for externally controlled integration time. The I^2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Figure 2 shows a sample write. Every I^2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master, and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgement period.

Every I^2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

For more information about the I^2C standard, please consult the Philips® I^2C specification documents.

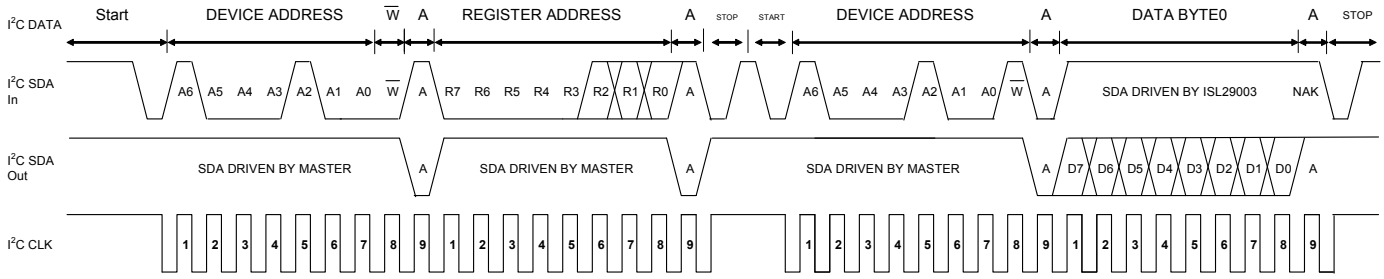


FIGURE 1. I²C READ TIMING DIAGRAM SAMPLE

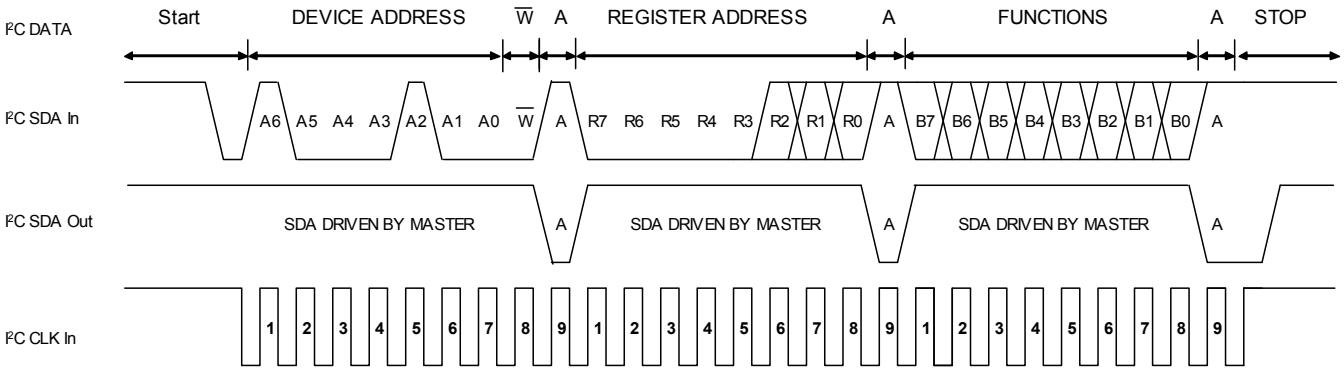


FIGURE 2. I²C WRITE TIMING DIAGRAM SAMPLE

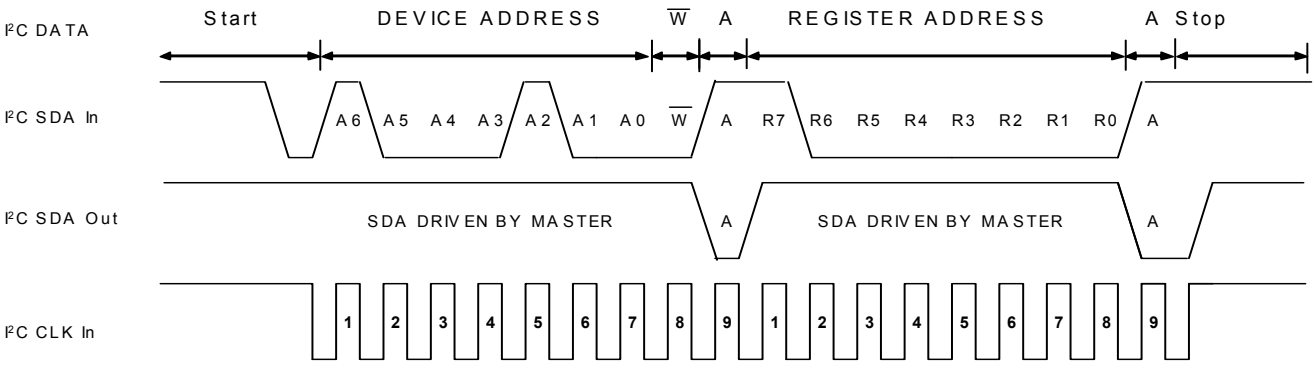


FIGURE 3. I²C SYNC_I²C TIMING DIAGRAM SAMPLE

Register Set

There are eight registers that are available in the ISL29010. Table 1 summarizes the available registers and their functions.

TABLE 1. REGISTER SET

ADDR	REG NAME	BIT								
		7	6	5	4	3	2	1	0	DEFAULT
00h	COMMAND	ADCE	ADCPD	TIMM	0	ADCM1	ADCM0	RES1	RES0	00h
01h	CONTROL	0	0	0	0	GAIN1	GAIN0	0	0	00h
04h	LSB SENSOR	S7	S6	S5	S4	S3	S2	S1	S0	00h
05h	MSB SENSOR	S15	S14	S13	S12	S11	S10	S9	S8	00h
06h	LSB TIMER	T7	T6	T5	T4	T3	T2	T1	T0	00h
07h	MSB TIMER	T15	T14	T13	T12	T11	T10	T9	T8	00h

TABLE 2. WRITE ONLY REGISTERS

ADDRESS	REGISTER NAME	FUNCTIONS/DESCRIPTION
b1xxx_xxxx	sync_I^{2}C	Writing a logic 1 to this address bit ends the current ADC-integration and starts another. Used only with External Timing Mode.
bx1xx_xxxx	clar_int	Writing a logic 1 to this address bit clears the interrupt.

Command Register 00(hex)

The Read/Write command register has five functions:

1. Enable; Bit 7.This function either resets the ADC or enables the ADC in normal operation. A logic 0 disables ADC to reset-mode. A logic 1 enables ADC to normal operation.

TABLE 3. ENABLE

BIT 7	OPERATION
0	Disable ADC-core to reset-mode (default)
1	Enable ADC-core to normal operation

2. ADCPD; Bit 6. This function puts the device in a power-down mode. A logic 0 puts the device in normal operation. A logic 1 powers down the device.

TABLE 4. ADCPD

BIT 6	OPERATION
0	Normal operation (default)
1	Power Down

3. Timing Mode; Bit 5. This function determines whether the integration time is done internally or externally. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between three consecutive external-sync sync_I^{2}C pulses commands.

TABLE 5. TIMING MODE

BIT 5	OPERATION
0	Internal Timing Mode. Integration time is internally timed determined by f_{OSC}, R_{EXT}, and number of clock cycles.
1	External Timing Mode. Integration time is externally timed by the I^{2}C host.

4. Photodiode Select Mode; Bits 3 and 2. Setting Bit 3 and Bit 2 to 1 and 0 enables ADC to give light count DATA output.

TABLE 6. PHOTODIODE SELECT MODE; BITS 2 AND 3

BITS 3:2	MODE
0:0	Disable ADC
0:1	Disable ADC
1:0	Light count DATA output in signed (n - 1) bit *
1:1	No operation.

* n = 4, 8, 12,16 depending on the number of clock cycles function.

5. Width; Bits 1 and 0. This function determines the number of clock cycles per conversion. Changing the number of clock cycles does more than just change the resolution of the device. It also changes the integration time, which is the period the device's analog-to-digital (A/D) converter samples the photodiode current signal for a lux measurement.

TABLE 7. WIDTH

BITS 1:0	NUMBER OF CLOCK CYCLES
0:0	2^{16} = 65,536
0:1	2^{12} = 4,096
1:0	2^{8} = 256
1:1	2^{4} = 16

Control Register 01(hex)

The Read/Write control register has one function:

1. Range/Gain; Bits 3 and 2. The Full Scale Range can be adjusted by an external resistor R_{EXT} and/or it can be adjusted via I^2C using the Gain/Range function. Gain/Range has four possible values, Range(k) where k is 1 through 4. Table 8 lists the possible values of Range(k) and the resulting FSR for some typical value R_{EXT} resistors.

TABLE 8. RANGE/GAIN TYPICAL FSR LUX RANGES

BITS 3:2	k	RANGE(k)	FSR LUX RANGE@ R_{EXT} = 100k	FSR LUX RANGE@ R_{EXT} = 50k	FSR LUX RANGE@ R_{EXT} = 500k
0:0	1	2,000	2,000	4,000	400
0:1	2	8,000	8,000	16,000	1,600
1:0	3	32,000	32,000	64,000	6,400
1:1	4	128,000	128,000	256,000	25,600

I^2Sensor Data Register 04(hex) and 05(hex)

When the device is configured to output a signed 15-bit data, the most significant byte is accessed at 04(hex), and the least significant byte can be accessed at 05(hex). The sensor data register is refreshed after every integration cycle.

Timer Data Register 06(hex) and 07(hex)

Note that the timer counter value is only available when using the External Timing Mode. The 06(hex) and 07(hex) are the LSB and MSB, respectively, of a 16-bit timer counter value corresponding to the most recent sensor reading. Each clock cycle increments the counter. At the end of each integration period, the value of this counter is made available over the I^2C. This value can be used to eliminate noise introduced by slight timing errors caused by imprecise external timing. Microcontrollers, for example, often cannot provide high-accuracy command-to-command timing, and the timer counter value can be used to eliminate the resulting noise.

TABLE 9. DATA REGISTERS

ADDRESS (hex)	CONTENTS
04	Least-significant byte of most recent sensor reading.
05	Most-significant byte of most recent sensor reading.
06	Least-significant byte of timer counter value corresponding to most recent sensor reading.
07	Most-significant byte of timer counter value corresponding to most recent sensor reading.

Calculating Lux

The ISL29010's output codes, DATA, are directly proportional to lux.

$$E = \alpha \times DATA \quad \text{(EQ. 1)}$$

The proportionality constant α is determined by the Full Scale Range (FSR), and the n-bit ADC, which is user defined in the command register. The proportionality constant can also be viewed as the resolution; the smallest lux measurement the device can measure is α in Equation 2.

$$\alpha = \frac{FSR}{2^n} \quad \text{(EQ. 2)}$$

Full-Scale Range (FSR) is determined by the software programmable Range/Gain, Range(k), in the command register and an external scaling resistor R_{EXT}, which is referenced to 100kΩ.

$$FSR = Range(k) \times \frac{100k\Omega}{R_{EXT}} \quad \text{(EQ. 3)}$$

The transfer function effectively for each timing mode becomes:

INTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{2^n} \times DATA \quad \text{(EQ. 4)}$$

EXTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{COUNTER} \times DATA \quad \text{(EQ. 5)}$$

n = 3, 7, 11, or 15. This is the number of clock cycles programmed in the command register.

Range(k) is the user defined range in the Gain/Range bit in the command register.

R_{EXT} is an external scaling resistor hardwired to the R_{EXT} pin.

DATA is the output sensor reading in number of counts available at the data register.

2^n represents the maximum number of counts possible in Internal Timing Mode. For the External Timing Mode, the maximum number of counts is stored in the data register named COUNTER.

COUNTER is the number of increments accrued between integration time for External Timing Mode.

Gain/Range, Range(k)

The Gain/Range can be programmed in the control register to give Range(k) determining the FSR. Note that Range(k) is not the FSR (see Equation 3). Range(k) provides four constants depending on programmed k that will be scaled by R_{EXT} (see Table 8). Unlike R_{EXT}, Range(k) dynamically adjusts the FSR. This function is especially useful when light conditions are varying drastically while maintaining excellent resolution.

Number of Clock Cycles, n-bit ADC

The number of clock cycles determines "n" in the n-bit ADC; 2^n clock cycles is a n-bit ADC. n is programmable in the command register in the width function. Depending on the application, a good balance of speed and resolution has to be considered when deciding for n. For fast and quick measurement, choose the

smallest n = 3. For maximum resolution without regard of time, choose n = 15. Table 10 compares the trade-off between integration time and resolution. See Equations 10 and 11 for the relation between integration time and n. See Equation 3 for the relation of n and resolution.

TABLE 10. RESOLUTION AND INTEGRATION TIME SELECTION

n	RANGE1 f_{OSC} = 327kHz		RANGE4 f_{OSC} = 655kHz	
	t_{INT} (ms)	RESOLUTION LUX/COUNT	t_{INT} (ms)	RESOLUTION (LUX/COUNT)
15	200	0.06	100	2
11	12.8	1.0	6.4	62.5
7	0.8	15.6	0.4	1,000
3	0.05	250	0.025	16,000

R_{EXT} = 100kΩ

External Scaling Resistor R_{EXT} and f_{osc}

The ISL29010 uses an external resistor R_{EXT} to fix its internal oscillator frequency, f_{OSC}. Consequently, R_{EXT} determines the f_{OSC}, integration time and the FSR of the device. f_{OSC}, a dual speed mode oscillator, is inversely proportional to R_{EXT}. For user simplicity, the proportionality constant is referenced to fixed constants 100kΩ and 655kHz:

$$f_{OSC}1 = \frac{1}{2} \times \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 6)}$$

$$f_{OSC}2 = \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 7)}$$

$f_{OSC}1$ is oscillator frequency when Range1 or Range2 are set. This is nominally 327kHz when R_{EXT} is 100kΩ.

$f_{OSC}2$ is the oscillator frequency when Range3 or Range4 are set. This is nominally 655kHz when R_{EXT} is 100kΩ.

When the Range/Gain bits are set to Range1 or Range2, f_{OSC} runs at half speed compared to when Range/Gain bits are set to Range3 and Range4.

$$f_{OSC}1 = \frac{1}{2}(f_{OSC}2) \quad \text{(EQ. 8)}$$

The automatic f_{OSC} adjustment feature allows significant improvement of signal-to-noise ratio when detecting very low lux signals.

Integration Time or Conversion Time

Integration time is the period during which the device's analog-to-digital ADC converter samples the photodiode current signal for a lux measurement. Integration time, in other words, is the time to complete the conversion of analog photodiode current into a digital signal (number of counts).

Integration time affects the measurement resolution. For better resolution, use a longer integration time. For short and fast conversions use a shorter integration time.

The ISL29010 offers user flexibility in the integration time to balance resolution, speed and noise rejection. Integration time can be set internally or externally and can be programmed in the command register 00(hex) Bit 5.

INTEGRATION TIME IN INTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) Bit 5. Most applications will be using this timing mode. When using the Internal Timing Mode, f_{OSC} and n-bits resolution determine the integration time. t_{INT} is a function of the number of clock cycles and f_{OSC}.

$$t_{INT} = 2^m \times \frac{1}{f_{osc}} \quad \text{for Internal Timing Mode only} \quad \text{(EQ. 9)}$$

m = 4, 8, 12, and16. n is the number of bits of resolution.

2^m therefore is the number of clock cycles. n can be programmed at the command register 00(hex) Bits 1 and 0.

Since f_{OSC} is dual speed depending on the Gain/Range bit, t_{INT} is dual time. The integration time as a function of R_{EXT} is shown in Equation 10:

$$t_{INT}1 = 2^m \times \frac{R_{EXT}}{327kHz \times 100k\Omega} \quad \text{(EQ. 10)}$$

$t_{INT}1$ is the integration time when the device is configured for Internal Timing Mode and Gain/Range is set to Range1 or Range2.

$$t_{INT}2 = 2^m \times \frac{R_{EXT}}{655kHz \times 100k\Omega} \quad \text{(EQ. 11)}$$

$t_{INT}2$ is the integration time when the device is configured for Internal Timing Mode and Gain/Range is set to Range3 or Range4.

TABLE 11. INTEGRATION TIMES FOR TYPICAL R_{EXT} VALUES

R_{EXT} (kΩ)	RANGE1 RANGE2		RANGE3 RANGE4	
	n = 15-BIT	n = 11-BIT	n = 11-BIT	n = 3
50	100	6.4	3.2	0.013
100**	200	13	6.5	0.025
200	400	26	13	0.050
500	1000	64	32	0.125

*Integration time in milliseconds
**Recommended R_{EXT} resistor value

INTEGRATION TIME IN EXTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) Bit 5. External Timing Mode is recommended when integration time can be synchronized to an external signal such as a PWM to eliminate noise.

To read the light count DATA output, the device needs three sync_I^{2}C commands to complete one measurement. The 1st sync_I^{2}C command starts the conversion of the diode array 1. The 2nd sync_I^{2}C completes the conversion of diode array 1 and starts the conversion of diode array 2. The 3rd sync_I^{2}C pules ends the conversion of diode array 2, outputs the light count DATA, and starts over again to commence conversion of diode array 1.

The integration time, t_{INT}, is the sum of two identical time intervals between the three sync pulses. t_{INT} is determined by Equation 12:

$$t_{INT} = \frac{k_{OSC}}{f_{OSC}} \quad \text{(EQ. 12)}$$

where k_{OSC} is the number of internal clock cycles obtained from Timer data register and f_{OSC} is the internal I^{2}C operating frequency.

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes, with the same dependence on R_{EXT}. However, in External Timing Mode, the number of clock cycles per integration is no longer fixed at 2^n. The number of clock cycles varies with the chosen integration time, and is limited to 2^{16} = 65,536. In order to avoid erroneous lux readings the integration time must be short enough not to allow an overflow in the counter register.

$$t_{INT} < \frac{65{,}535}{f_{OSC}} \quad \text{(EQ. 13)}$$

f_{OSC} = 327kHz*100kΩ/R_{EXT}. When Range/Gain is set to Range1 or Range2.

f_{OSC} = 655kHz*100kΩ/R_{EXT}. When Range/Gain is set to Range3 or Range4.

Noise Rejection

In general, integrating type ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the integration time. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms (k = 1,2...k_i) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise.

Flat Window Lens Design

A window lens will surely limit the viewing angle of the ISL29010. The window lens should be placed directly on top of the device. The thickness of the lens should be kept at minimum to minimize loss of power due to reflection and also to minimize loss due to absorption of energy in the plastic material. A thickness of t = 1mm is recommended for a window lens design. The bigger the diameter of the window lens, the wider the viewing angle is of the ISL29010. Table 12 shows the recommended dimensions of the optical window to ensure both 35° and 45° viewing angle. These dimensions are based on a window lens thickness of 1.0mm and a refractive index of 1.59.

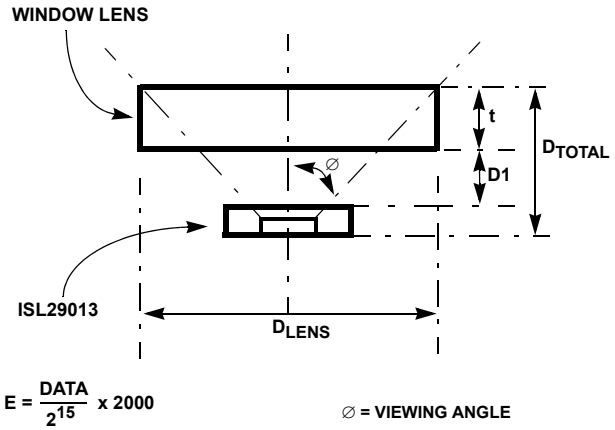


FIGURE 4. FLAT WINDOW LENS

TABLE 12. RECOMMENDED DIMENSIONS FOR A FLAT WINDOW DESIGN

D_{TOTAL}	D1	D_{LENS} @ 35 VIEWING ANGLE	D_{LENS} @ 45 VIEWING ANGLE
1.5	0.50	2.25	3.75
2.0	1.00	3.00	4.75
2.5	1.50	3.75	5.75
3.0	2.00	4.30	6.75
3.5	2.50	5.00	7.75

t = 1	Thickness of lens
D1	Distance between ISL29010 and inner edge of lens
D_{LENS}	Diameter of lens
D_{TOTAL}	Distance constraint between the ISL29010 and lens outer edge

* All dimensions are in mm.

Suggested PCB Footprint

It is important that the users check the "Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package" before starting ODFN product board mounting.

http://www.intersil.com/data/tb/TB477.pdf

Layout Considerations

The ISL29010 is relatively insensitive to layout. Like other I^{2}C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 4.7µF and 0.1µF, placed close to the device.

Typical Circuit

A typical application for the ISL29010 is shown in Figure 5. The ISL29010's I^2C address is internally hardwired as 1000100. The device can be tied onto a system's I^2C bus together with other I^2C compliant devices.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

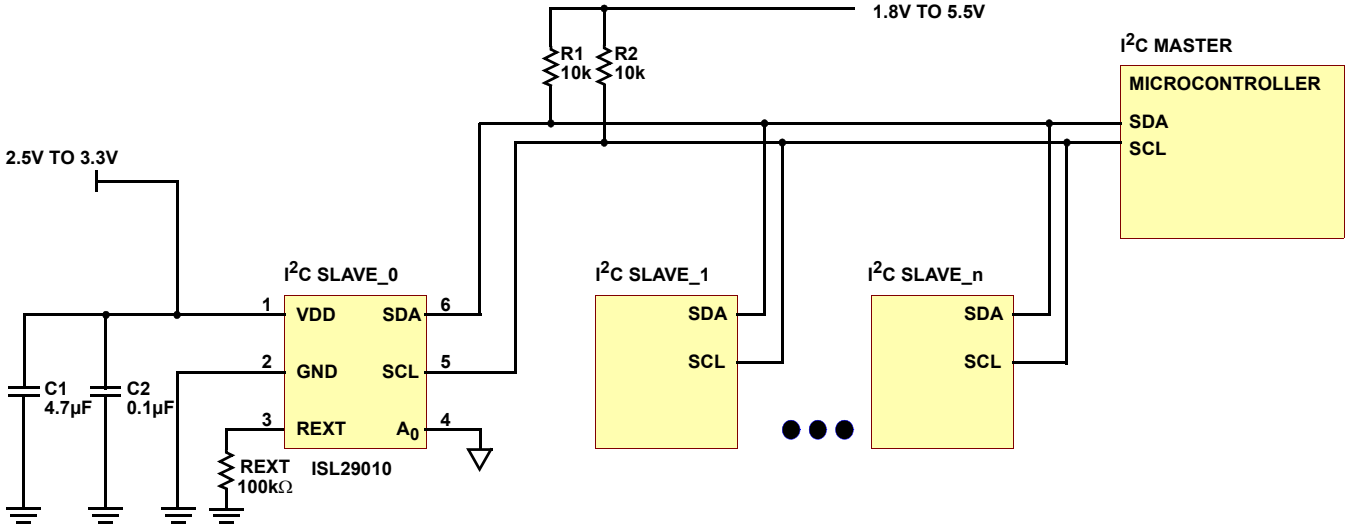


FIGURE 5. ISL29010 TYPICAL CIRCUIT

Typical Performance Curves (R_{EXT} = 100kΩ)

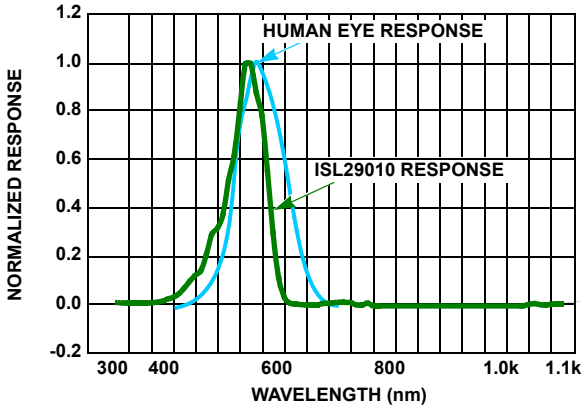


FIGURE 6. SPECTRAL RESPONSE

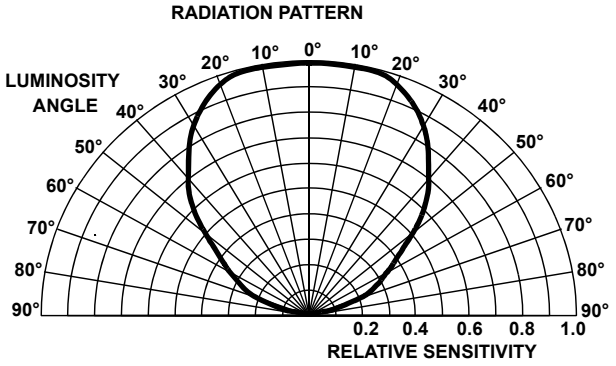


FIGURE 7. RADIATION PATTERN

Typical Performance Curves (R_{EXT} = 100kΩ) (Continued)

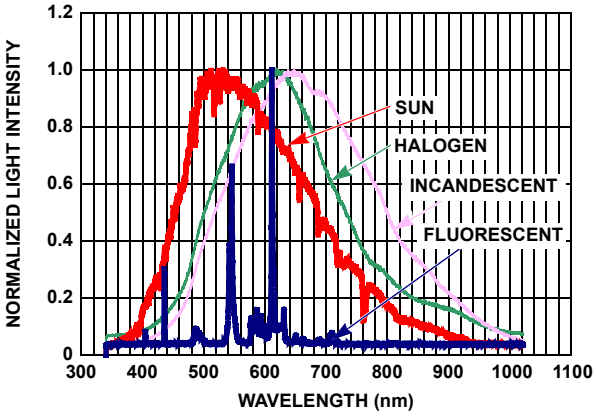


FIGURE 8. SPECTRUM OF LIGHT SOURCES FOR MEASUREMENT

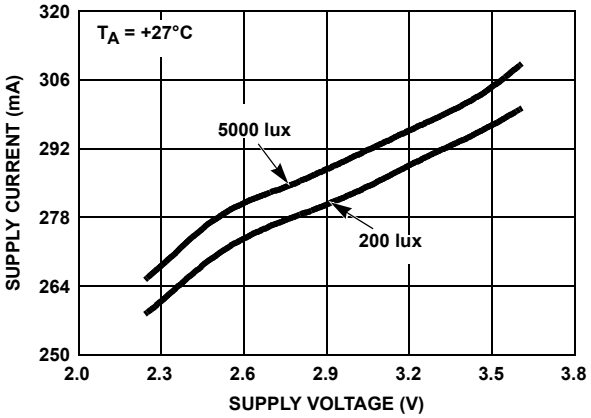


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE

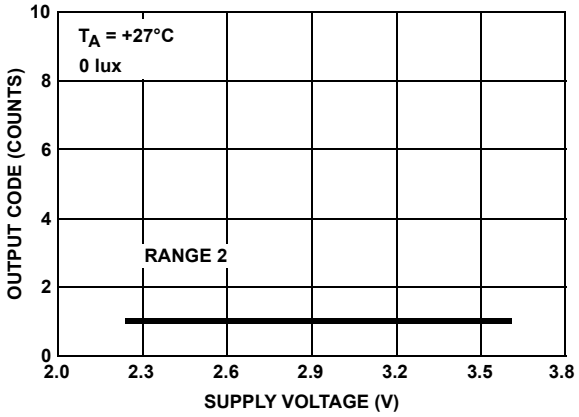


FIGURE 10. OUTPUT CODE FOR 0 LUX vs SUPPLY VOLTAGE

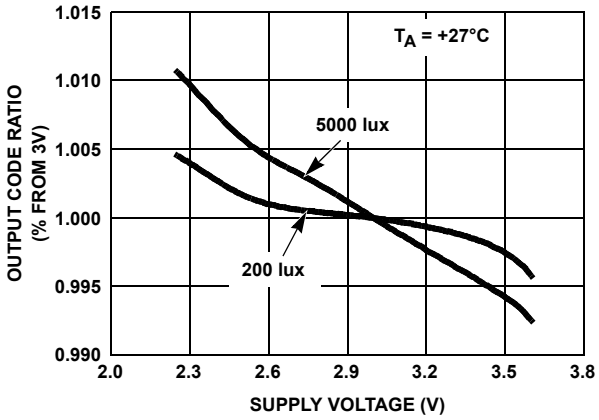


FIGURE 11. OUTPUT CODE vs SUPPLY VOLTAGE

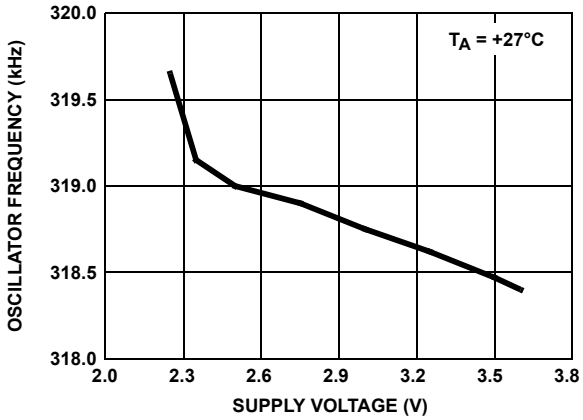


FIGURE 12. OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

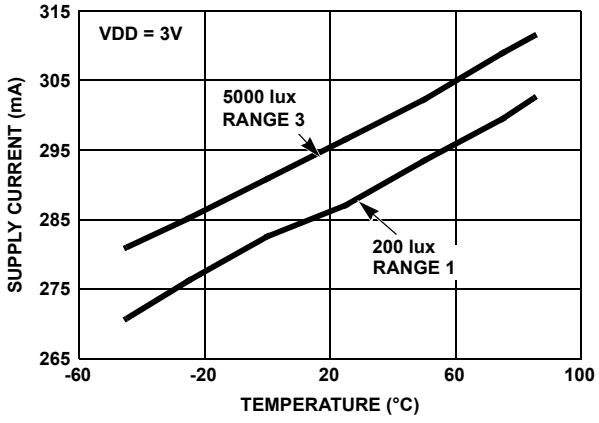


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (R_{EXT} = 100kΩ) (Continued)

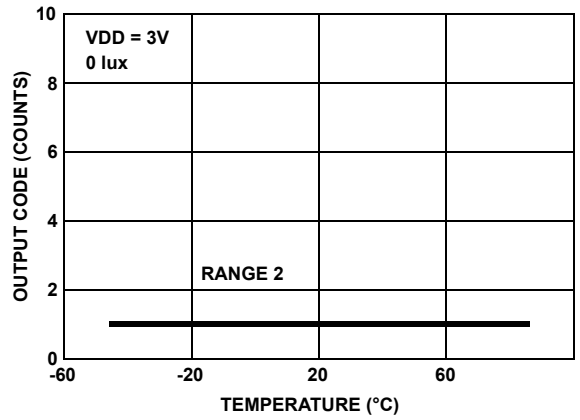


FIGURE 14. OUTPUT CODE FOR 0 LUX vs TEMPERATURE

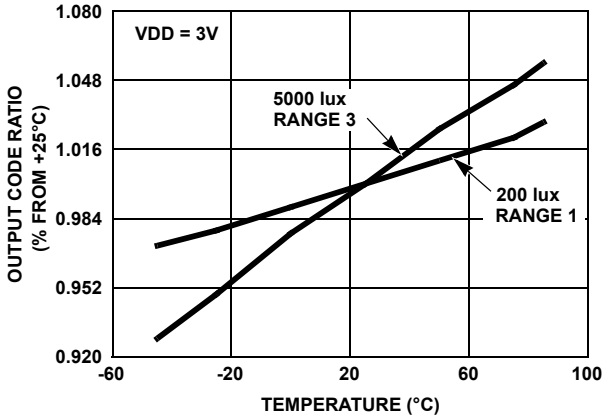


FIGURE 15. OUTPUT CODE vs TEMPERATURE

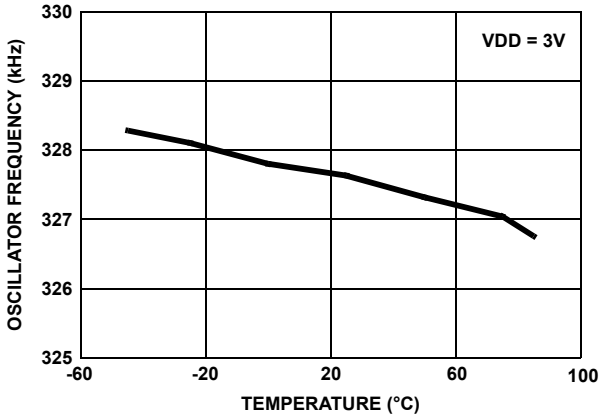


FIGURE 16. OSCILLATOR FREQUENCY vs TEMPERATURE

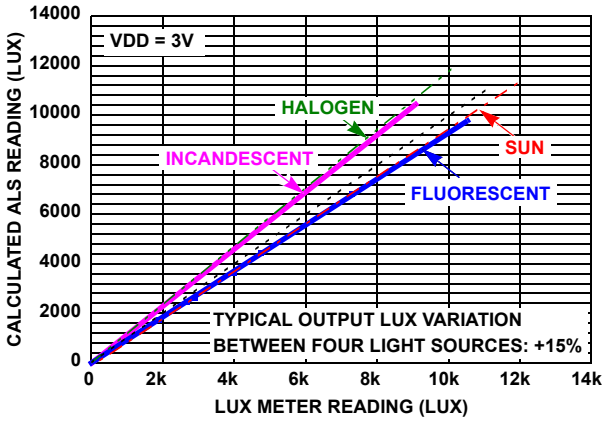


FIGURE 17. LIGHT SENSITIVITY vs LUX LEVEL

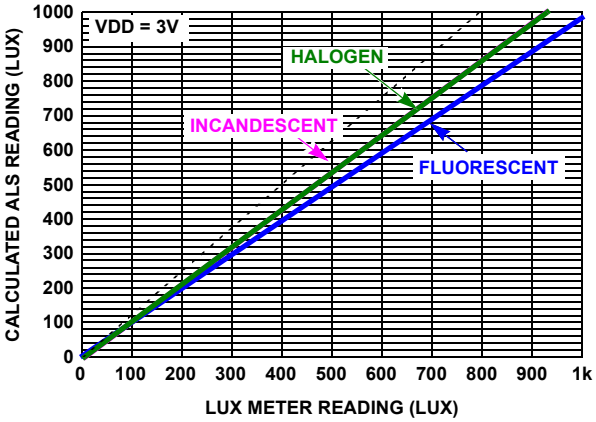


FIGURE 18. LIGHT SENSITIVITY vs LUX LEVEL

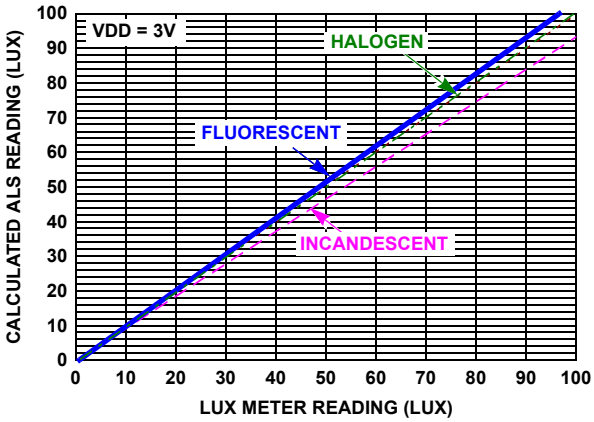


FIGURE 19. LIGHT SENSITIVITY vs LUX LEVEL

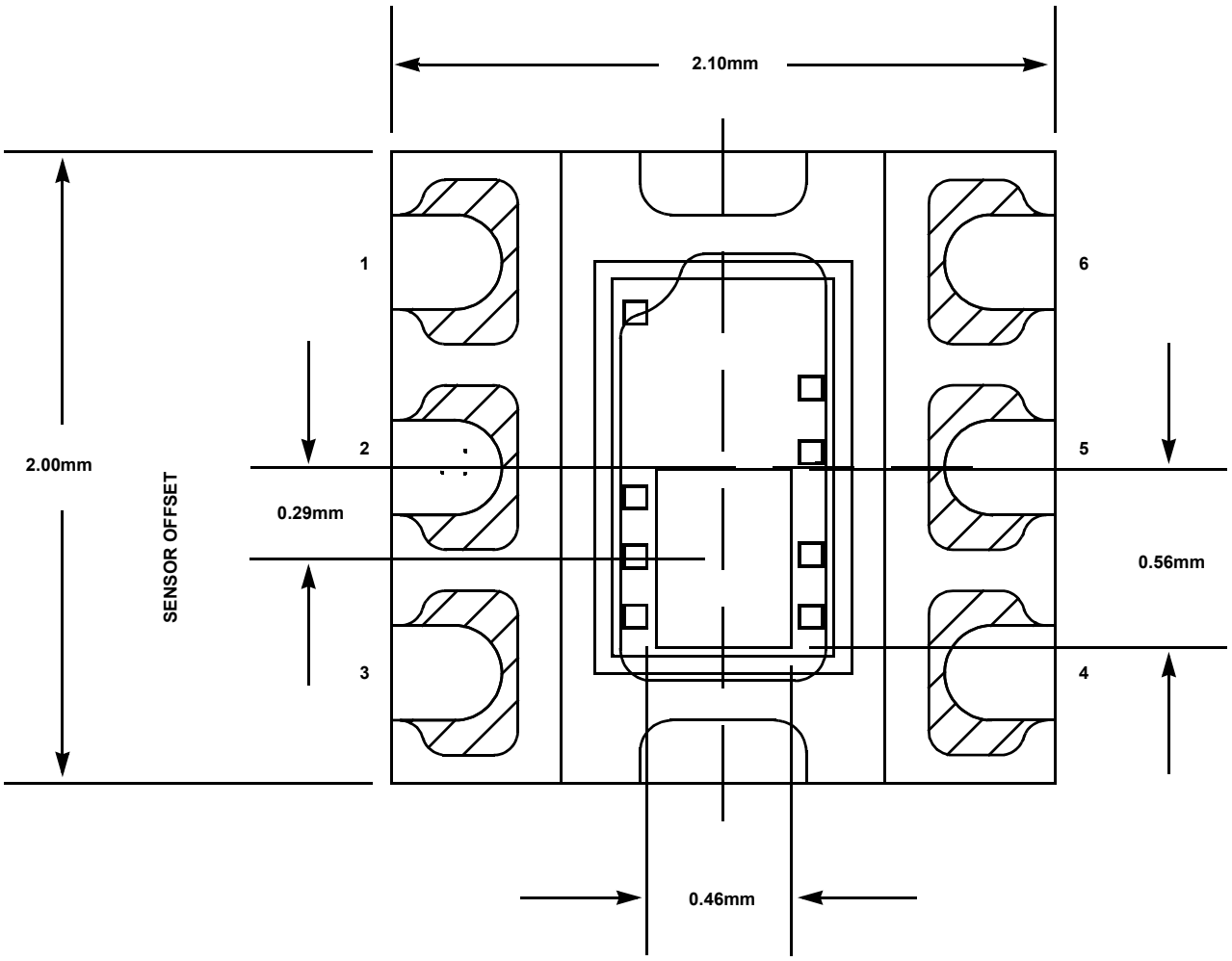


FIGURE 20. 6 LD ODFN SENSOR LOCATION OUTLINE

© Copyright Intersil Americas LLC 2008-2011. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

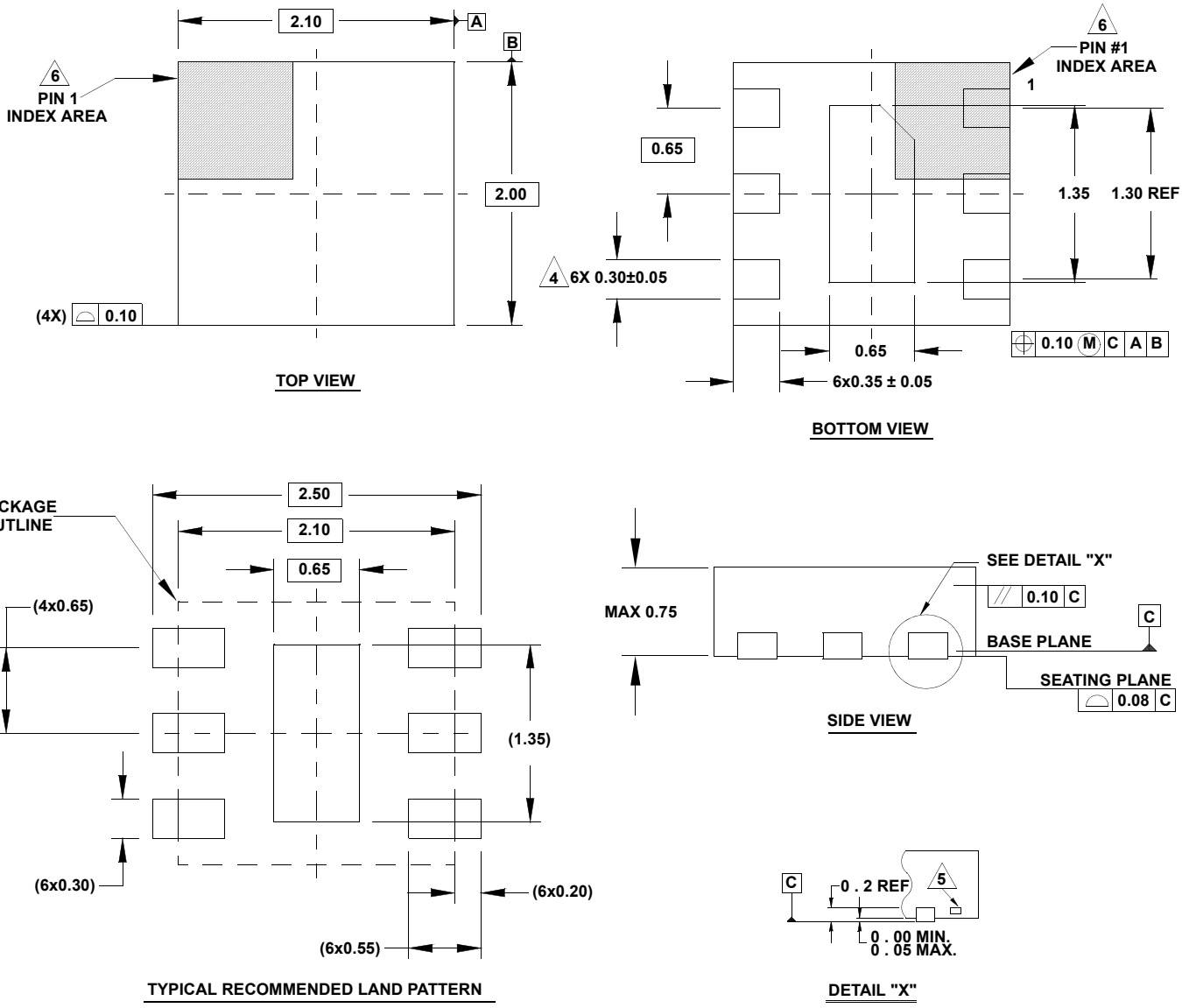
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

L6.2x2.1

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

Rev 3, 5/11



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.