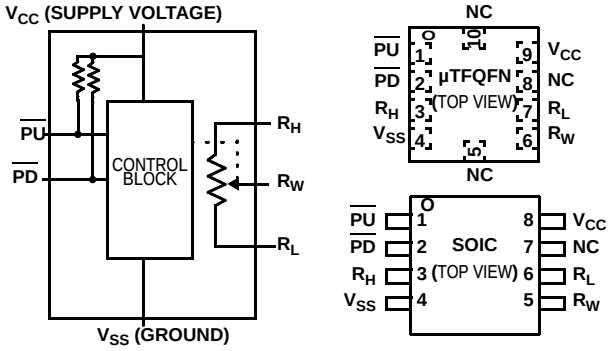
Low Noise, Low Power, 32 Taps, Push Button Controlled Potentiometer

The Intersil ISL23511 is a three-terminal digitally-controlled potentiometer (XDCP) implemented by a resistor array composed of 31 resistive elements and a wiper switching network. The ISL23511 features a push button control, a shutdown mode, as well as an industry-leading µTQFN package.

The push button control has individual $\overline{PU}$ and $\overline{PD}$ inputs for adjusting the wiper. To eliminate redundancy, the wiper position will automatically increment or decrement if one of these inputs is held longer than 1s.

Forcing both $\overline{PU}$ and $\overline{PD}$ low for more than 2s activates shutdown mode. Shutdown mode disconnects the top of the resistor chain and moves the wiper to the lowest position, minimizing power consumption.

The three terminals accessing the resistor chain naturally configure the ISL23511 as a voltage divider. A rheostat is easily formed by floating an end terminal or connecting it to the wiper.



Features

- Solid-state volatile potentiometer
- Push button controlled
- Single or Auto increment/decrement
  - Fast Mode after 1s button press
- Shutdown Mode
- 32 wiper tap points
  - Zero scale wiper position on power-up
- Low power CMOS
  - V_{CC} = 2.7V to 5.5V
  - Terminal voltage, 0 to V_{CC}
  - Standby current, 3µA max
- R_{TOTAL} value = 10kΩ, 50kΩ
- Packages
  - 8 Ld SOIC and 10 Ld µTQFN (2.1mmx1.6mm)
- Pb-free (RoHS compliant)

Applications

- Volume Control
- LED/LCD Brightness Control
- Contrast Control
- Programming Bias Voltages
- Ladder Networks

Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL23511WFB8Z* (Note 1)	23511 WFBZ	10	-40 to +125	8 Ld SOIC	M8.15
ISL23511UFB8Z* (Note 1)	23511 UFBZ	50	-40 to +125	8 Ld SOIC	M8.15
ISL23511WFRU10Z* (Note 2)	GA	10	-40 to +125	10 Ld µTQFN	L10.2.1x1.6A
ISL23511UFRU10Z* (Note 2)	FZ	50	-40 to +125	10 Ld µTQFN	L10.2.1x1.6A

*Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

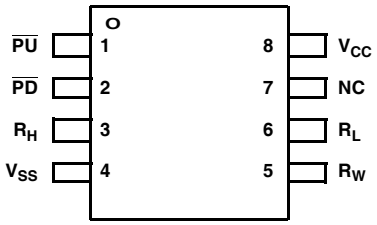
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

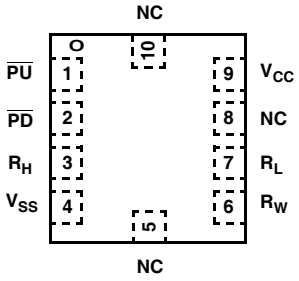
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
XDCP is a trademark of Intersil Americas Inc. Copyright Intersil Americas Inc. 2007, 2008. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

Pinouts

ISL23511
(8 LD SOIC)
TOP VIEW



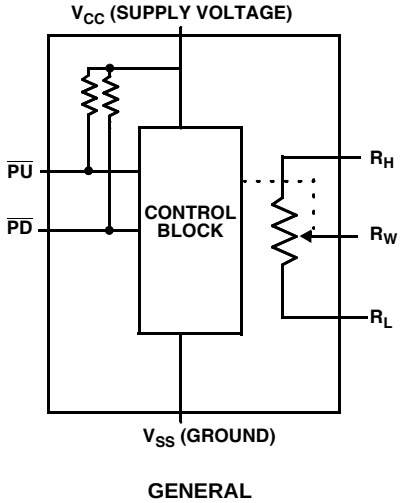
ISL23511
(10 LD µTQFN)
TOP VIEW



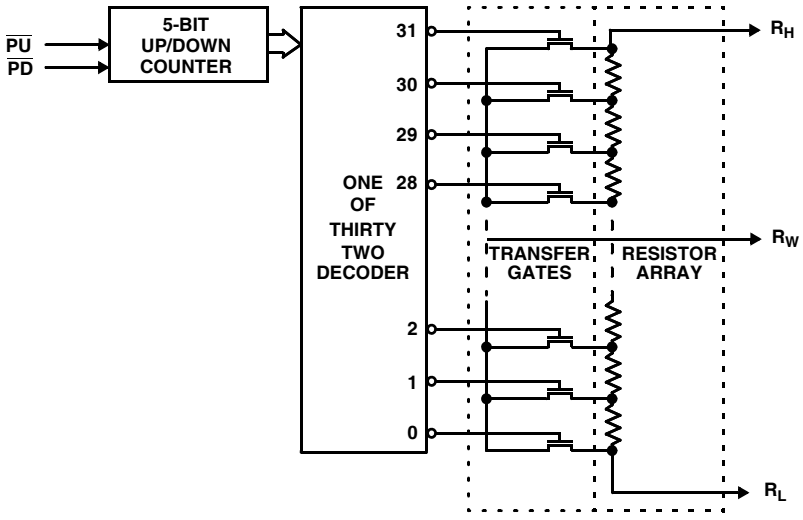
Pin Descriptions

SOIC PIN	µTQFN PIN	SYMBOL	BRIEF DESCRIPTION
1	1	$\overline{PU}$	The $\overline{PU}$ is a negative-edge triggered input with internal pull-up. Toggling $\overline{PU}$ will move the wiper close to R_H terminal.
2	2	$\overline{PD}$	The $\overline{PD}$ is a negative-edge triggered input with internal pull-up. Toggling $\overline{PD}$ will move the wiper close to R_L terminal.
3	3	R_H	The R_H and R_L pins of the ISL23511 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_H and RL references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$/$\overline{PD}$ input.
4	4	V_{SS}	Ground
5	6	R_W	The R_W pin is the wiper terminal of the potentiometer, which is equivalent to the movable terminal of a mechanical potentiometer.
6	7	R_L	The R_H and R_L pins of the ISL23511 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_H and R_L references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$/$\overline{PD}$ input.
7	5, 8, 10	NC	No connection
8	9	V_{CC}	Supply Voltage

Block Diagrams



GENERAL



DETAILED

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at $\overline{PU}$ and $\overline{PD}$ Pin with Respect to GND . -0.3V to V_{CC} + 0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND. . . . . -0.3V to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A @ +125°C
ESD Rating
Human Body Model 3kV
Machine Model. 250V

Thermal Information

Thermal Resistance (Typical, Note 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead SOIC	120	
10 Lead µTQFN	150	48.3

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Extended Industrial). . . . . -40°C to +125°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating. 15mW
Wiper Current . . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Potentiometer Specifications

Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±80		ppm/°C (Note 16)
		U option		±125		ppm/°C (Note 16)
R_W	Wiper Resistance	V_{CC} = 3.3V, wiper current $I_{RW} = V_{CC}/R_{TOTAL}$		130	400	Ω
V_{RH}, V_{RL}	V_{RH} and V_{RL} Terminal Voltages	V_{RH} and V_{RL} to GND	0		V_{CC}	V
	Noise on Wiper Terminal	From 0Hz to 10MHz		-80		dBV
$C_H/C_L/C_W$ (Note 17)	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}		0.05	0.4	µA
VOLTAGE DIVIDER MODE (0V @ R_L; V_{CC} @ R_H; measured at R_W unloaded)						
INL (Note 10)	Integral Non-linearity		-1		1	LSB (Note 6)
DNL (Note 9)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 6)
ZSerror (Note 7)	Zero-scale Error	W option	0	0.3	3	LSB (Note 6)
		U option	0	0.3	1	
FSerror (Note 8)	Full-scale Error	W option	-3	-0.3	0	LSB (Note 6)
		U option	-1	-0.3	0	
TC_V (Note 11)	Ratiometric Temperature Coefficient	Wiper from 5 hex to 1F hex for W and U option		±25		ppm/°C
f_{CUTOFF}	3dB Cut-Off Frequency	Wiper at the middle scale, W option		500		kHz
		Wiper at the middle scale, U option		75		kHz
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 15)	Integral Non-linearity	DCP register set between 1 hex and 1F hex; monotonic over all tap positions; W option	-1.5		1.5	MI (Note 12)
		DCP register set between 1 hex and 1F hex; monotonic over all tap positions; U option	-1		1	MI (Note 12)

Potentiometer Specifications Over recommended operating conditions, unless otherwise specified. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
RDNL (Note 14)	Differential Non-linearity	W and U option	-0.5		0.5	MI (Note 12)
Roffset (Note 13)	Offset	W option	0	1	3	MI (Note 12)
		U option	0	0.5	1	MI (Note 12)

DC Electrical Specifications Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
I_{CC}	V_{CC} Active Current	V_{CC} = 5.5V, perform wiper move operation			150	µA
I_{SB}	Standby Current			0.6	3	µA
I_{Lkg}	$\overline{PU}$, $\overline{PD}$ Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	-2		+2	µA
V_{IH}	$\overline{PU}$, $\overline{PD}$ Input HIGH Voltage		V_{CC} x 0.7			V
V_{IL}	$\overline{PU}$, $\overline{PD}$ input LOW Voltage				V_{CC} x 0.1	V
C_{IN} (Note 17)	$\overline{PU}$, $\overline{PD}$ Input Capacitance	V_{CC} = 3.3V, T_A = +25°C, f = 1MHz		10		pF
Rpull_up (Note 17)	Pull-up Resistor for $\overline{PU}$ and $\overline{PD}$			1		MΩ

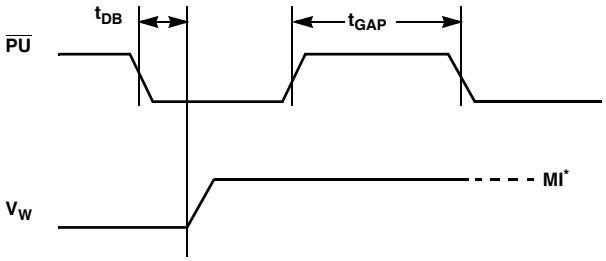
AC Electrical Specifications Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
t_{GAP}	Time Between Two Separate Push Button Events	2			ms
t_{DB}	Debounce Time		15	30	ms
$t_{S\ SLOW}$	Wiper Change on a Slow Mode	100	250	375	ms
$t_{S\ FAST}$	Wiper Change on a Fast Mode	25	50	75	ms
t_{stdn} (Note 17)	Time to Enter Shutdown Mode (keep $\overline{PU}$ and $\overline{PD}$ LOW)		2		s
t_R VCC	V_{CC} Power-up Rate	0.2		50	V/ms

NOTES:

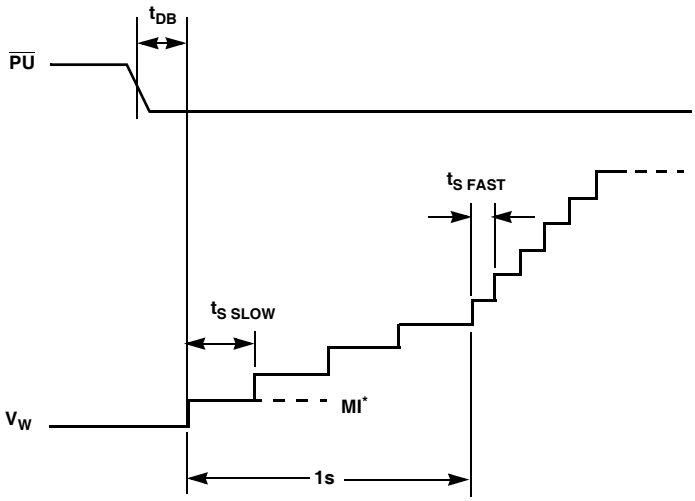
5. Typical values are for T_A = +25°C and 3.3V supply voltage.
6. LSB: $[V(RW)_{31} – V(RW)_0]/31$. $V(RW)_{31}$ and $V(RW)_0$ are voltage on RW pin for the DCP register set to 1F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.
8. FS error = $[V(RW)_{31} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB -1, for i = 1 to 31; i is the DCP register setting.
10. INL = $[V(RW)_i – i • LSB – V(RW)]$/LSB for i = 1 to 31
11. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 5 to 31 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{31} – RW_0|/31$. MI is a minimum increment. RW_{31} and RW_0 are the measured resistances for the DCP register set to 1F hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{31}/MI, when measuring between RW and RH.
14. RDNL = $(RW_i – RW_{i-1})$/MI, for i = 1 to 31.
15. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 1 to 31.
16. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 5 to 31, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
17. Limits should be considered typical and are not production tested.
18. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Slow Mode Timing



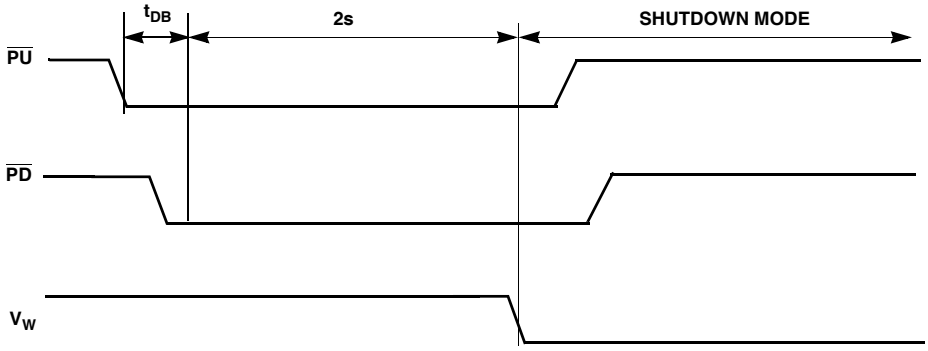
* MI in the AC timing diagram refers to the minimum incremental change in the wiper voltage.

Fast Mode Timing



* MI in the AC timing diagram refers to the minimum incremental change in the wiper voltage.

Shutdown Mode Timing



Typical Performance Curves

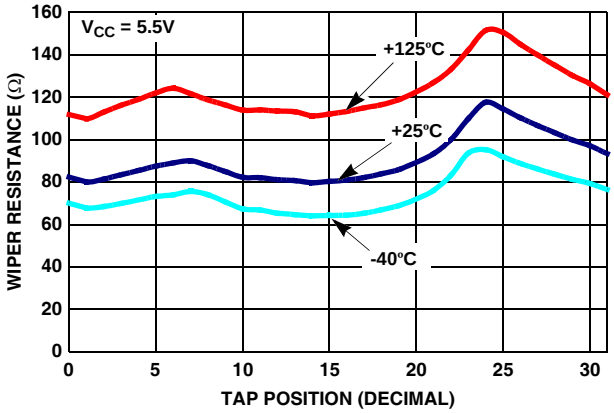


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

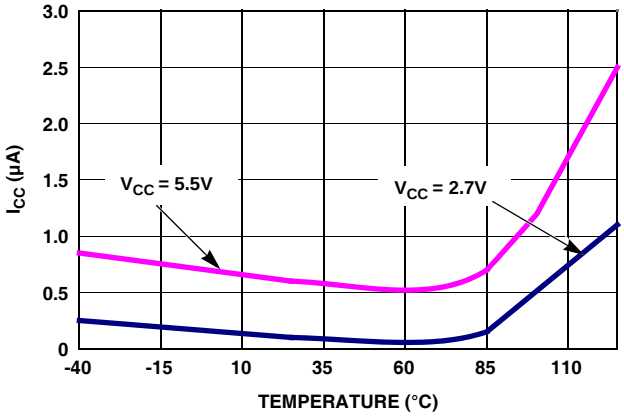


FIGURE 2. STANDBY I_{CC} vs TEMPERATURE

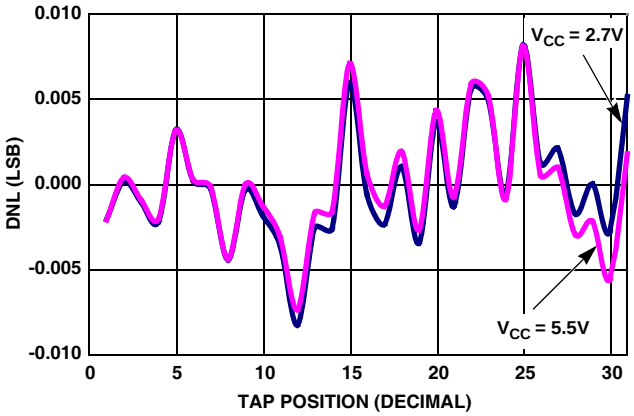


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

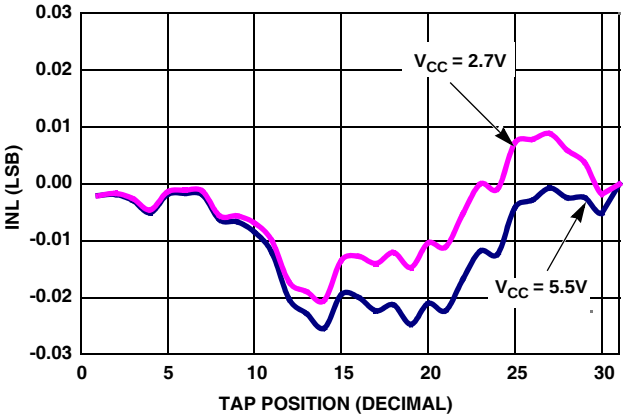


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

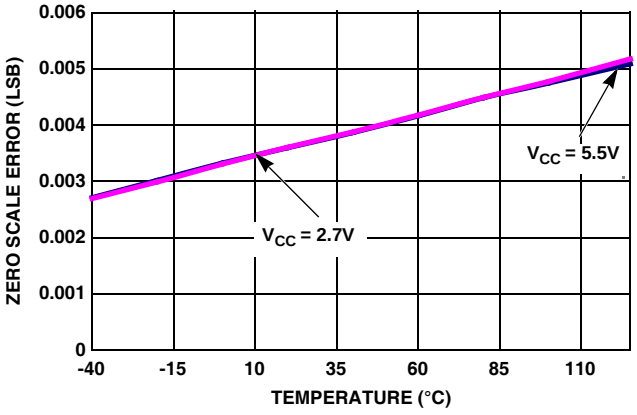


FIGURE 5. ZS ERROR vs TEMPERATURE

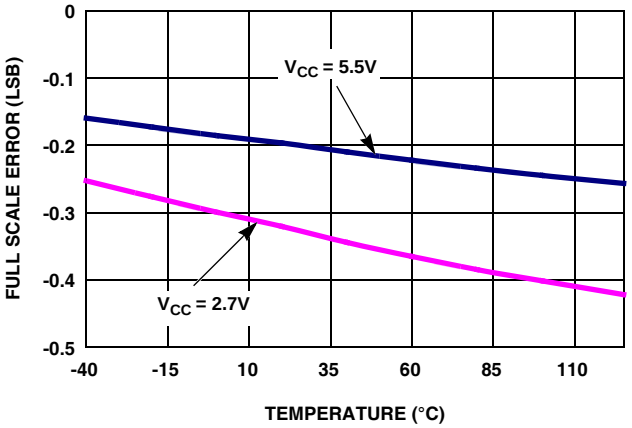


FIGURE 6. FS ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

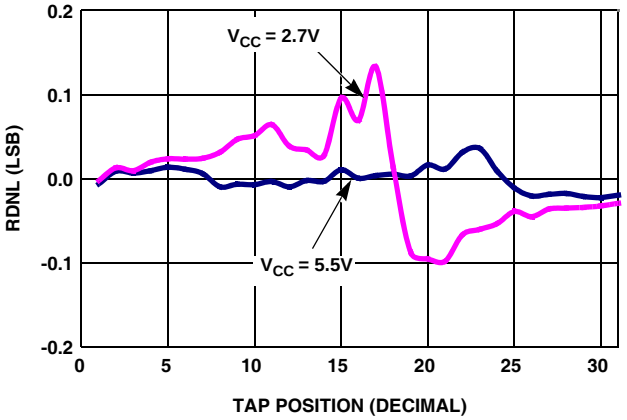


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

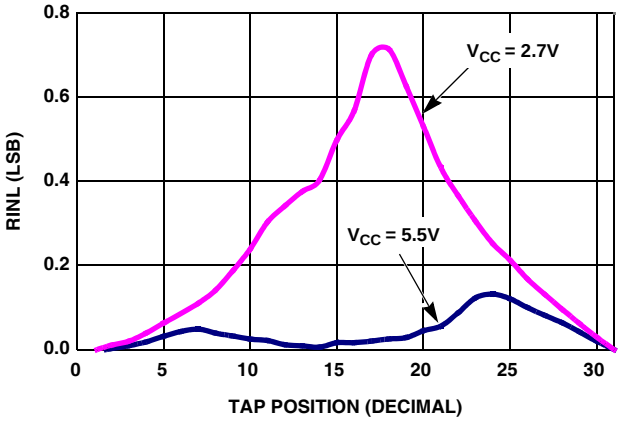


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

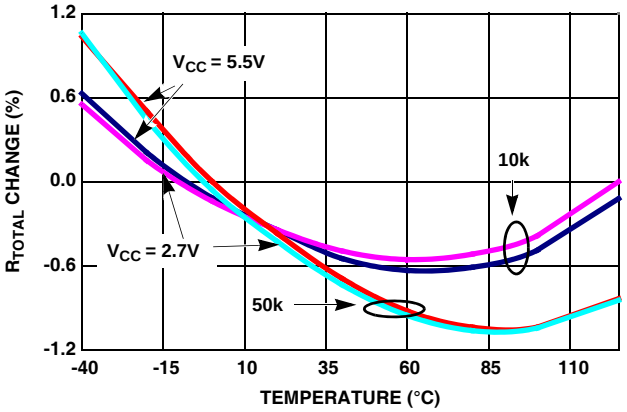


FIGURE 9. END-TO-END R_{TOTAL} % CHANGE vs TEMPERATURE

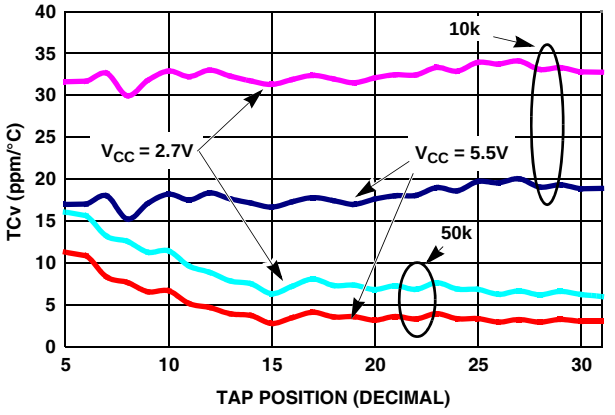


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

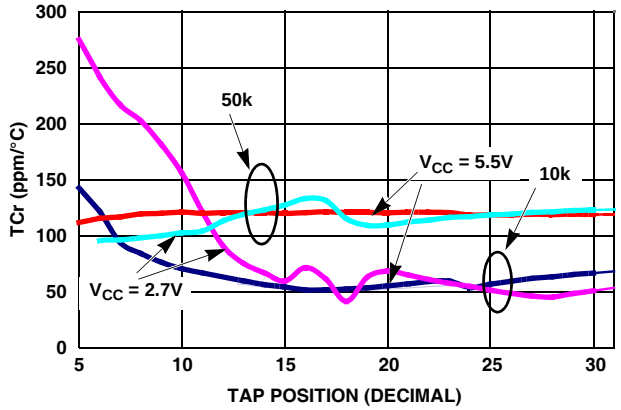


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

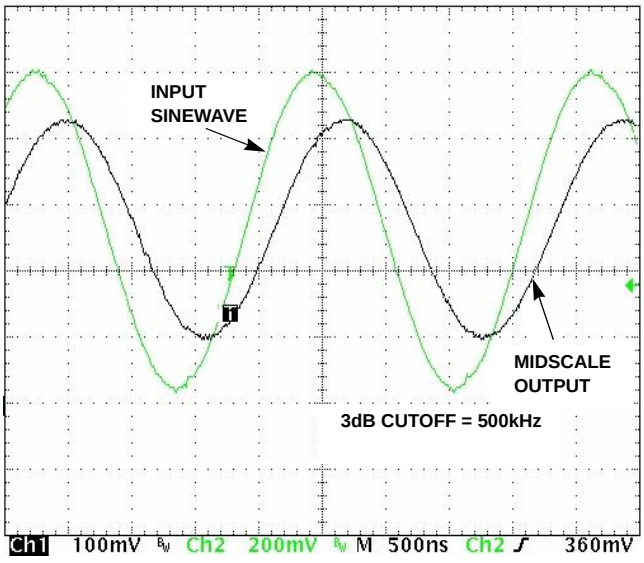


FIGURE 12. FREQUENCY RESPONSE (500kHz)

Power-up and Power-down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_{RH} and V_{RL}, i.e., $V_{CC} \geq V_{RH}, V_{RL}$. The V_{CC} ramp rate specification is always in effect.

Pin Descriptions

R_H and R_L

The R_H and R_L pins of the ISL23511 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_H and R_L references the relative position of the terminal in relation to wiper movement direction.

R_W

The R_W pin is the wiper terminal of the potentiometer which is equivalent to the movable terminal of a mechanical potentiometer. The default wiper position at power-up is at 0 tap.

$\overline{PU}$

The debounced $\overline{PU}$ input is used to increment the wiper position. An on-chip pull-up holds the $\overline{PU}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent higher tap position.

$\overline{PD}$

The debounced $\overline{PD}$ input is used to decrement the wiper position. An on-chip pull-up holds the $\overline{PD}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent lower tap position.

Device Operation

There are three sections of the ISL23511: the input control, the counter and decode section and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch, connecting a point on the resistor array to the wiper output. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The ISL23511 is designed to interface directly to two push button switches for effectively moving the wiper up or down. The $\overline{PU}$ and $\overline{PD}$ inputs increment or decrement a 5-bit counter respectively. The output of this counter is decoded to select one of the thirty-two wiper positions along the resistive array. The wiper increment input, $\overline{PU}$ and the wiper decrement input, $\overline{PD}$ are both connected to an internal pull-up so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position.

Internal debounce circuitry prevents inadvertent switching of the wiper position if $\overline{PU}$ or $\overline{PD}$ remain LOW for less than 15ms, typical. Each of the buttons can be pushed either once for a single increment/decrement or continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position depend on how long the button is being pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second, the device will be in the slow scan mode. Then, if the button is held for longer than 1s, the device will go into the fast scan mode. As soon as the button is released, the ISL23511 will return to a stand-by condition.

If both $\overline{PU}$ and $\overline{PD}$ buttons are pulled low more than 15ms from each other, all commands are ignored upon release of ALL buttons.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

Shutdown Mode

The ISL23511 enters into Shutdown Mode if both $\overline{PU}$ and $\overline{PD}$ inputs are kept LOW for 2s. In this mode, the resistors array is totally disconnected from its R_H pin and the wiper is moved to the position closest to the R_L pin, as shown in Figure 13.

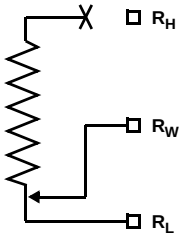


FIGURE 13. DCP CONNECTION IN SHUTDOWN MODE

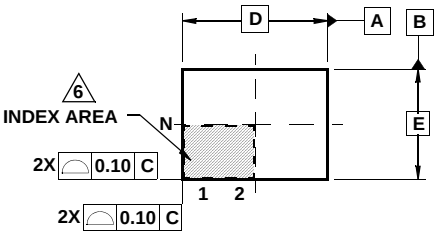
Note that $\overline{PU}$ and $\overline{PD}$ inputs must be brought LOW within t_{DB} time window of 15ms (see “Shutdown Mode Timing” on page 5) otherwise all commands will be ignored until both inputs are released.

Holding either $\overline{PU}$ or $\overline{PD}$ input LOW for more than 15ms will exit shutdown mode and return wiper to prior shutdown position. If $\overline{PU}$ or $\overline{PD}$ will be held LOW for more than 250ms, the ISL23511 will start auto-increment or auto-decrement of wiper position.

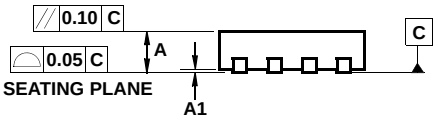
R_{TOTAL} with V_{CC} Removed

The end-to-end resistance of the array will fluctuate once V_{CC} is removed.

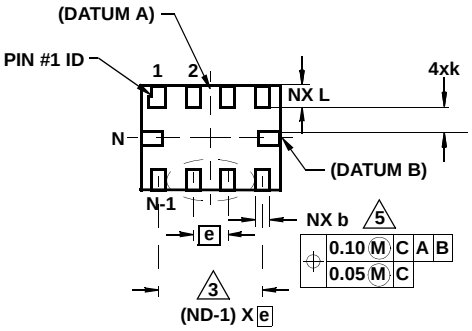
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



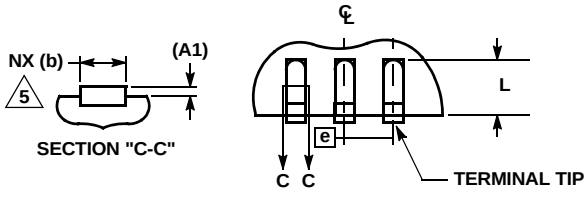
TOP VIEW



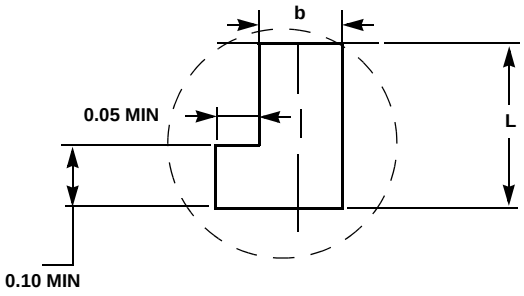
SIDE VIEW



BOTTOM VIEW



FOR ODD TERMINAL/SIDE



DETAIL “A” PIN 1 ID

L10.2.1x1.6A

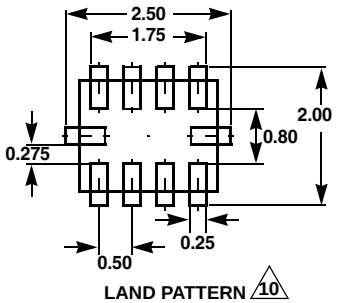
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		10		2
Nd		4		3
Ne		1		3
θ	0	-	12	4

Rev. 3 6/06

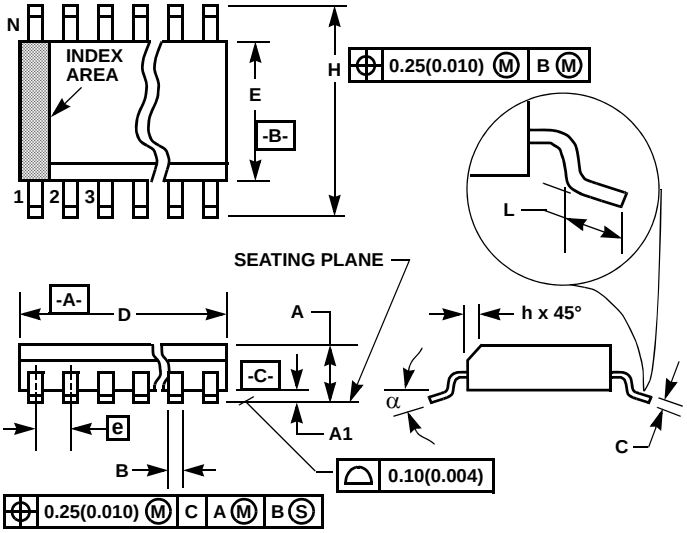
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com