Data Sheet | December 4, 2006 | FN6173.3

## Dual Channel Differential DSL Line Driver

The ISL1532 is a dual channel differential amplifier designed for driving full rate ADSL2+ signals at very low power dissipation. The high drive capability of 450mA makes this driver ideal for DMT designs. It contains two pairs of wideband, high-voltage, current mode feedback amplifiers designed on Intersil's HS30 Bipolar SOI process for low power consumption in DSL systems.

These drivers achieve an MTPR distortion measurement of better than 70dB, while consuming typically 5mA per DSL channel of total supply current. This supply current can be set using a resistor on the $I_{ADJ}$ pin. Two other pins ($C_0$ and $C_1$) can also be used to adjust supply current to one of four pre-set modes (full-$I_S$, 3/4-$I_S$, 1/2-$I_S$, and full power-down). $C_0$ and $C_1$ inputs are design to pull high initially. Floating these inputs will put the device in disable mode. This is contrary to EL1528 where $C_0$ and $C_1$ inputs pull low initially and is in the enable state when $C_0$ and $C_1$ pins are floated.

The ISL1532 operates on ±5V to ±15V supplies and retains its bandwidth and linearity over the complete supply range.

The device is supplied in a thermally-enhanced 20 Ld HTSSOP and the small footprint (4x5mm) 24 Ld QFN packages. The ISL1532 is specified for operation over the full -40°C to +85°C temperature range.

The ISL1532 provides larger output swing at heavy loads, higher slew rate, and higher bandwidth while maintaining pin-to-pin drop-in compatibility with the EL1528. The ISL1532 integrates 50k pull-up resistors on $C_0$ and $C_1$ pins.

## Features

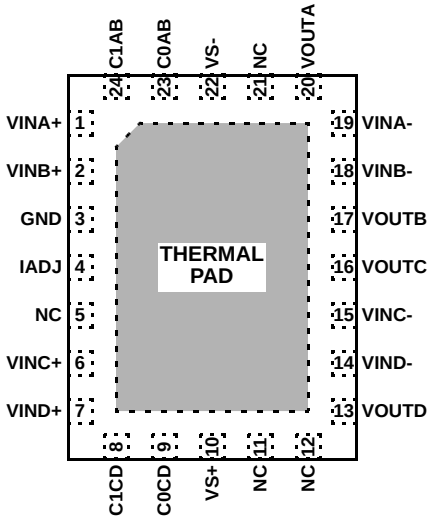
- 450mA output drive capability
- 44.4$V_{P-P}$ differential output drive into 100Ω
- ±5V to ±15V supply operation
- MTPR of -70dB
- Operates down to 2mA per amplifier supply current
- Current control pins
- Channel separation
  - 80dB @ 500kHz
- Direct pin-to-pin replacement for EL1528
- Pb-free plus anneal available (RoHS compliant)

## Applications

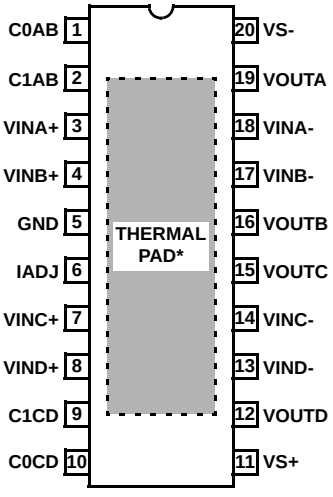
- Dual port ADSL2+ line drivers
- HDSL line drivers

## Pinouts

**ISL1532 (24 LD QFN)**
TOP VIEW




**ISL1532 (20 Ld HTSSOP)**
TOP VIEW




***THERMAL PAD INTERNALLY CONNECTED TO GND**



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Ordering Information

| PART NUMBER (See Note) | PART MARKING | TAPE & REEL | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL1532IRZ | 1532 IRZ | - | 24 Ld QFN | MDP0046 |
| ISL1532IRZ-T7 | 1532 IRZ | 7” | 24 Ld QFN | MDP0046 |
| ISL1532IRZ-T13 | 1532 IRZ | 13” | 24 Ld QFN | MDP0046 |
| ISL1532IVEZ | 1532 IVEZ | - | 20 Ld HTSSOP | MDP0048 |
| ISL1532IVEZ-T7 | 1532 IVEZ | 7” | 20 Ld HTSSOP | MDP0048 |
| ISL1532IVEZ-T13 | 1532 IVEZ | 13” | 20 Ld HTSSOP | MDP0048 |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Absolute Maximum Ratings ($T_A$ = +25°C)

$V_S$+ to $V_S$- Supply Voltage. . . . . -0.3V to 30V
$V_S$+ Voltage to GND . . . . . -0.3V to 30V
$V_S$- Voltage to GND . . . . . -30V to 0.3V
Driver $V_{IN}$+ Voltage . . . . . $V_S$- to $V_S$+
$C_0$, $C_1$ Voltage to GND . . . . . -0.3V to 6V
$I_{ADJ}$ Voltage to GND . . . . . -0.3V to 4V
Current into any Input . . . . . 8mA
Output Current from Driver (Static) . . . . . 50mA
Power Dissipation . . . . . See Curves
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +150°C

## ESD Rating

Human Body Model (Per MIL-STD-883 Method 3015.7). . . . . 3kV
Machine Model (Per EIAJ ED-4701 Method C-111) . . . . . 250V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.*

## Electrical Specifications

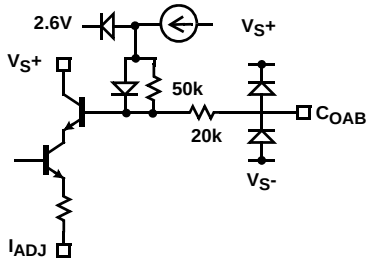
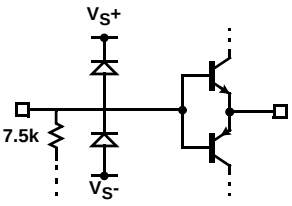
$V_S$ = ±12V, $R_F$ = 3kΩ, $R_L$= 65Ω, $I_{ADJ}$ = $C_0$ = $C_1$ = 0V, $T_A$ = +25°C. Amplifiers tested separately.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CHARACTERISTICS** | | | | | | |
| $I_S$+ (Full $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 0V, $R_{ADJ}$ = 0 | 3.75 | 4.9 | 6.5 | mA |
| $I_S$- (Full $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 0V, $R_{ADJ}$ = 0 | -6.3 | -4.7 | -3.5 | mA |
| $I_S$+ (3/4 $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = 5V, $C_1$ = 0V, $R_{ADJ}$ = 0 | | 3.8 | | mA |
| $I_S$- (3/4 $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = 5V, $C_1$ = 0V, $R_{ADJ}$ = 0 | | -3.5 | | mA |
| $I_S$+ (1/2 $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = 0V, $C_1$ = 5V, $R_{ADJ}$ = 0 | 1.87 | 2.6 | 3.75 | mA |
| $I_S$- (1/2 $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = 0V, $C_1$ = 5V, $R_{ADJ}$ = 0 | -3.75 | -2.4 | -1.75 | mA |
| $I_S$+ (Power-down) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 5V, $R_{ADJ}$ = 0 | | 0.25 | 1.0 | mA |
| $I_S$- (Power-down) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 5V, $R_{ADJ}$ = 0 | -1.0 | 0 | | mA |
| $I_{GND}$ | GND Supply Current per Amplifier | All outputs at 0V | | 0.25 | | mA |
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | -10 | 1 | +10 | mV |
| $\Delta V_{OS}$ | $V_{OS}$ Mismatch | | -5 | 0 | +5 | mV |
| $I_B$+ | Non-Inverting Input Bias Current | | -15 | | +14 | µA |
| $I_B$- | Inverting Input Bias Current | | -30 | | +30 | µA |
| $\Delta I_B$- | $I_B$- Mismatch | | -25 | 0 | +25 | µA |
| $R_{OL}$ | Transimpedance | | 1 | 3.4 | 8 | MΩ |
| $e_N$ | Input Noise Voltage | | | 3.5 | | $nV/\sqrt{Hz}$ |
| $i_N$ | -Input Noise Current | | | 2 | | $pA/\sqrt{Hz}$ |
| $V_{IH}$ | Input High Voltage | $C_0$ and $C_1$ inputs, with signal | 1.8 | | | V |
| | | $C_0$ and $C_1$ inputs, without signal | 1.6 | | | V |
| $V_{IL}$ | Input Low Voltage | $C_0$ and $C_1$ inputs | | | 0.8 | V |
| $I_{IH0}$, $I_{IH1}$ | Input High Current for $C_0$, $C_1$ | $C_0$ = 5V, $C_1$ = 5V | 10 | 20 | 40 | µA |
| $I_{IL}$ | Input Low Current for $C_0$ or $C_1$ | $C_0$ = 0V, $C_1$ = 0V | -3.0 | -0.3 | | µA |

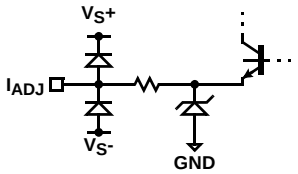
**Electrical Specifications** $V_S$ = ±12V, $R_F$ = 3kΩ, $R_L$= 65Ω, $I_{ADJ}$ = $C_0$ = $C_1$ = 0V, $T_A$ = +25°C. Amplifiers tested separately. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Loaded Output Swing ($R_L$ Single-ended to GND) | $R_L$ = 100Ω | | ±11.1 | | V |
| | | $R_L$ = 50Ω (+) | +10.5 | +10.95 | | V |
| | | $R_L$ = 50Ω (-) | | -10.95 | -10.5 | V |
| | | $R_L$ = 25Ω (+) | +10.0 | +10.7 | | V |
| | | $R_L$ = 25Ω (-) | | -10.5 | -9.6 | V |
| $I_{OL}$ | Linear Output Current | $A_V$ = 5, $R_L$ = 10Ω, f = 100kHz, THD = -60dBc (10Ω single-ended) | | 450 | | mA |
| $I_{OUT}$ | Output Current | $V_{OUT}$ = 1V, $R_L$ = 1Ω | | 1 | | A |
| **DYNAMIC PERFORMANCE** | | | | | | |
| BW | -3dB Bandwidth | $A_V$ = +5, $R_{L-DIFF}$ = 100Ω | | 50 | | MHz |
| HD2 | 2nd Harmonic Distortion | $f_C$ = 1MHz, $R_F$ = 5kΩ, $A_V$ = 10, $R_{L-DIFF}$ = 100Ω, $V_{OUT}$ = $2V_{PP-DIFF}$ | | -90 | | dBc |
| | | $f_C$ = 1MHz, $R_F$ = 5kΩ, $A_V$ = 10, $R_{L-DIFF}$ = 50Ω, $V_{OUT}$ = $2V_{PP-DIFF}$ | | -85 | | dBc |
| HD3 | 3rd Harmonic Distortion | $f_C$ = 1MHz, $R_F$ = 5kΩ, $A_V$ = 10, $R_{L-DIFF}$ = 100Ω, $V_{OUT}$ = $2V_{PP-DIFF}$ | | -80 | | dBc |
| | | $f_C$ = 1MHz, $R_F$ = 5kΩ, $A_V$ = 10, $R_{L-DIFF}$ = 50Ω, $V_{OUT}$ = $2V_{PP-DIFF}$ | | -65 | | dBc |
| MTPR | Multi-Tone Power Ratio | 26kHz to 1.1MHz, $R_{LINE}$ = 100Ω, $P_{LINE}$ = 20.4dBM | | -70 | | dBc |
| SR | Slew rate (single-ended) | $V_{OUT}$ from -8V to +8V measured at ±4V | 200 | 400 | | V/µs |

## Pin Descriptions

| 20 Ld HTSSOP | 24 Ld QFN | PIN NAME | FUNCTION | CIRCUIT |
|---|---|---|---|---|
| 1 | 23 | C0AB (Note 1) | DSL Channel 1 current control pin |   CIRCUIT 1 |
| 2 | 24 | C1AB (Note 1) | DSL Channel 1 current control pin | (Reference Circuit 1) |
| | 5, 11, 12, 21 | NC | Not connected | |
| 3 | 1 | VINA+ | Amplifier A non-inverting input |   CIRCUIT 2 |
| 4 | 2 | VINB+ | Amplifier B non-inverting input | (Reference Circuit 2) |

## Pin Descriptions

| 20 Ld HTSSOP | 24 Ld QFN | PIN NAME | FUNCTION | CIRCUIT |
|---|---|---|---|---|
| 6 | 4 | IADJ (Note 2) | Supply current control pin for both DSL Channels 1 and 2 |  CIRCUIT 3 |
| 5 | 3 | GND | Ground connection | |
| 7 | 6 | VINC+ | Amplifier C non-inverting input | (Reference Circuit 2) |
| 8 | 7 | VIND+ | Amplifier D non-inverting input | (Reference Circuit 2) |
| 9 | 8 | C1CD (Note 3) | DSL Channel 2 current control pin | (Reference Circuit 1) |
| 10 | 9 | C0CD (Note 3) | DSL Channel 2 current control pin | (Reference Circuit 1) |
| 11 | 10 | VS+ | Positive supply | |
| 12 | 13 | VOUTD | Amplifier D output | (Reference Circuit 2) |
| 13 | 14 | VIND- | Amplifier D inverting input | (Reference Circuit 2) |
| 14 | 15 | VINC- | Amplifier C inverting input | (Reference Circuit 2) |
| 15 | 16 | VOUTC | Amplifier C output | (Reference Circuit 2) |
| 16 | 17 | VOUTB | Amplifier B output | (Reference Circuit 2) |
| 17 | 18 | VINB- | Amplifier B inverting input | (Reference Circuit 2) |
| 18 | 19 | VINA- | Amplifier A inverting input | (Reference Circuit 2) |
| 19 | 20 | VOUTA | Amplifier A output | (Reference Circuit 2) |
| 20 | 22 | VS- | Negative supply | |



NOTES:

1. Amplifiers A and B comprise DSL Channel 1. $C_{0AB}$ and $C_{1AB}$ control $I_S$ settings for DSL Channel 1.
2. $I_{ADJ}$ controls bias current ($I_S$) setting for both DSL channels.
3. Amplifiers C and D comprise DSL Channel 2. $C_{0CD}$ and $C_{1CD}$ control $I_S$ settings for DSL Channel 2.

## Typical Performance Curves

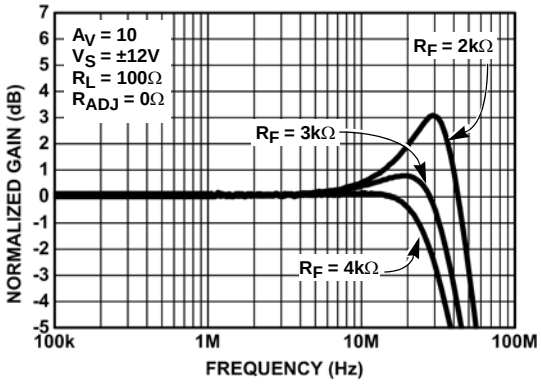



FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (FULL $I_S$)

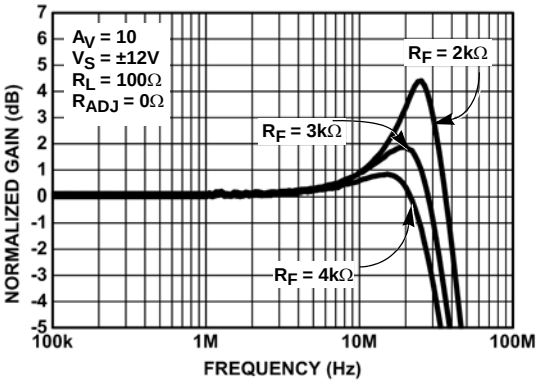



FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (3/4 $I_S$)

## Typical Performance Curves (Continued)

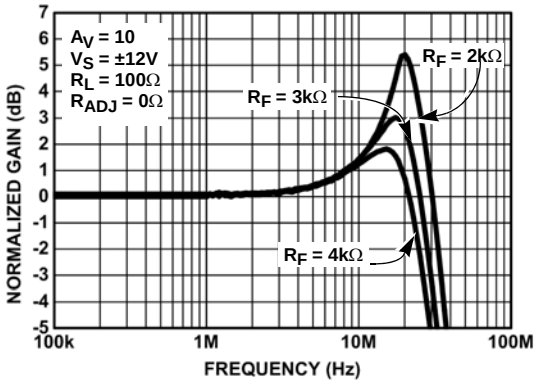



FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (1/2 $I_S$)

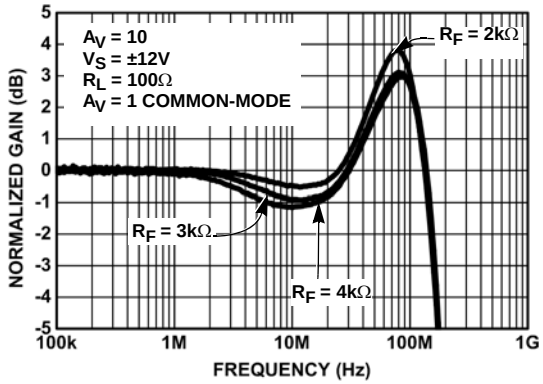



FIGURE 4. COMMON-MODE FREQUENCY RESPONSE vs $R_F$ (FULL $I_S$)

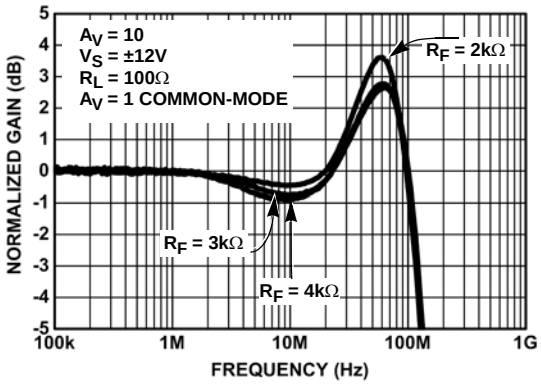



FIGURE 5. COMMON-MODE FREQUENCY RESPONSE vs $R_F$ (3/4 $I_S$)

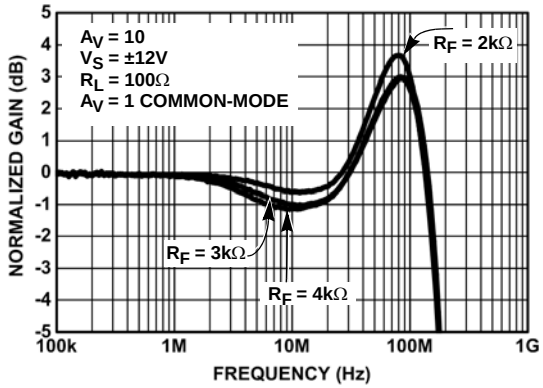



FIGURE 6. COMMON-MODE FREQUENCY RESPONSE vs $R_F$ (1/2 $I_S$)

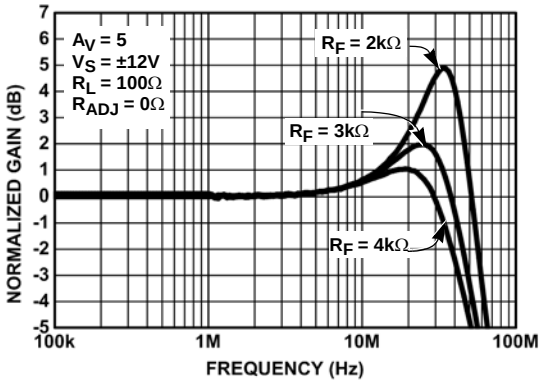



FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (FULL $I_S$)

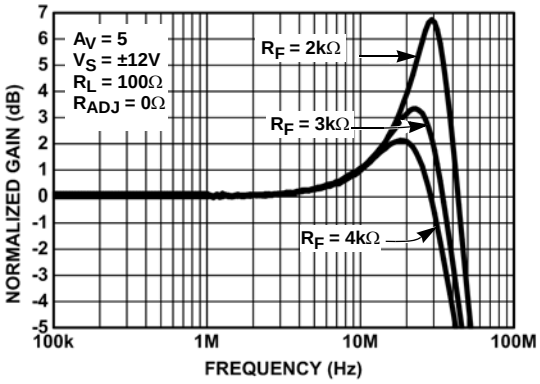



FIGURE 8. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (3/4 $I_S$)

## Typical Performance Curves (Continued)

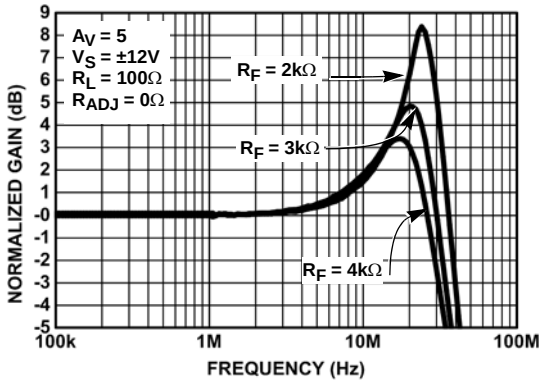



FIGURE 9. DIFFERENTIAL FREQUENCY RESPONSE vs $R_F$ (1/2 $I_S$)

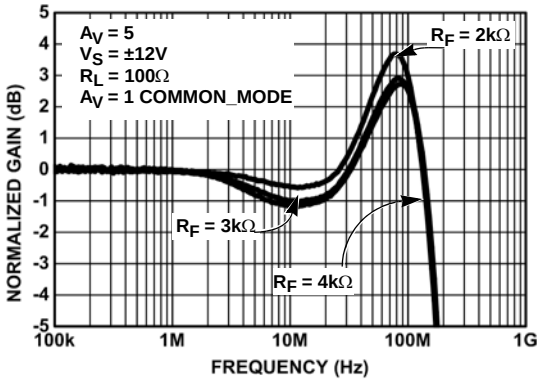



FIGURE 10. COMMON-MODE FREQUENCY RESPONSE vs $R_F$ (FULL $I_S$)

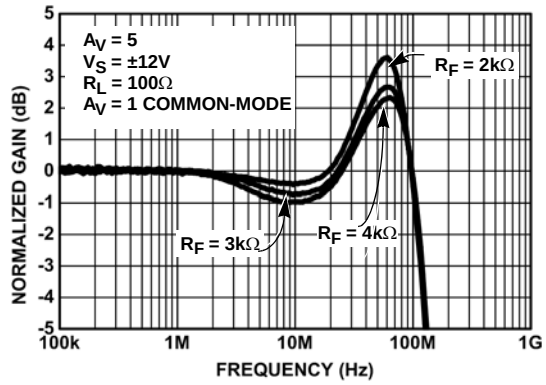



FIGURE 11. COMMON-MODEFREQUENCY RESPONSE vs $R_F$ (3/4 $I_S$)

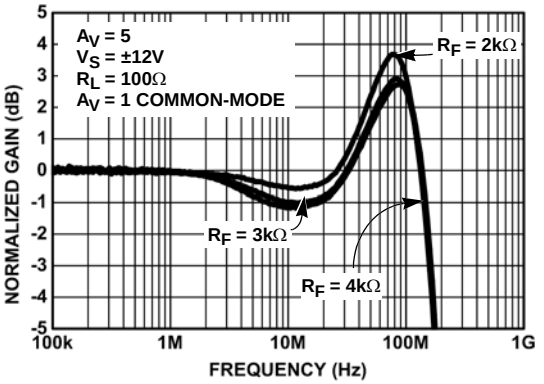



FIGURE 12. COMMON-MODE FREQUENCY RESPONSE vs $R_F$ (1/2 $I_S$)

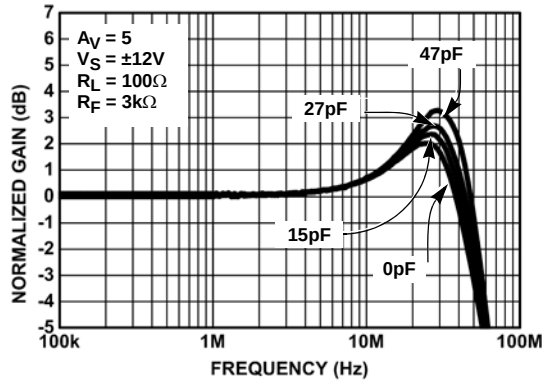



FIGURE 13. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (FULL $I_S$)

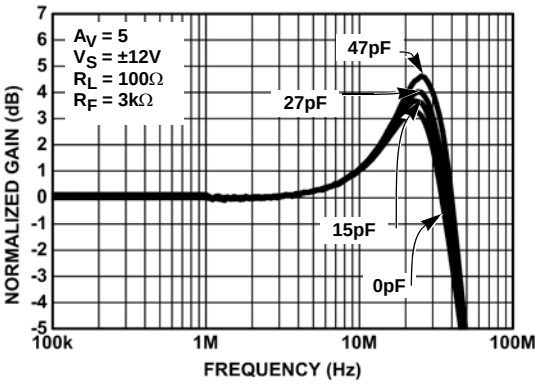



FIGURE 14. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (3/4 $I_S$)

## Typical Performance Curves (Continued)

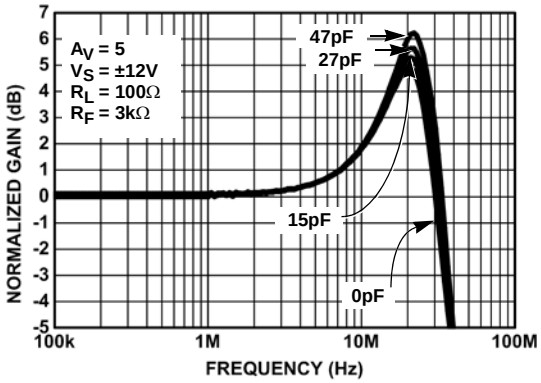



FIGURE 15. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (1/2 $I_S$)

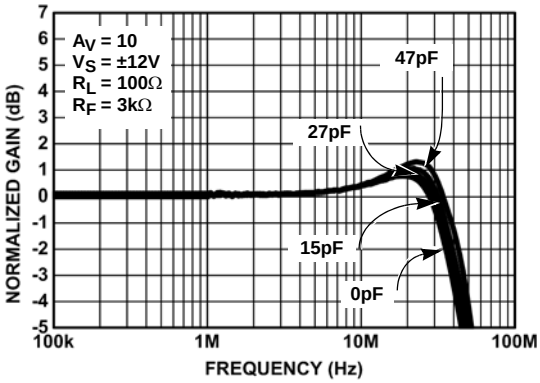



FIGURE 16. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (FULL $I_S$)

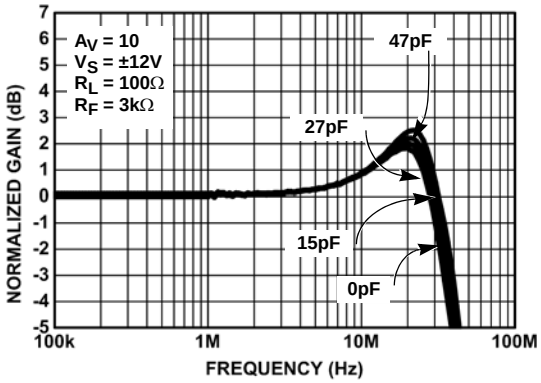



FIGURE 17. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (3/4 $I_S$)

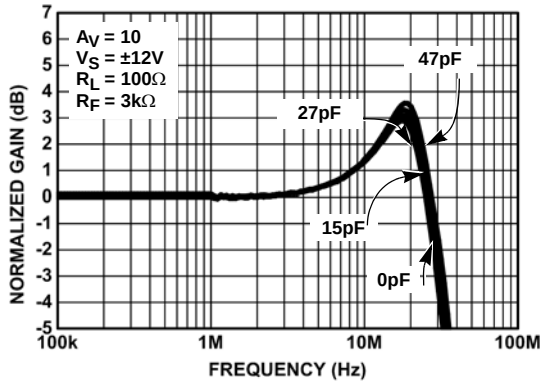



FIGURE 18. DIFFERENTIAL FREQUENCY RESPONSE vs $C_L$ (1/2 $I_S$)

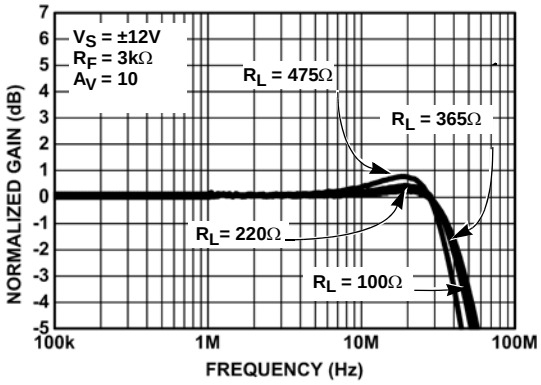



FIGURE 19. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (FULL $I_S$)

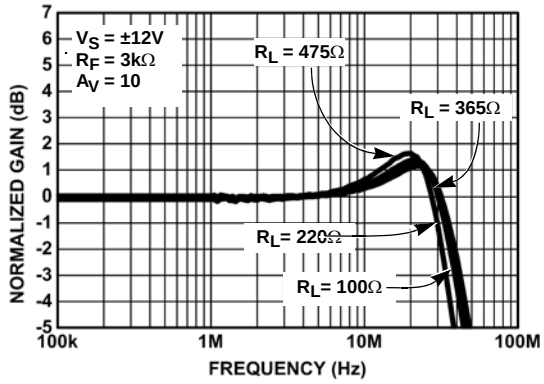



FIGURE 20. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (3/4 $I_S$)

## Typical Performance Curves (Continued)

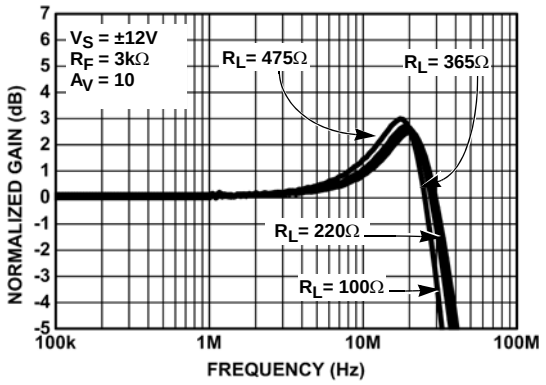



FIGURE 21. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (1/2 $I_S$)

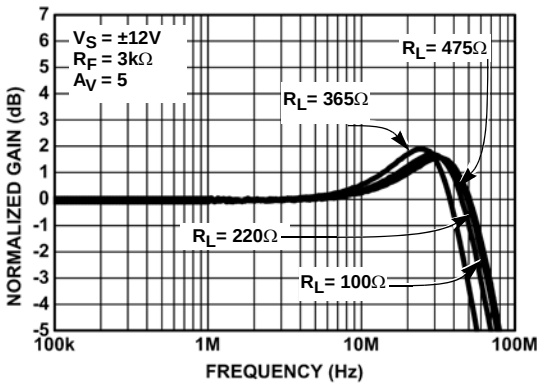



FIGURE 22. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (FULL $I_S$)

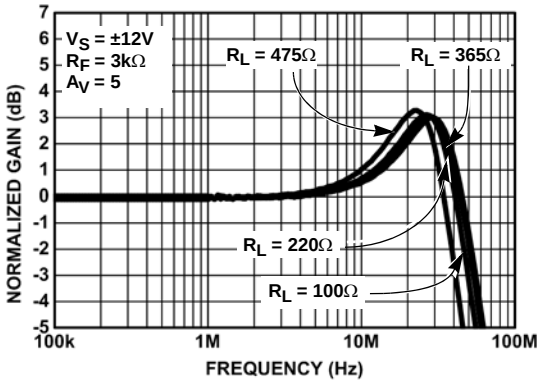



FIGURE 23. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (3/4 $I_S$)

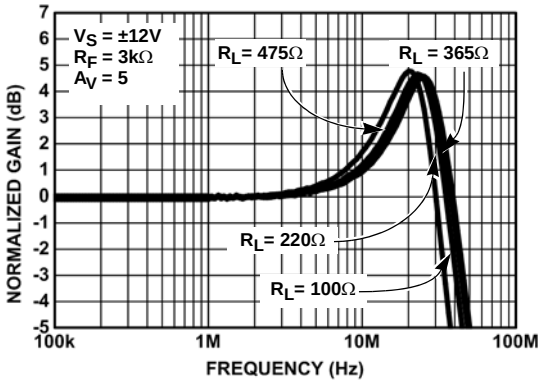



FIGURE 24. DIFFERENTIAL FREQUENCY RESPONSE vs $R_L$ (1/2 $I_S$)

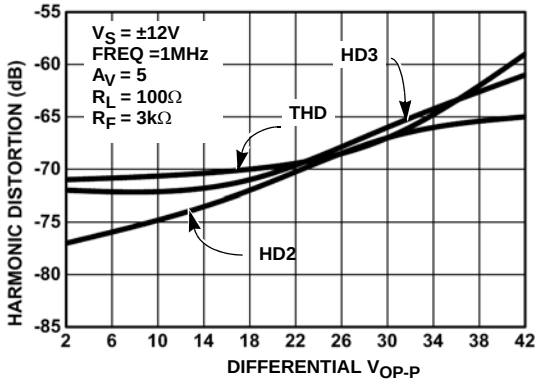



FIGURE 25. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL $I_S$)

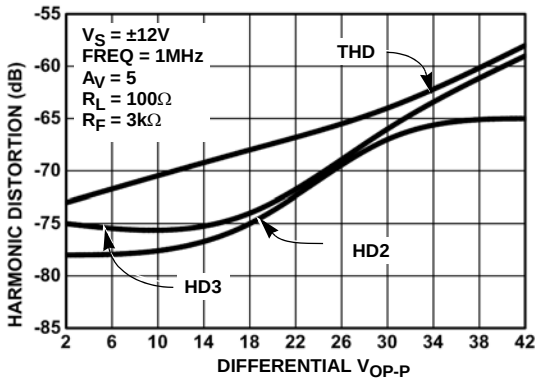



FIGURE 26. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 $I_S$)

## Typical Performance Curves (Continued)

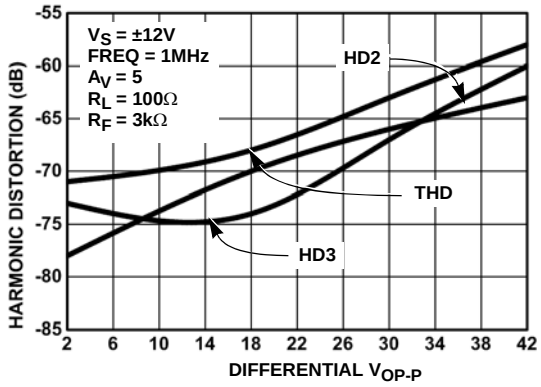



FIGURE 27. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 $I_S$)

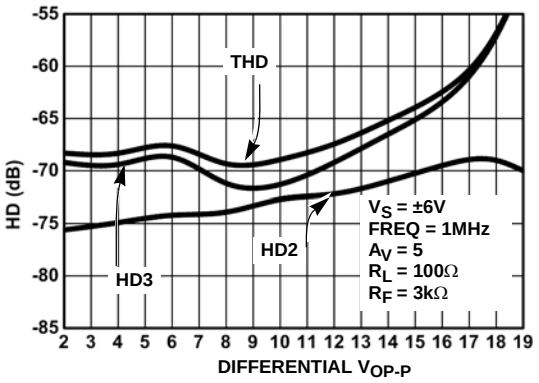



FIGURE 28. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL $I_S$)

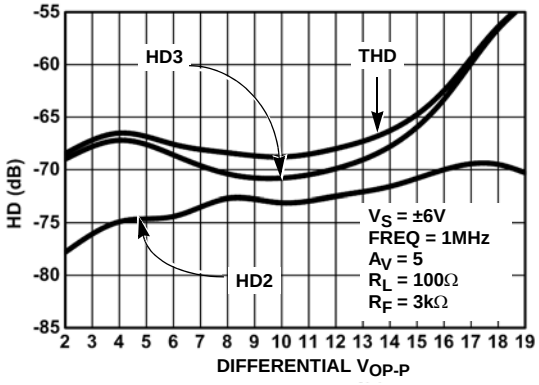



FIGURE 29. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 $I_S$)

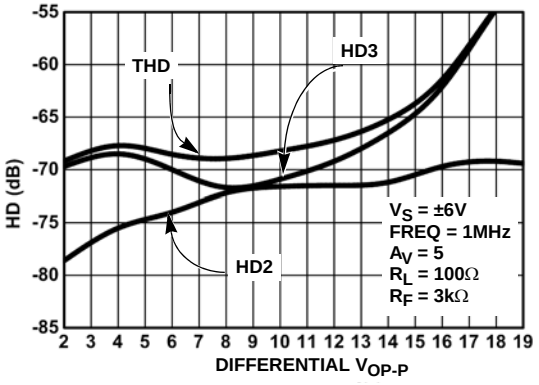



FIGURE 30. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 $I_S$)

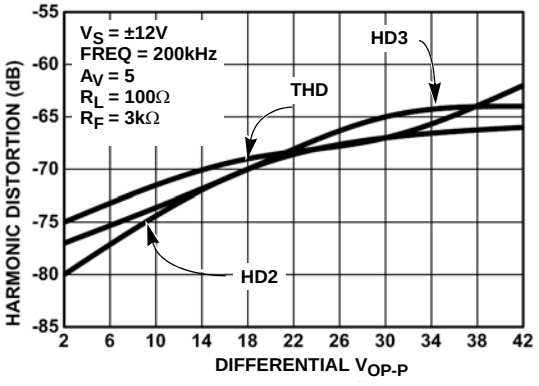



FIGURE 31. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL $I_S$)

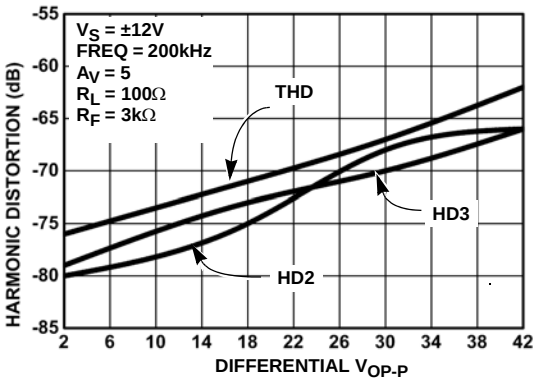



FIGURE 32. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 $I_S$)

## Typical Performance Curves (Continued)

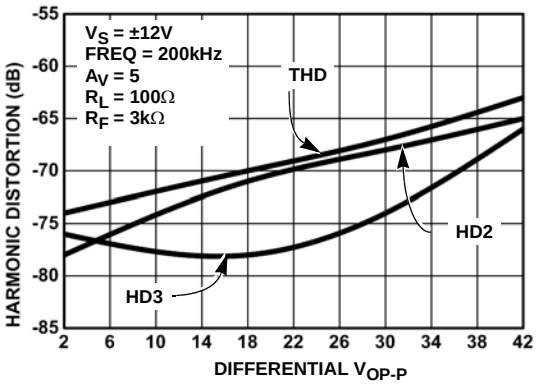



FIGURE 33. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 $I_S$)

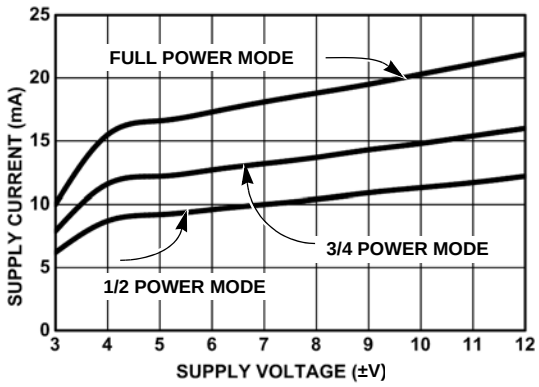



FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

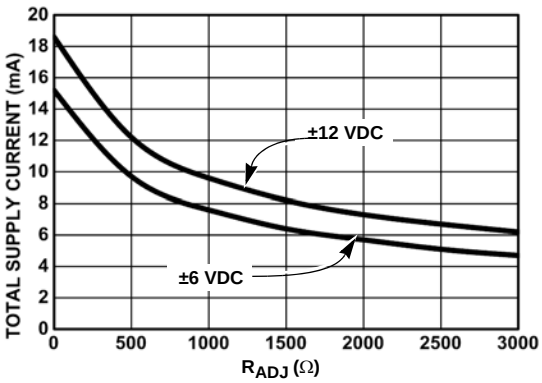



FIGURE 35. QUIESCENT SUPPLY CURRENT vs $R_{ADJ}$

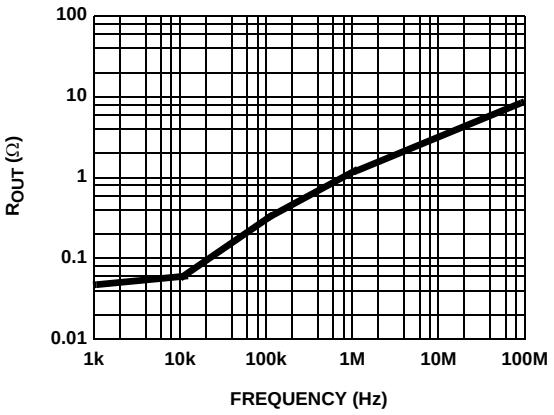



FIGURE 36. OUTPUT IMPEDANCE vs FREQUENCY

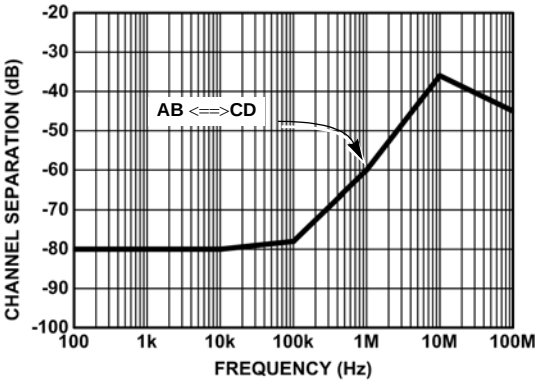



FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

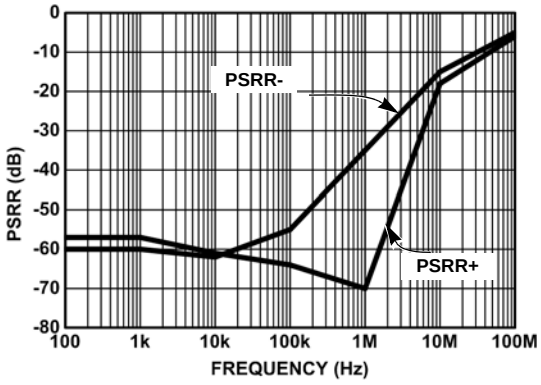



FIGURE 38. PSRR vs FREQUENCY

## Typical Performance Curves (Continued)

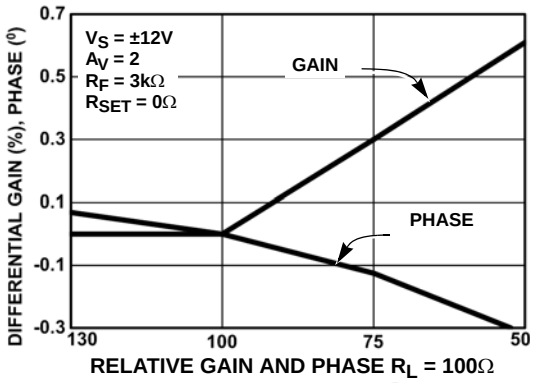



FIGURE 39. DIFFERENTIAL GAIN/PHASE (FULL $I_S$)

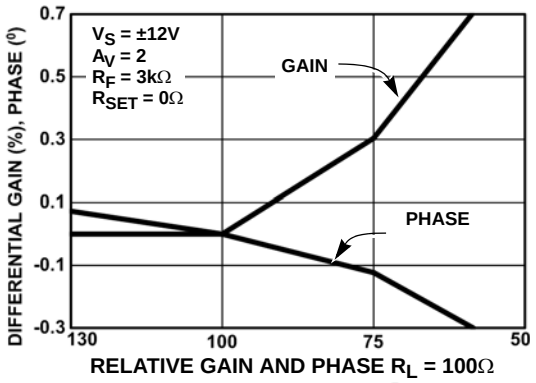



FIGURE 40. DIFFERENTIAL GAIN/PHASE (3/4 $I_S$)

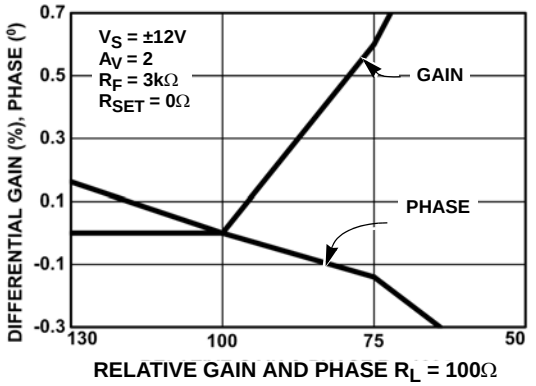



FIGURE 41. DIFFERENTIAL GAIN/PHASE (1/2 $I_S$)

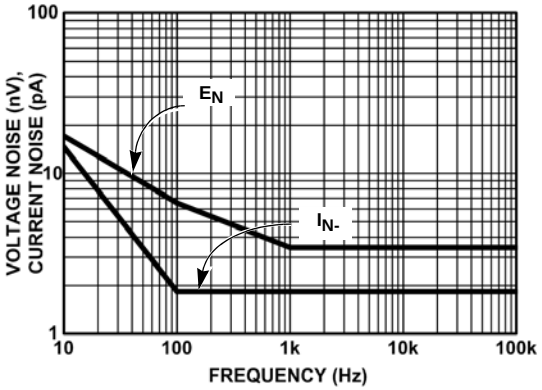



FIGURE 42. VOLTAGE AND CURRENT NOISE vs FREQUENCY

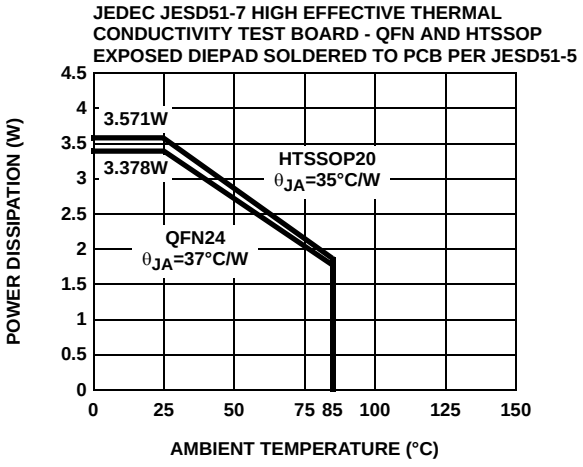



FIGURE 43. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

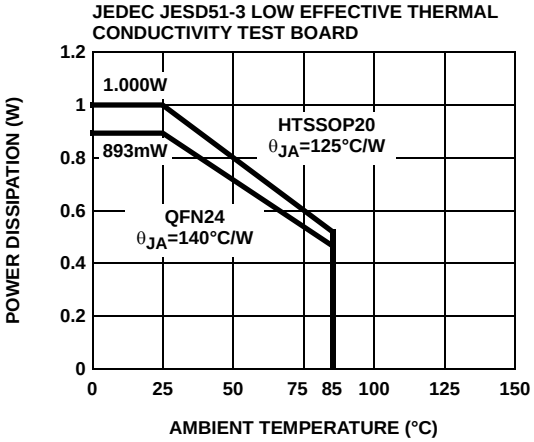



FIGURE 44. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Applications Information

The ISL1532 consists of two sets of high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 10MHz and produce low distortion levels. The ISL1532 has been optimized as a line driver for ADSL2+ CO application. The driver output stage has been sized to provide full ADSL2+ CO power level of 20dBM onto the telephone lines. Realizing that the actual peak output voltages and currents vary with the line transformer turns ratio, the ISL1532 is designed to support 450mA of output current which exceeds the level required for 1:2 transformer ratio. A typical ADSL2+ interface circuit is shown in Figure 45. Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

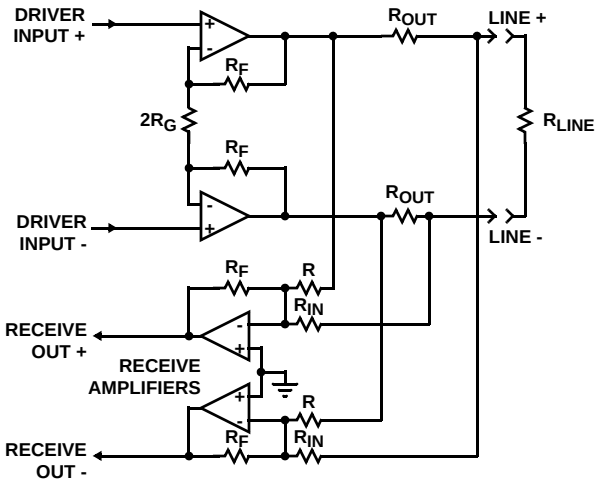



**FIGURE 45. TYPICAL LINE INTERFACE CONNECTION**

### Input Connections

The ISL1532 amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4” of unshielded wiring, or 6” of unterminated transmission line. Normal high-frequency construction obviates any such problem.

### Power Control Function

The ISL1532 contains two forms of power control operation. Two digital inputs, $C_0$ and $C_1$, can be used to control the supply current of the ISL1532 drive amplifiers. $C_0$ and $C_1$ inputs are designed to pull high initially. Floating these inputs will put the device in disable mode.

As the supply current is reduced, the ISL1532 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The four power modes of the ISL1532 are set up as shown in Table 1.

**TABLE 1. POWER MODES OF THE ISL1532**

| $C_1$ | $C_0$ | OPERATION |
|---|---|---|
| 0 | 0 | $I_S$ Full Power Mode |
| 0 | 1 | 3/4 $I_S$ Power Mode |
| 1 | 0 | 1/2 $I_S$ Power Mode |
| 1 | 1 | Power-down |

Another method for controlling the power consumption of the ISL1532 is to connect a resistor from the $I_{ADJ}$ pin to ground. When the $I_{ADJ}$ pin is grounded (the normal state), the supply current per channel is as per the Electrical Specifications table on page 3. When a resistor is inserted, the supply current is scaled according to the “$R_{SET}$ vs $I_S$” graphs in the Performance Curves section.

Both methods of power control can be used simultaneously. In this case, positive and negative supply currents (per amp) are given by the equations below:

$$I_S+ = 0.34mA + \frac{5.06mA}{1 + (R_{SET} / 1300)} \times (3/4\overline{C_1} + 1/2\overline{C_0} - \overline{C_1} \times \overline{C_0} \times 1/4) \quad \text{(EQ. 1)}$$

$$I_S- = \frac{-5.06mA}{1 + (R_{SET} / 1300)} \times (3/4\overline{C_1} + 1/2\overline{C_0} - \overline{C_1} \times \overline{C_0} \times 1/4)$$

### Power Supplies and Dissipation

Due to the high power drive capability of the ISL1532, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the ISL1532 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the ISL1532 is not constant with varying outputs. In reality, 50% of the total quiescent supply current needed to power each driver is converted in to output current. Therefore, in the equation below we should subtract the average output current, $I_O$, or 1/2 $I_Q$, whichever is the lowest. We’ll call this term $I_X$.

$$P_{Dquiescent} = V_S \times (I_S - 2I_X) \quad \text{(EQ. 2)}$$

where:

- $V_S$ is the supply voltage ($V_S$+ to $V_S$-)
- $I_S$ is the operating supply current ($I_S$+ - $I_S$-) / 2
- $I_X$ is the lesser of $I_O$ or 1/2 $I_Q$

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the ISL1532 is close to the maximum available

output swing. There is a trade off, however, with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right) \quad \text{(EQ. 3)}$$

where:

- $V_S$ is the supply voltage ($V_S$+ to $V_S$-)
- $\overline{V_O}$ is the average output voltage per channel
- $\overline{I_O}$ is the average output current per channel

The overall power dissipation ($P_{DISS}$) is obtained by summing $P_{Dquiescent}$ and $P_{Dtransistor}$.

### *Estimating Line Driver Power Dissipation in ADSL2+ CO Applications*

Figure 46 shows a typical ADSL CO line driver implementation. The average line power requirement for the ADSL2+ CO application is 20dBM (100mW) into a 100Ω line which translated to 3.16$V_{RMS}$ line voltage. The ADSL2+ DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 16.7V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:1 is selected. With 1:1 transformer ratio, the impedance across the driver side of the transformer is 100Ω, the average voltage is 3.16$V_{RMA}$ and the average current is 31.6mA. The power dissipated in the ISL1532 is a combination of the quiescent power and the output stage power when driving the line:

$$P_D = P_{quiescent} + P_{output\text{-}stage}$$

$$P_D = V_S \times (I_S - 2I_X) + (V_S - 2 \times V_{OUT\text{-}RMS}) \times I_{OUT\text{-}RMS} \quad \text{(EQ. 4)}$$

In the full power mode and with 1.5k $R_{ADJ}$ resistor, the ISL1532 consumes typically 2.7mA quiescent current per amplifier and still able to maintain very low distortion. The distortion results are shown in typical performance section of the data sheet. When driving a load, a large portion (about 50%) of the quiescent current becomes output load current. The total power dissipation per channel is:

$$P_D = 24 \times (2.7mA \times 2 \times 50\%) + 2 \times 31.6mA \times (12 - 3.16) \quad \text{(EQ. 5)}$$

where:

$P_D = 623mW$

The total power dissipation for dual channel is:

$P_{Dtotal}$

$= 2 \times P_D$

$= 1247mW$

The $\theta_{JA}$ requirement needs to be calculated. This is done using the equation:

$$\Theta_{JA} = \frac{T_{JUNCT} - T_{AMB}}{P_{DISS}} \quad \text{(EQ. 6)}$$

where:

- $T_{JUNCT}$ is the maximum die temperature (+150°C)
- $T_{AMB}$ is the maximum ambient temperature (+85°C)
- $P_{DISS}$ is the dissipation calculated above
- $\theta_{JA}$ is the junction to ambient thermal resistance for the package when mounted on the PCB

$$\Theta_{JA} = \frac{150 - 85}{1247mW} = 52°C/W \quad \text{(EQ. 7)}$$

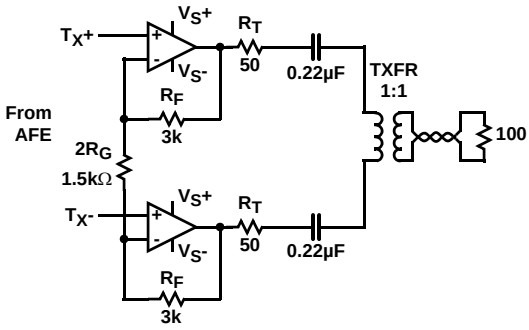
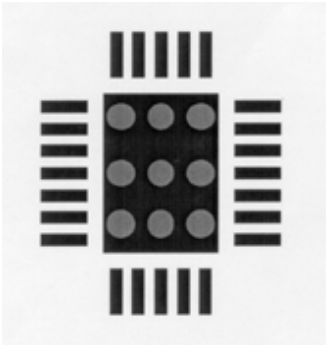



**FIGURE 46. TYPICAL ADSL CO LINE DRIVER IMPLEMENTATION**

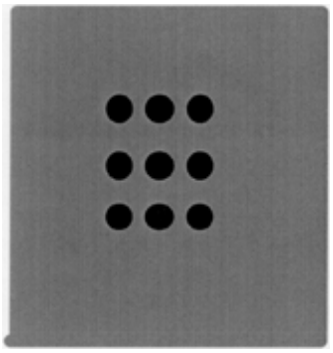
### *PCB Layout Considerations for QFN and HTSSOP Packages*

The ISL1532 die is packaged in two thermally-efficient packages: a 24 Ld QFN (leadless plastic) and 20 Ld HTSSOP packages. Both have the thermal pads underneath the package and can use PCB surface metal vias areas and internal ground planes to spread heat away from the package. The larger the PCB area, the lower the junction temperature of the device will be. In ADSL applications, multiple layer circuit boards with internal ground plane are generally used. 13 mil vias are recommended to connect the metal area under the device with the internal ground plane. Examples of the PCB layouts for the QFN and HTSSOP packages are shown in Figures 47 and 48 respectively. 37°C/W (QFN package) and +35°C/W (HTSSOP package) are obtained with the ISL1532 demoboard. The demoboard is a 4-layer board built with 2 oz. copper and has a dimension of 4 $in^2$.

A separate application note for the QFN package and layout recommendation is available. If using the QFN package, the layout and manufacturing process recommendations should be carefully reviewed.

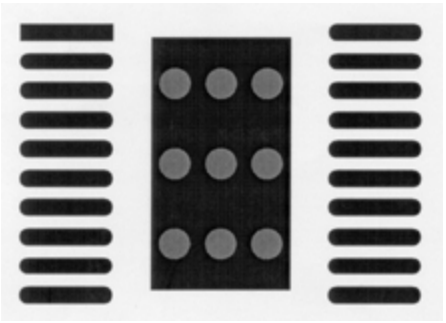


TOP METAL

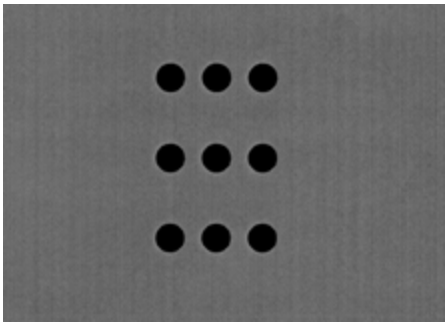


INTERNAL GROUND PLANE

FIGURE 47. PCB LAYOUT - QFN PACKAGE



TOP METAL



INTERNAL GROUND PLANE

FIGURE 48. PCB LAYOUT - HTSSOP PACKAGE

### Output Loading

While the drive amplifiers can output in excess of 500mA transiently, the internal metallization is not designed to carry more than 100mA of steady DC current and there is no current-limit mechanism. The device can safely drive RMS sinusoidal currents of 2 x 100mA, or 200mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

### Power Supplies and Component Placement

The power supplies should be well bypassed close to the ISL1532. A 2.2µF tantalum capacitor and a 0.1µF ceramic capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the ISL1532 demonstration board, and documentation can be obtained from the factory.

The parallel combination of the feedback resistor and gain setting resistor and parasitic capacitance on the inverting input node forms a pole in the feedback path. If the frequency of this pole is low, it can lead to frequency peaking. Since the ISL1532 is a current feedback amplifier, the feedback resistor value is predetermined by design. The only way to increase the frequency of this pole is to reduce the parasitic capacitance on the inverting input node. Ground plane near the inverting input should be avoided to minimize the parasitic capacitance.

### Single Supply Operation

The ISL1532 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND and the $C_0$ and $C_1$ pins are relative to GND. To calculate power dissipation, the equations in the previous section should be used, with $V_S$ equal to half the supply rail.

### Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1dB peaking) for different supply voltages and gains:

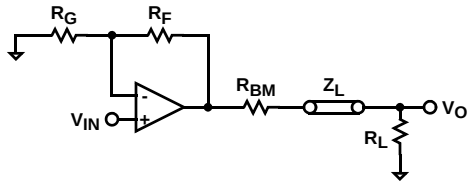
**TABLE 2. OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS AND SUPPLY VOLTAGES**

| | DRIVER VOLTAGE GAIN | |
|---|---|---|
| SUPPLY VOLTAGE | 5 | 10 |
| ±12V | 4k | 3k |

The ISL1532 features improved frequency compensation for all power modes and applications, allowing stable operation at very low power levels and eliminating any need for external "snubber" circuits. Differential circuits, such as ADSL2+ line driver applications, can be especially prone to common-mode oscillation. The ISL1532 is specifically compensated to eliminate this type of instability and allow for reliable operation even at very low power levels.

### *Cable Termination Techniques*

The traditional circuit for a line driver with passive termination is shown in Figure 49. $R_{BM}$ is the backmatch resistance added for proper termination at the source. This backmatch resistance is typically equal to the value of the cable line characteristic impedance and the load impedance. The output impedance of the amplifier is negligible in comparison with the value of the backmatch resistor it appears in series with. The gain equation reflects the output voltage across the load resistance with respect to the input voltage.




$$\frac{V_O}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{R_L}{R_{BM} + R_L}\right)$$

**FIGURE 49. TRADITIONAL CABLE TERMINATION TECHNIQUE**

While functional, this passive termination circuit has some disadvantages. The output impedance of the driver, while small, can be a noticeable quantity. The backmatch resistor is necessary to properly terminate the source end of a transmission line such as a twisted pair, but now the voltage delivered to the load is split between that backmatch resistance and the load resistance. Since there is a required voltage level at the load, the driver must now produce twice the voltage swing. The voltage swing and power dissipation increases. The power burned in the backmatch resistor is lost as heat which causes the total power dissipation to doubled. There also is quiescent power used in the op amp.

An alternative technique of cable termination using positive feedback is shown in Figure 50. With negative feedback already in place to set the gain, positive feedback can be used to adjust the output impedance. Lowering the backmatch resistor without compromising the total source termination impedance relaxes the output and supply voltage requirement for the amplifier and reduces the overall power dissipation. $R_{P1}$ and $R_{P2}$ are the only additions to the passive circuit and provide the positive feedback for the amplifier. This feedback synthesizes larger output impedance for the amplifier, allowing a reduction of the backmatch resistance. For convenience, a factor K is being introduced. It is the ratio between the backmatch resistance and the physical backmatch resistor.

$$K = \frac{R_L}{RBM} \qquad \text{(EQ. 8)}$$

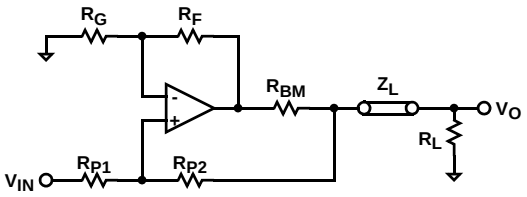



**FIGURE 50. ACTIVE TERMINATION TECHNIQUE**

The stability of the amplifier and the physical backmatch resistance tolerance typically limit K to around 4 or 5. The output impedance of the amplifier is increased by the positive feedback, allowing the backmatch resistance to decrease-keeping the total source impedance constant.

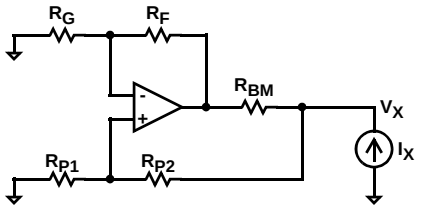



**FIGURE 51. MEASURING OUTPUT IMPEDANCE**

Figure 51 shows a standard method for measuring the output impedance of any circuit. Ohm's law applies, so a measured voltage ($V_X$) applied to a node divided by the test current gives the impedance seen at that node. Ideal op amp simplifications (input terminals are at the same voltage and there is no current flowing into the inputs) $R_{P2}$ is assumed much larger the $R_{BM}$ so the current through the positive feedback loop can be neglected. The voltage at the input terminals is given by a resistive divider of the output voltage on either side of the backmatch resistor. These feedback resistors alter the output resistance for the op amp, allowing reduction in the backmatch resistance. The derivations are as follows:

$$V+ = \frac{R_{P1}}{R_{P1} + R_{P2}} \times V_X$$

$$V- = \frac{R_G}{R_F + R_G} \times V_O$$

$$R_{SOURCE} = \frac{V_X}{I_X} = R_{BM} / \left(1 - \frac{R_{P1}}{R_{P1} + R_{P2}} \times \frac{R_F + R_G}{R_G}\right)$$

$$R_{SOURCE} = R_L = K \times RBM$$

$$K = 1 / \left[1 - \left(\frac{R_{P1}}{R_{P1} + R_{P2}}\right) \times \left(\frac{R_F + R_G}{R_G}\right)\right] \quad \text{(EQ. 9)}$$

The overall gain of the active termination circuit is:

$$\left(\frac{V_O}{V_{IN}}\right) = \frac{R_{P2} / (R_{P2} + R_{P1})}{\left(1 + \frac{1}{K}\right) / \left(\frac{R_G + R_F}{R_G}\right) - \left(\frac{R_{P1}}{R_{P2} + R_{P1}}\right)} \quad \text{(EQ. 10)}$$

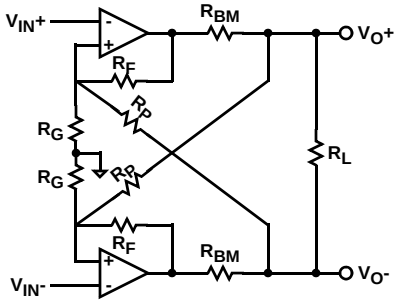



**FIGURE 52. DIFFERENTIAL LINE DRIVER USING ACTIVE TERMINATION TECHNIQUE**

In an ADSL2+ system, the POTS phone line, a twisted pair cable is used for data transmission. As shown in Figure 52, the single ended active terminate line driver is reconfigured to drive differential lines. The gain resistor is shared to allow accurate gain matching between the two amplifiers. Applying the same analysis technique as the single ended circuit, the following relationship can be derived:

$$K = 1 / \left(1 - \frac{R_F}{R_P}\right)$$

$$\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{1 + R_F / R_G + R_F / R_P}{2 \times \left(1 - \frac{R_F}{R_P}\right)} \quad \text{(EQ. 11)}$$

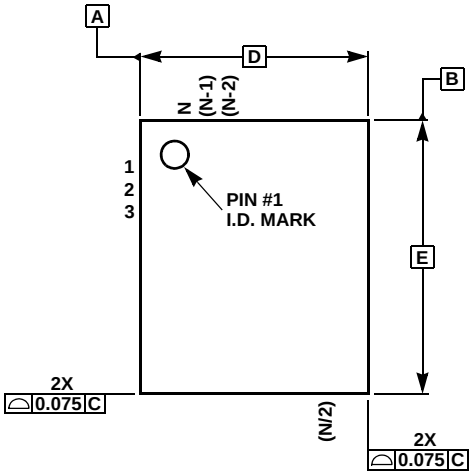
Table 3 is a quick comparison of the reduction in voltage and power requirements for the driver with passive or active termination. The key specification of a ADSL2+ CO driver are as follows: Peak output line power is 20dBM, POTS line impedance is 100Ω and the crest factor for ADSL DMT signal is 14.5dB. This specification translates to 16.76V peak-to-peak voltage on the line with 5.3 peak to average ratio PAR and 31.6mA average output current. In the passive termination case where the load and backmatch resistors are the same, the amplifier must provide 33.52V peak-to-peak at its outputs. A high voltage line driver typically needs 4V of total headroom. As a result the total supply voltage required is 37.5V. With the necessary output average current, that translates into 1.185W dissipated in addition to the quiescent power of the amplifier.

**TABLE 3.**

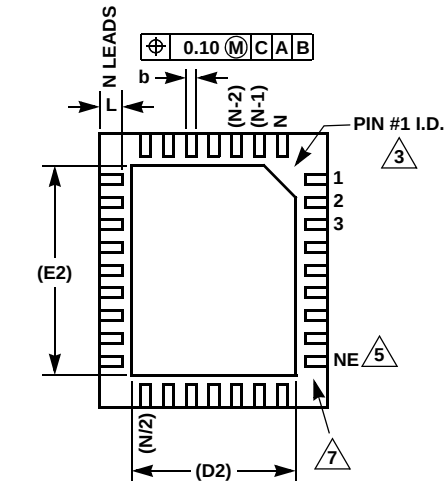
| PASSIVE TERMINATION | ACTIVE TERMINATION |
|---|---|
| $16.5V_{P-P}$ into a 100Ω line | $16.5V_{P-P}$ into a 100Ω line |
| $V_{OUT\ DRIVER} = V_{RBM} + V_{RLOAD}$ | $V_{OUT\ DRIVER} = V_{RBM} + V_{RLOAD}$ |
| $RBM = R_{LOAD}$ | $RBM = R_{LOAD}/5$ |
| $V_{RBM} = V_{RLOAD}$ | $V_{RBM} = V_{RLOAD}/5$ |
| $V_{OUT\ DRIVER} = 33.52V$ | $V_{OUT\ DRIVER} = 20.11V$ |
| $V_{SUPPLY} = 37.52$ | $V_{SUPPLY} = 24.11$ |
| $I_{OUT} = 31.6mA$ | $I_{OUT} = 31.6mA$ |
| $P_{OUT\ DRIVER} = V_{SUPPLY} * I_{OUT} = 1.185W$ (plus quiescent power) | $P_{OUT\ DRIVER} = V_{SUPPLY} * I_{OUT} = 0.714W$ (plus quiescent power) |

In the active case, a K of 5 is assumed. This reduces the backmatch resistor to 20% of its value in the passive case. The peak-to-peak output voltage provided by the driver is reduced to 20.11V which allows the use of the EL1508, a median voltage line driver. The EL1508 requires 2.5V of headroom. With 2.5V of supply voltage headroom, the power supply required becomes 22.61. With the same output current drive, the power dissipation is reduced by 39.7% to 0.714W. While it is true that additional power is dissipated in the feedback networks, the feedback resistors are typically much larger than the backmatch resistor and their losses are negligible.

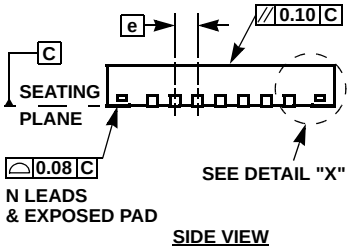
## QFN (Quad Flat No-Lead) Package Family



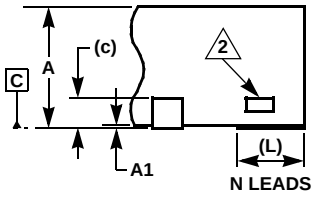

TOP VIEW




BOTTOM VIEW




SIDE VIEW




DETAIL X

## MDP0046

**QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)**

| SYMBOL | QFN44 | QFN38 | QFN32 | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|
| A | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/-0.02 | - |
| b | 0.25 | 0.25 | 0.23 | 0.22 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 7.00 | 5.00 | 8.00 | 5.00 | Basic | - |
| D2 | 5.10 | 3.80 | 5.80 | 3.60/2.48 | Reference | 8 |
| E | 7.00 | 7.00 | 8.00 | 6.00 | Basic | - |
| E2 | 5.10 | 5.80 | 5.80 | 4.60/3.40 | Reference | 8 |
| e | 0.50 | 0.50 | 0.80 | 0.50 | Basic | - |
| L | 0.55 | 0.40 | 0.53 | 0.50 | ±0.05 | - |
| N | 44 | 38 | 32 | 32 | Reference | 4 |
| ND | 11 | 7 | 8 | 7 | Reference | 6 |
| NE | 11 | 12 | 8 | 9 | Reference | 5 |

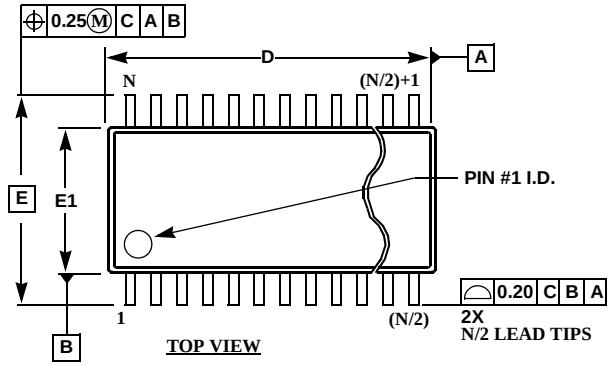
| SYMBOL | QFN28 | QFN24 | QFN20 | | QFN16 | TOLER-ANCE | NOTES |
|---|---|---|---|---|---|---|---|
| A | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/ -0.02 | - |
| b | 0.25 | 0.25 | 0.30 | 0.25 | 0.33 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 4.00 | 4.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| D2 | 2.65 | 2.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| E | 5.00 | 5.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| E2 | 3.65 | 3.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| e | 0.50 | 0.50 | 0.65 | 0.50 | 0.65 | Basic | - |
| L | 0.40 | 0.40 | 0.40 | 0.40 | 0.60 | ±0.05 | - |
| N | 28 | 24 | 20 | 20 | 16 | Reference | 4 |
| ND | 6 | 5 | 5 | 5 | 4 | Reference | 6 |
| NE | 8 | 7 | 5 | 5 | 4 | Reference | 5 |

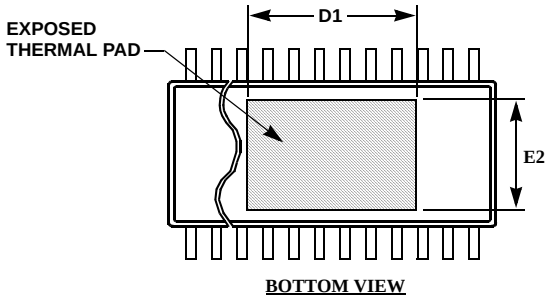
Rev 10 12/04

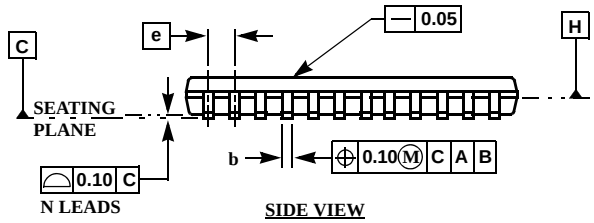
NOTES:

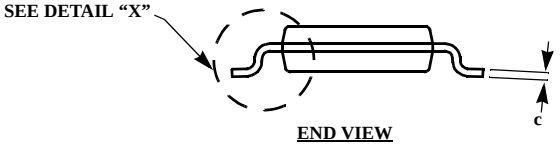
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

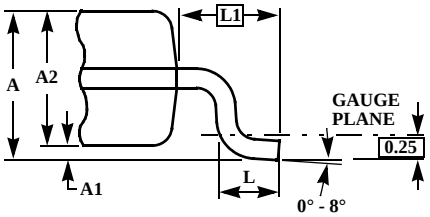
## HTSSOP (Heat-Sink TSSOP) Family




### MDP0048

**HTSSOP (Heat-Sink TSSOP) Family**

| SYMBOL | 14 LD | 20 LD | 24 LD | 28 LD | 38 LD | TOLERANCE |
|---|---|---|---|---|---|---|
| A | 1.20 | 1.20 | 1.20 | 1.20 | 1.20 | Max |
| A1 | 0.075 | 0.075 | 0.075 | 0.075 | 0.075 | ±0.075 |
| A2 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | +0.15/-0.10 |
| b | 0.25 | 0.25 | 0.25 | 0.25 | 0.22 | +0.05/-0.06 |
| c | 0.15 | 0.15 | 0.15 | 0.15 | 0.15 | +0.05/-0.06 |
| D | 5.00 | 6.50 | 7.80 | 9.70 | 9.70 | ±0.10 |
| D1 | 3.2 | 4.2 | 4.3 | 5.0 | 7.25 | Reference |
| E | 6.40 | 6.40 | 6.40 | 6.40 | 6.40 | Basic |
| E1 | 4.40 | 4.40 | 4.40 | 4.40 | 4.40 | ±0.10 |
| E2 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | Reference |
| e | 0.65 | 0.65 | 0.65 | 0.65 | 0.50 | Basic |
| L | 0.60 | 0.60 | 0.60 | 0.60 | 0.60 | ±0.15 |
| L1 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | Reference |
| N | 14 | 20 | 24 | 28 | 38 | Reference |

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NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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