ISE Design Suite 13: Release Notes Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Updated for the 13.1 Release. The Chapters “Download and Installation” and “Obtaining and Managing a License” have been moved to a new document titled **ISE Design Suite 13: Installation and Licensing Guide** (iil.pdf)

About This Guide

This guide contains release information for ISE® Design Suite 13, which includes the Integrated Software Environment (ISE) software, ChipScope™ Pro software, Embedded Tools (including Embedded Development Kit (EDK) and standalone Software Development Kit (SDK), System Generator for DSP software, and PlanAhead™ design tools. It also describes how to use Xilinx® online documentation.

Information on what is new, known issues, and technical support for ISE Design Suite 13 software is also included.

Information on how to download, install, and obtain a license for ISE Design Suite 13 can be found in the document titled ISE Design Suite 13: Installation and Licensing Guide (iil.pdf)

Guide Contents

This manual contains the following chapters:

- Chapter 1, What's New for Release 13.1
- Chapter 2, Important ISE Design Suite 13 Release Information
- Chapter 3, Architecture Support and Requirements
- Chapter 4, Technical Support, Services, and Documentation
- Chapter 5, Additional Resources

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Chapter 1

What's New for Release 13.1

This Chapter describes the new features in the Xilinx® ISE® Design Suite 13 software release. It contains the following sections.

- ISE Design Suite Highlights
- New Device Support
- What's New in Logic Edition
  - Project Navigator
  - PlanAhead
  - FPGA Editor
  - iMPACT
  - ChipScope Pro
  - ISE Simulator
- What's New in Embedded Edition
  - EDK Overall Enhancements
  - XPS Enhancements
  - SDK Enhancements
  - Project Navigator/EDK Integration Enhancements
  - MicroBlaze Soft Processor
  - Embedded IP
- What's New in DSP Edition
  - System Generator for DSP
- What's New in CORE Generator and IP
  - New IP Cores
  - Additional IP supporting AXI4 Interfaces
  - CORE Generator Enhancements
  - PlanAhead IP Design Flow Enhancements

What's New in HTML Format

You can find the identical What's New documentation online in HTML format at:

www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/whatsnew.htm

For links to this and other documentation you use in the Windows environment. Select **Start > All Programs > Xilinx ISE Design Suite 13.1 > Documentation > InfoCenter**.

What's New in Xilinx ISE Design Suite 13.1

ISE Design Suite Highlights

- Team Design
- Up to 100 times Simulation Acceleration via ISim HW Co-simulation
- AXI4 tool and IP support is now "Production" status
- Plug-and-Play IP Initiative
  - CORE Generator™ 2.0 introduction
  - IEEE P1735 Version 1 decryption interoperability
- Windows 7 Professional support

New Device Support

Xilinx introduces the following device support for the 13.1 release:

- Kintex™-7
- Virtex®-7 (Including 7VX485T)

What's New in Logic Edition

The following describes what's new in Logic Design Tools in ISE 13.1.

Project Navigator

- Embedded Development Kit (EDK) Integration Improvements
  - Support for multiple ELF files and automatic detection of ELF files referenced by EDK designs
  - Ability to control associations between ELF files and specific processors defined in XMP files
  - Ability to select an Evaluation Development Board in the New Project Wizard, New Project dialog box, or Design Properties dialog box
  - Ability to export hardware design before running implementation
  - Ability to automatically launch the Software Development Kit (SDK) when exporting a design
- Compare Projects feature includes additional categories and layout improvements
- SmartXplorer now features support for power-dedicated and custom strategies
- CORE Generator™ has the ability to update a core to the latest version as well as the ability to check all core versions

- Ability to create a new System Generator source in Project Navigator
- Ability to create a new System Generator source in Project Navigator
- Support for viewing TWR reports in Timing Analyzer

PlanAhead

ISE Simulator Integration

PlanAhead release 13 has integrated the Xilinx® ISE Simulator (ISim), into the design flow. This new integration enables development and verification of designs completely within the PlanAhead user interface. PlanAhead now has support for simulation-only sources added to the project, which is performed either in the new project wizard or in the add sources dialog. The Flow Navigator provides access to ISE Simulator.

You can invoke ISim:

- After RTL Design for behavioral simulation
- After Implementation for timing simulation

Hierarchical Design Methodology Support

PlanAhead release 13 supports the Hierarchical Design features as described in the following subsections.

- Incremental XST flow in RTL projects
- Importing a partition into a different hierarchy than the one in which the partition was created in the ISE Simulator
- AREA_GROUPS within partitions
- Black Box support in Synthesis and Implementation
- Boundary optimization for constants and unconnected inputs and outputs on partition ports.
- Defining partitions for Design Preservation in Netlist-based projects.

Team Based Design Support

PlanAhead 13 adds support for new team-based design methodology. Team based design supports multiple engineers implementing at a module level within a design to work in parallel. The flow then supports assembling the module level runs by a team leader at the top level with support for preservation levels to control the placement and routing information that is kept during import.

See the *Hierarchical Design Methodology Guide* (UG748) and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide* (UG632) for more information.

Design Preservation RTL Support

PlanAhead 13 enhances support for design preservation flows by adding incremental compilation for RTL synthesis of partitions with XST. The design preservation flow allows a designer to mark portions of a design to be preserved in subsequent iterations and enabled incremental compilation. In prior releases, design preservation was only supported post synthesis. RTL-level control was added to provide designers an easier to use flow to control partitions throughout the design flow from synthesis through implementation within the PlanAhead user interface.

See the *Hierarchical Design Methodology Guide* (UG748) and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide* (UG632) for more information.

Partial Reconfiguration Support

PlanAhead provides an interface to Partial Reconfiguration with appropriate licensing.

See the *Partial Reconfiguration User Guide* (UG702), for more information.

Project Navigator Project File (.xise) Support

The New Project wizard lets you specify an ISE project file without requiring the specification of all project sources. PlanAhead parses the XISE project file, and adds RTL and simulation sources, including CORE Generator cores and Block Memory Model (BMM) files. PlanAhead can now also determine relevant run options for Synthesis and Implementation tools, and configure the default run to match based on settings in the XISE project file.

New and Modified Project Management Features

The following subsections describe the new and modified features in PlanAhead 13 projects. In PlanAhead 13, you can:

- Import sources from Project Navigator
- Automatically or manually order source files for proper compilation by XST
- automatically discover the top-module name
- better support for `include statements inside HDL
- support for XST Synthesis XCF constraint files
- Identification of unused source files
- Ability to launch Runs without copying sources to the Run directory
- Ability to archive a project
- Ability to customize the Text Editor font

Graphical User Interface Enhancements

The PlanAhead software for release 13 has further enhanced the "layered complexity" of the Graphical User Interface (GUI) to provide an intuitive environment for both new and advanced users.

The left-side panel of the interface is a "Flow Navigator," exposes a push-button flow from Project Management, through RTL Design, Netlist Design, Implemented Design, to Device Programming and Debugging. The new integration with ISim provides timing and behavioral simulation, which are exposed where appropriate for use in the Flow Navigator menu options. A new information window as well as an enhanced Tcl Console and Messaging window is available.

Other Enhancements

- GUI Enhancement Details
- RTL Design Additions and Modifications
- Additional ChipScope Features
- Pin Planning Changes
- New and Modified Design Rule Checks
- Implementation Enhancements
- New 13.1 PlanAhead Video Tutorial

Please see the PlanAhead section in Chapter 2, "Important ISE Design Suite 13 Release Information," for details of what's new in the following areas:

FPGA Editor

- New Lock Layers toolbar button, which locks the current layer visibility settings for all zoom levels.

iMPACT

- New SPI/BPI programming support:
  - Numonyx P30 bottom boot is supported, in addition to top boot.
  - Winbond W25Q is supported up to 128Mb.
  - Winbond W25Q support for the CV revision has been added.

ChipScope Pro

- ChipScope Pro HDL (VHDL and Verilog) Debug probe using PlanAhead and XST Synthesis flow
  - Enable users to mark debug nets on HDL or XCF constraint file
  - When MARK_DEBUG attribute is used:
    - Nets are preserved (not optimized away)
    - Nets appear in the ChipScope view in the PlanAhead view so users can assign to debug cores
- ChipScope Pro HDL Debug probe using PlanAhead and Synplify Synthesis flow
  - Enable users to mark debug nets on HDL (VHDL and Verilog) or SDC
  - When MARK_DEBUG attribute is used:
    - Nets are preserved (not optimized away)
    - Nets appear in the ChipScope view in the PlanAhead view so users can assign to debug cores
- BERT for Virtex®-6 GTX and GTH available in PlanAhead and ChipScope Flow
  - Also added low- and mid-range line rate support for IBERT V6 GTH
- Startup Trigger Mode
  - Using Project Navigator, Core Inserter, and Analyzer Tools
  - Using PlanAhead and Analyzer Tools
- BERT sweep test plot GUI
  - Built-in graphical viewer of IBERT sweep test results for Virtex®-6 GTX/GTH FPGA transceivers
  - Standalone graphical viewer for offline analysis of IBERT sweep test results for Virtex®-6 FPGA GTX/GTH, Spartan®-6 FPGA GTP, and Virtex®-5 FPGA GTX transceivers
- Tutorials:
  - PlanAhead Tutorial: Debugging with ChipScope Analysis
  - ChipScope IBERT: Basic IBERT design flow

ISE Simulator

- Supports simulation of AXI BFM
- Relaunch of simulation from the ISim GUI

What's New in Embedded Edition

The following describes what's new in Embedded Tools and IP in ISE Design Suite 13.1.

EDK Overall Enhancements

- Consistent SDK workspace selection behavior across Project Navigator, Xilinx Platform Studio (XPS), and SDK.
- TDP device-based licensing support.

XPS Enhancements

- Changes to Base System Builder
  - AXI systems are now the default in Base System Builder for Spartan®-6, Virtex®-6, and 7 Series designs. Base System Builder only supports AXI systems for 7 Series designs.
  - New shared bus interconnect used for low frequency peripheral bus, reduces design size.
- Changes to System Assembly View (SAV)
  - New DRC feature allows you to run design rule checks at any time.
  - When AXI IP is added in SAV, the following functions are automatically completed: bus, clock, and reset connections, and address generation
  - When adding an AXI MicroBlaze processor instance, the following functions are automatically completed: interconnect, DRAM memory and cache connections, debug connections, clocks, and LMB BRAM
  - You can now modify the order of IP listed in the SAV
  - For multi-processor systems, you can filter on processor system instance in the SAV
- Other XPS Changes
  - All software development tools have been removed from XPS
  - Software projects have been removed from XPS
  - The main toolbar has been streamlined and now contains fewer buttons.
  - Create and Import IP (CIP) wizard now supports creation of AXI4 and AXI4-Lite slave peripherals
  - AXI BFMs project generation now included in CIP wizard. **Note**: A license for AXI BFMs must be purchased separately.
  - ELF files can now be assigned for implementation or simulation and remain synchronized with Project Navigator.
  - Debug Wizard supports inclusion of AXI monitors and hardware/software co-debug of AXI-based designs.
  - When the XPS design is a submodule in a Project Navigator project, simulation is only available in Project Navigator.

- When you export your design to SDK, the SDK workspace is no longer set automatically.

SDK Enhancements

- Updated to Eclipse 3.6 and CDT 7.0 Helios release.
  - Updated functionality and improved stability while retaining the familiar user interface
  - Capture console log to files.
- Cygwin no longer required or shipped
  - GNU Tool Chain for MicroBlaze and PowerPC built natively without Cygwin
  - GnuWin32 utilities provided for common UNIX/Linux functions
- Usability Updates
  - ELF-only debugging
  - Launch management
  - Flow checking, including BSP deletions and hardware change detection.
  - User assistance, including hints, context sensitive help and preference settings.
  - Software repository information saved to minimize setup when using revision control.
  - Automation for Flash read-only region behaviors.
- 7 Series initial support in XMD
- TDP device-based licensing support

Project Navigator/EDK Integration Enhancements

- Recognition of multiple processor instances in .xmp.
  - Previous versions assumed a single processor
  - Ability to control associations between ELF files and specific processors defined in XMP files.
- Separate .elf sources for implementation and simulation.
  - elf files now assigned per processor instance.
  - Automatic detection of ELF files referenced by EDK designs.
- New "Export Hardware Design to SDK without Bitstream" process allows you the ability to export hardware design before running implementation.
- Ability to automatically launch the Software Development Kit (SDK) after design export (optional).
  - SDK workspace handling consistent with XPS and standalone SDK.
- Ability to select an Evaluation Development Board in Project Navigator's New Project Wizard, New Project dialog box, or Design Properties dialog box.

MicroBlaze Soft Processor

- New version V8.10.a
- Support for 7 Series Kintex and Virtex devices
- AXI now the default interface for 7 Series designs
- MicroBlaze Configuration wizard support Fault Tolerant features
- Added Error Correction Code (ECC) to LMB BRAM memory connected to MicroBlaze
- Added parity protection on MicroBlaze cache and MMU memory
- New instructions added
  - Count Leading Zeros (CLZ)
  - Memory Barrier (MBAR)
- Stack overflow and underflow detection
- New parameter allows AXI4-Stream / FSL instructions in user mode

Embedded IP

- New Embedded IP
  - AXI 7-Series DDRx
  - AXI External Peripheral Controller
  - AXI to AHBLite Bridge
  - AXI Master Lite IP Interface (IPIF)
- Embedded IP now available in CORE Generator
  - CORE Generator AXI VDMA

What's New in DSP Edition

The following describes what's new in System Generator for DSP and DSP IP in ISE 13.1.

System Generator for DSP

- Support for MATLAB/Simulink 2011a.
- All System Generator blocks now support Kintex-7 and Virtex-7 devices.
- New blocks
  - 7 Series DSP48E1, Complex Multiply 5.0, DSP48 Macro 2.1, FIR Compiler 6.2, VDMA Interface 3.0.
- System Generator support for AXI PCore and HW Co-simulation.
- New context menus speed adding and connecting blocks (Beta). For details on this feature, see Chapter 5 of the System Generator for DSP Reference Guide.
- Choice to have tools automatic create a Hardware Interface Document. For more details on this feature, see the System Generator token topic in the System Generator for DSP Reference Guide.
- System Generator IP
  - Floating-point Operator, CORDIC, Divider Generator, CIC Compiler, DSP48 Macro, Multiply-Add, and Multiply-Accumulate.

What's New in CORE Generator and IP

The following describes what's new in CORE Generator™ software and IP cores:

Introducing CORE Generator IP with Virtex®-7 and Kintex™-7 support

New IP Cores

- Audio, Video and Image Processing IP
  - Object Segmentation v1.0 (AXI4-Lite)
    - Used in conjunction with the Image Characterization LogiCORE IP to convert statistical data provided into a list of objects that meet a user-defined set of object characteristics.
  - AXI Video Direct Memory Access v1.0 (AXI4, AXI4-Stream, AXI4-Lite)
    - Provides a flexible interface for controlling and synchronizing video frame stores from external memory. Multiple VDMAs from different clock domains can be linked together to control frame store reads and writes from multiple sources.
- Communication DSP Building Blocks
  - Linear Algebra Toolkit v1.0 (AXI4-Stream)
    - Implements basic Matrix operations - Matrix-Matrix Addition, Subtraction, Matrix-Scalar Multiplication and Matrix-Matrix Multiplication.
    - This IP provides flexible and optimized building blocks for developing complex composite functions for various signal and data processing applications.
- FPGA Features and Support
  - 7 Series FPGA Transceivers Wizard v1.3
    - Configures one or more Virtex-7 and Kintex-7 FPGA GTX transceivers either from scratch, or using industry standard templates, using a custom Verilog or VHDL wrapper.
    - Also provides an example design, testbench, and scripts to allow you to observe the transceivers operating in simulation and in hardware.
  - XADC Wizard v1.2
    - The XADC Wizard generates an HDL wrapper to configure a single 7 Series FPGA XADC primitive for user-specified channels and alarms.
- Standard Bus Interfaces and I/O
  - 7-Series Integrated Block for PCI Express (PCIe) v1.0 (AXI4-Stream)
    - Implements 1-lane, 2-lane, 4-lane, or 8-lane configurations. The IP uses the 7 Series Integrated Hard IP Block for PCI Express in conjunction with flexible architectural features to implement a PCI Express Base Specification v2.1 compliant PCI Express Endpoint or Root Port.
    - Unique features of the LogiCORE IP for PCI Express are the high performance AXI Interface, optimal buffering for high bandwidth applications, and BAR checking and filtering.
- Wireless IP
  - Triple Rate SDI v1.0 (AXI4-Stream)
    - Provides receiver and transmitter interfaces for the SMPTE SD-SDI, HD-SDI, and 3G-SDI standards.

  - The Triple-Rate SDI receiver and transmitter are provided as unencrypted source code in both Verilog and VHDL, allowing you to fully customize these interfaces as required by your specific applications.
- 3GPP LTE PUCCH Receiver v1.0 (AXI4-Stream)
  - Provides designers with an LTE Physical Uplink Control Channel Receiver block for the 3GPP TS 36.211 v9.0.0 Physical Channels and Modulation (Release 9) specification.
  - Support for channel estimation, demodulation and decoding.

Additional IP supporting AXI4 Interfaces

- The latest versions of CORE Generator IP have been updated with Production AXI4 interface support. For more detailed support information see www.xilinx.com/ipcenter/axi4_ip.htm.
- In general, the AXI4 interface will be supported by the latest version of an IP, for Virtex®-7, Kintex™-7, Virtex®-6 and Spartan®-6 device families. Older "Production" versions of IP will continue to support the legacy interface for the respective core on Virtex®-6, Spartan®-6, Virtex®-5, Virtex®-4 and Spartan®-3 device families only.
- For general information on Xilinx AXI4 support see www.xilinx.com/ipcenter/axi4.htm.
- A comprehensive listing of cores that have been updated in this release can be viewed at www.xilinx.com/ipcenter/coregen/updates_13_1.htm.

CORE Generator Enhancements

- Introducing support for IP-XACT based IP repositories for Xilinx and Alliance Program Member IP. (Requires no changes to existing CORE Generator, PlanAhead and Project Navigator user flows.)
- Addition of "Manage IP" pull-down menu to provide repository and IP management features.
- Display of AXI4 support by each IP in the IP catalog has been expanded to display the various AXI4 interfaces in separate sortable columns: AXI4, AXI4-Stream and AXI4-Lite
- Individual ports in IP symbols can now be grouped into AXI4 channels for simplified symbol views.

PlanAhead IP Design Flow Enhancements

- Introducing support for IP-XACT based IP repositories for Xilinx and Alliance Program Member IP (Requires no changes to the existing PlanAhead IP flow).
- Display of AXI4 support by each IP in the IP catalog has been expanded to display the various AXI4 interfaces in separate sortable columns: AXI4, AXI4-Stream, and AXI4-Lite.
- Support added for Automatic IP Upgrade flow.

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Chapter 2

Important ISE Design Suite 13 Release Information

Important 13.1 Release Information

- Pinouts on Kintex-7 and Virtex-7 devices are subject to change because package files are not yet finalized for these families. Pinout changes may require design re-implementation in a future Xilinx software release.
- Default IO standards for Kintex-7 and Virtex-7 devices will change in a future Xilinx software release.
- Changes will be made to XC7V1500T and XC7V2000T device models in a future Xilinx software release. 13.1 implementation design files (.NCD) targeting these devices will be invalidated at that time, and designs will need to be re-implemented.
- Changes will be made to the Kintex-7 and Virtex-7 GTX component models in a future Xilinx software release. This change will require that the 7 Series FPGA Transceivers Wizard be rerun for each instance.
- IBIS and HSPICE models are not yet available for Kintex-7 and Virtex-7 devices.

Known Issues

Known issues with **ISE Design Suite** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39243.htm

Known issues with **PlanAhead** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/40512.htm

Known issues with **EDK** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39843.htm

Known issues with **System Generator for DSP** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/29595.htm

Details of 13.1 Software and IP Changes

PlanAhead

GUI Enhancement Details: Main Menu Enhancements

- Workspace Views

The PlanAhead workspace views are redesigned with an auto-fit selection. A drop-down in the Main toolbar lets you select applicable views for the open Project. The workspace views now contain dock/undock, float, minimize/maximize, and restore buttons.

- Search Option

  PlanAhead has added a search text box on the main menu to search through all the menu options for the specified text.

- Export Options

  A new option in the PlanAhead **File >Export > Export IBIS Model** is available in an open design. The Input/Output Buffer Information Specification (IBIS) is used analyze the design. The IBIS model exported from PlanAhead is compliant with the IBIS version 4.2, and uses the defaults of that specification.

- Single Click Implementation

  PlanAhead now allows you to click on the Implementation button in the flow navigator and the tool will launch a dialog prompting if you want to launch synthesis first if you have an RTL project, and the synthesis run is out of date. This allows you to do "one-click" implementation of RTL. This feature requires that you have PlanAhead in GUI mode – if you close the project, only the currently running Synthesis run completes: the Implementation run does not launch.

- Source View Enhancements

  The PlanAhead release 13 provides enhanced views for source file structures and editing.

- Third Party Text Editor Support

  PlanAhead now allows the ability to use third-party editors for editing source code files.

- Message Manager

  A new Messages view consolidates error, critical warning, warning, and informational messages from PlanAhead and ISE point tools into a single view. Messages are linked to the source code to allow for quick exploration and resolution of any errors or warnings.

- Netlist View Additions and Modifications

  The following subsections describe the additions and modifications to the PlanAhead Netlist view.

- Clocking Resource View

  The new Clocking Resource view available in the PlanAhead GUI aids in the visualization and assignment of clocking-related sites and physical resources within the FPGA.

- Folders for Component Switching Limits

  There are new folders in the timing results view imported from TRCE that better organize the component pin switching limit violations with setup and hold violations. The violations are sorted and the worst violation is displayed first within a constraint.

- Enhanced Slack Histogram Report

  PlanAhead release 13 contains an improved slack histogram feature which creates a graphical bar chart corresponding to collections of paths within ranges from most negative to most positive.

- Device View Enhancements

  PlanAhead Release 13 contains the following enhancements.

- Device Resource Details

  The device view in PlanAhead has been enhanced to provide more detail for device resources such as pins on slices and BEL-level pins for Virtex®-6 and Virtex-7 devices, and the Timing Path provides annotation on pins upon full placement.

- Multiple Instance Drag and Drop

  PlanAhead now allows moving multiple instances in the device view at the same time. This allows users to move instances that are already placed in a group and all location constraints are translated together.

- Schematic View Enhancements

  PlanAhead supports tracing logic between two selected objects in the schematic view. Any two objects may be selected, and PlanAhead will trace and draw any intermediate logic connections between them within a schematic.

- XPA Integration

  PlanAhead Release 13 has added the ability to launch Xilinx Power Analyzer (XPA) to analyze power on implemented designs. To launch XPA click on the XPower Analyzer icon after opening an implemented design.

RTL Design Additions and Modifications

- Text Editor Options

  PlanAhead release 13 allows for customization of fonts for comments, and keywords, supports integration of third party text editors, and allows for easier use of Xilinx Language Templates. See *PlanAhead User Guide* (UG632), Chapter 5, RTL Design.

- IP Catalog

  The PlanAhead release 13 enhancements in the IP Catalog are:

  - The CORE Generator™ IP catalog now supports migration of older superseded cores to the currently supported version.
  - PlanAhead now supports canceling IP generation tasks that block other operations in the GUI.

- Source File Exploration

  PlanAhead can determine the top-module in an RTL design automatically, or give you the ability to define it manually.

  You can automatically or manually reorder source files for compilation and synthesis, and automatically or manually enable or disable RTL source files as required by the top-level module.

- Power Estimation Enhancements

  PlanAhead release 13 has Power Estimation available on Virtex-5, Virtex-6, and Spartan-6 device families.

- Partitions Control

  PlanAhead release 13 provides control of partitions at the RTL level in synthesis with XST.

Pin Planning Changes

The following subsections describe the PlanAhead 13 changes to the Pin Planning features.

- Package View Legend and Spreadsheet Manipulation

  A new legend to the Device and Package view allows you to view or hide specific layers and objects, and provides a legend for layer colors and pin shapes.

  The spreadsheet-like Package Pins view can be edited, sorted, flattened, and filtered for better visibility on multifunction pins.

- Alternate Part Definition

  PlanAhead release 13 has the ability to define alternative parts to a design (for Virtex-5, Virtex-6, and Spartan-6 devices only). Some restrictions apply to Spartan-6 LX25 and LX25T devices, which is detailed in Answer Record: AR34885.

- New Pin Assignment and Banking Rules

  The new pin assignment and banking rules are documented in "Appendix B, DRCs," of the *PlanAhead User Guide* (UG632), and include VCCaux reporting for Virtex-6 and newer devices.

- Write IOSTANDARDs to Exported UCF

  PlanAhead now has the option to write out all IOSTANDARD constraints to an exported UCF file with the File > Export > Export I/O Ports command.

Netlist View Additions and Modifications

The following subsections describe other additions and modifications to the PlanAhead Netlist view.

- Folders for Component Switching Limits

  There are new folders in the timing results view imported from TRCE that better organize the component pin switching limit violations with setup and hold violations. The worst violation is sorted and displayed first within a constraint.

- Enhanced Slack Histogram Report

  PlanAhead release 13 contains an improved slack histogram feature which creates a graphical bar chart corresponding to collections of paths within ranges from most negative to most positive.

Device View Enhancements

PlanAhead Release 13 contains the following enhancements.

- Device Resource Details

  The device view in PlanAhead has been enhanced to provide more detail for device resources such as pins on slices and BEL-level pins for Virtex®-6/7 devices, and the Timing Path provides annotation on pins upon full placement.

- Multiple Instance Drag and Drop

  PlanAhead now allows moving multiple instances in the device view at the same time.

- Schematic View Enhancements

  PlanAhead supports tracing logic between two selected objects in the schematic view.

New and Modified Design Rule Checks

The following is a list of new and modified Design Rule Check (DRCs) in PlanAhead 13:

- Attribute DRCs
  - AVAL - Checks for invalid attribute values.
  - ADEF - Checks for undefined attribute values.
- Bank DCI Cascade DRC
  - DCICIOSTD - Checks that the DCI Cascade constraint is legal.
- Bank I/O Standard DRC
  - VCCAUX2 - Warns of any requirements on LVPECL_33 and TMDS_33
- ChipScope DRCs
  - CSUC - Checks for unconnected channels.
  - CSCL - Checks for non-clock nets that are clocking clocked elements
  - CSBR - Device block RAM resources exceeded.
- DSP48 DRCs
  - DPCA - Checks the DSP48 cascade.
  - DPREG - Checks for DSP48 asynchronous feedback.
- FIFO DRC
  - FSYN - Checks for synchronous FIFO.
- IOB DRC
  - OPCSLR - Checks for part compatibility between monolithic and multi-die devices.
- Placer DRCs
  - PLCR - Placement constraint to check for clock regions.
  - PLCK - Check clock placement for valid location.
  - PLDL - Placement constraint for I/Os.
  - PLVP - Checks for valid LOC placement
- RAMB DRC
  - RAMB - Check for clock restrictions for READ_FIRST mode.
- Required Pin DRC
  - REQP - Checks for required pins that are not connected.

Implementation and Analysis Enhancements

PlanAhead 13 contains the following Implementation and Analysis enhancements.

- Implementation Enhancements

  The Implementation enhancements include:

  - Ease of file ordering for Implementation Runs.
  - Ability to store Run-specific constraints in a specified UCF file.

    Once you implement a design, PlanAhead automatically loads/stores the constraints from that Run in a run-specific UCF.

•Analysis Enhancements

PlanAhead release 13 provides better visualization of clock and timing paths.

- Hierarchical Design Methodology Support
  - Team Based Design Support

    PlanAhead 13 adds support for new team-based design methodology. Team based design supports multiple engineers implementing at a module level within a design to work in parallel. The flow then supports assembling the module level runs by a team leader at the top level with support for preservation levels to control the placement and routing information that is kept during import.

    See the *Hierarchical Design Methodology Guide* (UG748) and Chapter 13, Hierarchical Design Techniques in the *PlanAhead User Guide* (UG632) for more information.
- Partial Reconfiguration Support
  - PlanAhead provides an interface to Partial Reconfiguration with appropriate licensing.

    See the *Partial Reconfiguration User Guide* (UG702) for more information.

ISE Simulator

- Recompile and Relaunch simulation
  - You can now edit files, re-compile, and re-launch a simulation within the ISE Simulation GUI
- Full Access to Hardware Co-Simulation
  - The limited customer access restrictions have been removed.
  - An additional license is no longer required.
- Design Environment Integration
  - You can now launch ISim from PlanAhead and Project Navigator.
- ISim User Guide Improvements
  - There is a new section on Hardware Co-Simulation.
  - The Tcl Commands chapter has been re-organized.

XPS

- All software development tools have been removed from XPS.
- AXI based MicroBlaze designs are always built using instruction and data caches.
- The main toolbar has been streamlined and now contains fewer buttons.
- Create and Import IP (CIP) wizard now supports creation of AXI4 and AXI4-Lite slave peripherals.
- AXI BFMs project generation now included in CIP wizard.
- ELF files can now be assigned for implementation or simulation and remain synchronized with Project Navigator.
- Debug Wizard supports inclusion of AXI monitors and hardware/software co-debug of AXI-based designs.
- When the XPS design is a submodule in a Project Navigator project, simulation is only available in Project Navigator.

- When you export your design to SDK, the SDK workspace is no longer set automatically set.

SDK

- Cygwin no longer required:
  - Custom makefiles use Windows style paths
  - xbash removed
- MicroBlaze v8.10a support
- XMDStub support removed

Project Navigator/EDK Integration

- Project Navigator will no longer support xmp as the top-level source.
- New messaging to add top-level HDL results in consistent constraint handling.

Embedded IP

- Several Existing core updates
  - See individual change logs and datasheets for specifics.
- AXI Enhancements
  - AXI BRAM Controller – Microblaze ECC Block RAM support.
  - AXI Interconnect – Shared Bus Mode.
  - Partitioned Clock Domains – AXI VDMA, AXI CDMA, AXI DMA.
  - AXI Ethernet – Full checksum offload.

System Generator for DSP

VHDL Library Support for Black Box Import

This new Black Box feature allows you to import VHDL modules that have predefined library dependencies. For example, similar but independent sub-modules can now be compiled into different libraries other than “work”. A detailed example of how to use this new feature can be found in the online Help topic titled “Black Box VHDL Library Support”.

Performance Improvements

- Support for fast simulation model for AXI FFT that provides a 42x speedup.
- 33% improvement in 1st-time initialization of a model.
- 2-3x improvement in simulation speed.

MATLAB Support

- MATLAB 2010a and 2010b are fully supported.
- Beta support is provided for MATLAB 2011a.
- MATLAB must be installed in a directory with no spaces (e.g., C:\MATLAB\R2010b).

- The Fixed-Point Toolbox is required if a Gateway Out block has an output greater than 53 bits. Signals internal to the Xilinx Gateway In and Gateway Out blocks can be larger than 53 bits without needing the Fixed-Point Toolbox.
- For Linux, MATLAB 2010a requires the Red Hat Enterprise Desktop 5.2, 32-bit/64-bit Operating System. It does not work with Red Hat Enterprise Linux WS v4.7.

New Blocks

Complex Multiply 5.0

This block is based on the Xilinx® LogiCORE™ IP Complex Multiplier that implements AXI4-Stream compliant, high performance, optimized complex multipliers based on user-specified options.

DSP48 Macro 2.1

The Xilinx LogiCORE™ DSP48 Macro provides an easy-to-use interface that abstracts the XtremeDSP™ slice and simplifies its dynamic operation by enabling the specification of multiple operations via a set of user-defined arithmetic expressions. New in this version of the core is the ability to control resets and clock enables of the registers within the XtremeDSP Slice.

DSP48E1

The Xilinx DSP48E1 block is an efficient building block for DSP applications that use Xilinx Virtex®-6 devices. The DSP48E1 block provides access to the pre-added and control of the registers within the silicon.

FIR Compiler 6.2

This block is based on the Xilinx® LogiCORE™ IP FIR Compiler v6.2 that implements AXI4-Stream compliant, high performance, optimized complex multipliers based on user-specified options.

VDMA Interface 3.0 (Beta)

This block is based on the AXI Video Direct Memory Access (AXI VDMA) core which is a soft Xilinx IP core providing high-bandwidth direct memory access between external DDR memory and the AXI4-Stream interface. Initialization, status, and management registers are accessed through an AXI4-Lite slave interface which can be configured using an MCode block. A MATLAB utility function is provided to generate the necessary logic to easily connect your System Generator design to external DDR memory.

Previous Versions of System Generator for DSP Release Notes

Previous versions of System Generator for DSP release notes are located in Chapter 3 of the **System Generator for DSP Getting Started Guide (v 12.4)**. This getting started guide is located online at the following URL:

http://www.xilinx.com/support/documentation/dt_sysgendsp_sysgen12-4.htm

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Chapter 3

Architecture Support and Requirements

This chapter describes the operating systems and architectures that the ISE® Design Suite 13 software supports. It also describes system requirements for ISE Design Suite 13. This chapter comprises the following sections:

- Operating Systems
- Architectures
- Compatible Third-Party Tools
- System Requirements

Operating Systems

ISE Design Suite 13 supports three operating systems: Microsoft Windows®, Red Hat® Enterprise Linux, and SUSE Linux Enterprise.

Microsoft Windows

The following table lists Microsoft Windows support.

Table 3-1: **Microsoft Windows Support (English and Japanese)**

Product	XP Professional (32 & 64 bit)	7 Professional (32 & 64 bit)
Design Entry and Implementation Tools (ISE Design Suite Logic Edition 13 software)	Yes	Yes
ISE Simulator (ISim) software	Yes	Yes
ISE WebPACK™ software	Yes	Yes
ChipScope™ Pro software and ChipScope Pro Serial I/O Toolkit	Yes	Yes
Embedded Development Kit (EDK)	Yes	Yes
System Generator for DSP software	Yes	Yes

Linux Support

The following table lists Linux support.

Table 3-2: **Linux Support**

Product	Red Hat Enterprise 4 Workstation (32 & 64 bit)	Red Hat Enterprise 5 Workstation (32 & 64 bit)	SUSE Linux Enterprise (32 & 64 bit)
Design Entry and Implementation Tools (ISE Design Suite 13 software)	Yes	Yes	Yes
ISE Simulator (ISim) software	Yes	Yes	Yes
ISE WebPACK software	Yes	Yes	Yes
ChipScope Pro software and ChipScope Pro Serial I/O Toolkit	Yes	Yes	Yes
Embedded Development Kit (EDK)	Yes	Yes	Yes
System Generator for DSP software	Yes	Yes	Yes

Architectures

ISE Design Suite 13 supports the Virtex® device, Spartan® device, and CPLD device architecture families. The following table lists the architecture support.

Table 3-3: **Architecture Support**

	ISE WebPACK software	ISE Design Suite (Logic Edition, Embedded Edition, DSP Edition, System Edition)
Virtex Series	Virtex-4 devices: LX: XC4VLX15, XC4VLX25 SX: XC4VSX25 FX: XC4VFX12 Virtex-5 devices: LX: XC5VLX30, XC5VLX50 LXT: XC5VLX20T, XC5VLX30T, XC5VLX50T FXT: XC5VFX30T Virtex-6 devices: LXT: XC6VLX75T, XC6VLX75TL Virtex-7 devices: None	Virtex-4 devices: LX: All SX: All FX: All Virtex-5 devices: LX: All LXT: All SXT: All TXT: All FXT: All ***Note:*** Embedded Development Kit (EDK) does not support Virtex-5 TXT devices. Virtex-6 devices: LX/T: All including "L" (lower power) devices CXT: All • SXT: All including "L" devices HXT: All ***Note:*** Embedded Development Kit (EDK) does not support Virtex-6 HXT devices. Virtex-7 devices: All
Kintex Series	Kintex-7 devices: XC7K30T XC7K70T XC7K160T	Kintex-7 devices: All

Table 3-3: **Architecture Support**

	ISE WebPACK software	ISE Design Suite (Logic Edition, Embedded Edition, DSP Edition, System Edition)
Spartan Series	Spartan-3 devices: XC3S50 - XC3S1500 Spartan-3A devices: All Spartan-3AN devices: All Spartan-3A DSP devices: XC3SD1800A Spartan-3E devices: All Spartan-3L devices: XC3S1000L, XC3S1500L XA* Spartan-3 devices: All XA* Spartan-3E devices: All XA* Spartan-3A devices: All XA* Spartan-3A DSP devices: XC3SD1800A Spartan-6 devices: LX: XC6SLX4(L)-XC6SLX75(L) LXT: XC6SLX25T, XC6SLX45T, XC6SLX75T XA* Spartan-6 devices: All *Xilinx Automotive	Spartan-3 devices: All Spartan-3A devices: All Spartan-3AN devices: All Spartan-3A DSP devices: All Spartan-3E devices: All Spartan-3L devices: All XA* Spartan-3 devices: All XA* Spartan-3E devices: All XA* Spartan-3A devices: All XA* Spartan-3A DSP devices: All Spartan 6 device: LX/T: All including "L" (lower power) devices XA* Spartan-6 devices: All *Xilinx Automotive
CoolRunner™ XPLA3 devices CoolRunner-II devices XA* CoolRunner-II devices *Xilinx Automotive	All	All ***Note:*** Embedded Development Kit (EDK) does not support CPLDs.
XC9500 Series devices	All (Except 9500XV family)	All (Except 9500XV family) ***Note:*** Embedded Development Kit (EDK) does not support CPLDs.

Compatible Third-Party Tools

Third-Party Tool	Red Hat Linux	Red-Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP-64 bit	Windows-7 32-bit	Windows-7 64-bit
Simulation							
Mentor Graphics ModelSim SE (6.6d)	√	√	√	√	√	√	√
Mentor Graphics ModelSim PE (6.6d)	N/A	N/A	N/A	√	√	√	√
Mentor Graphics ModelSim DE (6.6d)	√	√	√	√	√	√	√

Third-Party Tool	Red Hat Linux	Red-Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP-64 bit	Windows-7 32-bit	Windows-7 64-bit
Mentor Questa (6.6d)	√	√	√	√	√	√	√
Cadence Incisive® Enterprise Simulator (IES) (10.2)	√	√	√	N/A	N/A	N/A	N/A
Synopsys VCS® and VCS MX (2010.06)	√	√	√	N/A	N/A	N/A	N/A
The MathWorks MATLAB® (2009b, 2010a)	√	√	√	√	√	√	√
The MathWorks Simulink® with Fixed-Point Toolbox (2009b, 2010a)	√	√	√	√	√	√	√
Synthesis							
Synopsys Synplify®/Synplify Pro (E-2010.09)	√	√	√	√	√	√	√
Mentor Graphics Precision® RTL/Plus (2010a)	√	√	√	√	√	√	√
Equivalence Checking							
Cadence Encounter® Conformal® (9.1)	√	√	√	N/A	N/A	N/A	N/A

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

System Memory Recommendations

This section gives the RAM and swap space needed to run ISE Design Suite 13 on your system. The tables below are intended to assist when ordering or building a computer to run FPGA implementation software. These guidelines are based on peak memory requirements for a given device size. For typical memory requirements, please see:

http://www.xilinx.com/ise/products/memory.htm

Memory Requirements Tables

Table 3-4: **Peak Memory Requirements: 32-bit OS**

Memory: 32-bit OS	Family	Device Size
2GB	Spartan-3	3S50 - 3S2000
	Spartan-6	6S4 - 6S45
	Virtex-4	4V12 - 4V25
	Virtex-5	5V20 - 5V50
	Kintex-7	7K30 - 7K70
4GB	Spartan-3	3S3400 - 3S5000
	Spartan-6	6S75 - 6S150
	Virtex-4	4V35 - 4V60
	Virtex-5	5V70 - 5V130
	Virtex-6	6V75
	Kintex-7	7K160

Table 3-5: **Peak Memory Requirements: 64-bit OS**

Memory: 64-bit OS	Family	Device Size
2GB	Spartan-3	3S50 - 3S1400
	Spartan-6	6S4 - 6S16
	Virtex-4	4V12 - 4V25
	Kintex-7	7K30
4GB	Spartan-3	3S1500 - 3S5000
	Spartan-6	6S45
	Virtex-4	4V20 - 4V60
	Virtex-5	5V20 - 5V110
	Virtex-6	6V75
	Kintex-7	7K70 - 7K160
8GB	Virtex-4	4V140 - 4V200
	Virtex-5	5V220 - 5V240
	Virtex-6	6V195 - 6V240
	Kintex-7	7K325

Table 3-5: **Peak Memory Requirements: 64-bit OS**

Memory: 64-bit OS	Family	Device Size
12GB	Virtex-5	5V330
	Virtex-6	6V315 - 6V365
	Kintex-7	7K410
	Virtex-7	7V450 - 7V485
16GB	Virtex-6	6V380 - 6V550
	Virtex-7	7V585 - 7V855
20GB	Virtex-6	6V565 - 6V760
	Virtex-7	7V865 - 7V870
24GB	Virtex-7	7V1500
32GB	Virtex-7	7V2000

Operating Systems and Available Memory

The Microsoft Windows and Linux® operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs may encounter this limitation. ISE Design Suite 13 has optimized memory and enabled software support for applications to increase RAM memory available to Xilinx software.

Windows XP Professional 32-bit

Xilinx applications are enabled to take advantage of the memory increase feature on Windows 32-bit. You must then modify Windows setting to get access to this larger memory.

The standard Windows OS architecture limits the maximum memory available to a Xilinx process to 2 Gigabyte (GB). In Windows XP Professional, Microsoft created an option to support the ability of an application to address 3 GB of RAM. Xilinx ISE applications have built-in support for this option. To take advantage of this capability, you must also modify your Windows XP OS to enable this feature, which requires that you modify your `boot.ini` file by adding a "/3GB" entry to the end of the "startup" line.

Before enabling 3 GB support for Xilinx applications, please read the Microsoft Knowledge Base Article #328269 at http://support.microsoft.com/?kbid=328269. If you upgrade your computer to Windows XP Service Pack 1 (SP1) and you are using the /3GB switch, Windows may not restart without a patch from Microsoft. Please see (Xilinx Answer 17905) for more information.

Additionally, before making this change, please read:

- Microsoft Bulletin Q17193 http://support.microsoft.com/default.aspx?scid=kb;en-us;Q171793, which contains information on "Application Use of 4GT RAM Tuning".
- Microsoft Bulletin Q289022 http://support.microsoft.com/default.aspx?scid=kb;en-us;q289022, contains instructions for editing your `boot.ini` file.

Linux

ISE Design Suite 13 supports both Linux 32-bit and Linux 64-bit. The latter allows greater memory allocation. Xilinx has documented Linux kernel modifications that allow a Xilinx application to address over 3 GB of memory.

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the hugemem kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site: http://www.redhat.com/docs/manuals/enterprise/

ISE supports the 64-bit version of Red Hat Enterprise Linux, which allows greater memory allocation out of the box.

Cable Installation Requirements

Platform Cable USB II and Parallel Cable IV are high-performance cables that enable Xilinx® design tools to program and configure target hardware.

To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.

To install Parallel Cable IV, a system must have a parallel port connector and support parallel port communication.

Cables are officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows XP Professional, Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- All Linux: Root privileges are required to install cable drivers on Linux.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.
- Linux LibUSB support: Preliminary support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website. See Answer Record #25249 for details.

For additional information regarding Xilinx cables, refer to the following documents:

- USB Cable Installation Guide (UG344)
- Platform Cable USB II Data Sheet (DS593)
- Parallel Cable IV Data Sheet (DS097)

Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 3-6: **Equipment and Permissions Requirements**

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Drive	You must have a DVD-ROM for ISE Design Suite (if you have received a DVD, rather than downloading from the web), and CD-ROM for MXE on your system. ***Note:*** ModelSim Xilinx Edition and ModelSim Xilinx Edition Starter will no longer be available on CDs or for download beginning December 10th, 2010. Xilinx will also stop generating licenses and providing updated libraries for both products on December 10th, 2010. This means that ISE® Design Suite 12.3 was the last version of Xilinx ISE software to support ModelSim Xilinx Edition-III. Please see Product Discontinuance Notice XCN10028 for more details.
Ports	To program devices, you must have an available parallel, or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable. ***Note:*** Installation of the cable driver software requires Windows XP Pro SP1 (or later), or Windows-7. If you are not using one of these operating systems, the cables may not work properly.

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

ChipScope Pro Analyzer

Cable Installation Requirements

For Linux, cable drivers require root privileges to install. To install Platform Cable USB II for USB 2.0 port, you must have Windows XP SP2. The Platform Cable USB II is a high-performance download cable that attaches to user hardware for use with the ChipScope Pro Analyzer tool for device programming, configuring, and debugging.

System Memory Recommendations

The ChipScope Pro Analyzer software requires 1024 megabytes (MB) of system memory. The ChipScope Pro Core Inserter tool has the same requirements as ISE. For more

information on ISE memory recommendations, see:
http://www.xilinx.com/ise/products/memory.htm.

System Generator for DSP System Requirements and Recommendations

Hardware Recommendations

Table 3-7: **System Generator for DSP Hardware Recommendations**

Recommendation	Notes
4.00 GB of RAM	N/A
600 MB of hard disk space	Minimum Requirement
Xilinx Hardware Co-Simulation Platform	Required for the Hardware Co-Simulation Flow

OS and Software Requirements

Table 3-8: **System Generator for DSP OS and Software Requirements**

Requirement	Notes
Windows XP Professional SP2, 32-bit/64-bit or Windows-7, 32-bit/64-bit or Red Hat Linux 4u7, 32-bit & 64-bit	N/A
Xilinx ISE Design Suite 13.1	N/A
MathWorks MATLAB Version 2010a or 2010b. Beta support for MATLAB Version 2011a.	MATLAB 2010a requires Red Hat Enterprise Desktop 5.2, 32-bit/64-bit Operating System. It does not work with Red Hat Enterprise Linux WS v4.7.
MathWorks Simulink with Fixed-Point Toolbox Version 2010a or 2010b. Beta support for MathWorks Simulink with Fixed-Point Toolbox Version 2011a.	MATLAB must be installed in a directory with no spaces (e.g., C:\MATLAB\R2010a) The Fixed-Point Toolbox is required if a Gateway Out block has an output greater than 53 bits. Signals internal to the Xilinx Gateway In and Gateway Out blocks can be larger than 53 bits without needing the Fixed-Point Toolbox.

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Chapter 4

Technical Support, Services, and Documentation

This chapter describes how to access technical support, services, and documentation that are available. This chapter contains the following sections:

- Technical Support
- Education Services
- Documentation

Technical Support

For technical questions, visit the Xilinx® support site,

www.xilinx.com/support/

where you can search the Answers Database or utilize the following self support features:

- Documentation Center , www.xilinx.com/support/documentation/index.htm
- Download Center, www.xilinx.com/support/download/index.htm
- Answer Browser, www.xilinx.com/support/answers/index.htm
- Xilinx User Community Forums, http://forums.xilinx.com
- Design Resources - Video Demonstrations, www.xilinx.com/design

If you cannot resolve your issue using our online resources, you can contact Xilinx Technical Support directly at:

www.xilinx.com/support/techsup/tappinfo.htm

Education Services

Xilinx provides targeted, high-quality education services designed by experts in programmable logic design, and delivered by Xilinx qualified trainers. Available are onsite and online instructor led courses, and recorded e-learning for self paced learning.

For more information on training courses, free on-demand training, live online training, and upcoming events, visit the Xilinx Training website,

www.xilinx.com/support/education-home.htm

Documentation

Xilinx offers technical documentation to assistant users with using the ISE® Design Suite tools.

Context-Sensitive Help

Context-sensitive online Help is available for most ISE Design Suite tools that are available with a graphical user interface (GUI). From Project Navigator, select **Help > Help Topics** to access the online Help.

Software Manuals

Detailed software manuals about the ISE Design Suite applications and command-line functions are included as part of the software installation. After you install the software, you can select the **Help > Software Manuals** command in Project Navigator to access the software manuals collection.

Note: If you do not already have Adobe Acrobat Reader installed, you must do so to view the software manuals.

A new documentation navigation page is now the default startup page in Xilinx Platform Studio (XPS). From the documentation tab you can browse to all Embedded Development Kit (EDK) documentation. From outside XPS, open the file `edk_documentation_locator.htm`, which is found at `$XILINX_EDK/doc`.

To locate the Software Manuals on the website:

1. Go to the Documentation Center, http://www.xilinx.com/support/documentation/index.htm
2. Click the **Design Tools** tab.
3. Click the Design Tool category, such as ISE, or click the **See All Design Tools Documentation** link.

User Tutorials

Tutorials can be found online at:

http://www.xilinx.com/support/techsup/tutorials/index.htm

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Chapter 5

Additional Resources

Answer Database

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support/.

Additional Documentation

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To obtain the current version of the USB Cable Installation Guide, see the Xilinx website at:

http://www.xilinx.com/support/documentation/user_guides/ug344.pdf

To obtain the current version of the data sheet for Platform Cable USB II, see the Xilinx Website at:

http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf

To obtain the current version of the data sheet for Parallel Cable IV, see the Xilinx Website at:

http://www.xilinx.com/support/documentation/data_sheets/ds097.pdf

Third-Party Licenses

The Third-Party Licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx ISE® Design Suite software tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology.

To view the Third-Party Licenses details, see the Xilinx Third-Party Licenses Guide.