ISD ARM® Cortex®-M0 SoC

ISD91032 Series

Datasheet

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1 GENERAL DESCRIPTION

The ISD91032 is a new member of Nuvoton ARM® Cortex®-M0 Audio SoC family. The 1.8V to 5.5V operating voltage makes it an ideal fit for battery powered consumer products. The highly integrated architecture – 32bit ARM® Cortex®-M0 processor, wide operating voltage, speaker driver, embedded flash memory and multi-function GPIO – is designed to provide fast Time-to-Market and cost effective solution, enable audio feature to wide range of industrial and consumer products such as voice recognition and audio/voice feedback for portable medical devices, security systems, public transit vehicles, home appliances, and novelty items.

2 FEATURES

- **Core**
  - ARM® Cortex®-M0 core runs up to 50MHz
  - One 24-bit System tick timer for operating system support
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the interrupt inputs, each with 4 levels of priority
  - Serial Wire Debug supports
- **Power Management**
  - Wide operating voltage range from 1.8V to 5.5V (not include ADC/PGC)
  - Power Management Unit (PMU) provides different levels of power control.
  - Deep Power Down (DPD) mode with specific register retention is the lowest power state.
  - Wakeup from DPD via specific WAKEUP pin (GPA4) or LIRC timed operation.
  - Standby Power Down (SPD/STOP) mode is the lowest power state with RAM retention (typically < 5uA) and LXT or LIRC operation (typically <7uA).
  - Wakeup from SPD can be from any GPIO, RTC, or WDT interrupts.
- **Flash EPROM Memory**
  - 64 KB Flash EPROM for program code and data storage
  - Additional 4 KB of flash can be configured as boot sector for ISP loader
  - Support ISP and ICP code update
  - 512-Byte page erase and 4-Byte word programming
  - Configurable boundary to delineate code and data flash
  - Support 2 wire ICP update from ICE interface
- **SRAM Memory**
  - 6KB embedded SRAM
- **Clock Control**
  - Built-in high speed (HIRC, factory trimmed within +/-1% to 49.152MHz) and low speed (LIRC, 10KHz) oscillators, no external components necessary.

- External 32 KHz crystal/resonator input (LXT)

- **GPIO**
  - Max. 22 GPIOs can be configured individually for below four I/O modes:
    - Quasi bi-direction
    - Input with pull-up option
    - Push-Pull output
    - Open-Drain output
  - TTL/Schmitt trigger input selectable by pair
  - Each I/O pin can be configured as interrupt source with edge/level setting

- **ADC**
  - 10-bit SAR ADC
  - Programmable gain amplifier with 64 steps from -18dB to 45dB in 1dB step size
  - DMA support for minimal CPU intervention

- **Differential Audio PWM Output (DPWM)**
  - Direct connection of speaker
  - 0.5W drive capability into 8Ω load @5V
  - Configurable up-sampling to support sample rates from 8 ~ 32 KHz
  - DMA support for minimal CPU intervention

- **13-bit DAC**
  - An alternative to DPWM for driving external PA
  - Minimum output impedance with 10KΩ

    Note:
  - Direct speaker driving (output impedance <10KΩ) may cause DAC damage
  - Do not enable DPWM and DAC simultaneously

- **PDMA**
  - 2-channel DMAs support data transfer between SRAM and peripherals of ADC, DPWM, SPI0 or SPIM

- **Timers**
  - Three timers with 8-bit pre-scalar and 16-bit counter
  - Counter auto re-load
  - Timer1 can toggles for IR carrier generator
  - One fixed frequency timer

- **Watch Dog Timer**
  - Multiple clock sources
  - 8 selectable time-out periods from micro seconds to seconds (depending on clock source)
  - WDT can wake up power-down/sleep
  - Interrupt or reset selectable on watchdog time-out

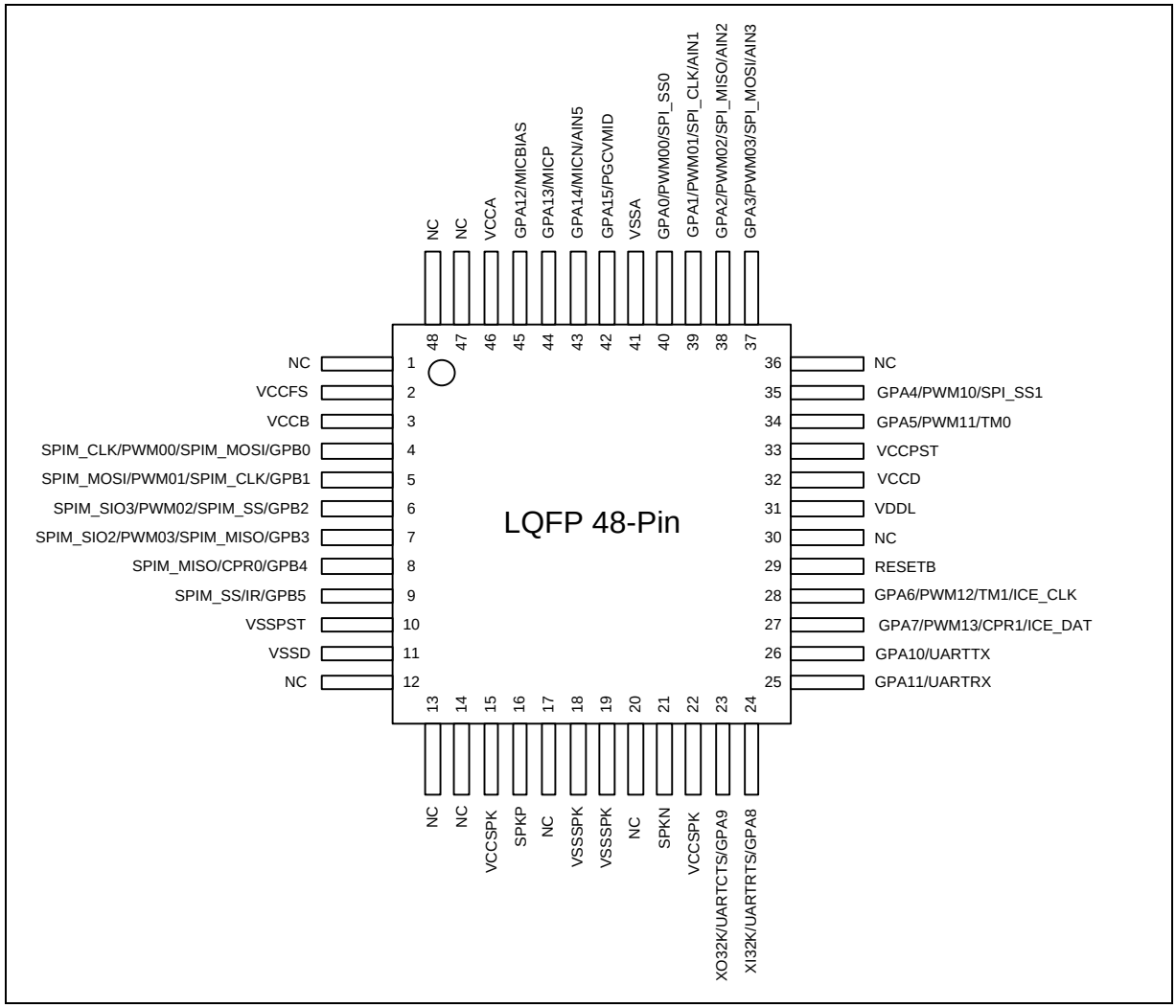
- **RTC Timer**

- Clock from LIRC 10KHz or LXT 32KHz
- Selectable interrupt frequencies (0.25, 0.5, 1, 2, 4, 8, 16, 32 Hz based on LXT 32KHz)
- Support wake up function

- **Two sets of PWM/Capture**
  - Built-in one 16-bit timer and four 16-bit comparators for 4 PWM outputs as a set
  - 2 sets support up to 8 individual PWM outputs or up to 4 complementary paired outputs
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scalar and Dead-Zone generator for complementary paired PWM
  - PWM interrupt synchronous to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs
  - Support Capture interrupt
- **UART**
  - UART port with flow control (TX, RX, CTS and RTS)
- **SPI0**
  - Master up to 24.576 Mbps / Slave up to 12.288 Mbps
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode
  - Two 32-bit buffers or DMA support for burst transfers
- **SPIM**
  - Supports general SPI master interface protocol
  - 8-, 16-, 24-, and 32-bit length of transaction
  - Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
  - DMA support for burst transfers
- **Voltage Detector (VD) or Brown-Out Detector (BOD)**
  - With 16 levels: 1.8/1.9/2.0/2.1/2.2/2.4/2.6/2.8/3.0/3.1/3.4/3.6/3.7/.3.9/4.2/4.6V
  - Supports BOD Interrupt and Reset Option
- **Low Voltage Reset: 1.6V**
- **Built-in Low Dropout Voltage Regulator (LDO)**
  - Capable of delivering 25mA load current at 3.3V
  - Configurable output voltage: 8 options of 1.5V/1.7V/1.8V/2.4V/2.5V/2.7V/3V/3.3V
  - 1.5V LDO for core logic
- **Operating Temperature: -40°C ~ 85°C**
- **Package**
  - LQFP-48 Green package (RoHS)

3 PART INFORMATION AND PIN CONFIGURATION

3.1 LQFP 48-Pin Diagram



3.2 Pin/Pad Description

LQFP48 Pin No.	Name	Type	Alt CFG	Description
1	NC			Remain unconnected
2	VCCFS	**P**		Power supply for the LDO of VCCB, normally connect to VCCD
3	VCCB	**P**		Power supply for GPB0~5 and driving external, could be VCCFS based LDO regulator output. If used, a 1µF capacitor must be placed to ground. If not used then tie to VCCD.
4	GPB0	**I/O**	0	General purpose input/output pin; port B, bit0
	SPIM_CLK	**O**	1	SPIM Serial Clock
	PWM00	**O**	2	PWM0 channel 0 output
	SPIM_MOSI	**O**	3	SPIM Master Out Slave In
5	GPB1	**I/O**	0	General purpose input/output pin; port B, bit1
	SPIM_MOSI	**I/O**	1	SPIM Master Out Slave In
	PWM01	**O**	2	PWM0 channel 1 output
	SPIM_CLK	**O**	3	SPIM Serial Clock
6	GPB2	**I/O**	0	General purpose input/output pin; port B, bit2
	SPIM_SIO3	**I/O**	1	SPIM Quad Mode Serial I/O 3
	PWM02	**O**	2	PWM0 channel 2 output
	SPIM_SS	**O**	3	SPIM Slave Select
7	GPB3	**I/O**	0	General purpose input/output pin, port B, bit3
	SPIM_SIO2	**I/O**	1	SPIM quad mode Serial I/O 2
	PWM03	**O**	2	PWM0 channel 3 output
	SPIM_MISO	**I**	3	SPIM Master In Slave Out
8	GPB4	**I/O**	0	General purpose input/output pin, port B, bit4
	SPIM_MISO	**I/O**	1	SPIM Master In Slave Out
	CPR0	**I**	2	Capture input based on PWM0 timer
9	GPB5	**I/O**	0	General purpose input/output pin, port B, bit5
	SPIM_SS	**O**	1	SPIM Slave Select
	IR	**O**	2	IR carrier generator based on Timer1 interval
10	VSSPST	**P**		Digital ground, connect to VSSD
11	VSSD	**P**		Digital ground

LQFP48 Pin No.	Name	Type	Alt CFG	Description
12	NC			Remain unconnected
	VPP	**P**		Remain unconnected
13	NC			Remain unconnected
14	NC			Remain unconnected
15	VCCSPK	**P**		Power Supply for DPWM Speaker Driver
16	SPKP	**O**		Positive Speaker Driver Output
17	NC			Remain unconnected
18	VSSSPK	**P**		Ground for DPWM Speaker Driver
19				
20	NC			Remain unconnected
21	SPKN	**O**		Negative Speaker Driver Output
22	VCCSPK	**P**		Power Supply for DPWM Speaker Driver
23	GPA9	**I/O**	0	General purpose input/output pin; port A, bit9
	UARTCTS	**I**	2	UART Clear To Send Input
	XO32K	**O**	3	32K Crystal Oscillator Output
24	GPA8	**I/O**	0	General purpose input/output pin; port A, bit8
	UARTRTS	**O**	2	UART Request To Send Output
	XI32K	**I**	3	32K Crystal Oscillator Input
25	GPA11	**I/O**	0	General purpose input/output pin; port A, bit11
	UARTRX	**I**	2	UART Receiver Serial In
26	GPA10	**I/O**	0	General purpose input/output pin; port A, bit10
	UARTTX	**O**	2	UART Transmitter Serial Out
27	GPA7	**I/O**	0	General purpose input/output pin; port A, bit7
	PWM13	**O**	1	PWM1 channel 3 output
	CRP1	**I**	2	Capture input based on PWM1 timer
	ICE_DAT	**I/O**	X	SWD Interface, Serial Data
28	GPA6	**I/O**	0	General purpose input/output pin; port A, bit6
	PWM12	**O**	1	PWM1 channel 2 output

LQFP48 Pin No.	Name	Type	Alt CFG	Description
	TM1	**I**	2	Timer1 external clock input
	ICE_CLK	**I**	X	SWD Interface, Serial Clock
29	RESETB	**I**		Reset input, low active, internal pull-high
30	NC			Remain unconnected
31	VDDL	**P**		Regulator output decoupling pin for core logic. A 1uF cap returning to VSSD must be placed on it..
32	VCCD	**P**		Main Digital Power Supply
33	VCCPST	**P**		Digital power, connect to VCCD
34	GPA5	**I/O**	0	General purpose input/output pin; port A, bit5
	PWM11	**O**	1	PWM1 channel 1 output
	TM0	**I**	2	Timer0 external clock input
35	GPA4	**I/O**	0	General purpose input/output pin; port A, bit4
	PWM10	**O**	1	PWM1 channel 0 output
	SPI_SS1	**O**	2	SPI0 Slave Select 1
36	NC			Remain unconnected
37	GPA3 (AIN3)	**I/O**	0	General purpose input/output pin; port A, bit3 ADC input channel 3
	PWM03	**O**	1	PWM0 channel 3 output
	SPI_MOSI	**I/O**	2	SPI0 Master Out Slave In
38	GPA2 (AIN2)	**AIO**	0	General purpose input/output pin; port A, bit2 ADC input channel 2
	PWM02	**O**	1	PWM0 channel 2 output
	SPI_MISO	**I/O**	2	SPI0 Master In Slave Out
39	GPA1 (AIN1)	**I/O**	0	General purpose input/output pin; port A, bit1 ADC input channel 1
	PWM01	**O**	1	PWM0 channel 1 output
	SPI_CLK	**I/O**	2	SPI0 Serial Clock
40	GPA0	**I/O**	0	General purpose input/output pin; port A, bit0
	PWM00	**O**	1	PWM0 channel 0 output
	SPI_SS0	**I/O**	2	SPI0 Slave Select 0
41	VSSA	**AP**		Ground for Analog Circuitry

LQFP48 Pin No.	Name	Type	Alt CFG	Description
42	GPA15	**I/O**	0	General purpose input/output pin; port A, bit15
	PGCVMID	**AO**	1	Mid Rail Reference, Connect 4.7uF to VSSA
43	GPA14	**I/O**	0	General purpose input/output pin; port A, bit14
	MICN	**AI**	1	Negative Microphone Input
	AIN5	**AI**	2	ADC input channel 5
44	GPA13	**I/O**	0	General purpose input/output pin; port A, bit13
	MICP	**AI**	1	Positive Microphone Input
45	GPA12	**I/O**	0	General purpose input/output pin; port A, bit12 **Note**: GPA12/MICBIAS is sensitive to the noise, it is easy to make IC hang-up when the input level is beyond the input voltage spec (VDD+0.3V ~ VSS-0.3V). Recommend using GPA12/MICBIAS as output or input with pull-up/low to avoid floating condition.
	MICBIAS	**AO**	1	Microphone Bias Output
46	VCCA	**AP**		Power Supply for Analog Circuitry
47	NC			Remain unconnected
48	NC			Remain unconnected

Pin/Pad Type: I=Digital Input, O=Digital Output, AI=Analog Input, AO=Analog Output, P=Power, AP=Analog Power

3.3 Alternative Function List of GPIO

GPIO	Power	ALT=1		ALT=2		ALT=3		Special
		Name	I/O type	Name	I/O type	Name	I/O type	
GPA0	VCCD	PWM00	O	SPI_SS0	I/O	-		
GPA1	VCCD	PWM01	O	SPI_CLK	I/O	-		AIN1
GPA2	VCCD	PWM02	O	SPI_MISO	I/O	-		AIN2
GPA3	VCCD	PWM03	O	SPI_MOSI	I/O	-		AIN3
GPA4	VCCD	PWM10	O	SPI_SS1	O	-		
GPA5	VCCD	PWM11	O	TM0	I	-		
GPA6	VCCD	PWM12	O	TM1	I	-		ICE_CLK
GPA7	VCCD	PWM13	O	CPR1	I	-		ICE_DAT
GPA8	VCCD	-		UARTRTS	O	XI32K	I	
GPA9	VCCD	-		UARTCTS	I	XO32K	O	
GPA10	VCCD	-		UARTTX	O	-		
GPA11	VCCD	-		UARTRX	I	-		
GPA12	VCCA	MICBIAS	AO	-		-		
GPA13	VCCA	MICP	AI	-		-		
GPA14	VCCA	MICN	AI	AIN5	AI	-		
GPA15	VCCA	PGCVMID	AO	-		-		
GPB0	VCCB	SPIM_CLK	O	PWM00	O	SPIM_MOSI	I/O	
GPB1	VCCB	SPIM_MOSI	I/O	PWM01	O	SPIM_CLK	O	
GPB2	VCCB	SPIM_SIO3	I/O	PWM02	O	SPIM_SS	O	
GPB3	VCCB	SPIM_SIO2	I/O	PWM03	O	SPIM_MISO	I/O	
GPB4	VCCB	SPIM_MISO	I/O	CPR0	I	-		
GPB5	VCCB	SPIM_SS	O	IR	O	-		

1. ICE_CLK and ICE_DAT are default setting and have specific control.
2. AIN1, AIN2 and AIN3 are ADC inputs, select GPIO with input mode and disable pull-up option.

4 BLOCK DIAGRAM

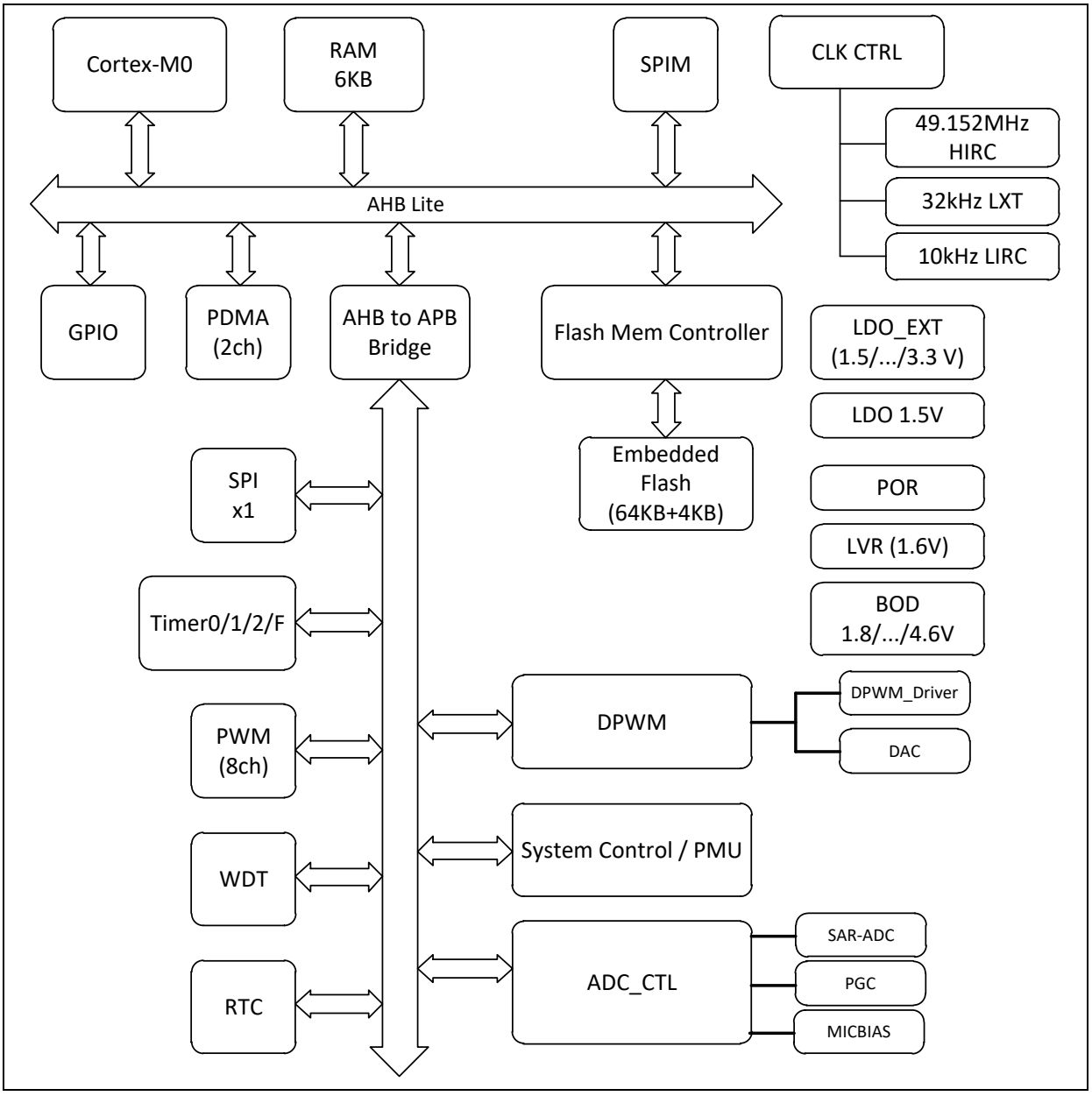
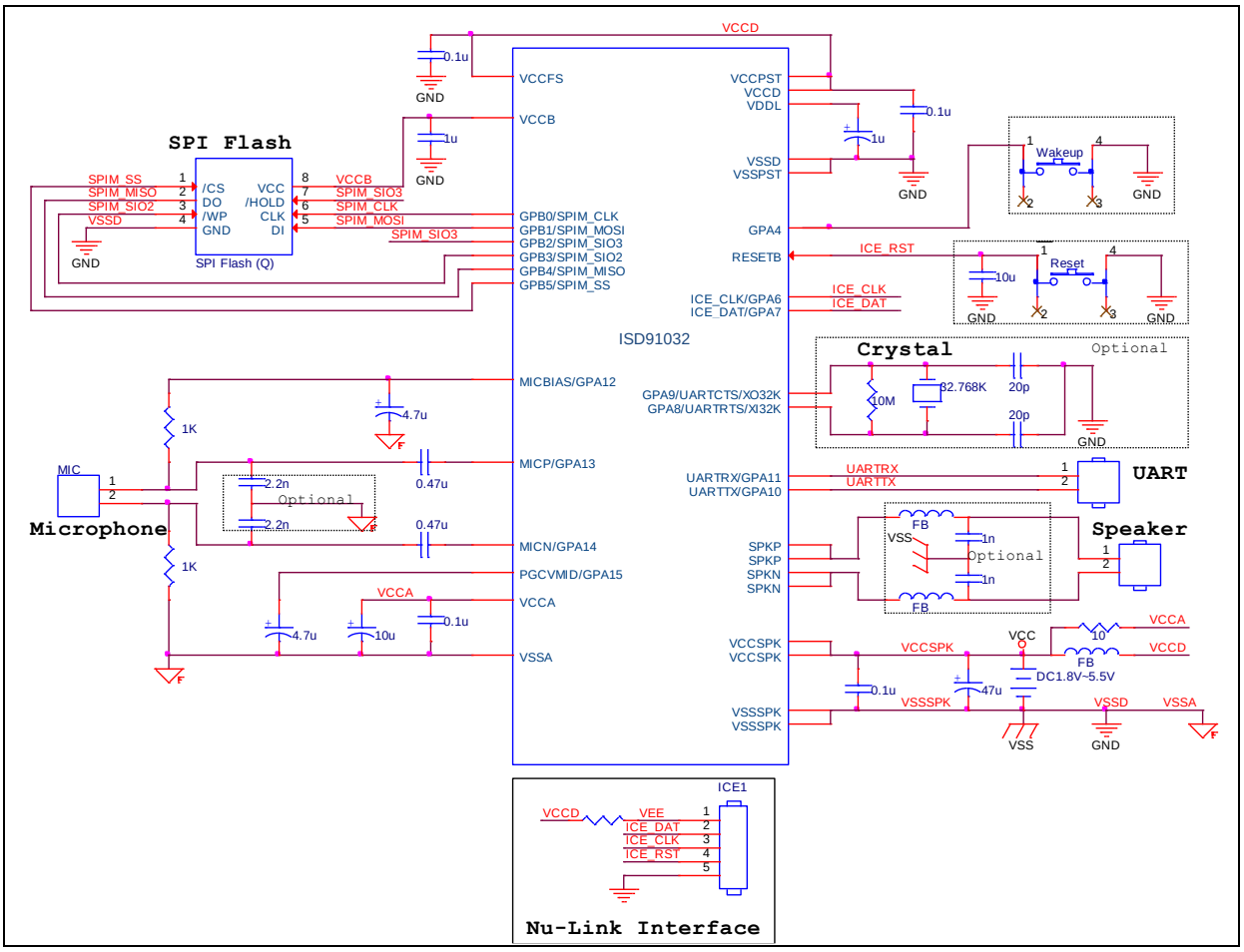


Figure 4-1 ISD91032 Function Block Diagram

5 REFERENCE APPLICATION CIRCUIT



Note:

1. Power domains: VCCD/VSSD, VDDL/VSSD, VCCB/VSSD, VCCA/VSSA, VCCSPK/VSSSPK.
2. The LC (FB with C) circuitry in Speaker part is for EMI.
3. For the interface of SPI-Flash, the GPB2 & GPB3 connections could be as above for quad mode operation, or they could be used for GPIO with VCCB pull-up on /WP & /HOLD instead.
4. For 2-battery (1.5V*2) application, connecting VCCD to VCCB could avoid unnecessary voltage drop on VCCB and GPB0~5.
5. Besides a GPIO, GPA4 is the only wake-up pin of DPD mode.
6. Disabling 32K oscillator before using GPA8 and GPA9 for GPIO.

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by an I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current Sunk by Total I/O Pins			100	mA
Maximum Current Sourced by Total I/O Pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

(VDD-VSS=4.5V, TA = 25°C, No load unless otherwise specified.)

Parameter	Sym	Specification				Test Conditions
		Min	Typ	Max	Unit	
Operation voltage	V_{DD}	1.8		5.5	V	V_{DD}=1.8V~5.5V up to 49.152Mhz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	1.8		5.5	V	
Operating Current at Normal Run Mode @49.152MHz (Run while(1) {} at APROM)	I_{DD1}		15		mA	V_{DD}=4.5V, enable all IP's clock
	I_{DD2}		10		mA	V_{DD}=4.5V, disable all IPs' clock
	I_{DD3}		12		mA	V_{DD}=1.8V, enable all IPs' clock
	I_{DD4}		8		mA	V_{DD}=1.8V, disable all IPs' clock
Operating Current at Normal Run Mode @24.576MHz (Run while(1) {} at APROM)	I_{DD5}		9		mA	V_{DD}=4.5V, enable all IP's clock
	I_{DD6}		6		mA	V_{DD}=4.5V, disable all IPs' clock
	I_{DD7}		7		mA	V_{DD}=1.8V, enable all IPs' clock
	I_{DD8}		4		mA	V_{DD}=1.8V, disable all IPs' clock

Operating Current at Idle Mode (Run "WFI" at APROM)	I_{IDLE1}		10		mA	Enable all IP's clock
	I_{IDLE2}		6		mA	Disable all IP's clock
Operating Current at SPD (Standby Power-Down) Mode	I_{SBD1}		4		uA	V_{DD}=4.5V, disable all IP
	I_{SBD2}		6			V_{DD}=4.5V, disable all IP except LXT or LIRC is operating
Operating Current at DPD (Deep Power-Down) Mode	I_{DPD}		2		uA	V_{DD}=4.5V, disable LIRC, PA.4 internal pull-up for wakeup
Input Current GPA0~12/GPB with pull-up active	I_{IN1}	3.6	-	95	uA	V_{DD}=4.5V, V_{IN} = 0V
Input Current GPA13~15 with pull-up active	I_{IN2}	100		400	uA	V_{DD}=4.5V, V_{IN} = 0V
Input Current at RESETB	I_{IN3}		80		uA	V_{DD}=4.5V, V_{IN} = 0V
Input Leakage Current GPA/ GPB	I_{LK}	-1	-	+1	uA	$0<V_{IN}<V_{DD}$
Input Low Voltage GPA/GPB (TTL)	V_{IL1}	-0.3	-	$0.2V_{DD}$	V	
Input High Voltage GPA/GPB (TTL)	V_{IH1}	$0.7V_{DD}$	-	V_{DD} +0.2	V	
Negative Going Threshold (Schmitt input)	V_{ILS}		$0.4V_{DD}$		V	Schmitt trigger selected
Positive Going Threshold (Schmitt input)	V_{IHS}		$0.6V_{DD}$		V	Schmitt trigger selected
Hysteresis voltage of GPA/GPB(Schmitt input)	V_{HY}		$0.2V_{DD}$		V	Schmitt trigger selected
High level output voltage	V_{OH}	2.8			V	I_{OH}=4mA, VDD≥3.3V
Low level output voltage	V_{OL}			0.4	V	I_{OL}=3mA
Sink Current	I_{SINK}	5.6			mA	V_{OL}=0.2V, $4.5≤V_{DD}≤5.5V$
	I_{SINK}	4.3			mA	V_{OL}=0.2V, $3.3≤V_{DD}<4.5V$
	I_{SINK}	2.1			mA	V_{OL}=0.2V, $1.8≤V_{DD}<3.3V$
Source Current	I_{SR}	-2.6			mA	$V_{OH}=V_{DD}$-0.2V, $4.5≤V_{DD}≤5.5V$
	I_{SR}	-2.0			mA	$V_{OH}=V_{DD}$-0.2V, $3.3≤V_{DD}<4.5V$
	I_{SR}	-1.0			mA	$V_{OH}=V_{DD}$-0.2V, $1.8≤V_{DD}<3.3V$

Notes:

1. RESETB pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.

6.3 AC Electrical Characteristics

(VDD-VSS=4.5V, TA = 25°C, No load unless otherwise specified.)

6.3.1 External 32 KHz XTAL Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage		1.8		5.5	V
Input Clock Frequency	External Crystal	-	32.768	-	KHz

6.3.2 Internal 49.152 MHz RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage		1.8		5.5	V
Center Frequency		-	49.152	-	MHz
Calibrated Oscillator Frequency	+25°C; V_{DD}=3.0V	-1		+1	%
	V_{DD}=1.8V~5V	-4	-	+4	%

6.3.3 Internal 10 KHz RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage		1.8		5.5	V
Central Frequency			10		kHz
Calibrated Internal Oscillator Frequency	+25□C; V_{DD} =3.0V	-5	-	+5	%
	V_{DD}=1.8V~5.5V	-35	-	+35	%

6.4 Analog Characteristics

6.4.1 10-bit SAR ADC

Parameter	Symbol	Min	Typ	Max	Unit
Resolution	-	-	10		bit
Offset Error	EO	-4	±0.5	+2	LSB
Gain Error (Transfer gain)	EG		±1	±2.5	%
Monotonic			9		bit
ADC Clock Frequency	FADC	-	-	2.4	MHz
Sample & Conversion Time	TADC	-	12	-	Clock
Sample Rate	FS	-	-	200	ksps
Supply Voltage	VCCA	2		5.5	V
Supply Current (Avg.)	IDD	-	-	1.5	mA

Input Voltage Range	VIN	0	-	AVDD	V
Integral Non-Linearity Error	INL	-2	±1	+2	LSB
Differential Non-Linearity	DNL	-1	±0.5	+1	LSB

6.4.2 LDO for VCCB (1.5/1.7/1.8/2.4/2.5/2.7/3.0/3.3V)

Parameter	Condition	Min	Typ	Max	Unit
Input Voltage		1.8	-	5.5	V
LDO output Voltage	Adjustable	1.5		3.3	V
Load Current				25	mA

6.4.3 PGA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operation Voltage	VCCA		2.4		5.5	V
Operation Current	IDD			1.5		mA
Programmable Gain			-18		45	dB
Programmable Gain Step Size		Guaranteed Monotonic		1		dB

6.4.4 MICBIAS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Bias Voltage	VMICBIAS		90%,65%,70%,50% of VCCA			V
Bias Current Source	IMICBIAS			3		mA

6.4.5 BOD/LVR

Parameter	Symbol	Min	Typ	Max	Unit
Operation Current	IDD		50		μA
BOD Voltage	BOD_SEL[3:0] =1111		4.6		V
	BOD_SEL[3:0] =1110		4.2		V
	BOD_SEL[3:0] =1101		3.9		V
	BOD_SEL[3:0] =1100		3.7		V
	BOD_SEL[3:0] =1011		3.6		V
	BOD_SEL[3:0] =1010		3.4		V
	BOD_SEL[3:0] =1001		3.1		V
	BOD_SEL[3:0] =1000		3.0		V
	BOD_SEL[3:0] =0111		2.8		V
	BOD_SEL[3:0] =0110		2.6		V

	BOD_SEL[3:0] =0101		2.4		V
	BOD_SEL[3:0] =0100		2.2		V
	BOD_SEL[3:0] =0011		2.1		V
	BOD_SEL[3:0] =0010		2.0		V
	BOD_SEL[3:0] =0001		1.9		V
	BOD_SEL[3:0] =0000		1.8		V
BOD Hysteresis	V_{hys}	30		125	mV
LVR Voltage	LVR		1.6		V

6.4.6 DAC

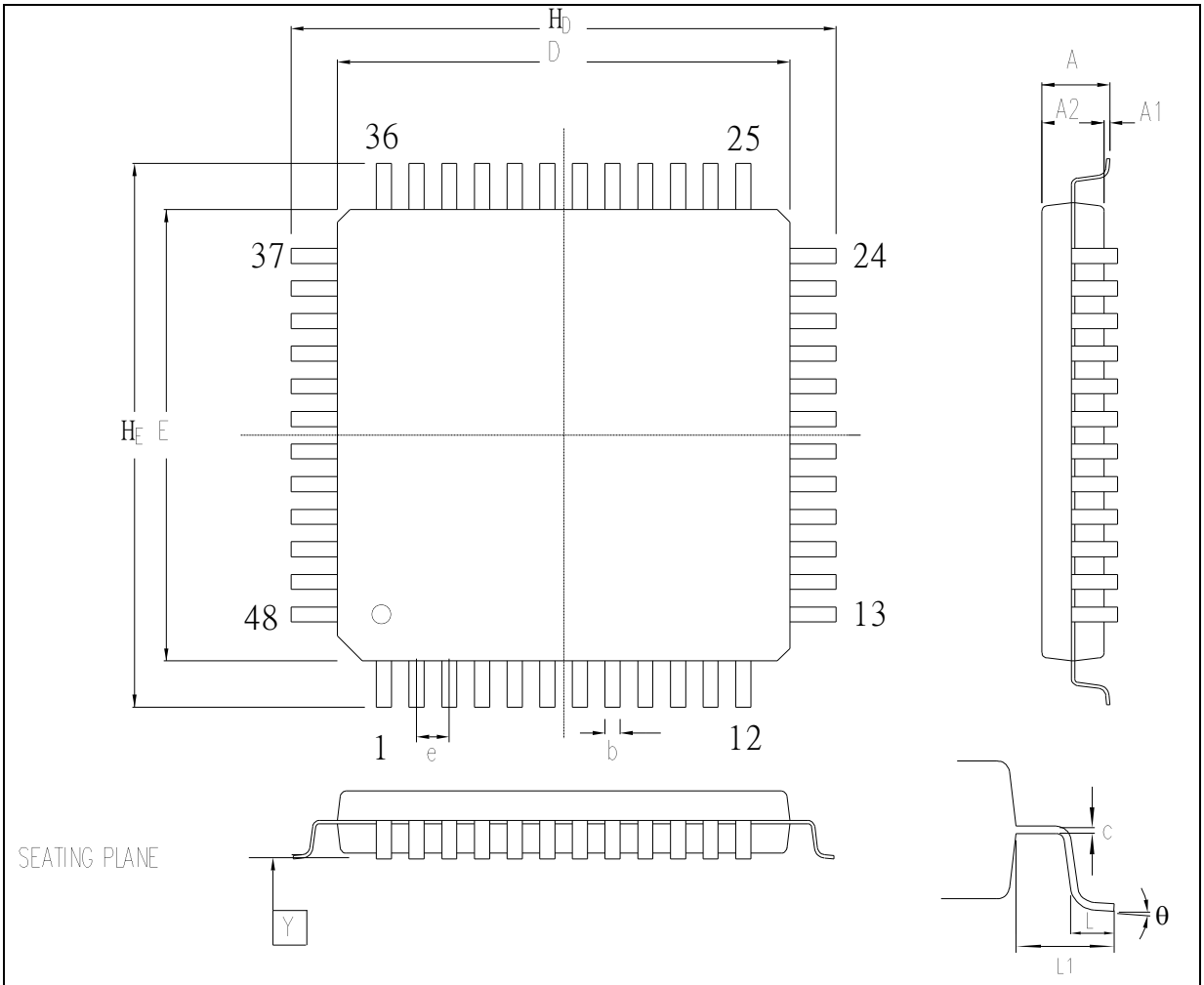
Parameter	Condition	Min	Typ	Max	Unit
Sample Rate				5	MHz
Resolution			13		bit
Output Voltage Swing	V_{DDSPK}=4.5V			V_{DDSPK}	V

6.4.7 DPWM

Parameter	Condition	Min	Typ	Max	Unit
Output Power				500	mW
Load Impedance			8		Ω
Switching Frequency	Derived from 49.152 MHz clock	126		1890	KHz
Bandwidth			16		KHz
THD+N	No Load / Load		-60 / -40		dB

7 PACKAGE DIMENSIONS

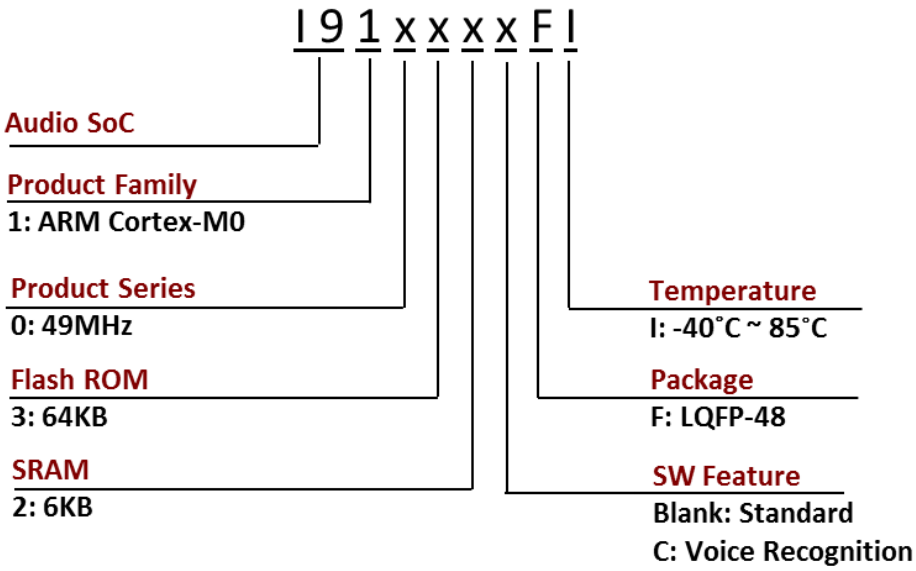
7.1 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8 ORDERING INFORMATION



9 REVISION HISTORY

Version	Date	Substantial Changes	Page
A1.21	Nov 2016	Initial Release (Preliminary)	-
A1.22	Dec 2016	Update Analog Characteristics	18
A1.23	Apr 2019	Add note to remind the damage when enable both DAC and DPWM together	4
A1.24	May 2019	Add note for GPA12 sensitive to noise when pin floating, and will cause IC hang-up	10
A1.25	Nov 2019	Change cover title Change header & footer title Change Cortex™ to Cortex® Change 13-bit DAC content Add Package Dimensions	-

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