

ISD1800 SERIES

**SINGLE-CHIP, SINGLE-MESSAGE
VOICE RECORD/PLAYBACK DEVICE
6- TO 16-SECOND DURATION**

1. GENERAL DESCRIPTION	3
2. FEATURES	3
3. BLOCK DIAGRAM	4
4. PIN CONFIGURATION	5
5. PIN DESCRIPTION.....	6
6. FUNCTIONAL DESCRIPTION	9
6.1. Detailed Description	9
6.2. Functional Description Example.....	10
7. TIMING DIAGRAMS	12
8. ABSOLUTE MAXIMUM RATINGS ^[1]	16
8.1. Operating Conditions.....	17
9. ELECTRICAL CHARACTERISTICS.....	18
9.1. DC Parameters	18
9.2. AC Parameters ^[1]	19
10. TYPICAL APPLICATION CIRCUIT	20
11. PACKAGE DRAWING AND DIMENSIONS.....	22
11.1. 28-Lead 300mil Small Outline IC (SOIC) Package – Samples Only	22
11.2. 28-Lead 600mil Plastic Dual Inline Package (PDIP) – Samples Only	23
11.3. ISD1800 Bonding Physical Layout (Die).....	24
12. ORDERING INFORMATION	25
13. VERSION HISTORY	26

1. GENERAL DESCRIPTION

Nuvoton's ISD1800 ChipCorder[®] provides high-quality, single chip, single-message, record/playback solution with user-selectable durations of 6 to 16 seconds. The CMOS devices include an on-chip oscillator (with external control), microphone preamplifier, automatic gain control, anti-aliasing filter, multilevel storage array, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passive components, two push buttons, and a power source. Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Nuvoton's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

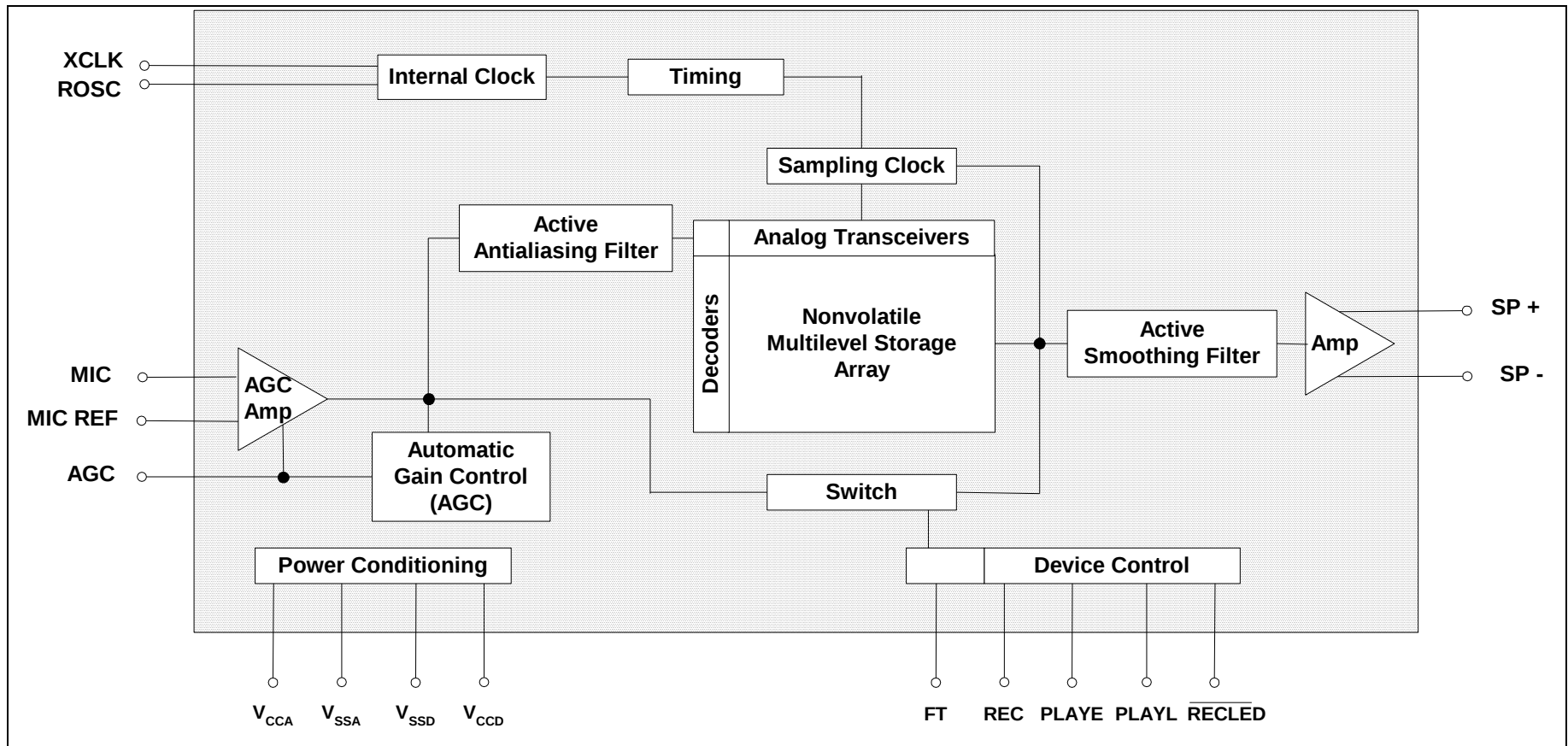
2. FEATURES

- Easy-to-use single-chip, single-message voice record/playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
 - Playback can be edge- or level-activated
- Variable record/playback duration controlled by external resistor selection, which sets sample rate.

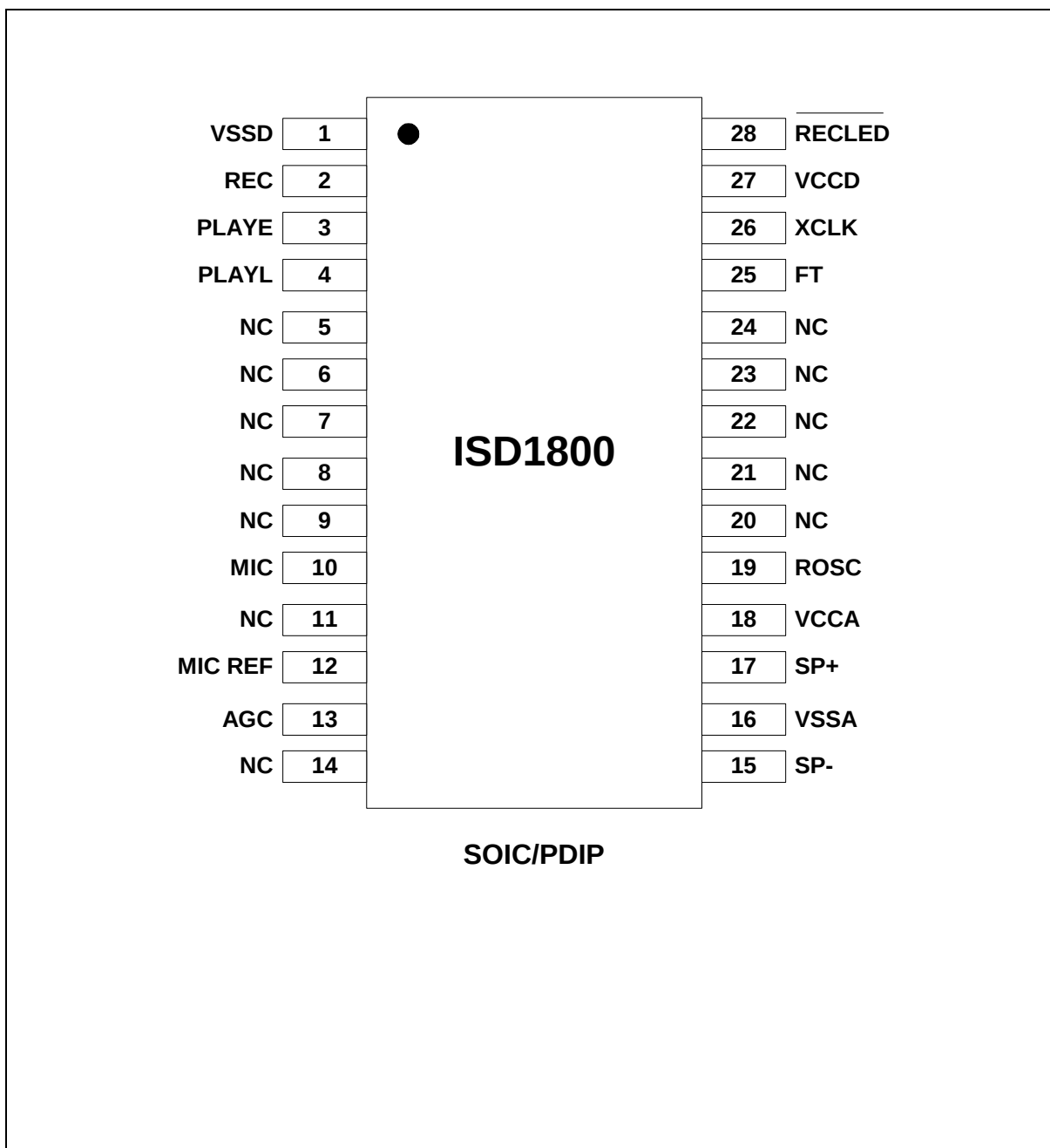
Sample Rate Duration	8 KHz	6.4 KHz	5.3 KHz	4 HKz
I1806	6 secs	7.5 secs	9 secs	12 secs
I1810	8 secs	10 secs	12 secs	16 secs
ROSC	80 K Ω	100 K Ω	120 K Ω	160 K Ω

- Automatic power-down mode
 - Enters standby mode immediately following a record or playback cycle
 - 0.5 μ A standby current (typical)
- On-chip 8 Ω speaker driver
- Zero-power message storage
 - Eliminates battery backup circuits
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip oscillator
- No algorithm development required
- Single +3 volt power supply
- Available in die form
 - 28-pin 300mil SOIC available for samples only
 - 28-pin 600mil PDIP available for samples only

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

PIN NAME	PIN NO.	I/O	FUNCTION
V _{SSD} , V _{SSA}	1, 16		Ground Supplies: Similar to V _{CCA} and V _{CCD} , the analog and digital circuits internal to the I1800 device use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.
REC ¹	2	I	Record: The REC input is an active-HIGH record signal. The device records whenever REC is HIGH. This pin must remain HIGH for the duration of the recording. REC takes precedence over either playback (PLAYL or PLAYE) signal. If REC is pulled HIGH during a playback cycle, the playback immediately ceases and recording begins. A record cycle is completed when REC is pulled LOW. An End-of-Message (EOM) marker is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when REC goes LOW. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.
PLAYE	3	I	Playback, Edge-activated: When a HIGH-going transition is detected on this input pin, a playback cycle begins. Playback continues until an End-of-Message (EOM) marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking PLAYE LOW during a playback cycle will not terminate the current cycle. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.
PLAYL	4	I	Playback, Level-activated: When this input pin level transits from LOW to HIGH, a playback cycle is initiated. Playback continues until PLAYL is pulled LOW or an End-of-Message (EOM) marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.
NC	5, 6, 7, 8, 9, 11, 14, 20, 21, 22, 23, 24		Not Connected.

PIN NAME	PIN NO.	I/O	FUNCTION
MIC	10	I	Microphone Input: The microphone input transfers its signals to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of the preamplifier. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with an internal 10 K Ω resistance on this pin, determines the low-frequency cutoff for the I1800 passband.
MIC REF	12	I	Microphone Reference: The MIC REF input is the inverting input to the microphone preamplifier. This provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device.
AGC	13	I	Automatic Gain Control: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. Nominal values of 4.7 μ F give satisfactory results in most cases. Connecting this pin to ground (V_{SSA}) provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to the power supply (V_{CCA}) provides minimum gain to the preamplifier circuitry.
SP-/SP+	15, 17	O	Speaker Outputs: The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 8 Ω . A single output may be used, but, for direct-drive loud-speakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP- are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The SP+ pin and the SP- pin are internally connected through a 50 K Ω resistance. When not in playback mode, they are floating.

ISD1800 SERIES

nuvoTon

PIN NAME	PIN NO.	I/O	FUNCTION
V _{CCA} , V _{CCD}	18, 27		Voltage Supplies: Analog and digital circuits internal to the I1800 device use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the power supply as possible. It is important that the power supply be decoupled as close as possible to the package.
ROSC	19	I	The Resistor Controlled Oscillator input: This enables the user to vary the I1800 device record and playback duration. The resistor connected between the ROSC pin and V _{SS} (R2) determines the sample frequency and the filter upper pass band for the I1800 device. Please refer to the table in Duration Section for duration selection.
FT	25	I	Feed Through: This mode allows use of the speaker drivers for external signals. The signal between the MIC and MIC_REF pins will pass through the AGC, the filter and the speaker drivers to the speaker outputs SP+ and SP-. The input FT controls the feed through mode. To operate this mode, the control pins REC, PLAYE and PLAYL are held LOW at V _{SS} . The pin FT is held HIGH to V _{CC} . For normal operation of record, play and power down, the FT pin is held at V _{SS} . The FT pin has a weak pull-down to V _{SS} .
XCLK	26		The External Clock input: For the I1800 devices has an internal pull-down resistor. This pin is used for test purposes only. Do not bond this pad.
RECLED	28	O	Record LED output: The RECLED output is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, RECLED pulses LOW momentarily when an End-of-Message (EOM) or end-of-memory marker is encountered in a playback cycle.

Note: ¹ The REC signal is internally debounced on the rising edge to prevent a false re-triggering from a push-button switch.

Publication Release Date: Jan 15, 2016

Revision 1.0

6. FUNCTIONAL DESCRIPTION

6.1. DETAILED DESCRIPTION

Speech/Sound Quality

Nuvoton's patented ChipCorder® technology provides natural record and playback. The input voice signals are stored directly in nonvolatile cells and are reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a single message.

Duration

The ISD1800 devices offer single-chip solutions with 6 to 16 seconds of record/playback duration capacity. Sampling rate and duration are determined by an external resistor connected to the ROSC pin. These specifications apply with the required resistor value for playback duration.

Sample Rate Duration	8 KHz	6.4 KHz	5.3 KHz	4 HKz
I1806	6 secs	7.5 secs	9 secs	12 secs
I1810	8 secs	10 secs	12 secs	16 secs
ROSC	80 KΩ	100 KΩ	120 KΩ	160 KΩ

Non-Volatile Storage

The ISD1800 product utilizes the on-chip Flash memory providing zero-power message storage. The message is retained for up to 100 years without power. In addition, the device can be re-recorded typically over 100,000 times.

Basic Operation

The ISD1800 ChipCorder® device is controlled by the REC pin, and either of two playback pins, PLAYE (edge-activated playback), and PLAYL (level-activated playback). The ISD1800 parts are configured for design simplicity in a single-message application. Device operation is explained in section 7.2, "Functional Description Example".

Automatic Power-Down Mode

At the end of a playback or record cycle, the ISD1800 device automatically returns to a low-power standby mode, consuming typically 0.5μA, provided that Play REC, XCLK, and FT pins are LOW (see DC parameters, section 10). During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after REC is released LOW.

6.2. FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1800 devices.

1. Record a message filling the memory

Pulling the REC pin HIGH initiates a record cycle from the beginning of the message space. The device will automatically power down after REC is release LOW. An EOM marker is written at the end of message. If REC is held HIGH, the recording continues until the message space has been filled. Once the message space is filled, recording ceases.

2. Edge-activated playback

Pulling the PLAYE pin HIGH initiates a playback cycle from the beginning of the message space. When the device reaches the EOM marker, it automatically powers down. If a recording has filled the message space, the entire message is played. A subsequent rising edge on PLAYE initiates a new play cycle from the beginning of the memory.

3. Level-activated playback

Pulling the PLAYL pin HIGH initiates a playback cycle from the beginning of the message space. When the device reaches the EOM marker, it automatically powers down. If a recording has filled the message space, the entire message is played. A subsequent rising edge on PLAYL initiates a new play cycle from the beginning of the memory.

4. Level-activated playback (truncated)

If PLAYL is pulled LOW any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent rising edge on PLAYL initiates a new play cycle from the beginning of the memory.

5. Record (interrupting playback)

The REC pin takes precedence over other operations. Any HIGH-going transition on REC initiates a new record operation from the beginning of the memory, regardless of any current operation in progress.

6. Record a message, partially filling the memory

A record operation need not fill the entire memory. Releasing the REC pin LOW before filling the message space causes the recording to stop and an EOM marker to be placed. The device powers down automatically.

7. Playback a message that partially fills the memory

Pulling the PLAYE or PLAYL pin HIGH initiates a playback cycle. The playback cycle ceases when the EOM marker is encountered and the device then powers down.

8. RECLED operation

The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal, which can be used to drive an LED as a “record-in-progress” indicator. It returns to a HIGH state when the REC pin is released LOW or when the recording is completed due to the memory being filled. This pin also pulses LOW to indicate the end of a message has been reached.

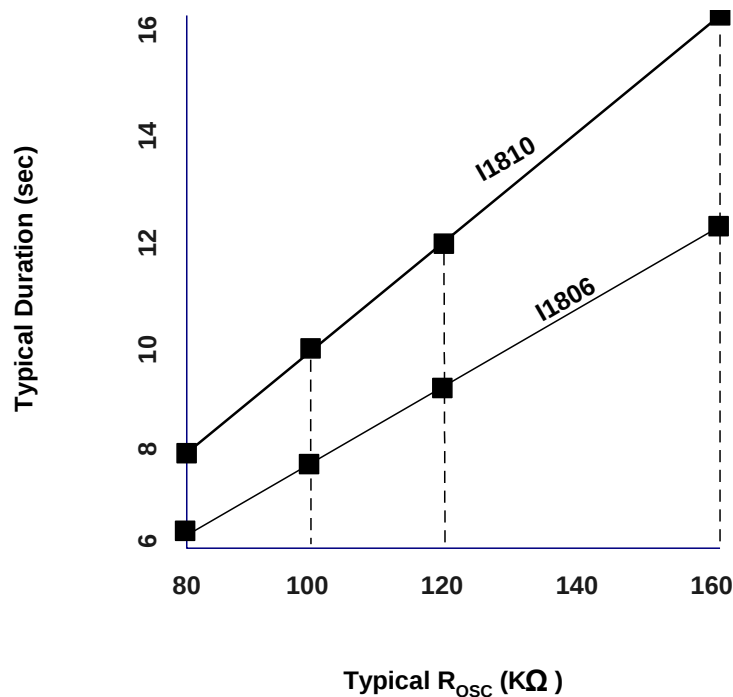
9. ROSC operation

The duration of the device can be varied by changing the value of R2 (R_{OSC}). This means the ISD1800 device can actually be between 6 to 16 seconds duration. See the curve below, which charts typical durations when the R_{OSC} is varied from 80 K Ω to 160 K Ω .

This feature allows frequency shifting where a recorded voice or sound can be played back faster or slower than normal for special effects. For example, use a 100 K Ω resistor to make the recording and then playback with either an 80 K Ω resistor for faster “chipmunk” talk or with a 120 K Ω resistor for a slower, lower voice.

Another feature is a “Pause” or interrupt function that can be done by taking the R_{OSC} resistor to V_{CC} to stop playback momentarily, resuming when the resistor is connected back to ground.

Chart 1: ISD Duration Versus R_{OSC} at $T_A = 25^\circ\text{C}$ and $V_{\text{CC}} = 3.0\text{V}$



7. TIMING DIAGRAMS

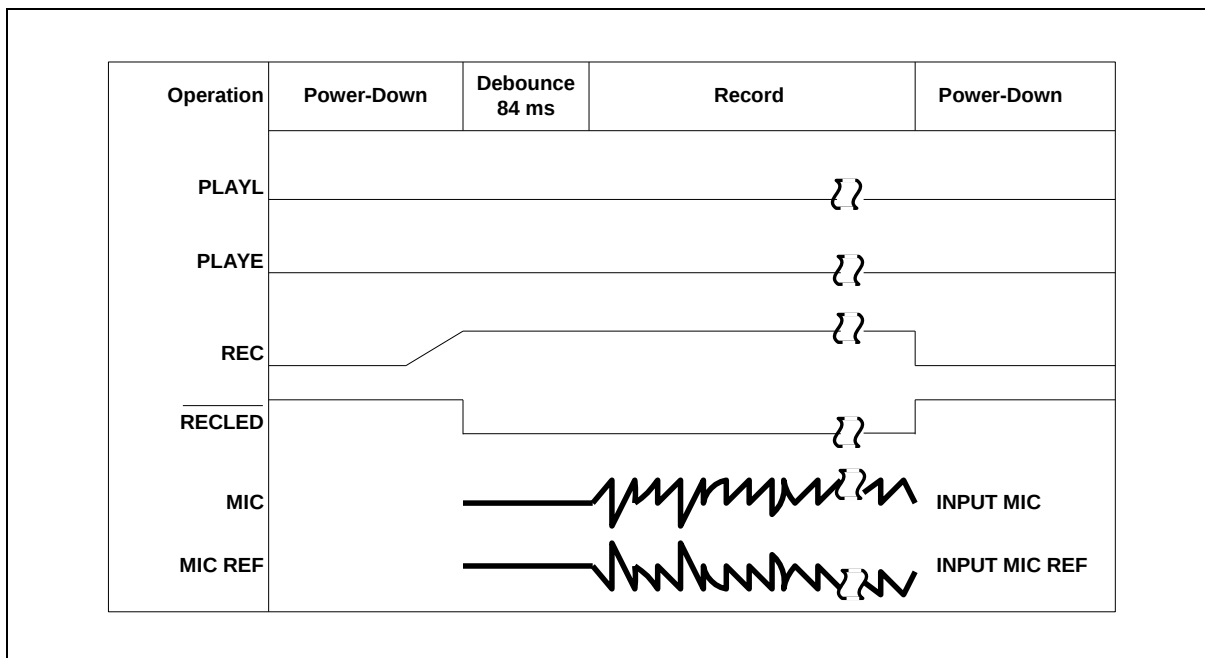


FIGURE 1: RECORD MESSAGE UNTIL RECORD GOES LOW

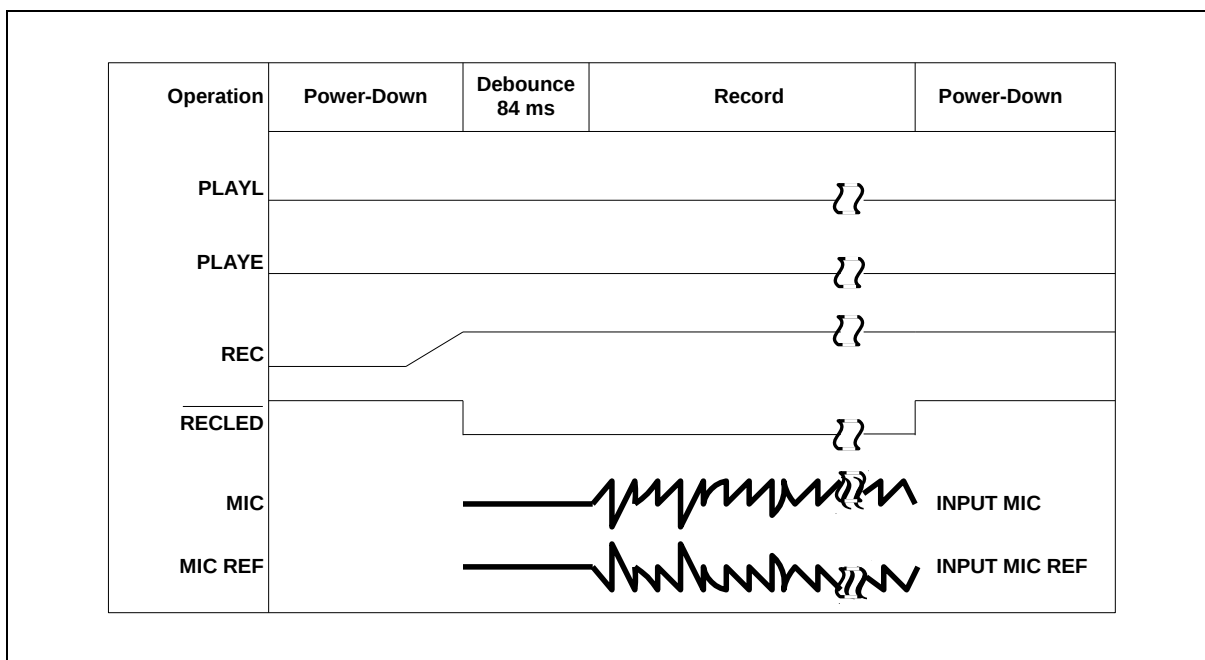


FIGURE 2: RECORD MESSAGE UNTIL ARRAY IS FULL

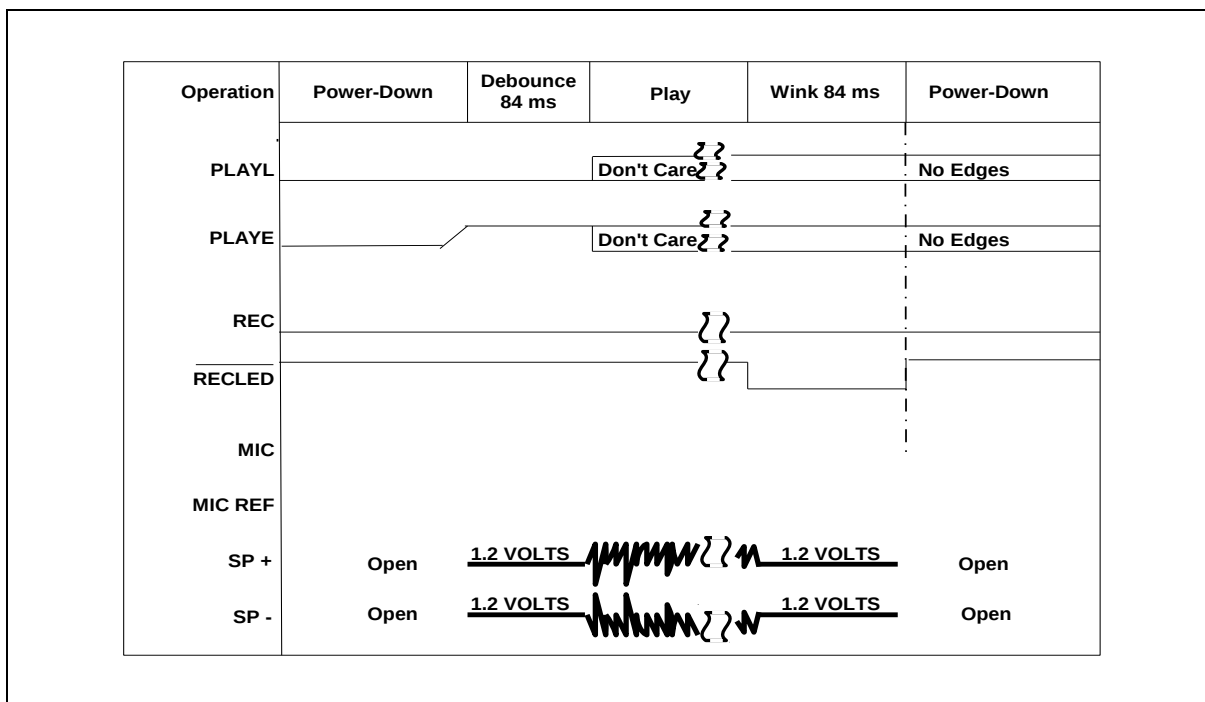


FIGURE 3: PLAY EDGE (PLAYE) PLAY UNTIL END OF MESSAGE

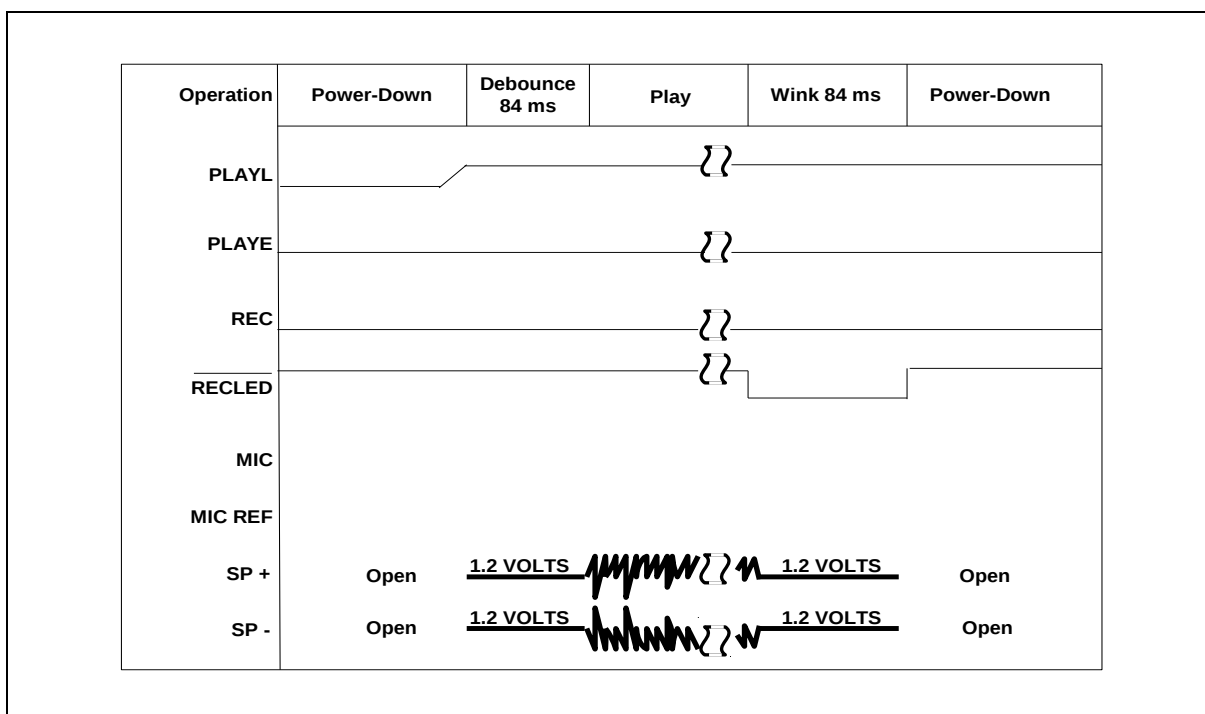


FIGURE 4: PLAY LEVEL (PLAYL) PLAY UNTIL END OF MESSAGE

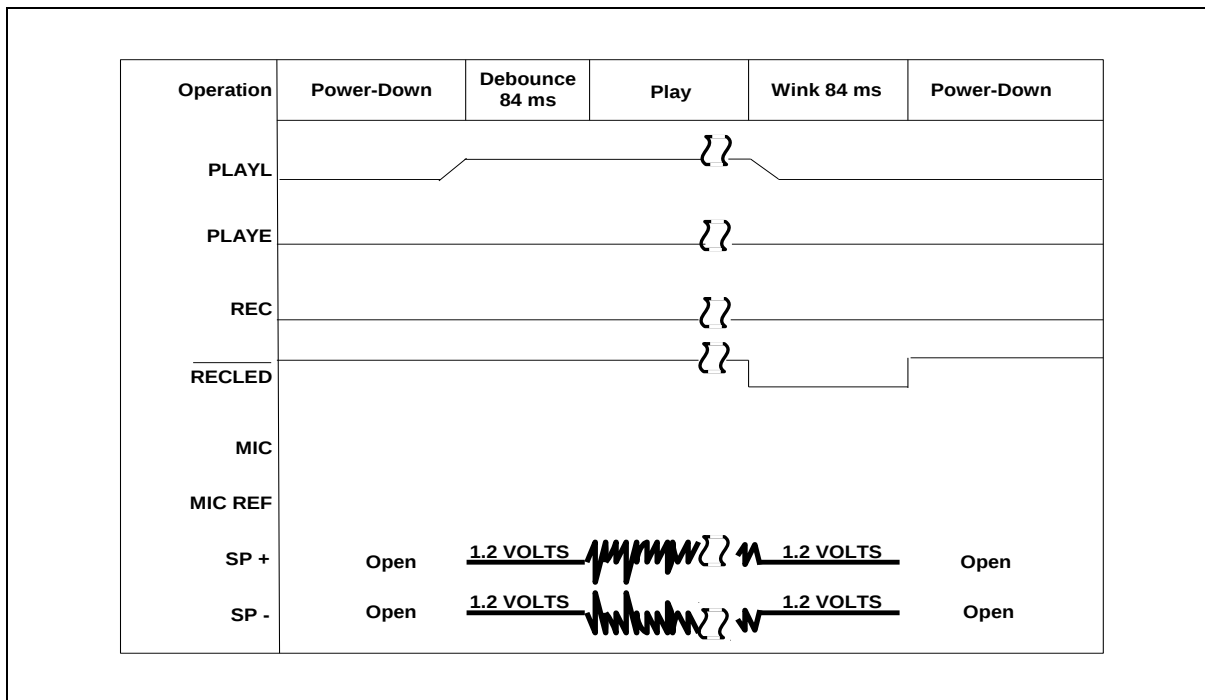


FIGURE 5: PLAY UNTIL PLAY LEVEL (PLAYL) FALLS

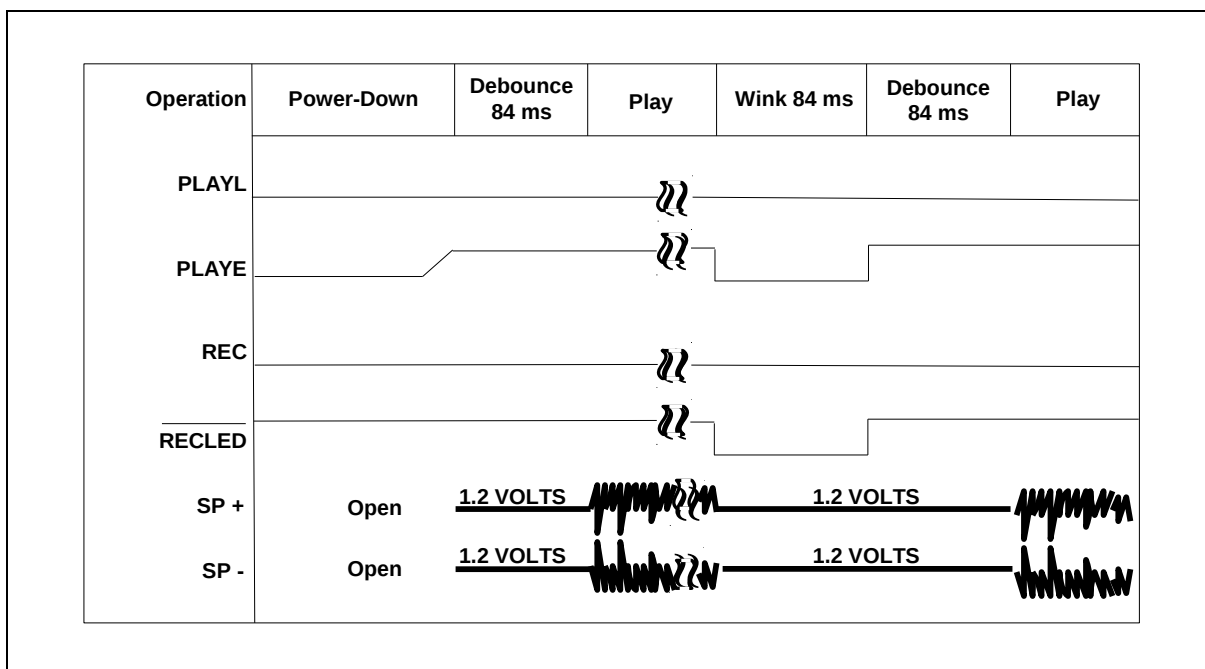


FIGURE 6: LOOPING PLAY, PLAYE TO RECLED

Note: Looping playback operation can be performed by connecting the RECLED pin to PLAYE pin.

8. ABSOLUTE MAXIMUM RATINGS ^[1]

ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V _{SS} -0.3V) to (V _{CC} +0.3V)
V _{CC} - V _{SS}	-0.3V to +7.0V

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V _{SS} -0.3V) to (V _{CC} +0.3V)
Lead temperature (Soldering – 10sec)	300°C
V _{CC} - V _{SS}	-0.3V to +7.0V

^[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

8.1. OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITION	VALUE
Operating temperature range	0°C to +50°C
Play voltage (V_{CC}) ^[1]	+2.7V to +4.5V
Ground voltage (V_{SS}) ^[2]	0V
Record Supply voltage (V_{CC}) ^[1]	+2.7V to 4.5V

OPERATING CONDITIONS (PACKAGED PARTS)

CONDITION	VALUE
Commercial operating temperature range (Case temperature)	0°C to +70°C
Play voltage (V_{CC}) ^[1]	+2.7V to +4.5V
Ground voltage (V_{SS}) ^[2]	0V
Record Supply voltage (V_{CC}) ^[1]	+2.7V to 4.5V

^[1] $V_{CC} = V_{CCA} = V_{CCD}$

^[2] $V_{SS} = V_{SSA} = V_{SSD}$

9. ELECTRICAL CHARACTERISTICS

9.1. DC PARAMETERS

PARAMETER	SYMBOL	MIN ^[2]	TYP ^[1]	MAX ^[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 4.0 \text{ mA}$ ^[3]
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -1.6 \text{ mA}$ ^[3]
V_{CC} Current (Operating)	I_{CC}			30	mA	$V_{CC} = 4.5\text{V}$
V_{CC} Current (Standby)	I_{SB}		0.5	10	μA	^[4] ^[5]
Input Leakage Current	I_{ILPD1}			± 1	μA	Force V_{SS} ^[6]
Input Current HIGH	I_{ILPD2}	30	150	400	μA	Force V_{CC} ^[7]
Input Current HIGH	I_{ILPD3}	3		130	μA	Force V_{CC} ^[8]
Output Load Impedance	R_{EXT}	8			Ω	Speaker Load, SP+ to SP-
Preamp Input Resistance	R_{MIC}, R_{MICREF}		10		K Ω	
MIC SP+/- Gain	A_{MSP}		40		dB	AGC = 0.0V

Notes:

^[1] Typical values @ $T_A = 25^\circ$ and $V_{CC} = 3.0\text{V}$.

^[2] All Min/Max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

^[3] Record LED output, $RECLED$.

^[4] V_{CCA} and V_{CCD} connected together.

^[5] REC, PLAYL, PLAYE, XCLK, and FT must be at V_{SSD} .

^[6] REC, PLAYL and PLAYE.

^[7] REC, PLAYL and PLAYE.

^[8] Test limits of Final Test.

9.2. AC PARAMETERS^[1]

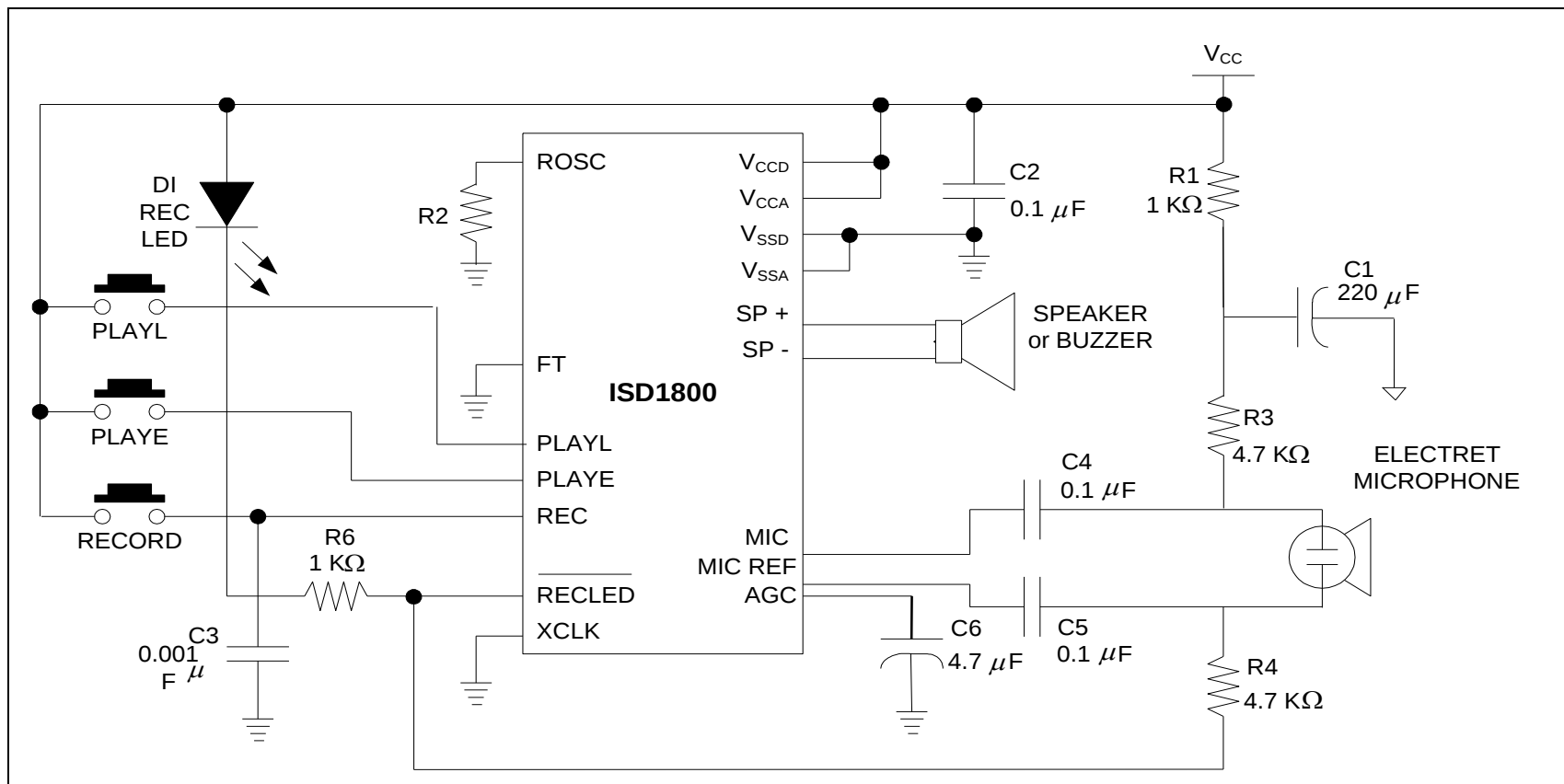
CHARACTERISTIC	SYMBOL		MIN ^[3]	TYP ^[2]	MAX ^[3]	UNITS	CONDITIONS
Sampling Frequency	F_S			8		KHz	^[4]
Filter Pass Band	F_{CF}	ISD1806		2.2		KHz	3 dB Roll-Off Point $R_{OSC} = 100\text{ K}\Omega$ ^{[5][6]}
		ISD1810		2.2			
Record Duration	T_{REC}	ISD1806		7.5		sec	$R_{OSC} = 100\text{ K}\Omega$ ^[4]
		ISD1810		10			
Playback Duration	T_{PLAY}	ISD1806		7.5		sec	$R_{OSC} = 100\text{ K}\Omega$ ^[4]
		ISD1810		10			
EOM Pulse Width	T_{EOM}			84		msec	
Debounce Time	T_{DB}			84		msec	
Total Harmonic Distortion	THD			1		%	@ 1KHz, $V_{IN}=15\text{mV}$ pk-to-pk
Speaker Output Power	P_{OUT}			24.4		mW	$R_{EXT} = 8\Omega$
Voltage Across Speaker Pins	V_{OUT}			1.25	2.5	Vp-p	$R_{EXT} = 600\Omega$
MIC Input Voltage				15	300	mV	Peak-to-Peak ^[7]

Notes:

- ^[1] These specifications apply with $R_{OSC} = 100\text{ K}\Omega$, unless stated.
- ^[2] Typical values @ $T_A = 25^\circ$ and $V_{CC} = 3.0\text{V}$.
- ^[3] All Min/Max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.
- ^[4] Oscillator stability may vary as much as $\pm 5\%$ over the operating temperature and voltage ranges. (Only the 7.5 sec duration of I1806 and 10 sec duration of I1810 are tested/guaranteed)
- ^[5] Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions)
- ^[6] Filter specification applies to the anti-aliasing filter and to the smoothing filter.
- ^[7] Balanced input signal applied between MIC and MIC REF as shown in the applications example. Single-ended MIC or MIC REF recommended to be less than 100 mV peak to peak.

10. TYPICAL APPLICATION CIRCUIT

Typical application circuit (1)

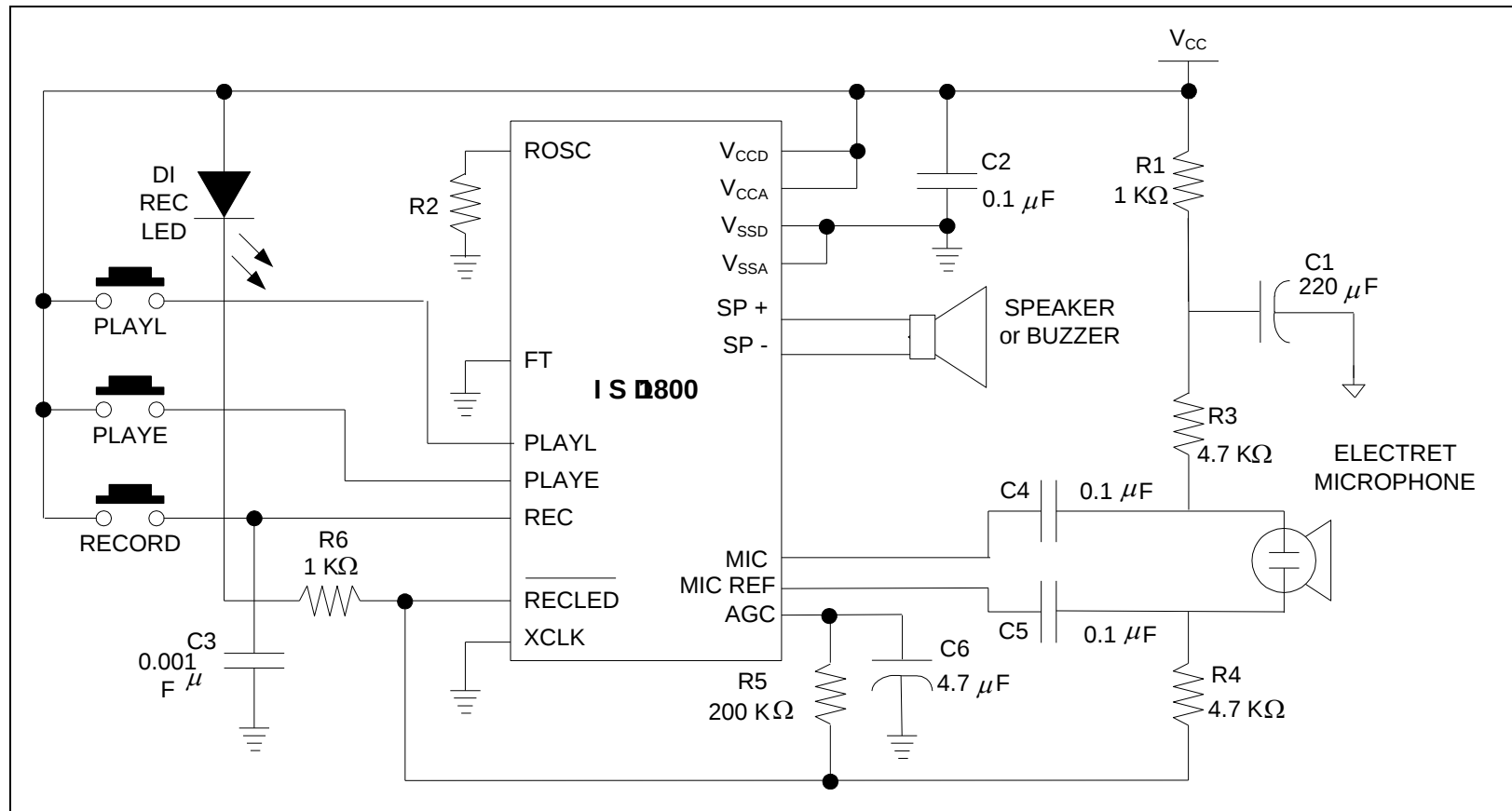


ISD1800 SERIES

nuvoTon

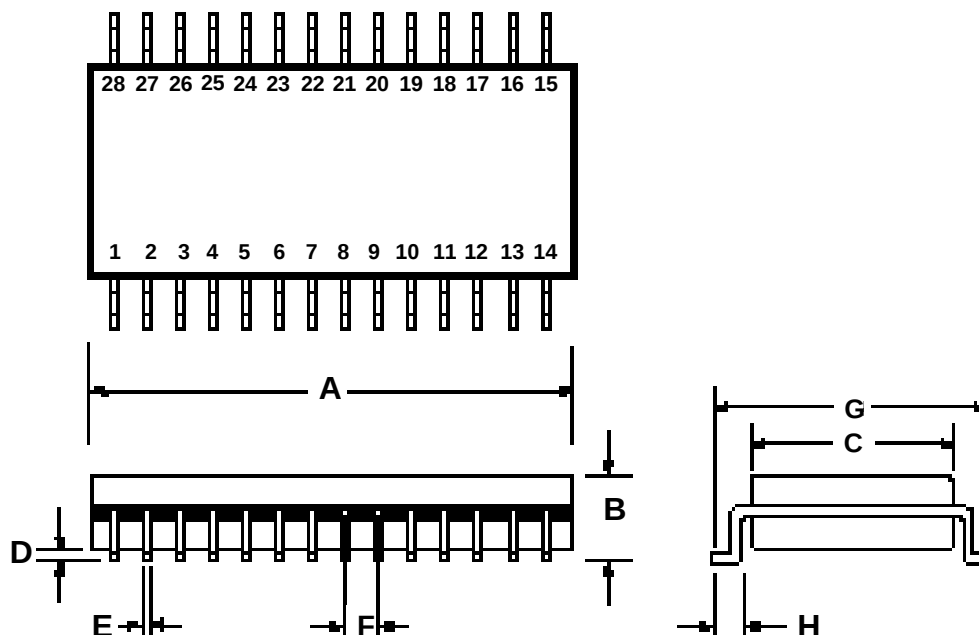
Alternate application circuit (2)

This circuit forces AGC high before recording, and low after recording is started. So when recording device always starts from recording silence and then keeps recording at high signal input level. Thus avoids feeding excessive strong signal to the device at beginning, while maintains high level recording after. This circuit delivers higher playback volume.



11. PACKAGE DRAWING AND DIMENSIONS

11.1. 28-LEAD 300MIL SMALL OUTLINE IC (SOIC) PACKAGE – SAMPLES ONLY



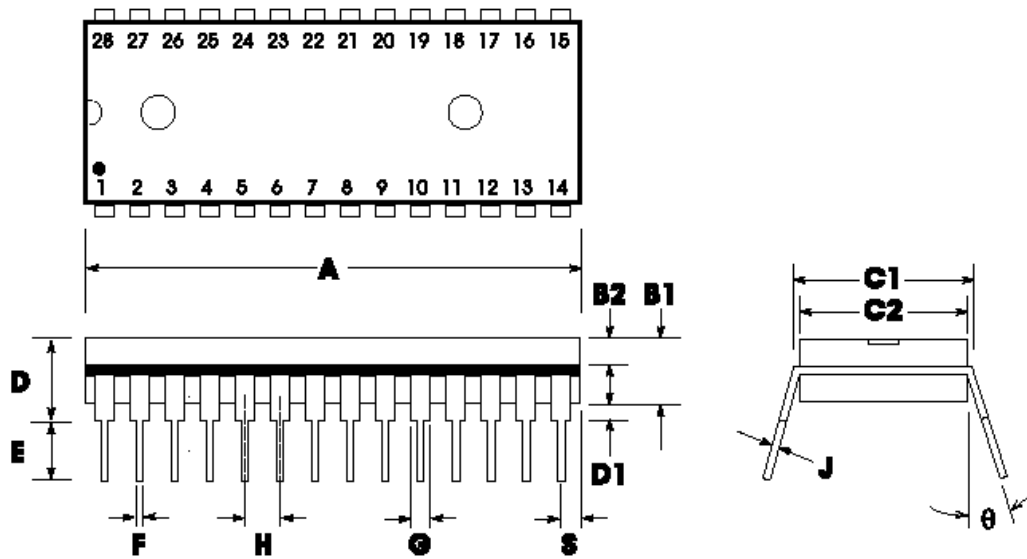
	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.016	0.35	0.41	0.48
F		0.050			1.27	0
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: Lead coplanarity to be within 0.004 inches.

ISD1800 SERIES

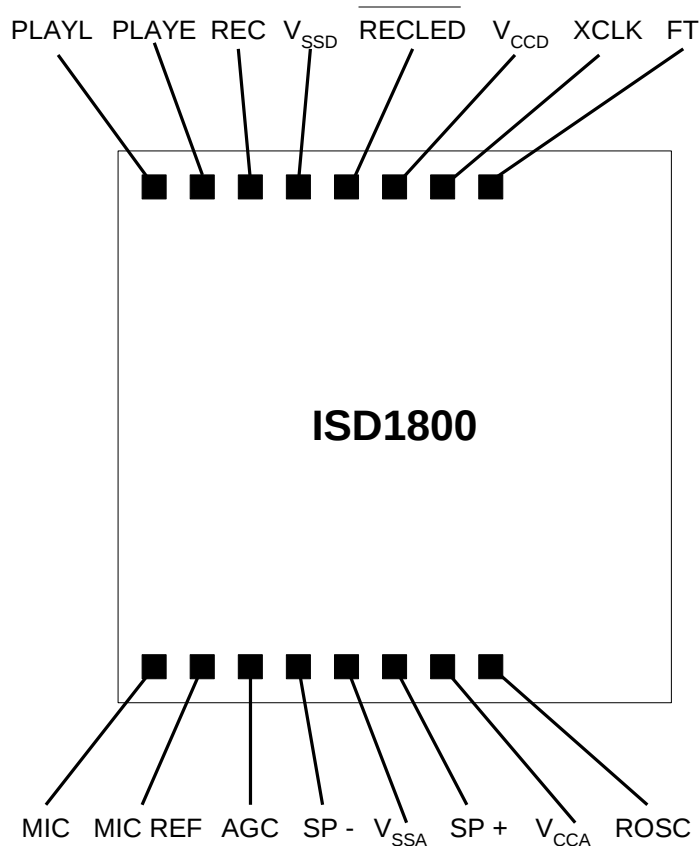
nuvoTon

11.2. 28-LEAD 600MIL PLASTIC DUAL INLINE PACKAGE (PDIP) – SAMPLES ONLY



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.62
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

11.3. ISD1800 BONDING PHYSICAL LAYOUT (DIE)

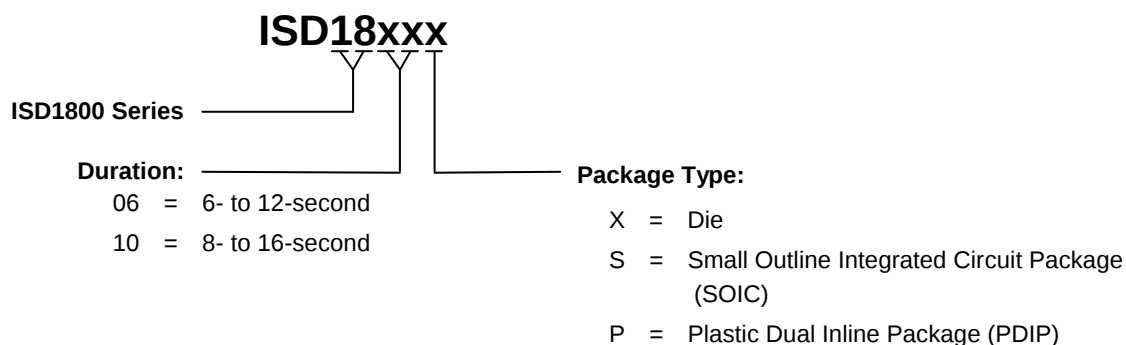


Notes:

1. The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.
2. Die thickness is subject to change, please contact Nuvoton factory for status and availability.

12. ORDERING INFORMATION

Product Number Descriptor Key



When ordering, please refer to the following part numbers that are supported in volume for this product series. Consult the local Nuvoton Sales Representative or Distributor for availability information.

Package	Part Number	Ordering Number	Comments
Die	ISD1806X	I1806X	
SOIC	ISD1806S	I1806S	Samples Only
PDIP	ISD1806P	I1806P	Samples Only
Die	ISD1810X	I1810X	
SOIC	ISD1810S	I1810S	Samples Only
PDIP	ISD1810P	I1810P	Samples Only

For the latest product information, access Nuvoton's worldwide website at <http://www.Nuvoton-usa.com>

13. VERSION HISTORY

VERSION	DATE	DESCRIPTION
0.0	May 2003	Preliminary Specifications. Create one datasheet for both I1806 and I1810 products. Revise duration section with both products. Change filter passband values from 2.6 kHz to 2.2kHz in AC Parameters section.
0.1	Mar 2005	Revise series name from I1800 to ISD1800 Update block diagram Revise AGC in pin description Revise the MIC and MIC REF polarity in applications diagram Update die information section Update the ordering information section Update the disclaim section
0.2	Apr 2005	Revise record cycles info in feature and storage sections Update the disclaim section
0.3	Jun 2005	Revise Pout and Vout data in AC Parameters section
0.31	Oct 17, 2008 Nov 7, 2008	Change logo Update Typical Application Circuit in Section 10
0.32	Dec 1, 2008	SOIC available on samples only Revise Bonding Physical Layout
1.0	Jan 15, 2016	Add alternate application circuit

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

The contents of this document are provided only as a guide for the applications of Nuvoton products. Nuvoton makes no representation or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice. No license, whether express or implied, to any intellectual property or other right of Nuvoton or others is granted by this publication. Except as set forth in Nuvoton's Standard Terms and Conditions of Sale, Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property.

The contents of this document are provided "AS IS", and Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property. In no event, shall Nuvoton be liable for any damages whatsoever (including, without limitation, damages for loss of profits, business interruption, loss of information) arising out of the use of or inability to use the contents of this documents, even if Nuvoton has been advised of the possibility of such damages.

Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Nuvoton makes no representation or warranty that such applications shall be suitable for the use specified.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Nuvoton Reliability Report, and are neither warranted nor guaranteed by Nuvoton. This product incorporates SuperFlash®.

Information contained in this ISD® ChipCorder® datasheet supersedes all data for the ISD ChipCorder products published by ISD® prior to August, 1998.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

Copyright© 2005, Nuvoton Technology Corporation. All rights reserved. ChipCorder® and ISD® are trademarks of Nuvoton Technology Corporation. SuperFlash® is the trademark of Silicon Storage Technology, Inc. All other trademarks are properties of their respective owners.

Headquarters

No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.Nuvoton.com.tw/>

Nuvoton Technology Corporation America

2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
<http://www.Nuvoton-usa.com/>

Nuvoton Technology (Shanghai) Ltd.

27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office

9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Nuvoton Technology Corporation Japan

7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokukyu,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Nuvoton Technology (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.

Publication Release Date: Jan 15, 2016

Revision 1.0