128K x36/32 and 256K x18 4Mb, ECC, PIPELINE 'NO WAIT' STATE BUS SYNCHRONOUS SRAM

AUGUST 2019

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- /CKE pin to enable clock and suspend operation
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:
  NLP: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
  NVP: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
- JTAG Boundary Scan for BGA packages
- Industrial and Automotive temperature support
- Lead-free available
- Error Detection and Error Correction

DESCRIPTION

The 4Mb product family features high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 128K words by 36 bits and 256K words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology. Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, /CKE is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

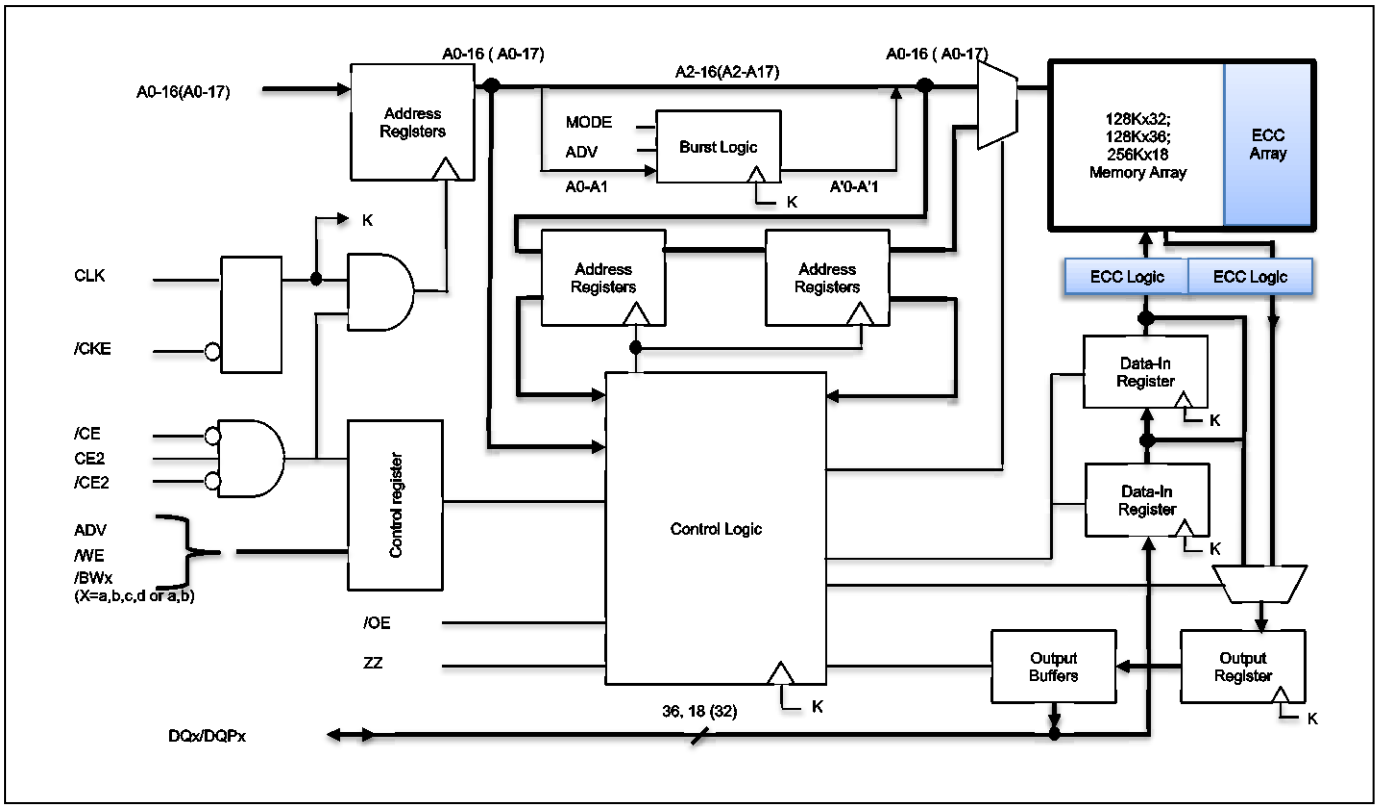
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when /WE is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected

FAST ACCESS TIME

Symbol	Parameter	250	200	Units
t_{KQ}	Clock Access Time	2.6	3.1	ns
t_{KC}	Cycle time	4	5	ns
f_{MAX}	Frequency	250	200	MHz

BLOCK DIAGRAM

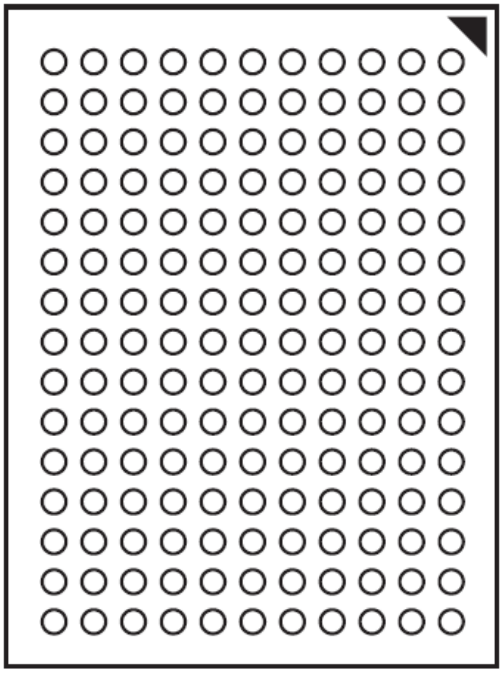


PIN CONFIGURATION

128K x 36, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/CKE	ADV	NC	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/WE	/OE	NC	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array

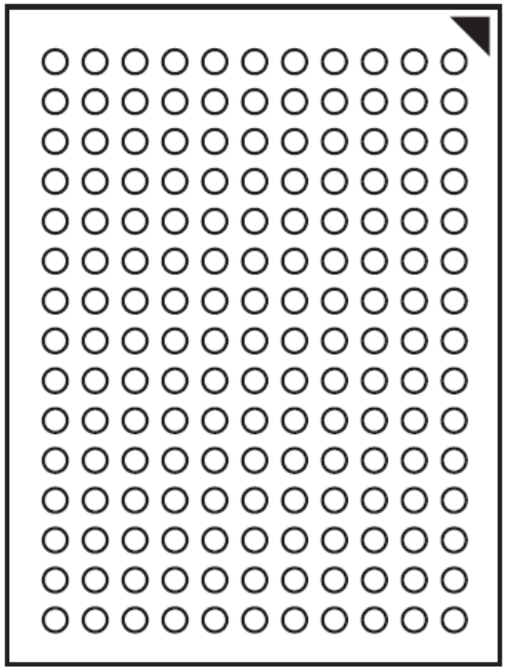
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Advance/Load
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
MODE	Burst Sequence Selection
ZZ	Asynchronous Power Sleep Mode
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

128K x 32, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/CKE	ADV	NC	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/WE	/OE	NC	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array

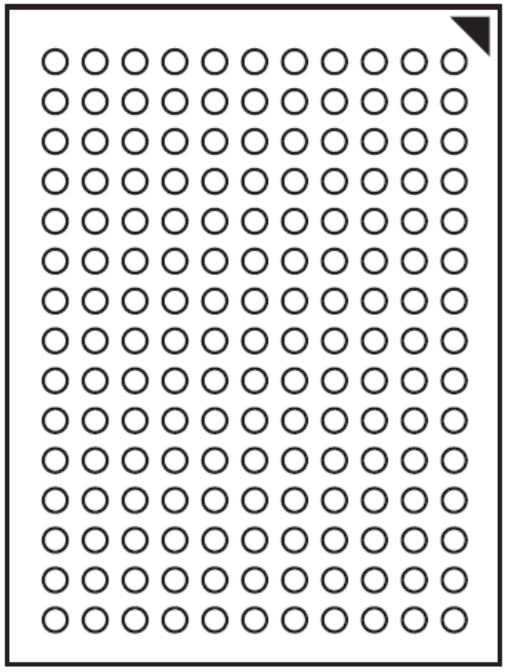
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Advance/Load
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
MODE	Burst Sequence Selection
ZZ	Asynchronous Power Sleep Mode
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

256K x 18, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWb	NC	/CE2	/CKE	ADV	NC	A	A
B	NC	A	CE2	NC	/BWa	CLK	/WE	/OE	NC	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array

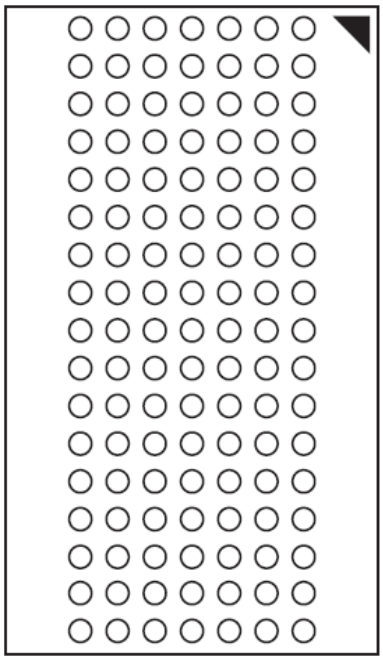
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Advance/Load
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-b)	Synchronous Byte Write Inputs
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
MODE	Burst Sequence Selection
ZZ	Asynchronous Power Sleep Mode
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

128K x 36, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	NC	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/WE	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/CKE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0*	V_{SS}	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
1.27 mm Ball Pitch, 7 x 17 Ball Array

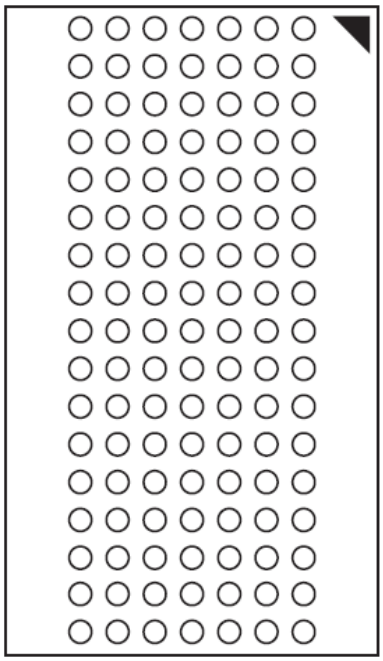
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Advance/Load
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
MODE	Burst Sequence Selection
ZZ	Asynchronous Power Sleep Mode
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

128K x 32, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	NC	V_{SS}	NC	V_{SS}	NC	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	NC	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/WE	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/CKE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	NC	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
1.27 mm Ball Pitch, 7 x 17 Ball Array

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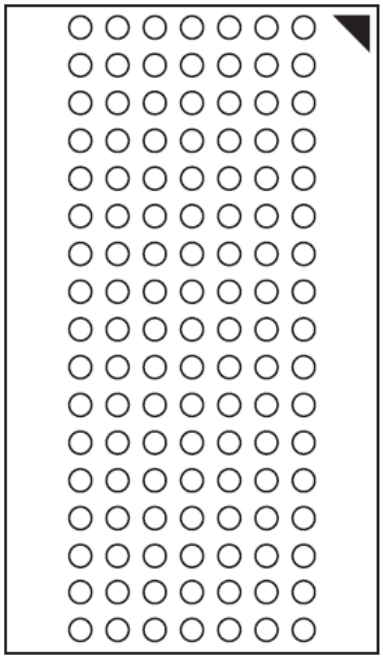
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
MODE	Burst Sequence Selection
ZZ	Asynchronous Power Sleep Mode
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

256K x 18, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	/CE	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	/OE	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	/BWb	NC	NC	NC	DQa
H	DQb	NC	VSS	/WE	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	VSS	CLK	V_{SS}	NC	DQa
L	DQb	NC	NC	NC	/BWa	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	/CKE	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
1.27 mm Ball Pitch, 7 x 17 Ball Array

PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
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DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
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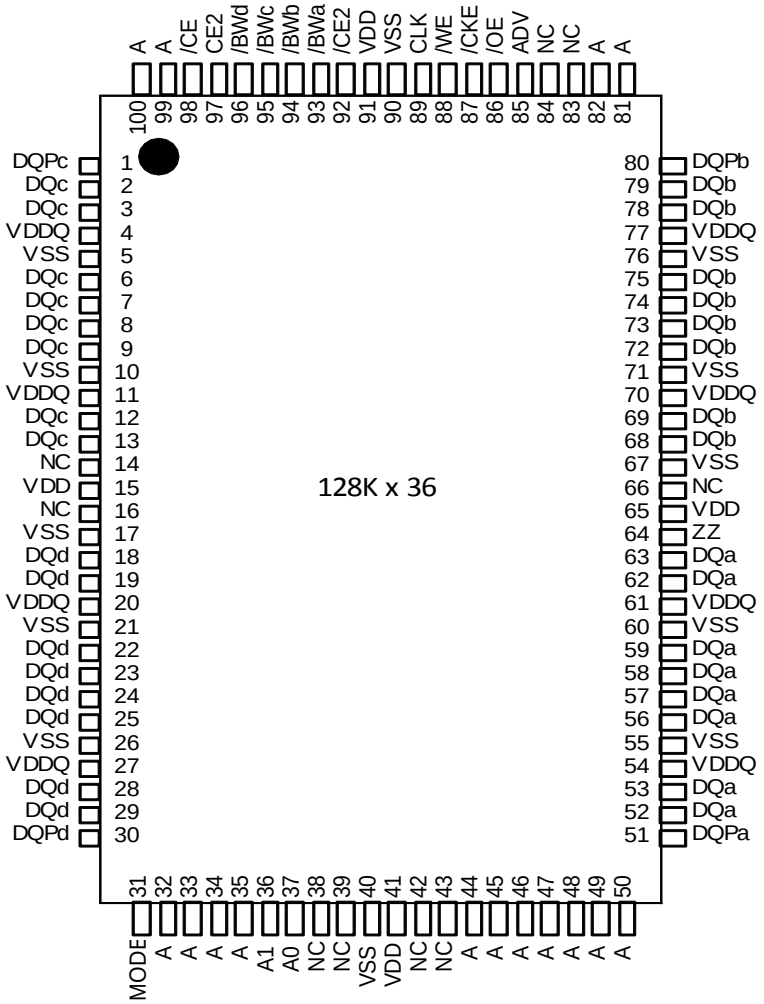
TCK,TDI,TDO,TMS	JTAG Pins
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground
NC	No Connect

128K x 36, 100PIN QFP (Top View)

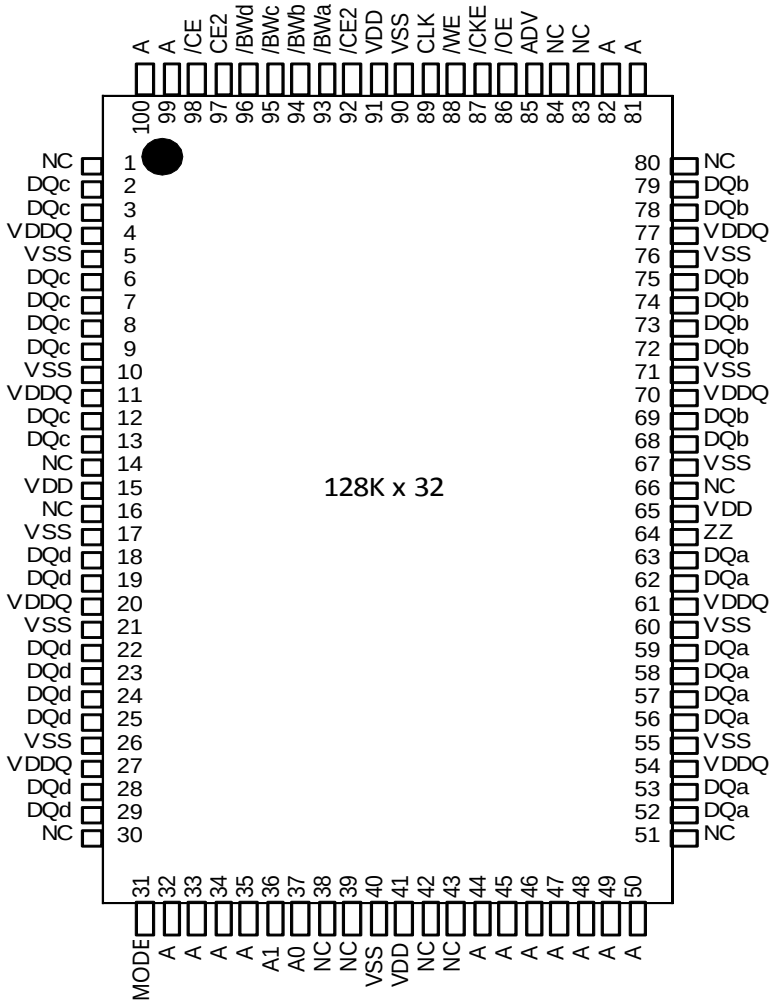


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
A	Synchronous Address Inputs	ZZ	Asynchronous Power Sleep Mode
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	DQx	Synchronous Data I/O
/WE	Synchronous Read/Write Control Input	DQPx	Synchronous Parity Data I/O
CLK	Synchronous Clock	V_{DD}	Power Supply
/CKE	Clock Enable	V_{DDQ}	I/O Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	V_{SS}	Ground
/BWx (x=a-d)	Synchronous Byte Write Inputs	NC	No Connect
/OE	Asynchronous Output Enable		

128K x 32, 100PIN QFP (Top View)



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
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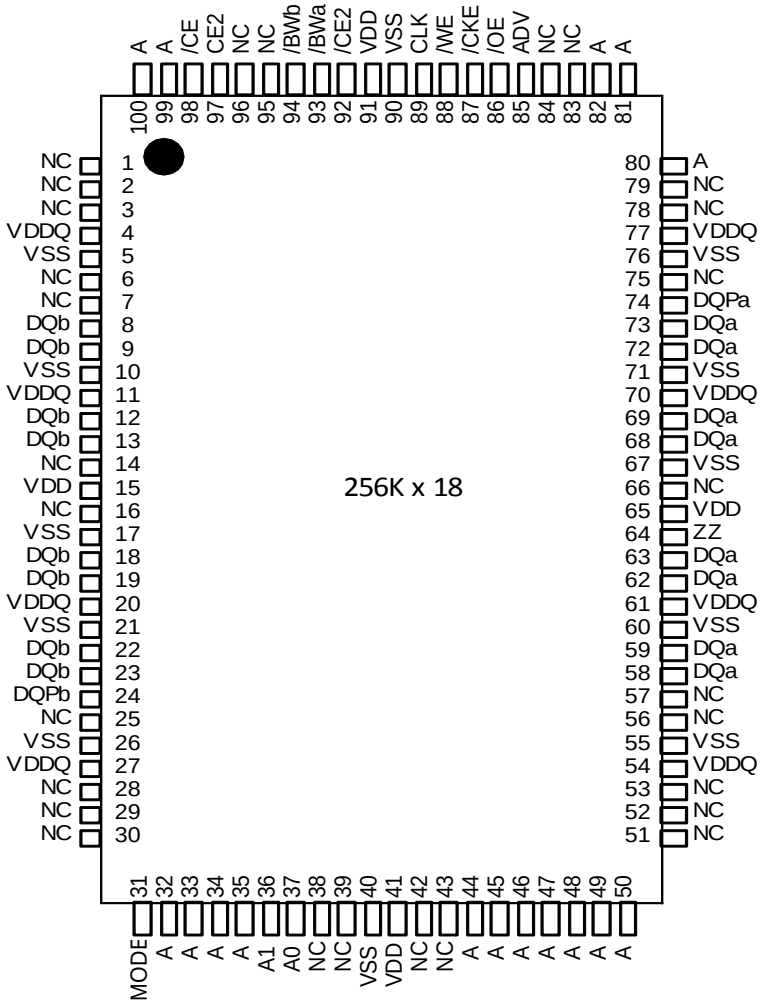
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	DQx	Synchronous Data I/O
/WE	Synchronous Read/Write Control Input	V_{DD}	Power Supply
CLK	Synchronous Clock	V_{DDQ}	I/O Power Supply
/CKE	Clock Enable	V_{SS}	Ground
/CE,CE2,/CE2	Synchronous Chip Enable	NC	No Connect
/BWx (x=a-d)	Synchronous Byte Write Inputs		
/OE	Asynchronous Output Enable		

256K x 18, 100PIN QFP (Top View)



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

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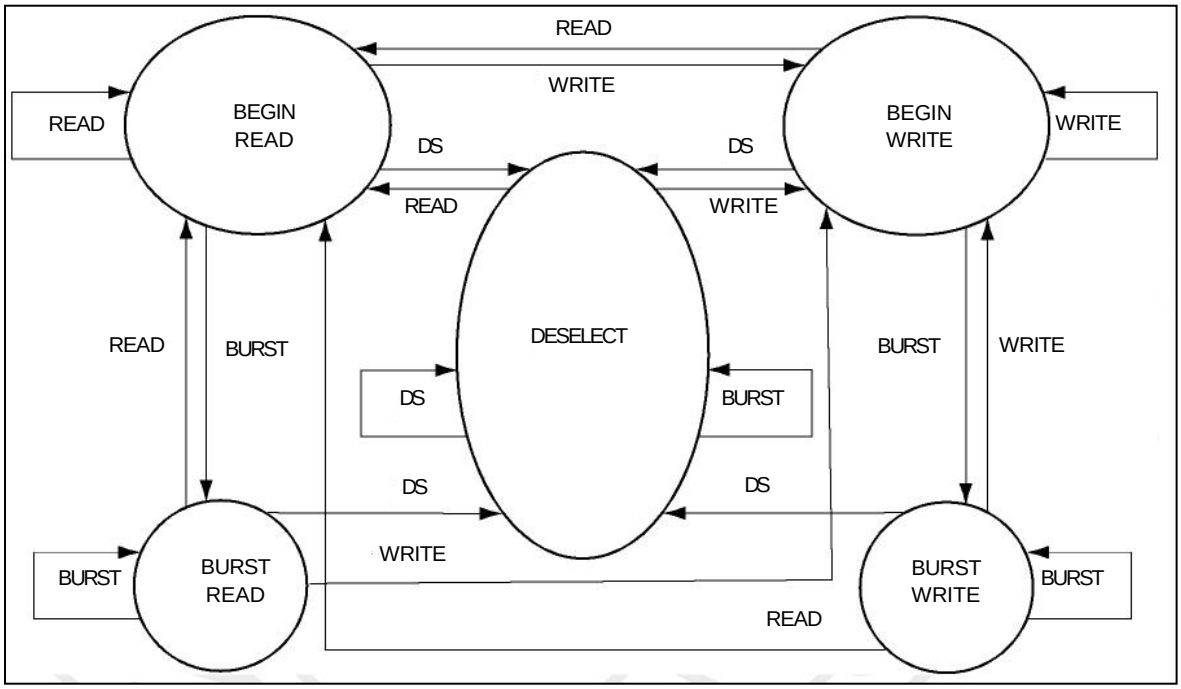
Symbol	Pin Name	Symbol	Pin Name
A	Synchronous Address Inputs	ZZ	Asynchronous Power Sleep Mode
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	DQx	Synchronous Data I/O
/WE	Synchronous Read/Write Control Input	DQPx	Synchronous Parity Data I/O
CLK	Synchronous Clock	V_{DD}	Power Supply
/CKE	Clock Enable	V_{DDQ}	I/O Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	V_{SS}	Ground
/BWx (x=a-b)	Synchronous Byte Write Inputs	NC	No Connect
/OE	Asynchronous Output Enable		

STATE DIAGRAM



TRUTH TABLE

SYNCHRONOUS TRUTH TABLE

Operation	Address Used	/CE	CE2	/CE2	ADV	/WE	/BWx	/OE	/CKE	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. /WE = L means Write operation in Write Truth Table.
5. /WE = H means Read operation in Write Truth Table.
6. Operation finally depends on status of asynchronous pins (ZZ and /OE).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	/OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:
1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with /OE, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	/WE	/BWa	/BWb
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36/32)

Operation	/WE	/BWa	/BWb	/BWc	/BWd
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

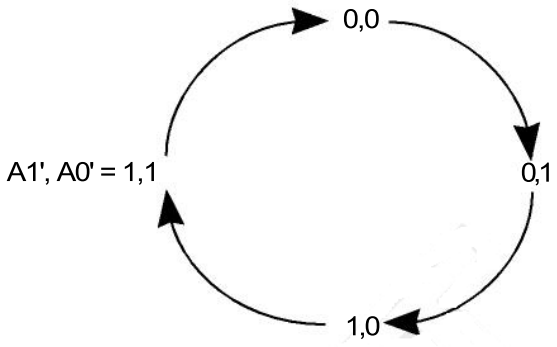
Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

ADDRESS SEQUENCE IN BURST MODE

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{dd} or NC)

External Address	1st Burst Address	2nd Burst Address	3rd Burst Address
A1 A0	A1 A0	A1 A0	A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{ss})



Power Up Sequence

Vddq → Vdd[1] → I/O Pins[2]

Notes:
1. Vdd can be applied at the same time as Vddq
2. Applying I/O inputs is recommended after Vddq is stable. The inputs of the I/O pins can be applied at the same time as Vddq as long as Vih (level of I/O pins) is lower than Vddq.

ERROR DETECTION AND CORRECTION

- Independent ECC with Hamming code for each byte.
- Detect and correct one bit error per byte.
- Better reliability than parity code schemes that could detect error bit but NOT correct it.
- Backward compatible : Drop in replacement to current in industry standard devices without ECC.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LF Value	VF Value	Unit
T_{STG}	Storage Temperature	–65 to +150	–65 to +150	°C
P_D	Power Dissipation	1.6	1.6	W
I_{OUT}	Output Current (per I/O)	100	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ}+0.5	–0.3 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to Vss for Address and Control Inputs	–0.5 to V_{DD}+0.5	–0.3 to V_{DD} + 0.3	V
V_{DDQ}	Voltage on V_{DDQ} Supply Relative to Vss	–0.5 to V_{DD}	–0.3 to V_{DD}	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	–0.3 to 3.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

Option	Range	VDD	VDDQ	Ambient Temperature
IS61NLPXXXXX	Commercial	3.3V ± 5%	3.3V / 2.5V ± 5%	0°C to +70°C
	Industrial	3.3V ± 5%	3.3V / 2.5V ± 5%	-40°C to +85°C
IS61NVPXXXXX	Commercial	2.5V ± 5%	2.5V ± 5%	0°C to +70°C
	Industrial	2.5V ± 5%	2.5V ± 5%	-40°C to +85°C
IS64NLPXXXXX	Automotive	3.3V ± 5%	3.3V / 2.5V ± 5%	-40°C to +125°C
IS64NVPXXXXX	Automotive	2.5V ± 5%	2.5V ± 5%	-40°C to +125°C

CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		Unit
			Min.	Max.	Min.	Max.	
Voh	Output HIGH Voltage	Ioh=-4.0 mA(3.3V)	2.4	—	2.0	—	V
		Ioh=–1.0 mA(2.5V)					
Vol	Output LOW Voltage	Iol=8.0 mA(3.3V)	—	0.4	—	0.4	V
		Iol=1.0 mA(2.5V)					
Vih	Input HIGH Voltage		2.0	Vdd+0.3	1.7	Vdd+0.3	V
Vil	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
Ili	Input Leakage Current	Vss≤Vin≤Vdd	–5	5	–5	5	µA
Ilo	Output Leakage Current	Vss≤Vout≤Vddq,/OE=Vih	–5	5	–5	5	µA

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: Vih (AC) ≤ Vdd + 2.0V (Pulse width less than tkc /2)
3. Undershoot:
   3.3V and 2.5V: Vil (AC) ≥ -2.0V (Pulse width less than tkc /2)

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-250		-200		Unit
				MAX		MAX		
				x18	x36/32	x18	x36/32	
Icc	AC Operating, Supply Current	Device Selected, OE = Vih, ZZ ≤ Vil,All Inputs ≤ 0.2V or ≥ Vdd – 0.2V,Cycle Time ≥ tkc min.	Com.	235	235	200	200	mA
			Ind.	260	260	210	210	
			Auto	285	285	235	235	
Isb	Standby Current TTL Input	Device Deselected,Vdd = Max.,All Inputs ≤ Vil or ≥ Vih,ZZ ≤ Vil, f = Max.	Com.	100	100	100	100	mA
			Ind.	110	110	110	110	
			Auto	130	130	130	130	
Isb1	Standby Current CMOS Input	Device Deselected,Vdd = Max.,Vin ≤ Vss + 0.2V or ≥Vdd – 0.2V,f = 0	Com.	80	80	70	70	mA
			Ind.	85	85	75	75	
			Auto	100	100	100	100	

Note:
1. MODE pin has an internal pullup and should be tied to Vdd or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥Vdd–0.2V.

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, Vdd = 3.3V.

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	EC-250		EC-200		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}	Clock Frequency	—	250	—	200	MHz
t_{KC}	Cycle Time	4	—	5	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	ns
t_{KL}	Clock Low Time	1.7	—	2	—	ns
t_{KQ}	Clock Access Time	—	2.6	—	3.1	ns
t_{KQX}[2]	Clock High to Output Invalid	0.8	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0.8	—	1	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	2.6	—	3.1	ns
t_{OEQ}	Output Enable to Output Valid	—	2.6	—	3.1	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	2.6	—	3	ns
t_{AS}	Address Setup Time	1.2	—	1.4	—	ns
t_{SS}	Address Status Setup Time	1.2	—	1.4	—	ns
t_{WS}	Read/Write Setup Time	1.2	—	1.4	—	ns
t_{CES}	Chip Enable Setup Time	1.2	—	1.4	—	ns
t_{SE}	Clock Enable Setup Time	1.2	—	1.4	—	ns
t_{ADVS}	Address Advance Setup Time	1.2	—	1.4	—	ns
t_{DS}	Data Setup Time	1.2	—	1.4	—	ns
t_{SH}	Address Status Hold Time	1.2	—	1.4	—	ns
t_{AH}	Address Hold Time	0.3	—	0.4	—	ns
t_{HE}	Clock Enable Hold Time	0.3	—	0.4	—	ns
t_{WH}	Write Hold Time	0.3	—	0.4	—	ns
t_{CEH}	Chip Enable Hold Time	0.3	—	0.4	—	ns
t_{ADVH}	Address Advance Hold Time	0.3	—	0.4	—	ns
t_{DH}	Data Hold Time	0.3	—	0.4	—	ns
t_{POWER}[4]	V_{DD} (typical) to First Access	1	—	1	—	ms

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. t_{POWER} is the time that the power needs to be supplied above V_{DD} (min) initially before READ or WRITE operation can be initiated.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
V_{TT}	1.5V
V_{LOAD}	3.3V
R1, R2	317Ω, 351Ω
Output Load	See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
V_{TT}	1.25V
V_{LOAD}	2.5V
R1, R2	1667Ω, 1538Ω
Output Load	See Figures 1 and 2

I/O OUTPUT LOAD EQUIVALENT

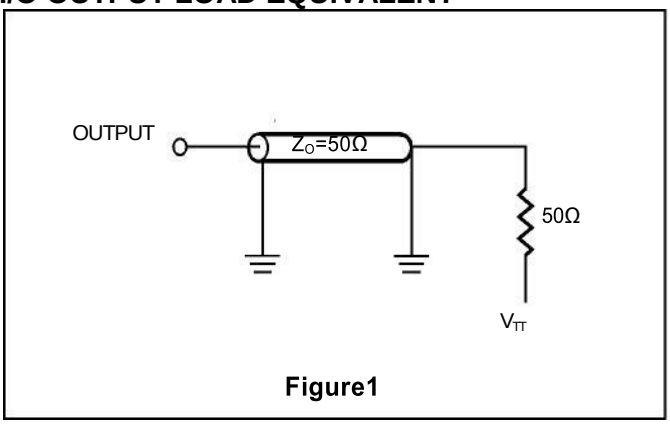


Figure1

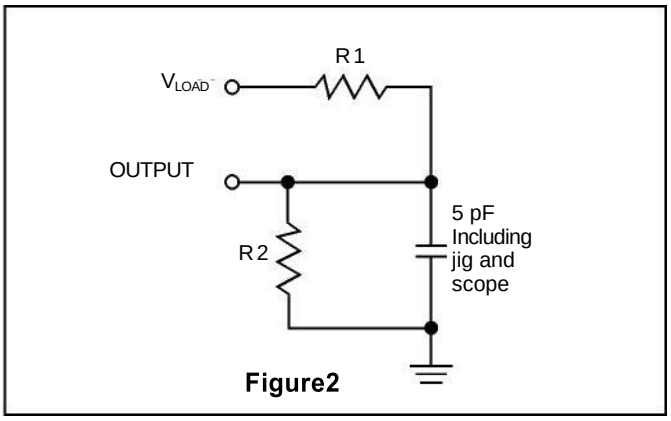
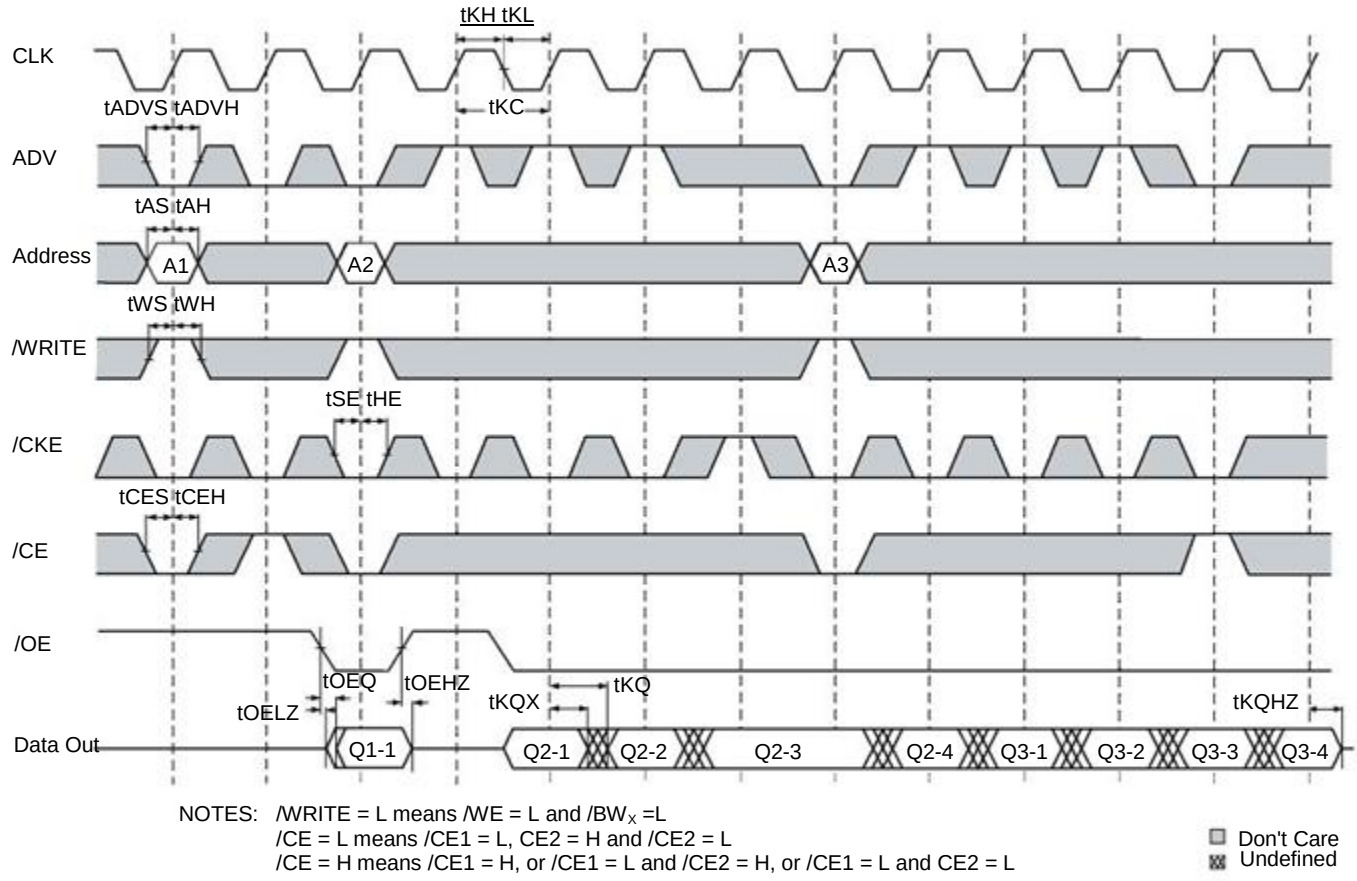
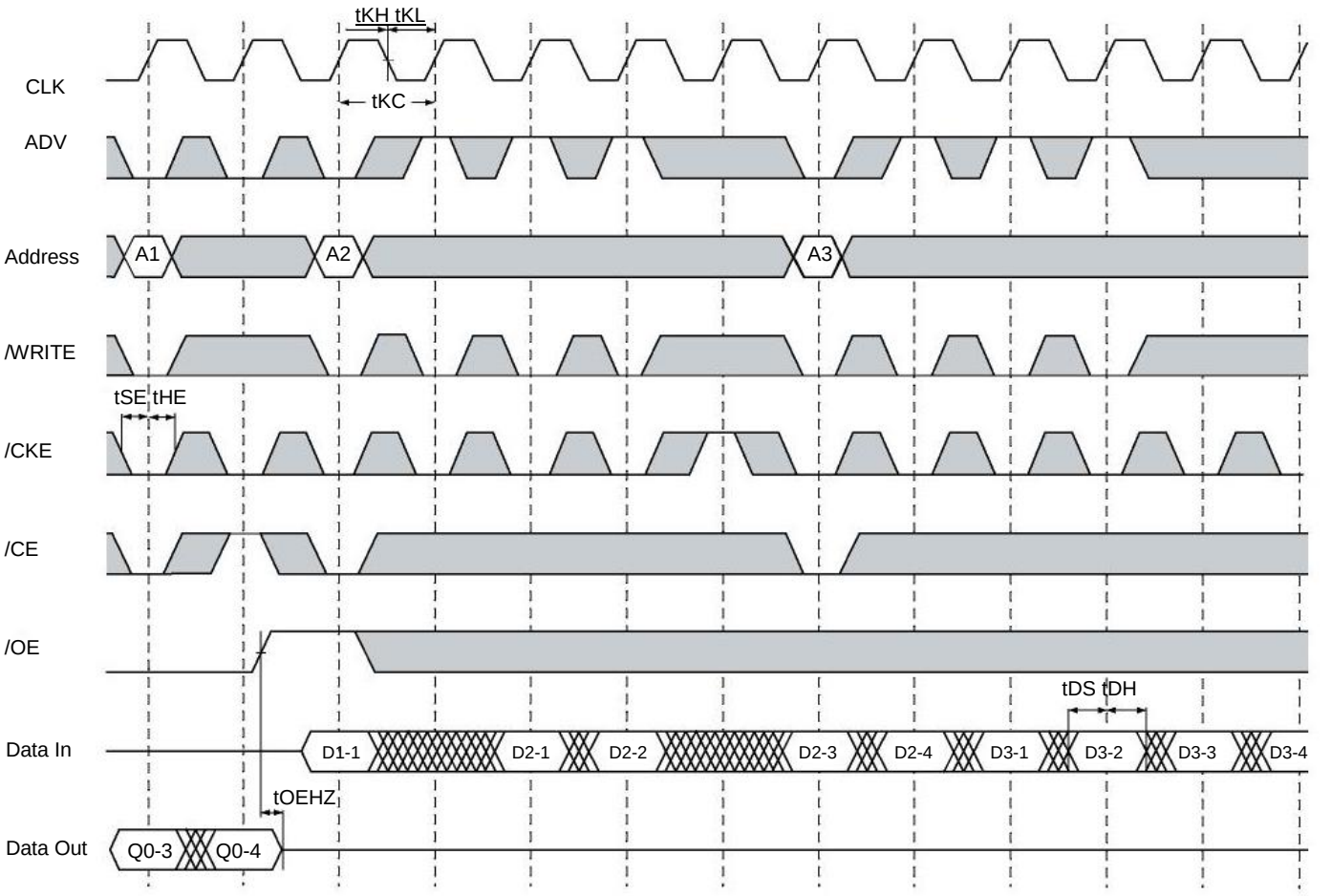


Figure2

READ CYCLE TIMING

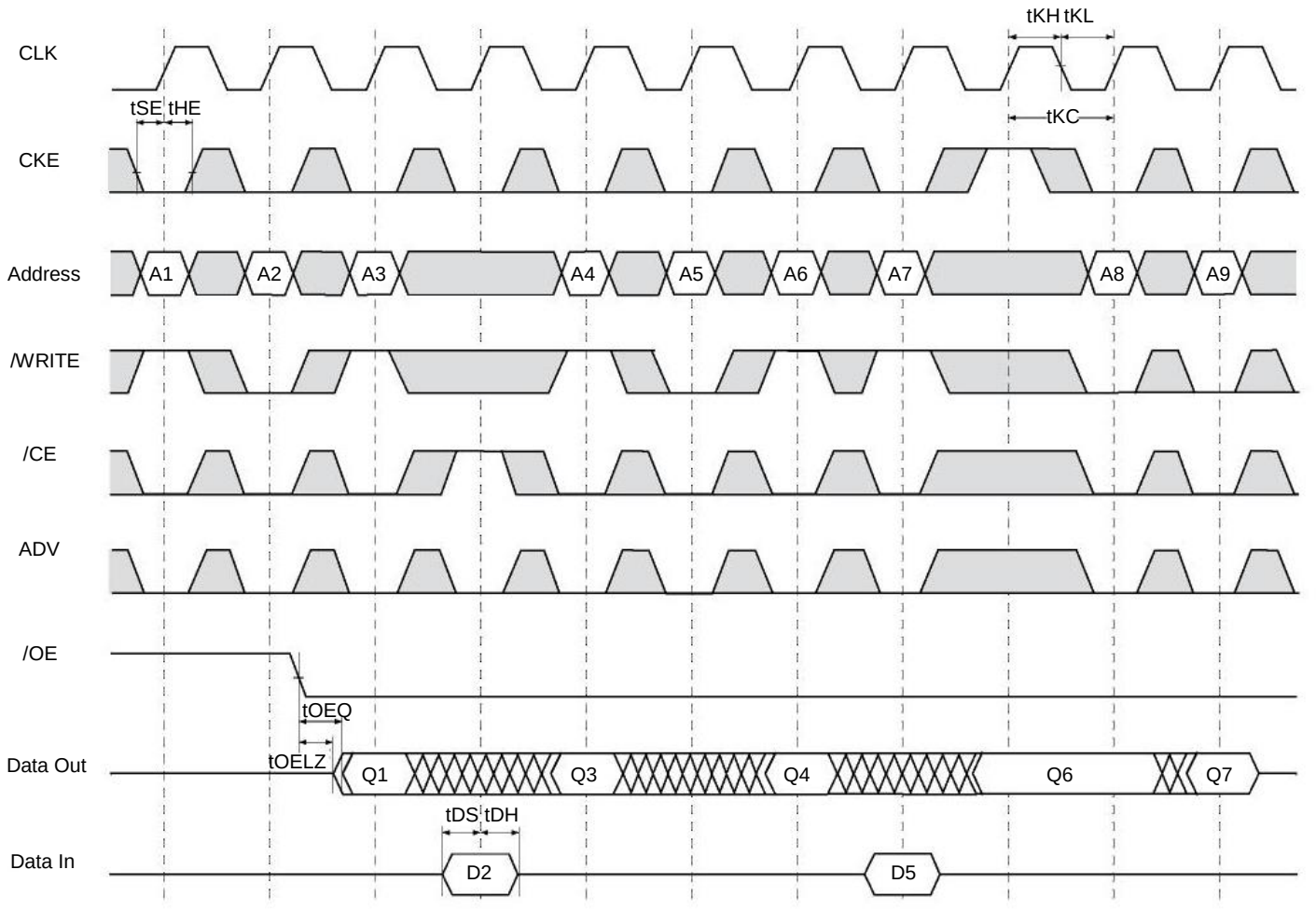


WRITE CYCLE TIMING



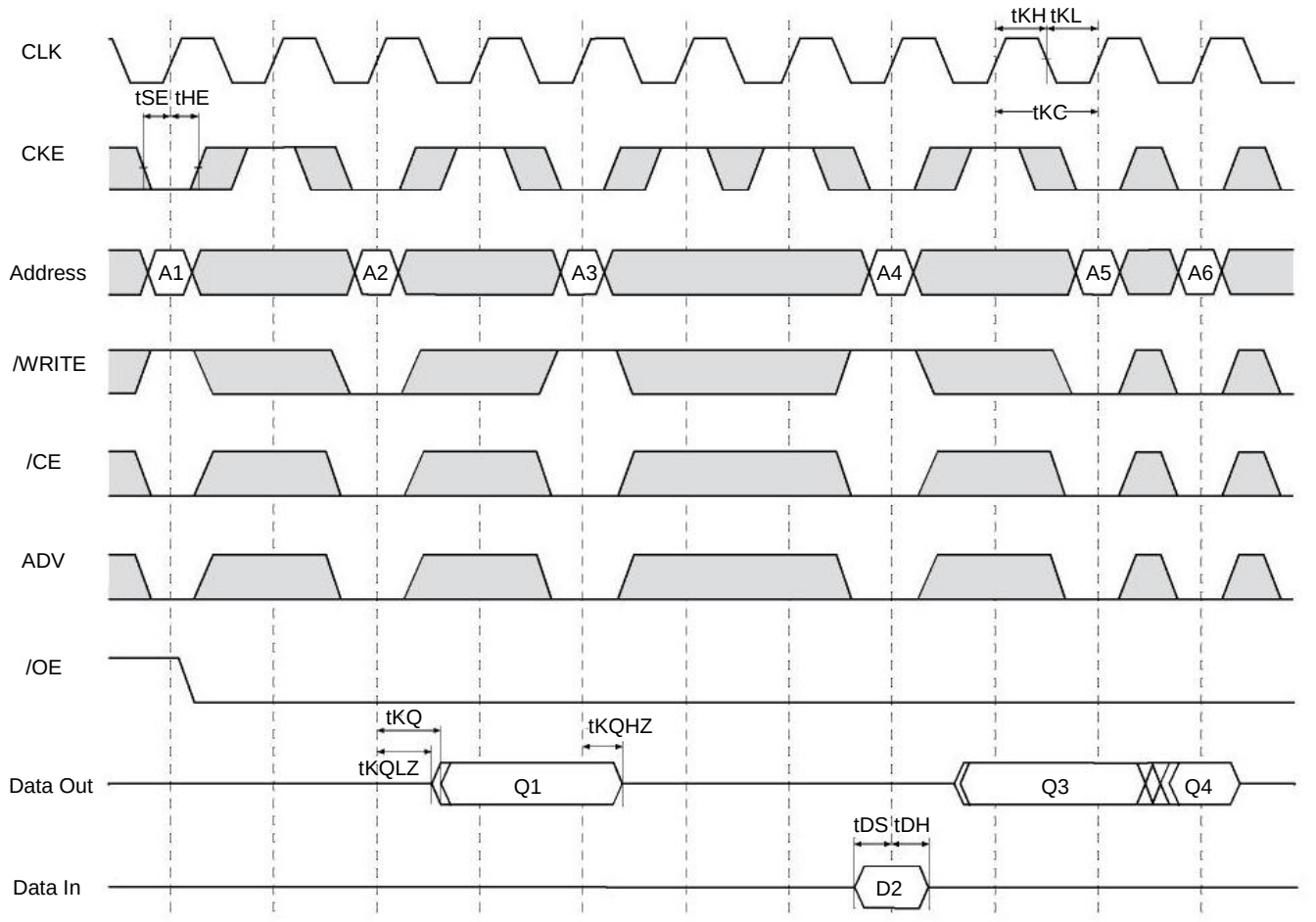
NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

SINGLE READ/WRITE CYCLE TIMING



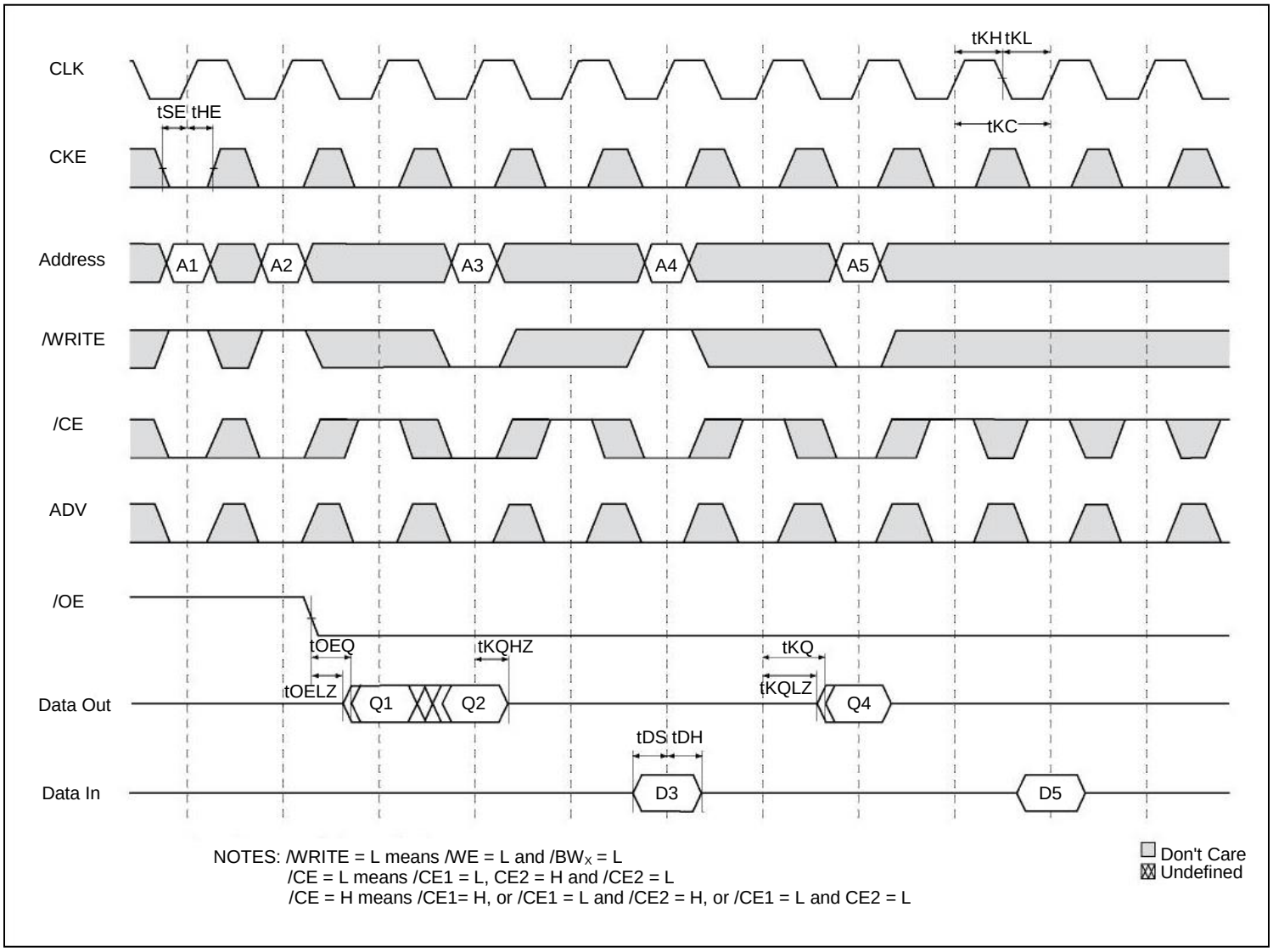
NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

/CKE OPERATION TIMING



NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

/CE OPERATION TIMING

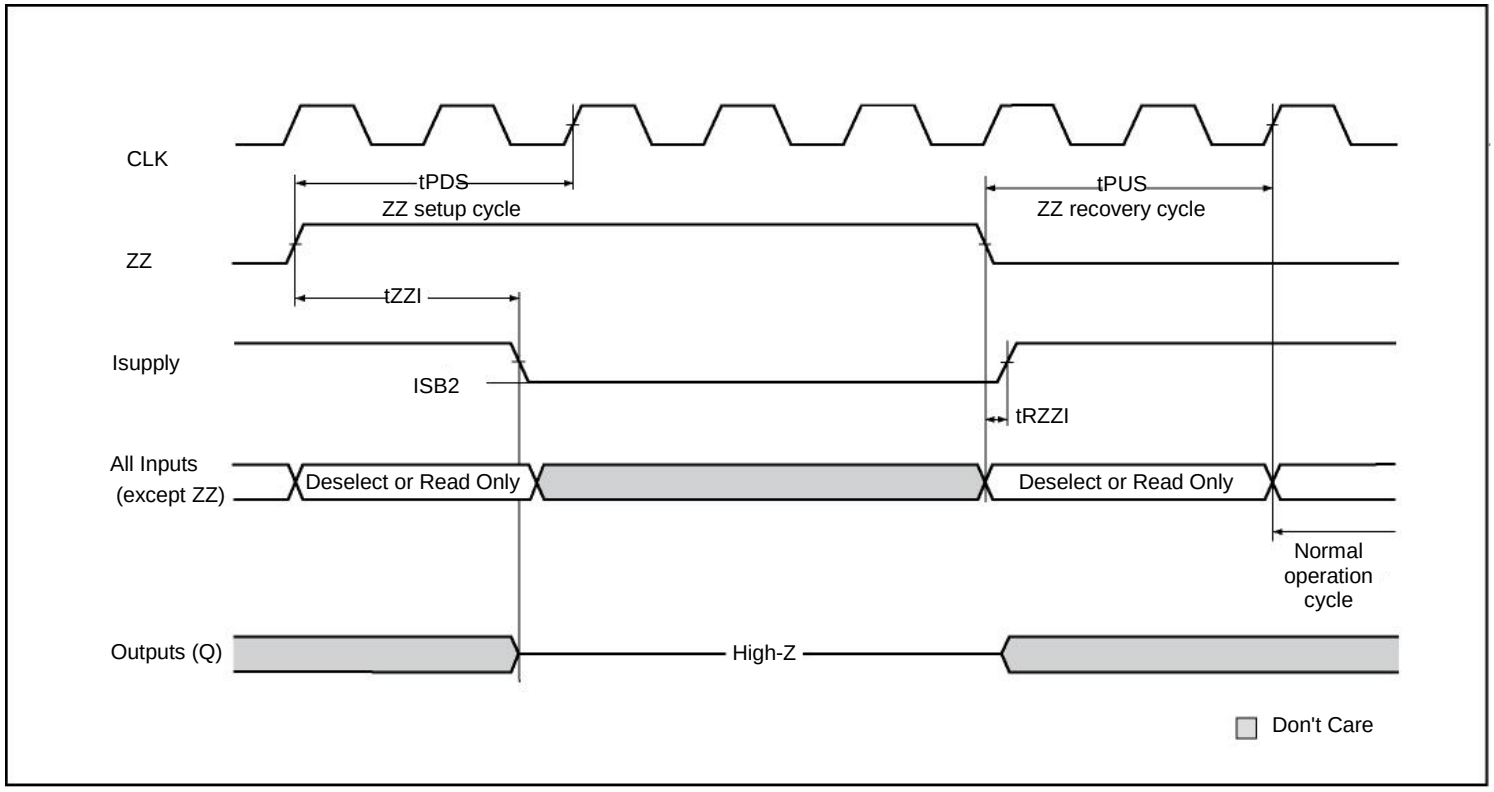


NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
Isb2	Current during SNOOZE MODE	ZZ ≥ Vih	Com.	—	35	mA
			Ind.	—	40	
			Auto.	—	60	
tpds	ZZ active to input ignored		—	—	2	cycle
tpus	ZZ inactive to input sampled		—	2	—	cycle
tzzi	ZZ active to SNOOZE current		—	—	2	cycle
trzzi	ZZ inactive to exit SNOOZE current		—	0	—	ns

SLEEP MODE TIMING



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

Test Access Port Signal List:

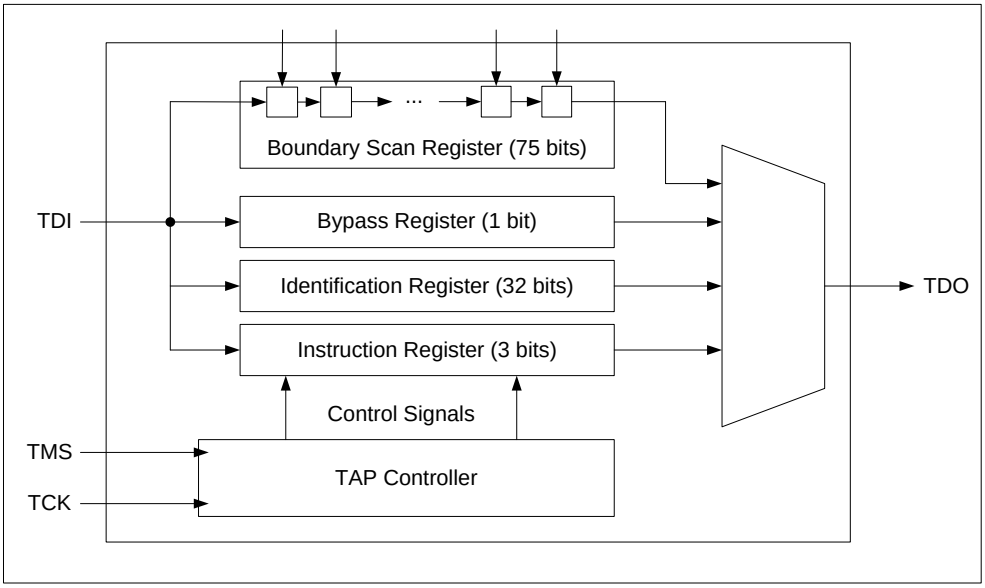
1. Test Clock (TCK)
This signal uses VDD as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)
This signal uses VDD as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

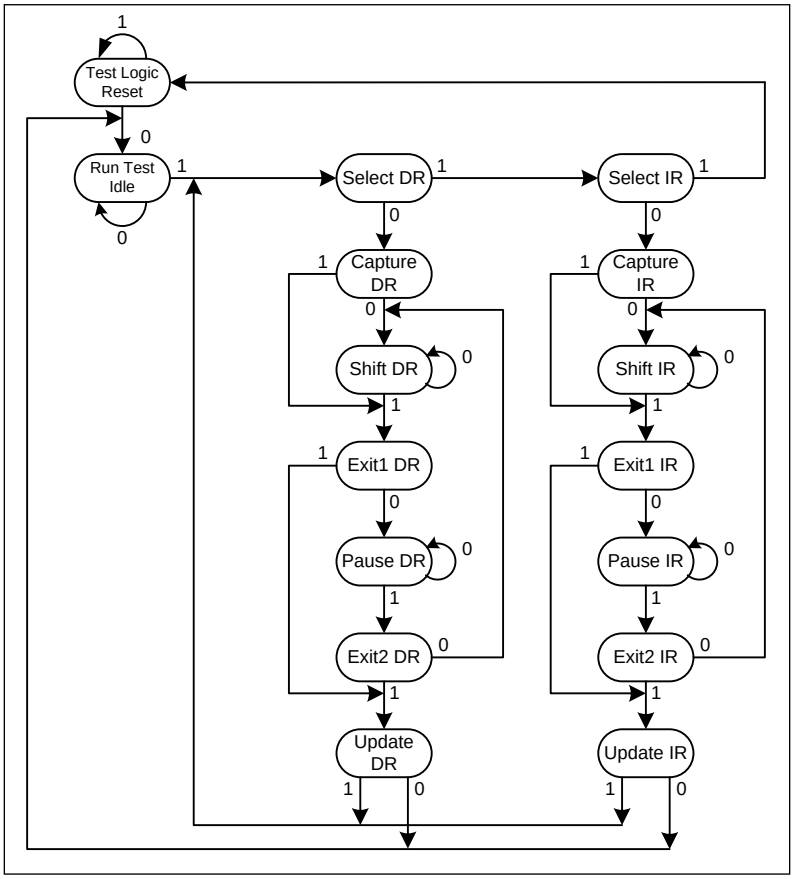
3. Test Data-In (TDI)
This signal uses VDD as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

4. Test Data-Out (TDO)
This signal uses VDDQ as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

1. Instruction Register
This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

2. Bypass Register
The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

3. Boundary Scan Register
The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

4. Identification (ID) Register
The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	75

TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

1. EXTEST
The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls. However, this product forces all SRAM outputs to High-Z state and this instruction is not 1149.1 compliant.

2. IDCODE
The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

3. SAMPLE Z
If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

4. SAMPLE/PRELOAD
When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

6. BYPASS
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

7. PRIVATE
Do not use these instructions. They are reserved for future use and engineering mode.

JTAG TAP DC ELECTRICAL CHARACTERISTICS (V_{DDQ}=3.3V Operating Range)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.0	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.8	V	
JTAG Output High Voltage	V_{OH1}	2.4	-	V	$\|I_{OH1}\|$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	2.9	-	V	$\|I_{OH2}\|$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Load Current	I_X	-10	+10	uA	$0 \le Vin \le V_{DD}$

Notes:
1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

JTAG TAP DC ELECTRICAL CHARACTERISTICS (V_{DDQ}=2.5V Operating Range)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	1.7	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.7	V	
JTAG Output High Voltage	V_{OH1}	2.0	-	V	$\|I_{OH1}\|$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	2.1	-	V	$\|I_{OH2}\|$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Load Current	I_X	-10	+10	uA	$0 \le Vin \le V_{DD}$

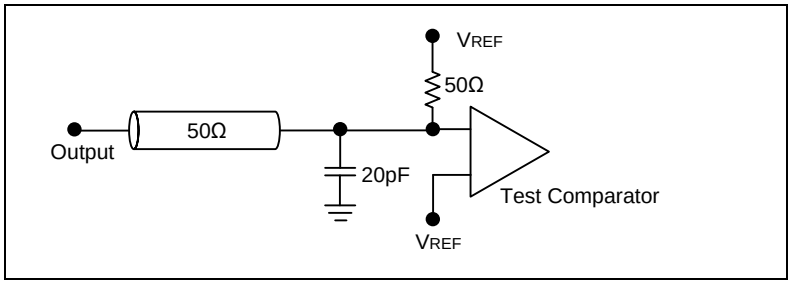
Notes:
2. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

JTAG AC Test Conditions

(Over the Operating Temperature Range)

Parameter	Symbol	2.5V Option	3.3V Option	Units
Input Pulse High Level	V_{IH1}	2.5	3.0	V
Input Pulse Low Level	V_{IL1}	0	0	V
Input rise and fall time	T_{R1}	1.5	1.5	ns
Test load termination supply voltage	V_{REF}	1.25	1.5	V
Input and Output Timing Reference Level	V_{REF}	1.25	1.5	V

TAP Output Load Equivalent

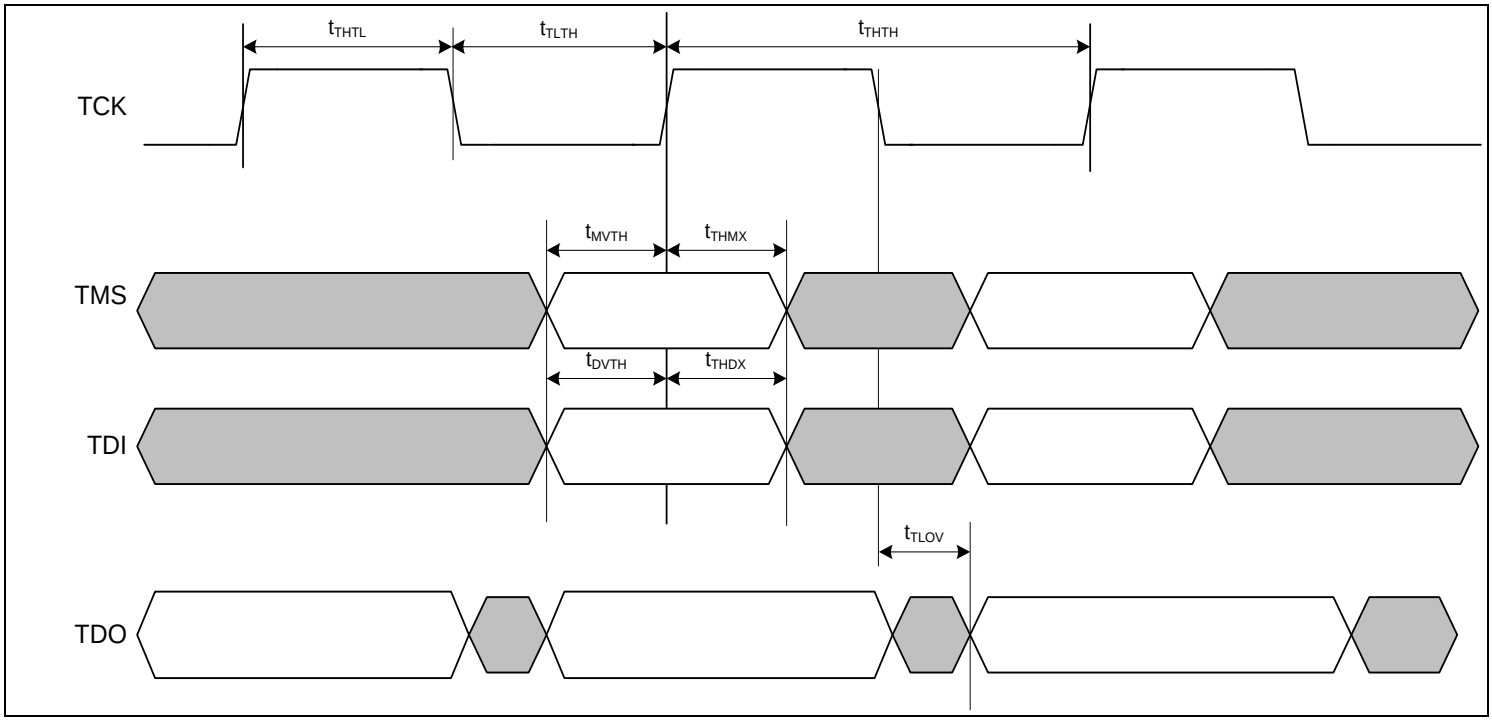


JTAG AC Characteristics

(Over the Operating Temperature Range)

Parameter	Symbol	Min	Max	Units
TCK cycle time	t_{THTH}	100	–	ns
TCK high pulse width	t_{THTL}	40	–	ns
TCK low pulse width	t_{TLTH}	40	–	ns
TMS Setup	t_{MVTH}	10	–	ns
TMS Hold	t_{THMX}	10	–	ns
TDI Setup	t_{DVTH}	10	–	ns
TDI Hold	t_{THDX}	10	–	ns
TCK Low to Valid Data*	t_{TLOV}	–	20	ns

JTAG Timing Diagram



Instruction Set

Code	Instruction	TDO Output	Notes
000	EXTEST	Boundary Scan Register	2, 6
001	IDCODE	32-bit Identification Register	
010	SAMPLE-Z	Boundary Scan Register	1, 2
011	PRIVATE	Do Not Use	5
100	SAMPLE(/PRELOAD)	Boundary Scan Register	4
101	PRIVATE	Do Not Use	5
110	PRIVATE	Do Not Use	5
111	BYPASS	Bypass Register	3

Notes:
1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place Qs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

ID Register Definition

Instruction Field	Description	128K x 36/32	256K x 18
Revision Number (31:28)	Reserved for version number.	xxxx	xxxx
Device Depth (27:23)	Defines depth of SRAM. 128K or 256K	00110	00111
Device Width (22:18)	Defines Width of the SRAM. x36/32 or x18	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	xxxxx	xxxxx
ISSI JEDEC ID (11:1)	Allows unique identification of SRAM vendor.	00011010101	00011010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1

Boundary Scan Order

165 BGA					119 BGA				
	X36/32		X18			X36/32		X18	
Bit #	Signal	Bump ID	Signal	Bump ID	Bit #	Signal	Bump ID	Signal	Bump ID
1	MODE	1R	MODE	1R	1	MODE	3R	MODE	3R
2	NC	6N	NC	6N	2	NC	4L	NC	4L
3	NC	11P	NC	11P	3	NC	7R	NC	7R
4	A	8P	A	8P	4	A	4T	A	2T
5	A	8R	A	8R	5	A	3T	A	3T
6	A	9R	A	9R	6	A	5B	A	5B
7	A	9P	A	9P	7	A	5C	A	5C
8	A	10P	A	10P	8	A	5A	A	5A
9	A	10R	A	10R	9	A	5T	A	5T
10	A	11R	A	11R	10	A	6R	A	6R
11	ZZ	11H	ZZ	11H	11	ZZ	7T	ZZ	7T
12	DQPa	11N	NC	11N	12	DQPa	6P	NC	6P
13	DQa	11M	NC	11M	13	DQa	7N	NC	7N
14	DQa	11L	NC	11L	14	DQa	6M	NC	6M
15	DQa	11K	NC	11K	15	DQa	7P	NC	7L
16	DQa	11J	NC	11J	16	DQa	6N	NC	6K
17	DQa	10M	DQa	10M	17	DQa	7L	DQa	7P
18	DQa	10L	DQa	10L	18	DQa	6K	DQa	6N
19	DQa	10K	DQa	10K	19	DQa	6L	DQa	6L
20	DQa	10J	DQa	10J	20	DQa	7K	DQa	7K
21	DQb	11G	DQa	11G	21	DQb	6H	DQa	6H
22	DQb	11F	DQa	11F	22	DQb	7G	DQa	7G
23	DQb	11E	DQa	11E	23	DQb	7H	DQa	6F
24	DQb	11D	DQa	11D	24	DQb	6F	DQa	7E
25	DQb	10G	DQPa	11C	25	DQb	7E	DQPa	6D
26	DQb	10F	NC	10F	26	DQb	6G	NC	6G
27	DQb	10E	NC	10E	27	DQb	6E	NC	6E
28	DQb	10D	NC	10D	28	DQb	7D	NC	7D
29	DQPb	11C	NC	10G	29	DQPb	6D	NC	7H
30	NC	11A	A	11A	30	NC	6T	A	6T
31	A	10A	A	10A	31	A	6A	A	6A
32	A	10B	A	10B	32	A	6C	A	6C
33	NC	9A	NC	9A	33	NC	4G	NC	4G
34	NC	9B	NC	9B	34	NC	4A	NC	4A
35	ADV	8A	ADV	8A	35	ADV	4B	ADV	4B
36	/OE	8B	/OE	8B	36	/OE	4F	/OE	4F
37	/CKE	7A	/CKE	7A	37	/CKE	4M	/CKE	4M
38	/WE	7B	/WE	7B	38	/WE	4H	/WE	4H
39	CLK	6B	CLK	6B	39	CLK	4K	CLK	4K
40	NC	11B	NC	11B	40	NC	7C	NC	7C

Continue next page

165 BGA					119 BGA				
	X36/32		X18			X36/32		X18	
Bit #	Signal	Bump ID	Signal	Bump ID	Bit #	Signal	Bump ID	Signal	Bump ID
41	NC	1A	NC	1A	41	NC	1B	NC	1B
42	/CE2	6A	/CE2	6A	42	/CE2	6B	/CE2	6B
43	/BWa	5B	/BWa	5B	43	/BWa	5L	/BWa	5L
44	/BWb	5A	NC	5A	44	/BWb	5G	NC	5G
45	/BWc	4A	/BWb	4A	45	/BWc	3G	/BWb	3G
46	/BWd	4B	NC	4B	46	/BWd	3L	NC	3L
47	CE2	3B	CE2	3B	47	CE2	2B	CE2	2B
48	/CE	3A	/CE	3A	48	/CE	4E	/CE	4E
49	A	2A	A	2A	49	A	3A	A	3A
50	A	2B	A	2B	50	A	2A	A	2A
51	NC	1B	NC	1B	51	NC	1C	NC	1C
52	DQPc	1C	NC	1C	52	DQPc	2D	NC	2D
53	DQc	1D	NC	1D	53	DQc	1E	NC	1E
54	DQc	1E	NC	1E	54	DQc	2F	NC	2F
55	DQc	1F	NC	1F	55	DQc	1D	NC	1G
56	DQc	1G	NC	1G	56	DQc	2E	NC	2H
57	DQc	2D	DQb	2D	57	DQc	1G	DQb	1D
58	DQc	2E	DQb	2E	58	DQc	2H	DQb	2E
59	DQc	2F	DQb	2F	59	DQc	2G	DQb	2G
60	DQc	2G	DQb	2G	60	DQc	1H	DQb	1H
61	DQd	1J	DQb	1J	61	DQd	2K	DQb	2K
62	DQd	1K	DQb	1K	62	DQd	1L	DQb	1L
63	DQd	1L	DQb	1L	63	DQd	1K	DQb	2M
64	DQd	1M	DQb	1M	64	DQd	2M	DQb	1N
65	DQd	2J	DQPb	1N	65	DQd	1N	DQPb	2P
66	DQd	2K	NC	2K	66	DQd	2L	NC	2L
67	DQd	2L	NC	2L	67	DQd	2N	NC	2N
68	DQd	2M	NC	2M	68	DQd	1P	NC	1P
69	DQPd	1N	NC	2J	69	DQPd	2P	NC	1K
70	A	3P	A	3P	70	A	2R	A	2R
71	A	3R	A	3R	71	A	2C	A	2C
72	A	4R	A	4R	72	A	3B	A	3B
73	A	4P	A	4P	73	A	3C	A	3C
74	A1	6P	A1	6P	74	A1	4N	A1	4N
75	A0	6R	A0	6R	75	A0	4P	A0	4P

Note : DQPa, DQPb, DQPc, and DQPd pins of x36 IO option are NC of x32 IO option.

ORDERING INFORMATION

The ordering code information of the product family

IS Product Function Density Version – Speed Package Temperature

None	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
A3	Automotive	-40°C to 125°C

TQ	100 TQFP
B3	165 PBGA
B2	119 PBGA

200	fMAX=200MHz
250	fMAX=250MHz

E	ECC function
C	Die Revision

12836	128Kx36
12832	128Kx32
25618	256Kx18

Mark	V_{DD}	Function
NLP	3.3V	No-Wait(ZBT) Pipelined
NVP	2.5V	No-Wait(ZBT) Pipelined

61	Commercial & Industrial SRAM
64	Automotive

Integrated Silicon Solution Inc

Commercial Range: 0°C to 70°C

VDD	SPEED	X36	X32	X18	Package
VDD =3.3V VDDQ=2.5V or VDDQ=3.3V	250MHz	IS61NLP12836EC-250B3	IS61NLP12832EC-250B3	IS61NLP25618EC-250B3	165 BGA
		IS61NLP12836EC-250B2	IS61NLP12832EC-250B2	IS61NLP25618EC-250B2	119 BGA
		IS61NLP12836EC-250TQL	IS61NLP12832EC-250TQL	IS61NLP25618EC-250TQL	100 QFP, Lead-free
		IS61NLP12836EC-250B3L	IS61NLP12832EC-250B3L	IS61NLP25618EC-250B3L	165 BGA, Lead-free
		IS61NLP12836EC-250B2L	IS61NLP12832EC-250B2L	IS61NLP25618EC-250B2L	119 BGA, Lead-free
	200MHz	IS61NLP12836EC-200B3	IS61NLP12832EC-200B3	IS61NLP25618EC-200B3	165 BGA
		IS61NLP12836EC-200B2	IS61NLP12832EC-200B2	IS61NLP25618EC-200B2	119 BGA
		IS61NLP12836EC-200TQL	IS61NLP12832EC-200TQL	IS61NLP25618EC-200TQL	100 QFP, Lead-free
		IS61NLP12836EC-200B3L	IS61NLP12832EC-200B3L	IS61NLP25618EC-200B3L	165 BGA, Lead-free
		IS61NLP12836EC-200B2L	IS61NLP12832EC-200B2L	IS61NLP25618EC-200B2L	119 BGA, Lead-free
VDD =2.5V VDDQ=2.5V	250MHz	IS61NVP12836EC-250B3	IS61NVP12832EC-250B3	IS61NVP25618EC-250B3	165 BGA
		IS61NVP12836EC-250B2	IS61NVP12832EC-250B2	IS61NVP25618EC-250B2	119 BGA
		IS61NVP12836EC-250TQL	IS61NVP12832EC-250TQL	IS61NVP25618EC-250TQL	100 QFP, Lead-free
		IS61NVP12836EC-250B3L	IS61NVP12832EC-250B3L	IS61NVP25618EC-250B3L	165 BGA, Lead-free
		IS61NVP12836EC-250B2L	IS61NVP12832EC-250B2L	IS61NVP25618EC-250B2L	119 BGA, Lead-free
	200MHz	IS61NVP12836EC-200B3	IS61NVP12832EC-200B3	IS61NVP25618EC-200B3	165 BGA
		IS61NVP12836EC-200B2	IS61NVP12832EC-200B2	IS61NVP25618EC-200B2	119 BGA
		IS61NVP12836EC-200TQL	IS61NVP12832EC-200TQL	IS61NVP25618EC-200TQL	100 QFP, Lead-free
		IS61NVP12836EC-200B3L	IS61NVP12832EC-200B3L	IS61NVP25618EC-200B3L	165 BGA, Lead-free
		IS61NVP12836EC-200B2L	IS61NVP12832EC-200B2L	IS61NVP25618EC-200B2L	119 BGA, Lead-free

Industrial Range: -40°C to 85°C

VDD	SPEED	X36	X32	X18	Package
VDD =3.3V VDDQ=2.5V or VDDQ=3.3V	250MHz	IS61NLP12836EC-250B3I	IS61NLP12832EC-250B3I	IS61NLP25618EC-250B3I	165 BGA
		IS61NLP12836EC-250B2I	IS61NLP12832EC-250B2I	IS61NLP25618EC-250B2I	119 BGA
		IS61NLP12836EC-250TQLI	IS61NLP12832EC-250TQLI	IS61NLP25618EC-250TQLI	100 QFP, Lead-free
		IS61NLP12836EC-250B3LI	IS61NLP12832EC-250B3LI	IS61NLP25618EC-250B3LI	165 BGA, Lead-free
		IS61NLP12836EC-250B2LI	IS61NLP12832EC-250B2LI	IS61NLP25618EC-250B2LI	119 BGA, Lead-free
	200MHz	IS61NLP12836EC-200B3I	IS61NLP12832EC-200B3I	IS61NLP25618EC-200B3I	165 BGA
		IS61NLP12836EC-200B2I	IS61NLP12832EC-200B2I	IS61NLP25618EC-200B2I	119 BGA
		IS61NLP12836EC-200TQLI	IS61NLP12832EC-200TQLI	IS61NLP25618EC-200TQLI	100 QFP, Lead-free
		IS61NLP12836EC-200B3LI	IS61NLP12832EC-200B3LI	IS61NLP25618EC-200B3LI	165 BGA, Lead-free
		IS61NLP12836EC-200B2LI	IS61NLP12832EC-200B2LI	IS61NLP25618EC-200B2LI	119 BGA, Lead-free
VDD =2.5V VDDQ=2.5V	250MHz	IS61NVP12836EC-250B3I	IS61NVP12832EC-250B3I	IS61NVP25618EC-250B3I	165 BGA
		IS61NVP12836EC-250B2I	IS61NVP12832EC-250B2I	IS61NVP25618EC-250B2I	119 BGA
		IS61NVP12836EC-250TQLI	IS61NVP12832EC-250TQLI	IS61NVP25618EC-250TQLI	100 QFP, Lead-free
		IS61NVP12836EC-250B3LI	IS61NVP12832EC-250B3LI	IS61NVP25618EC-250B3LI	165 BGA, Lead-free
		IS61NVP12836EC-250B2LI	IS61NVP12832EC-250B2LI	IS61NVP25618EC-250B2LI	119 BGA, Lead-free
	200MHz	IS61NVP12836EC-200B3I	IS61NVP12832EC-200B3I	IS61NVP25618EC-200B3I	165 BGA
		IS61NVP12836EC-200B2I	IS61NVP12832EC-200B2I	IS61NVP25618EC-200B2I	119 BGA
		IS61NVP12836EC-200TQLI	IS61NVP12832EC-200TQLI	IS61NVP25618EC-200TQLI	100 QFP, Lead-free
		IS61NVP12836EC-200B3LI	IS61NVP12832EC-200B3LI	IS61NVP25618EC-200B3LI	165 BGA, Lead-free
		IS61NVP12836EC-200B2LI	IS61NVP12832EC-200B2LI	IS61NVP25618EC-200B2LI	119 BGA, Lead-free

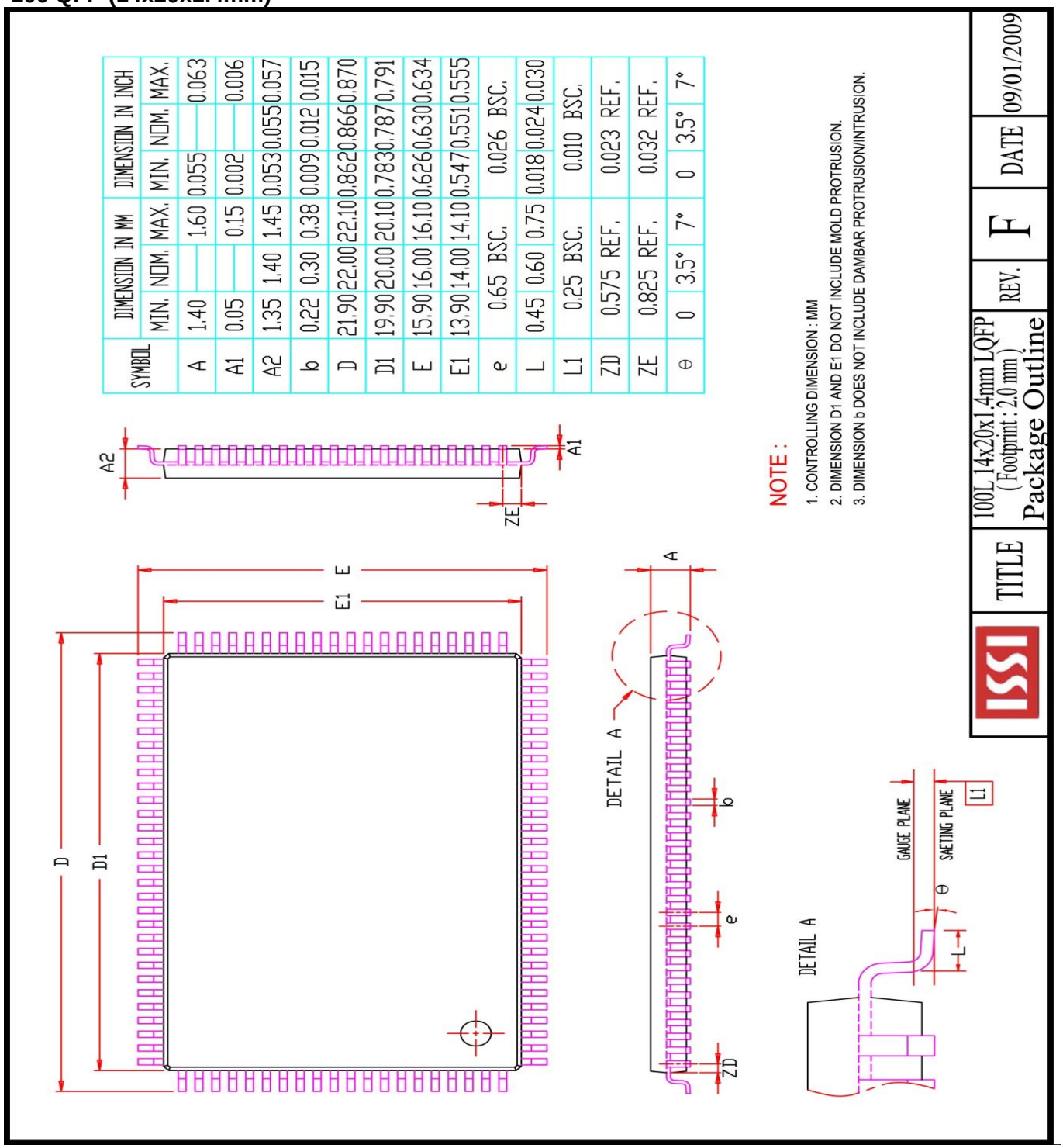
Automotive(A3) Range: -40°C to 125°C

VDD	SPEED	X36	X32	X18	Package
VDD =3.3V VDDQ=2.5V or VDDQ=3.3V	250MHz	IS64NLP12836EC-250B3A3	IS64NLP12832EC-250B3A3	IS64NLP25618EC-250B3A3	165 BGA
		IS64NLP12836EC-250B2A3	IS64NLP12832EC-250B2A3	IS64NLP25618EC-250B2A3	119 BGA
		IS64NLP12836EC-250TQLA3	IS64NLP12832EC-250TQLA3	IS64NLP25618EC-250TQLA3	100 QFP, Lead-free
		IS64NLP12836EC-250B3LA3	IS64NLP12832EC-250B3LA3	IS64NLP25618EC-250B3LA3	165 BGA, Lead-free
		IS64NLP12836EC-250B2LA3	IS64NLP12832EC-250B2LA3	IS64NLP25618EC-250B2LA3	119 BGA, Lead-free
	200MHz	IS64NLP12836EC-200B3A3	IS64NLP12832EC-200B3A3	IS64NLP25618EC-200B3A3	165 BGA
		IS64NLP12836EC-200B2A3	IS64NLP12832EC-200B2A3	IS64NLP25618EC-200B2A3	119 BGA
		IS64NLP12836EC-200TQLA3	IS64NLP12832EC-200TQLA3	IS64NLP25618EC-200TQLA3	100 QFP, Lead-free
		IS64NLP12836EC-200B3LA3	IS64NLP12832EC-200B3LA3	IS64NLP25618EC-200B3LA3	165 BGA, Lead-free
		IS64NLP12836EC-200B2LA3	IS64NLP12832EC-200B2LA3	IS64NLP25618EC-200B2LA3	119 BGA, Lead-free
VDD =2.5V VDDQ=2.5V	250MHz	IS64NVP12836EC-250B3A3	IS64NVP12832EC-250B3A3	IS64NVP25618EC-250B3A3	165 BGA
		IS64NVP12836EC-250B2A3	IS64NVP12832EC-250B2A3	IS64NVP25618EC-250B2A3	119 BGA
		IS64NVP12836EC-250TQLA3	IS64NVP12832EC-250TQLA3	IS64NVP25618EC-250TQLA3	100 QFP, Lead-free
		IS64NVP12836EC-250B3LA3	IS64NVP12832EC-250B3LA3	IS64NVP25618EC-250B3LA3	165 BGA, Lead-free
		IS64NVP12836EC-250B2LA3	IS64NVP12832EC-250B2LA3	IS64NVP25618EC-250B2LA3	119 BGA, Lead-free
	200MHz	IS64NVP12836EC-200B3A3	IS64NVP12832EC-200B3A3	IS64NVP25618EC-200B3A3	165 BGA
		IS64NVP12836EC-200B2A3	IS64NVP12832EC-200B2A3	IS64NVP25618EC-200B2A3	119 BGA
		IS64NVP12836EC-200TQLA3	IS64NVP12832EC-200TQLA3	IS64NVP25618EC-200TQLA3	100 QFP, Lead-free
		IS64NVP12836EC-200B3LA3	IS64NVP12832EC-200B3LA3	IS64NVP25618EC-200B3LA3	165 BGA, Lead-free
		IS64NVP12836EC-200B2LA3	IS64NVP12832EC-200B2LA3	IS64NVP25618EC-200B2LA3	119 BGA, Lead-free

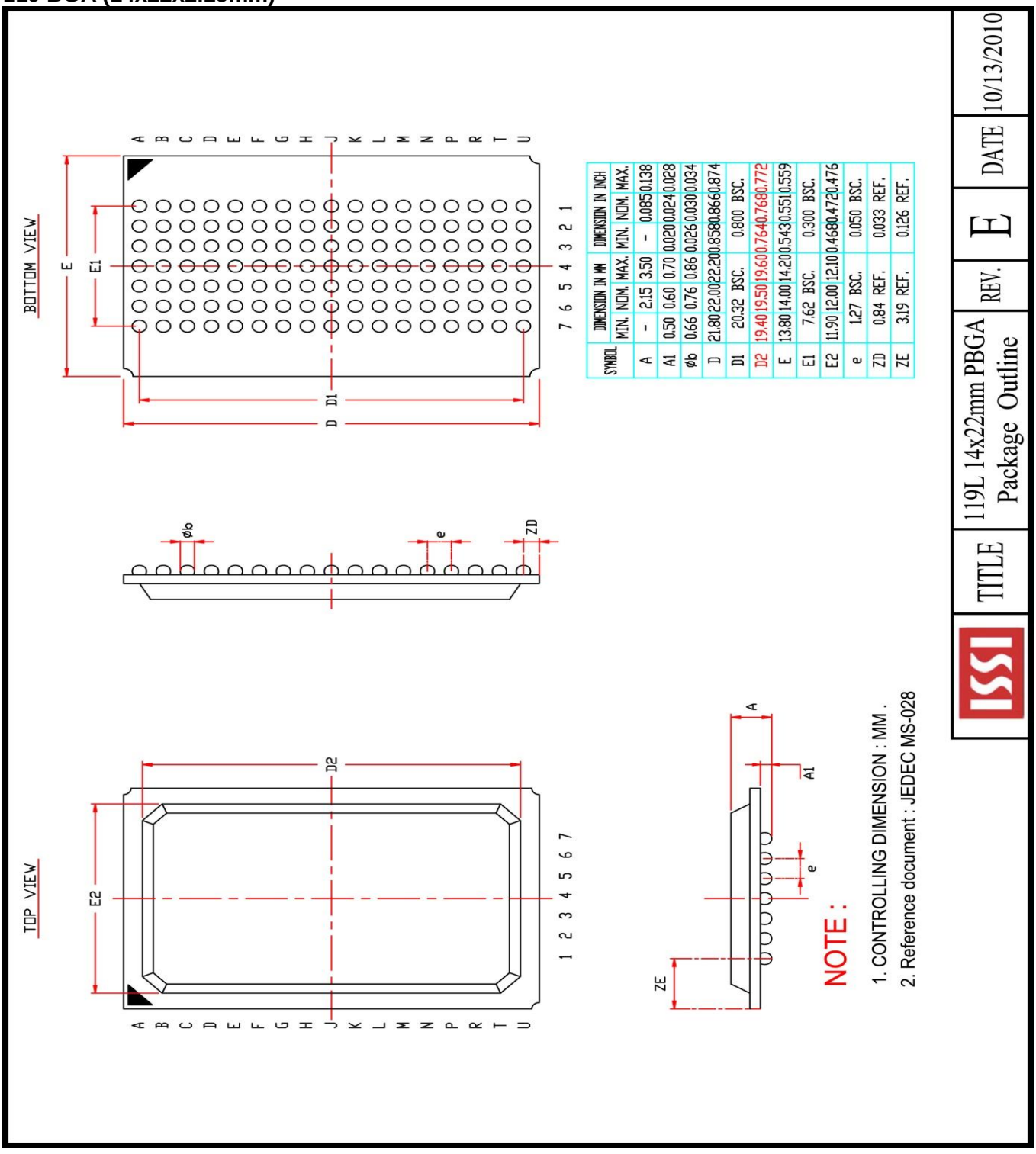
- Note : Not all automotive options listed are currently available. Please contact ISSI for parts

PACKAGE OUTLINE DRAWING

100 QFP (14x20x1.4mm)

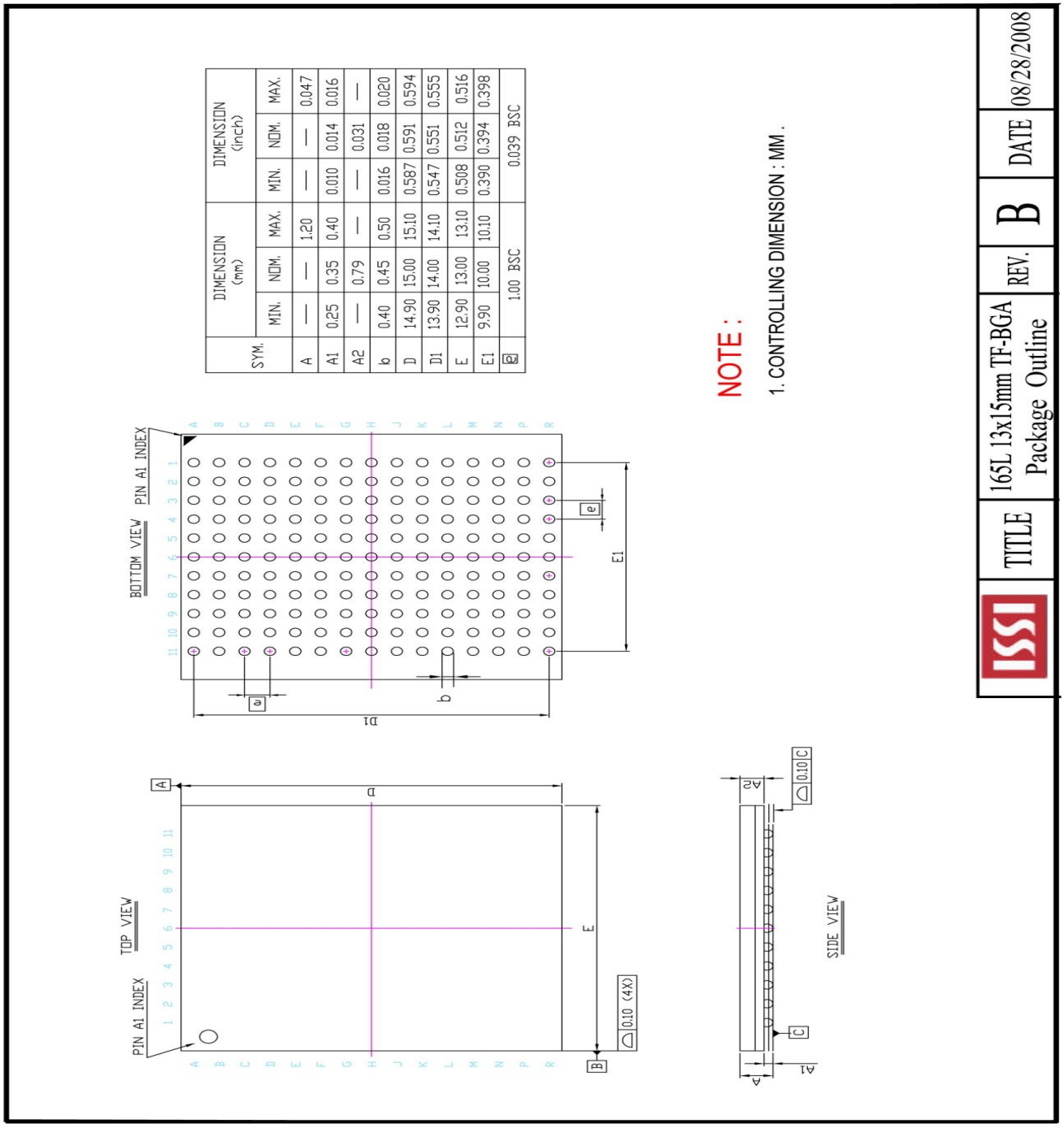


119 BGA (14x22x2.15mm)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	2.15	3.50	–	0.085	0.138
A1	0.50	0.60	0.70	0.020	0.024	0.028
Øb	0.66	0.76	0.86	0.026	0.030	0.034
D	21.80	22.00	22.20	0.858	0.866	0.874
D1		20.32 BSC.			0.800 BSC.	
D2	19.40	19.50	19.60	0.764	0.768	0.772
E	13.80	14.00	14.20	0.543	0.551	0.559
E1		7.62 BSC.			0.300 BSC.	
E2	11.90	12.00	12.10	0.468	0.472	0.476
e		1.27 BSC.			0.050 BSC.	
ZD		0.84 REF.			0.033 REF.	
ZE		3.19 REF.			0.126 REF.	

165 BGA (13x15x1.2mm)



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.35	0.40	0.010	0.014	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		