1M x 16Bits x 2Banks Low Power Synchronous DRAM

Description

These IS42SM/RM/VM16200D are low power 33,554,432 bits CMOS Synchronous DRAM organized as 2 banks of 1,048,576 words x 16 bits. These products are offering fully synchronous operation and are referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve high bandwidth. All input and output voltage levels are compatible with LVCMOS.

Features

- JEDEC standard 3.3V, 2.5V, 1.8V power supply
- Auto refresh and self refresh
- All pins are compatible with LVCMOS interface
- 4K refresh cycle / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full Page for Sequential Burst
  - 4 or 8 for Interleave Burst
- Programmable CAS Latency : 2,3 clocks
- All inputs and outputs referenced to the positive edge of the system clock
- Data mask function by DQM
- Internal dual banks operation
- Burst Read Single Write operation
- Special Function Support
  - PASR(Partial Array Self Refresh)
  - Auto TCSR(Temperature Compensated Self Refresh)
  - Programmable Driver Strength Control
  - Full Strength or 1/2, 1/4, 1/8 of Full Strength
  - Deep Power Down Mode
- Automatic precharge, includes CONCURRENT Auto Precharge Mode and controlled Precharge

Copyright © 2014 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

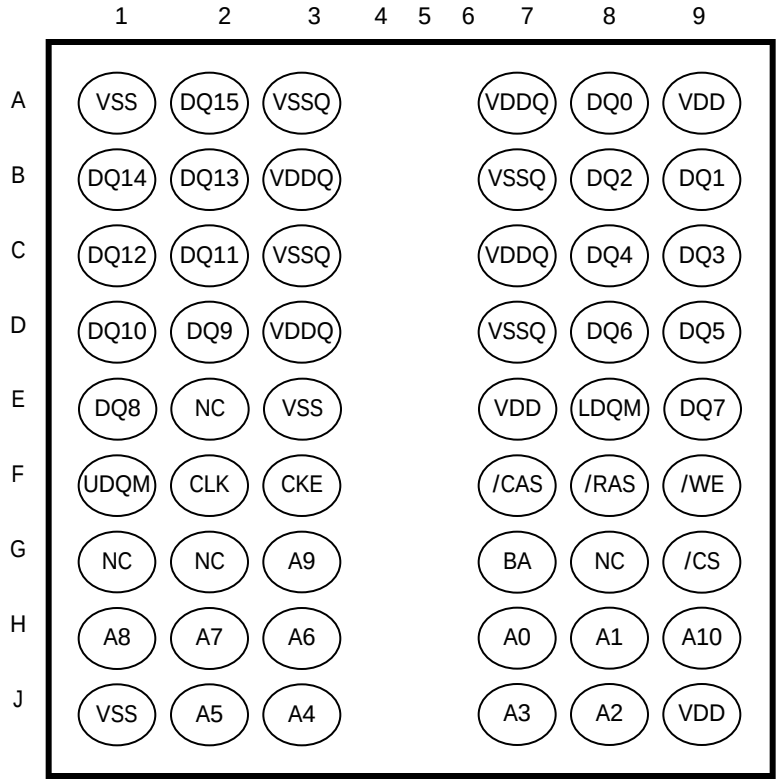
Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

Figure1: 54Ball FBGA Ball Assignment



[Top View]

Table2: Pin Descriptions

Pin	Pin Name	Descriptions
CLK	System Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
/CS	Chip Select	Enable or disable all inputs except CLK, CKE and DQM.
BA	Bank Address	Selects bank to be activated during RAS activity. Selects bank to be read/written during CAS activity.
A0~A10	Address	Row Address : RA0~RA10 Column Address : CA0~CA8 Auto Precharge : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	RAS, CAS and WE define the operation. Refer function truth table for details.
LDQM,UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode.
DQ0~DQ15	Data Input/Output	Data input/output pin.
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers.
NC	No Connection	No connection.

Figure2: Functional Block Diagram

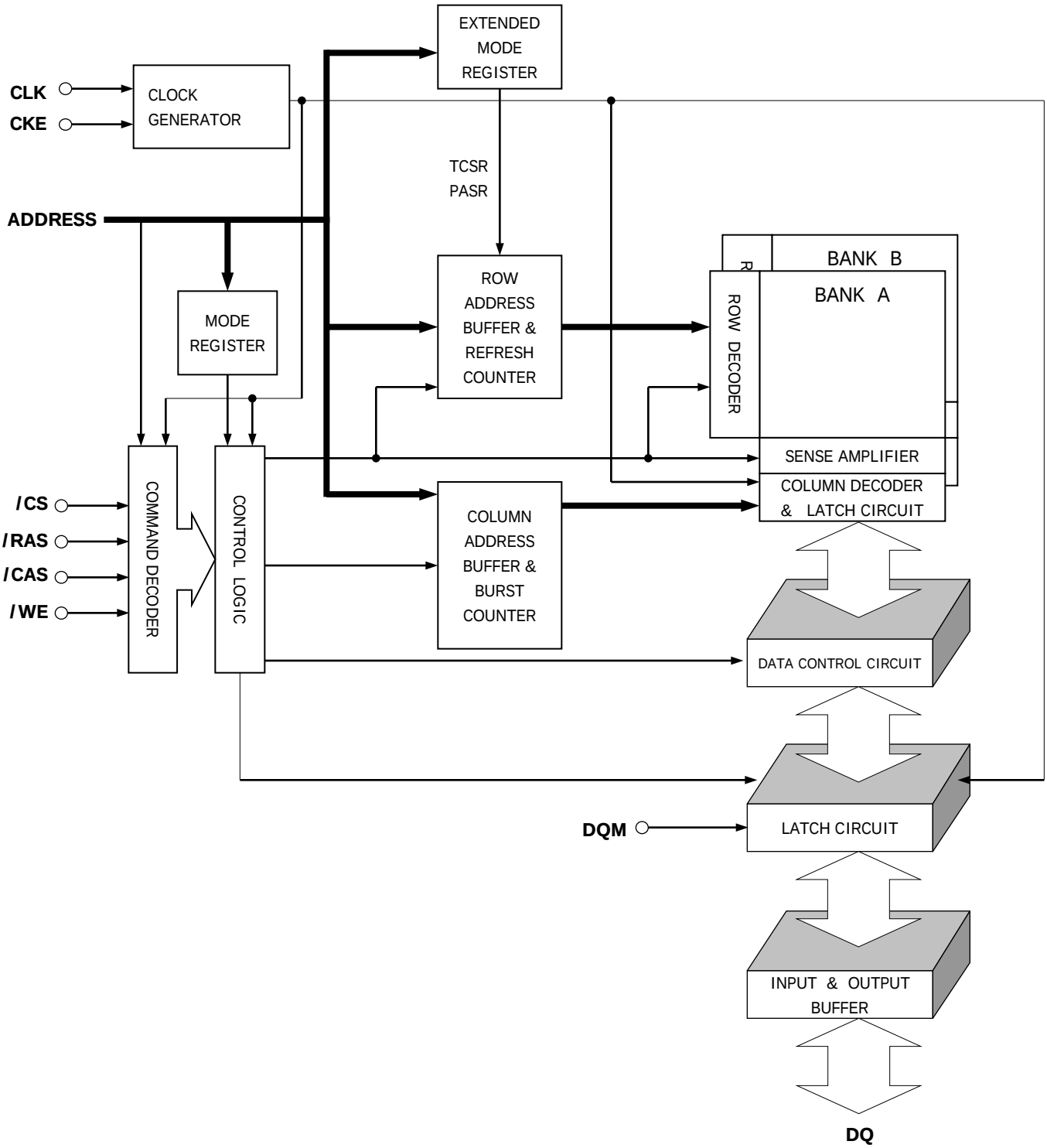


Figure3: Simplified State Diagram

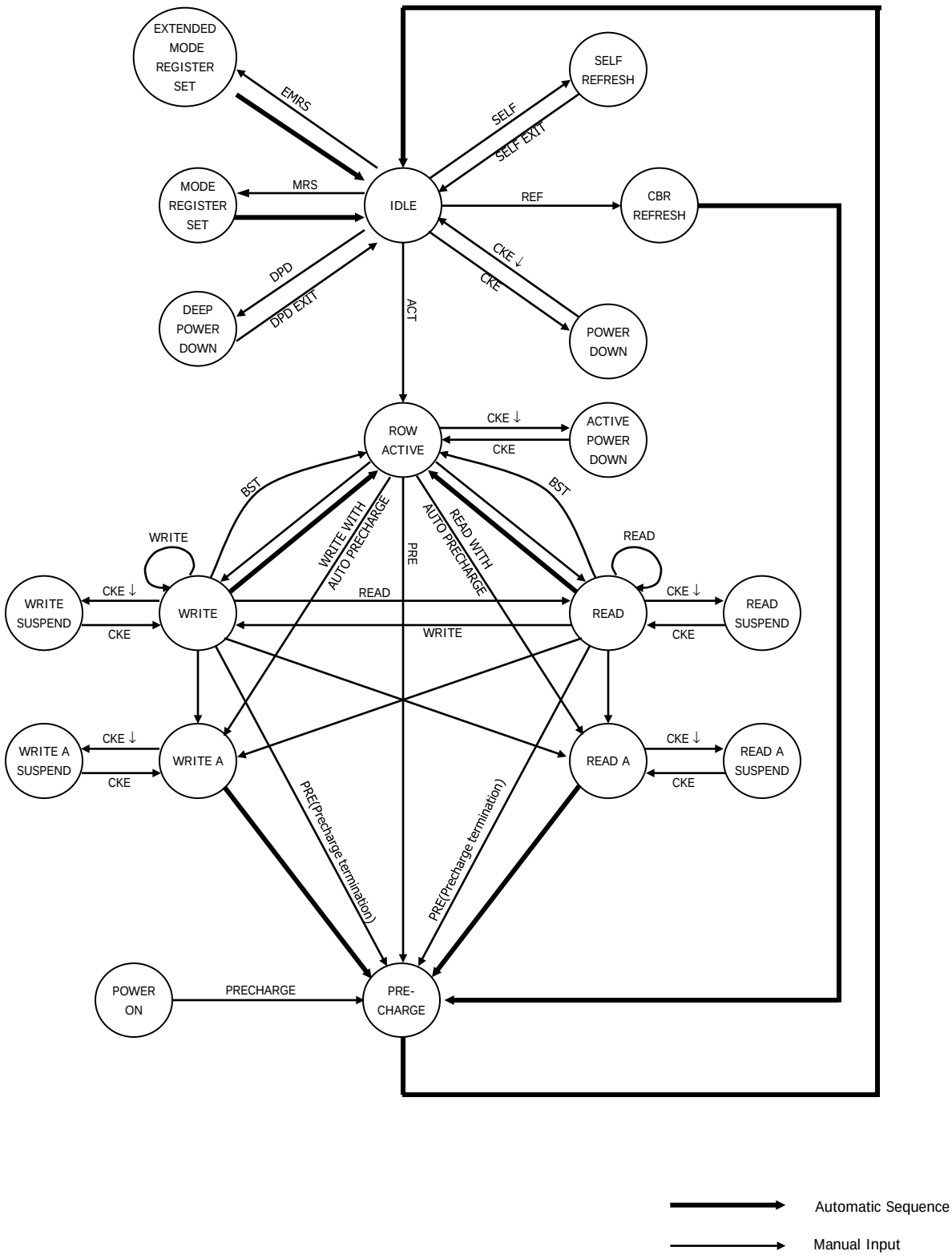
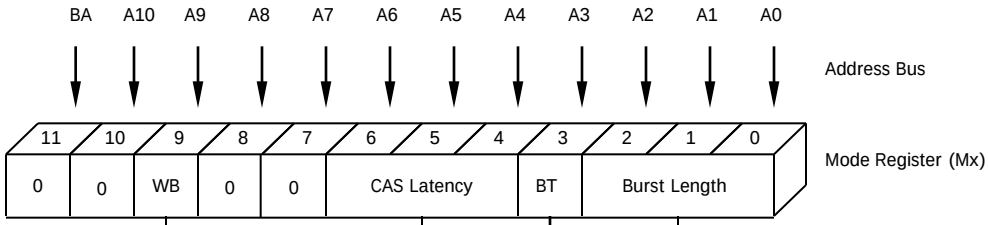


Figure4: Mode Register Definition



M9	Write Burst Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	-
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleave

M2	M1	M0	Burst Length	
			M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Note: M11(BA) must be set to “0” to select Mode Register (vs. the Extended Mode Register)

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

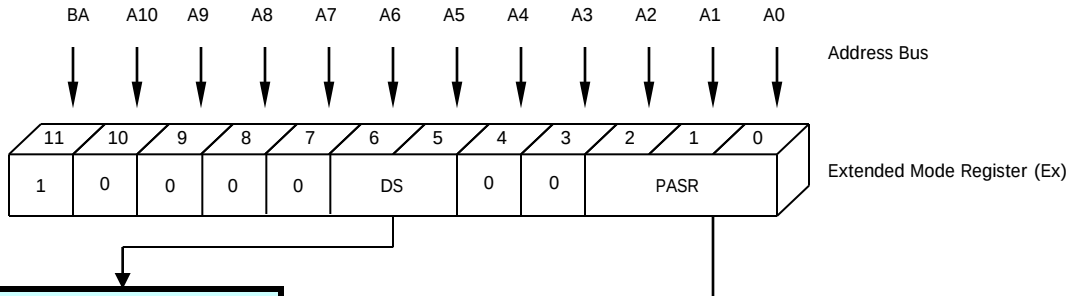
Table 3: Burst Definition

Burst Length	Starting Column Address			Order of Access Within a Burst	
	A2	A1	A0	Sequential	Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page	n=A0-8 (Location 0-511)			C_n, C_n+1. C_n+2, C_n+3, C_n+4... ...C_n-1, C_n...	Not Supported

Note :

1. For full-page accesses: y = 512
2. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A8 select the unique column to be accessed, and mode register bit M3 is ignored.

Figure5: Extended Mode Register



E6	E5	Driver Strength
0	0	Full Strength
0	1	1/2 Strength
1	0	1/4 Strength
1	1	1/8 Strength

E2	E1	E0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	One Bank (BA=0)
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Half of One Bank (BA=0, Row Address MSB=0)
1	1	0	Quarter of One Bank (BA=0, Row Address 2 MSB=0)
1	1	1	Reserved

Note: E11(BA) must be set to “1” to select Extended Mode Register (vs. the base Mode Register)

Functional Description

In general, this 32Mb SDRAM (1M x 16Bits x 2banks) is a dual-bank DRAM that operates at 3.0V/3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 512 columns by 16-bits

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA select the bank, A0-A10 select the row). The address bits (BA select the bank, A0-A8 select the column) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Power up and Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and VDDQ(simultaneously) and the clock is stable(stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. CKE must be held high during the entire initialization period until the PRECHARGE command has been issued. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command. And a extended mode register set command will be issued to program specific mode of self refresh operation(PASR). The following these cycles, the Low Power SDRAM is ready for normal operation.

Register Definition

Mode Register

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 should be set to zero. M11 should be set to zero to prevent extended mode register.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Extended Mode Register

The Extended Mode Register controls the functions beyond those controlled by the Mode Register. These additional functions are special features of the mobile DRAM device. They include Temperature Compensated Self Refresh (TCSR) Control, and Partial Array Self Refresh (PASR) and Driver Strength (DS).

The Extended Mode Register is programmed via the Mode Register Set command (BA=1) and retains the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be programmed with E7 through E10 set to “0”. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 when the burst length is set to two; by A2-A8 when the burst length is set to four; and by A3-A8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Bank(Row) Active

The Bank Active command is used to activate a row in a specified bank of the device. This command is initiated by activating CS, RAS and deasserting CAS, WE at the positive edge of the clock. The value on the BA selects the bank, and the value on the A0-A10 selects the row. This row remains active for column access until a precharge command is issued to that bank. Read and write operations can only be initiated on this activated bank after the minimum tRCD time is passed from the activate command.

Read

The READ command is used to initiate the burst read of data. This command is initiated by activating CS, CAS, and deasserting WE, RAS at the positive edge of the clock. BA input select the bank, A0-A8 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the READ burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses. The length of burst and the CAS latency will be determined by the values programmed during the MRS command.

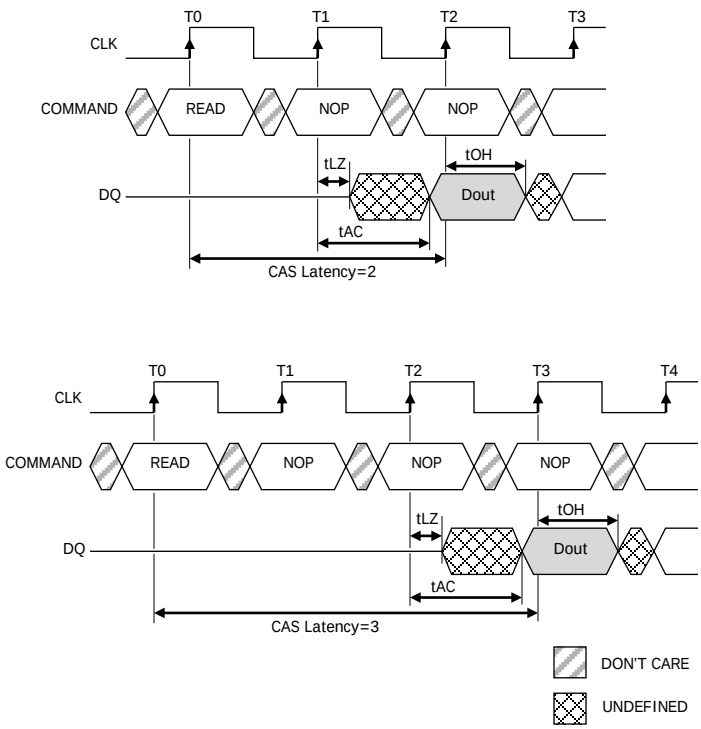
Write

The WRITE command is used to initiate the burst write of data. This command is initiated by activating CS, CAS, WE and deasserting RAS at the positive edge of the clock. BA input select the bank, A0-A8 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the WRITE burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks. If a READ command is registered at clock edge n, and the latency is *m* clocks, the data will be available by clock edge *n* + m. The DQs will start driving as a result of the clock edge one cycle earlier *(n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 6. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure6: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Table4: Command Truth Table

Function	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10	Note
Device Deselect (NOP)	H	X	H	X	X	X	X	X		
No Operation (NOP)	H	X	L	H	H	H	X	X		
Mode Register Set	H	X	L	L	L	L	X	OP CODE		4
Extended Mode Register Set	H	X	L	L	L	L	X	OP CODE		4
Active (select bank and activate row)	H	X	L	L	H	H	X	Bank/Row		
Read	H	X	L	H	L	H	L/H	Bank/Col	L	5
Read with Autoprecharge	H	X	L	H	L	H	L/H	Bank/Col	H	5
Write	H	X	L	H	L	L	L/H	Bank/Col	L	5
Write with Autoprecharge	H	X	L	H	L	L	L/H	Bank/Col	H	5
Precharge All Banks	H	X	L	L	H	L	X	X	H	
Precharge Selected Bank	H	X	L	L	H	L	X	Bank	L	
Burst Stop	H	H	L	H	H	L	X	X		
Auto Refresh	H	H	L	L	L	H	X	X		3
Self Refresh Entry	H	L	L	L	L	H	X	X		3
Self Refresh Exit	L	H	H	X	X	X	X	X		2
			L	H	H	H				
Precharge Power Down Entry	H	L	H	X	X	X	X	X		
			L	H	H	H				
Precharge Down Exit	L	H	H	X	X	X	X	X		
			L	H	H	H				
Clock Suspend Entry	H	L	H	X	X	X	X	X		
			L	V	V	V				
Clock Suspend Exit	L	H	X				X	X		
Deep Power Down Entry	H	L	L	H	H	L	X	X		6
Deep Power Down Exit	L	H	X				X	X		

Note :

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
   H: High Level, L: Low Level, X: Don't Care, V: Valid
2. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high and will put the device in the all banks idle state once tXSR is met. Command Inhibit or NOP commands should be issued on any clock edges occuring during the tXSR period. A minimum of two NOP commands must be provided during tXSR period.
3. During refresh operation, internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
4. A0-A10 define OP CODE written to the mode register, and BA must be issued 0 in the mode register set, and 1 in the extended mode register set.
5. DQM “L” means the data Write/Ouput Enable and “H” means the Write inhibit/Output High-Z. Write DQM Latency is 0 CLK and Read DQM Latency is 2 CLK.
6. Standard SDRAM parts assign this command sequence as Burst Terminate. For Bat Ram parts, the Burst Terminate command is assigned to the Deep Power Down function.

Table5: Function Truth Table

Current State	Command							Action	Note
	/CS	/RAS	/CAS	/WE	BA	A0-A10	Description		
Idle	L	L	L	L	OP CODE		Mode Register Set	Set the Mode Register	14
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	5
	L	L	H	L	BA	X	Precharge	No Operation	
	L	L	H	H	BA	Row Add.	Bank Activate	Activate the Specified Bank and Row	
	L	H	L	L	BA	Col Add./ A10	Write/WriteAP	ILLEGAL	4
	L	H	L	H	BA	Col Add./ A10	Read/ReadAP	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation or Power Down	3
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	3
	L	H	H	L	X	X	Burst Stop	No Operation or Power Down	3
Row Active	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Precharge	7
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add./A10	Write/Write AP	Start Write : Optional AP(A10=H)	6
	L	H	L	H	BA	Col Add./A10	Read/Read AP	Start Read : Optional AP(A10=H)	6
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
	L	H	H	L	X	X	Burst Stop	No Operation	
Read	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst : Start the Precharge	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	Termination Burst : Start Write(AP)	8,9
	L	H	L	H	BA	Col Add./A10	Read/Read AP	Terimination Burst : Start Read(AP)	8
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	H	H	L	X	X	Burst Stop	Burst Stop, Row Active	

Table5: Function Truth Table

Current State	Command							Action	Note
	/CS	/RAS	/CAS	/WE	BA	A0-A10	Description		
Write	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst : Start the Precharge	10
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	Termination Burst : Start Write(AP)	8
	L	H	L	H	BA	Col Add./A10	Read/ReadAP	Terimination Burst : Start READ(AP)	8,9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	H	H	L	X	X	Burst Stop	Burst Stop, Row Active	
Read with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add./A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	H	H	L	X	X	Burst Stop	ILLEGAL	13
Write with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add./A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	H	H	L	X	X	Burst Stop	ILLEGAL	13

Table5: Function Truth Table

Current State	Command							Action	Note
	/CS	/RAS	/CAS	/WE	BA	A0-A10	Description		
Precharging	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	No Operation : Bank(s) Idle after tRP	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add./ A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add./ A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation : Bank(s) Idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation : Bank(s) Idle after tRP	
	L	H	H	L	X	X	Burst Stop	No Operation : Bank(s) Idle after tRP	
Row Activating	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,11,12
	L	H	L	L	BA	Col Add./A10	Write/Write AP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add./A10	Read/Read AP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation : Row Active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation : Row Active after tRCD	
	L	H	H	L	X	X	Burst Stop	No Operation : Row Active after tRCD	
Write Recovering	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	Start Write : Optional AP(A10=H)	
	L	H	L	H	BA	Col Add./A10	Read/Read AP	Start Write : Optional AP(A10=H)	9
	L	H	H	H	X	X	No Operation	No Operation : Row Active after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation : Row Active after tDPL	
	L	H	H	L	X	X	Burst Stop	No Operation : Row Active after tDPL	

Table5: Function Truth Table

Current State	Command							Action	Note
	/CS	/RAS	/CAS	/WE	BA	A0-A10	Description		
Write Recovering with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add./ A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add./ A10	Read/ReadAP	ILLEGAL	4,9,12
	L	H	H	H	X	X	No Operation	No Operation : Precharge after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation : Precharge after tDPL	
	L	H	H	L	X	X	Burst Stop	No Operation : Precharge after tDPL	
Refreshing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add./A10	Write/Write AP	ILLEGAL	13
	L	H	L	H	BA	Col Add./A10	Read/Read AP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation : Idle after tRC	
	H	X	X	X	X	X	Device Deselect	No Operation : Idle after tRC	
	L	H	H	L	X	X	Burst Stop	No Operation : Idle after tRC	
Mode Register Accessing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add./A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add./A10	Read/Read AP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation : Idle after 2 Clock Cycle	
	H	X	X	X	X	X	Device Deselect	No Operation : Idle after 2 Clock Cycle	
	L	H	H	L	X	X	Burst Stop	ILLEGAL	13

Note :

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if tRCD is not satisfied.
7. Illegal if tRAS is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tDPL.
11. Illegal if tRRD is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.
14. Mode Register Set and Extended Mode Register Set is same command truth table except BA.

Table6: CKE Truth Table

Current State	CKE		Command						Action	Note
	Prev Cycle	Current Cycle	/CS	/RAS	/CAS	/WE	BA	A0-A10		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	2
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	3
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	3
	L	H	L	H	H	L	X	X	ILLEGAL	3
	L	H	L	H	L	X	X	X	ILLEGAL	3
	L	H	L	L	X	X	X	X	ILLEGAL	3
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	2
	L	H	H	X	X	X	X	X	Power Down Mode Exit, All Banks Idle	3
			L	H	H	H	X	X		
	L	H	L	L	X	X	X	X	ILLEGAL	3
				X	L	X	X	X		
				X	X	L	X	X		
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
Deep Power Down	H	X	X	X	X	X	X	X	INVALID	2
	L	H	X	X	X	X	X	X	Deep Power Down Mode Exit	6
	L	L	X	X	X	X	X	X	Maintain Deep Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	4
	H	H	L	H	X	X				4
	H	H	L	L	H	X				4
	H	H	L	L	L	H	X	X	Auto Refresh	
	H	H	L	L	L	L	OP CODE		Mode Register Set	5
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	4
	H	L	L	H	X	X				4
	H	L	L	L	H	X				4
	H	L	L	L	L	H	X	X	Entry Self Refresh	5
	H	L	L	L	L	L	OP CODE		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	5
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to Operations of the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Note :

1. H: Logic High, L: Logic Low, X: Don't care
2. For the given current state CKE must be low in the previous cycle.
3. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
4. The address inputs depend on the command that is issued.
5. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
6. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously.
   When exiting deep power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high and is maintained for a minimum 100usec.

Table7A: 3.3V Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Ambient Temperature (Industrial)	T_A	-40 ~ 85	°C
Ambient Temperature (Commercial)		0 ~ 70	
Storage Temperature	T_{STG}	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W

Note :
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table8A: 3.3V Capacitance (T_A=25 °C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	CLK	C_{I1}	2	4	pF
	A0~A10, BA, CKE, /CS, /RAS, /CAS, /WE, L(U)DQM	C_{I2}	2	4	pF
Data Input/Output Capacitance	DQ0~DQ15	C_{IO}	3	5	pF

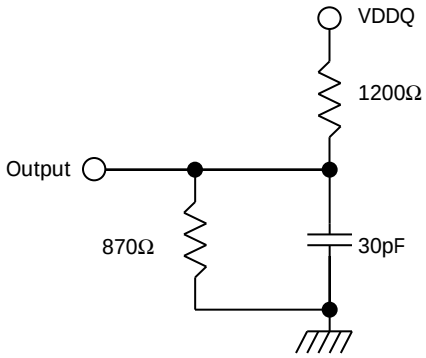
Table9A: 3.3V DC Operating Condition (Voltage referenced to VSS=0V, T_A= -40 ~ 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	2.7	3.3	3.6	V	
	VDDQ	2.7	3.3	3.6	V	1
Input High Voltage	V_{IH}	2.2	-	VDDQ+0.3	V	2
Input Low Voltage	V_{IL}	-0.3	0	0.5	V	3
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH}= -0.1mA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL}= +0.1mA
Input Leakage Current	I_{LI}	-1	-	1	uA	4
Output Leakage Current	I_{LO}	-1.5		1.5	uA	5

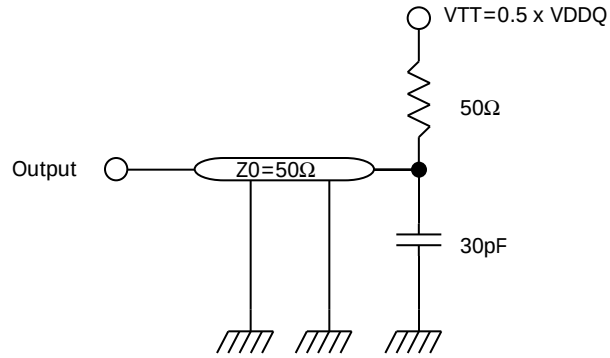
Note :
1. VDDQ must not exceed the level of VDD
2. VIH(max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
3. VIL(min) = -2.0V AC. The overshoot voltage duration is ≤ 3ns.
4. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5. DOUT is disabled, 0V ≤ VOUT ≤ VDDQ.

Table10A: 3.3V AC Operating Condition (T_A= -40 ~ 85 °C, VDD = 2.7V-3.6V, VSS=0V)

Parameter	Symbol	Value	Unit
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	2.4 / 0.4	V
Input Timing Measurement Reference Level Voltage	V_{TRIP}	0.5 x VDDQ	V
Input Rise / Fall Time	t_R / t_F	1 / 1	ns
Output Timing Measurement Reference Level Voltage	V_{OUTREF}	0.5 x VDDQ	V
Output Load Capacitance for Access Time Measurement	C_L	30	pF



DC Output Load Circuit



AC Output Load Circuit

Table7B: 2.5V Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Ambient Temperature (Industrial)	T_A	-40 ~ 85	°C
Ambient Temperature (Commercial)		0 ~ 70	
Storage Temperature	T_{STG}	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 3.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W

Note :

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table8B: 2.5V Capacitance (T_A=25 °C, f=1MHz, VDD=2.5V)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	CLK	C_{I1}	2	4	pF
	A0~A10, BA, CKE, /CS, /RAS, /CAS, /WE, L(U)DQM	C_{I2}	2	4	pF
Data Input/Output Capacitance	DQ0~DQ15	C_{IO}	3	5	pF

Table9B: 2.5V DC Operating Condition (Voltage referenced to VSS=0V, T_A= -40 ~ 85 °C)

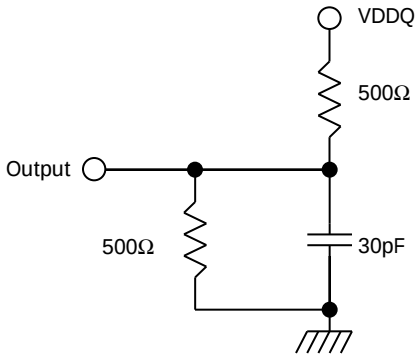
Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	3.0	V	
	VDDQ	2.3	2.5	3.0	V	1
Input High Voltage	V_{IH}	0.8 x VDDQ	-	VDDQ+0.3	V	2
Input Low Voltage	V_{IL}	-0.3	0	0.3	V	3
Output High Voltage	V_{OH}	0.9 x VDDQ	-	-	V	I_{OH}= -0.1mA
Output Low Voltage	V_{OL}	-	-	0.2	V	I_{OL}= +0.1mA
Input Leakage Current	I_{LI}	-1	-	1	uA	4
Output Leakage Current	I_{LO}	-1.5		1.5	uA	5

Note :

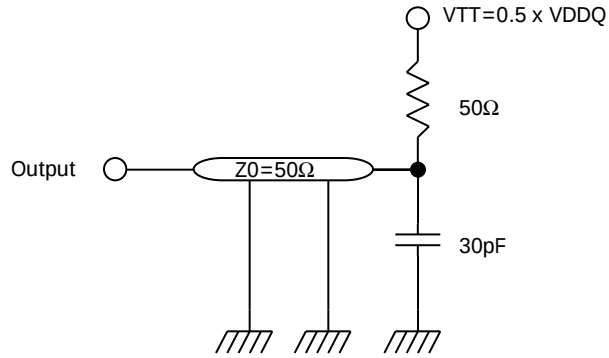
1. VDDQ must not exceed the level of VDD
2. VIH(max) = VDDQ+1.5V AC. The overshoot voltage duration is ≤ 3ns.
3. VIL(min) = -1.0V AC. The overshoot voltage duration is ≤ 3ns.
4. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5. DOUT is disabled, 0V ≤ VOUT ≤ VDDQ.

Table10B: 2.5V AC Operating Condition (T_A= -40 ~ 85 °C, VDD = 2.3V-3.0V, VSS=0V)

Parameter	Symbol	Value	Unit
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	0.9 x VDDQ / 0.2	V
Input Timing Measurement Reference Level Voltage	V_{TRIP}	0.5 x VDDQ	V
Input Rise / Fall Time	t_R / t_F	1 / 1	ns
Output Timing Measurement Reference Level Voltage	V_{OUTREF}	0.5 x VDDQ	V
Output Load Capacitance for Access Time Measurement	C_L	30	pF



DC Output Load Circuit



AC Output Load Circuit

Table7C: 1.8V Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Ambient Temperature (Industrial)	T_A	-40 ~ 85	°C
Ambient Temperature (Commercial)		0 ~ 70	
Storage Temperature	T_{STG}	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 2.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 2.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W

Note :

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table8C: 1.8V Capacitance (T_A=25 °C, f=1MHz, VDD=1.8V)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	CLK	C_{I1}	2	4	pF
	A0~A10, BA, CKE, /CS, /RAS, /CAS, /WE, L(U)DQM	C_{I2}	2	4	pF
Data Input/Output Capacitance	DQ0~DQ15	C_{IO}	3	5	pF

Table9C: 1.8V DC Operating Condition (Voltage referenced to VSS=0V, T_A= -40 ~ 85 °C)

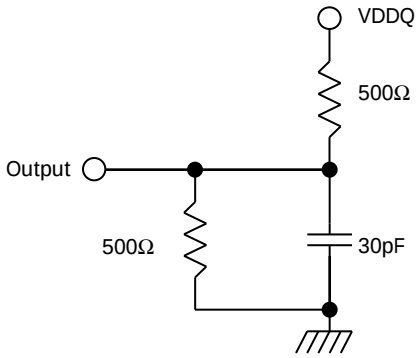
Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	1.7	1.8	1.95	V	
	VDDQ	1.7	1.8	1.95	V	1
Input High Voltage	V_{IH}	0.8 x VDDQ	-	VDDQ+0.3	V	2
Input Low Voltage	V_{IL}	-0.3	0	0.3	V	3
Output High Voltage	V_{OH}	0.9 x VDDQ	-	-	V	I_{OH}= -0.1mA
Output Low Voltage	V_{OL}	-	-	0.2	V	I_{OL}= +0.1mA
Input Leakage Current	I_{LI}	-1	-	1	uA	4
Output Leakage Current	I_{LO}	-1.5		1.5	uA	5

Note :

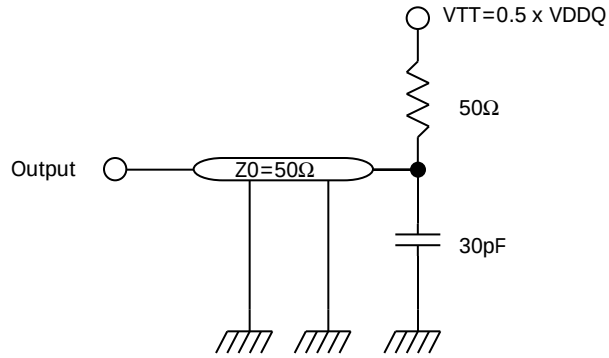
1. VDDQ must not exceed the level of VDD
2. VIH(max) = VDDQ+1.5V AC. The overshoot voltage duration is ≤ 3ns.
3. VIL(min) = -1.0V AC. The overshoot voltage duration is ≤ 3ns.
4. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5. DOUT is disabled, 0V ≤ VOUT ≤ VDDQ.

Table10C: 1.8V AC Operating Condition (T_A= -40 ~ 85 °C, VDD = 1.7V-1.95V, VSS=0V)

Parameter	Symbol	Value	Unit
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	0.9 x VDDQ / 0.2	V
Input Timing Measurement Reference Level Voltage	V_{TRIP}	0.5 x VDDQ	V
Input Rise / Fall Time	t_R / t_F	1 / 1	ns
Output Timing Measurement Reference Level Voltage	V_{OUTREF}	0.5 x VDDQ	V
Output Load Capacitance for Access Time Measurement	C_L	30	pF



DC Output Load Circuit



AC Output Load Circuit

Table11A: 3.3V DC Characteristic (DC operating conditions unless otherwise noted)

Parameter			Sym	Test Condition	Speed		Unit	Note
					-6	-75		
Operating Current			IDD1	Burst Length=1, One Bank Active, tRC ≥ tRC(min) IOL = 0 mA	50	45	mA	1
Precharge Standby Current in Power Down Mode			IDD2P	CKE ≤ VIL(max), tCK = 10ns	200		uA	
			IDD2PS	CKE & CLK ≤ VIL(max), tCK = ∞	200			
Precharge Standby Current in Non Power Down Mode			IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	10		mA	
			IDD2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	4			
Active Standby Current in Power Down Mode			IDD3P	CKE ≤ VIL(max), tCK = 10ns	1		mA	
			IDD3PS	CKE & CLK ≤ VIL(max), tCK = ∞	1			
Active Standby Current in Non Power Down Mode			IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	20		mA	
			IDD3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	10			
Burst Mode Operating Current			IDD4	tCK>tCK(min), IOL = 0 mA, Page Burst All Banks Activated, tCCD = 1 clk	85	80	mA	1
Auto Refresh Current (4K Cycle)			IDD5	tRC ≥ tRFC(min), All Banks Active	40		mA	2
Self Refresh Current	PASR	TCSR	IDD6	CKE ≤ 0.2V			uA	
	2 Banks	45~85°C			250			
		-25~45°C			200			
	1 Bank	45~85°C			210			
		-25~45°C			180			
Deep Power Down Mode Current			IDD7		20		uA	

Note :

1. Measured with outputs open.
2. Refresh period is 64ms.

Table11B: 2.5V DC Characteristic (DC operating conditions unless otherwise noted)

Parameter			Sym	Test Condition	Speed		Unit	Note
					-6	-75		
Operating Current			IDD1	Burst Length=1, One Bank Active, tRC ≥ tRC(min) IOL = 0 mA	50	45	mA	1
Precharge Standby Current in Power Down Mode			IDD2P	CKE ≤ VIL(max), tCK = 10ns	200		uA	
			IDD2PS	CKE & CLK ≤ VIL(max), tCK = ∞	200			
Precharge Standby Current in Non Power Down Mode			IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	10		mA	
			IDD2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	4			
Active Standby Current in Power Down Mode			IDD3P	CKE ≤ VIL(max), tCK = 10ns	1		mA	
			IDD3PS	CKE & CLK ≤ VIL(max), tCK = ∞	1			
Active Standby Current in Non Power Down Mode			IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	20		mA	
			IDD3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	10			
Burst Mode Operating Current			IDD4	tCK>tCK(min), IOL = 0 mA, Page Burst All Banks Activated, tCCD = 1 clk	85	80	mA	1
Auto Refresh Current (4K Cycle)			IDD5	tRC ≥ tRFC(min), All Banks Active	40		mA	2
Self Refresh Current	PASR	TCSR	IDD6	CKE ≤ 0.2V			uA	
	2 Banks	45~85°C			250			
		-25~45°C			200			
	1 Bank	45~85°C			210			
		-25~45°C			180			
Deep Power Down Mode Current			IDD7		20		uA	

Note :

1. Measured with outputs open.
2. Refresh period is 64ms.

Table11C: 1.8V DC Characteristic (DC operating conditions unless otherwise noted)

Parameter			Sym	Test Condition	Speed		Unit	Note
					-6	-75		
Operating Current			IDD1	Burst Length=1, One Bank Active, tRC ≥ tRC(min) IOL = 0 mA	50	45	mA	1
Precharge Standby Current in Power Down Mode			IDD2P	CKE ≤ VIL(max), tCK = 10ns	200		uA	
			IDD2PS	CKE & CLK ≤ VIL(max), tCK = ∞	200			
Precharge Standby Current in Non Power Down Mode			IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	10		mA	
			IDD2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	4			
Active Standby Current in Power Down Mode			IDD3P	CKE ≤ VIL(max), tCK = 10ns	1		mA	
			IDD3PS	CKE & CLK ≤ VIL(max), tCK = ∞	1			
Active Standby Current in Non Power Down Mode			IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2 clks.	20		mA	
			IDD3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞ Input signals are stable.	10			
Burst Mode Operating Current			IDD4	tCK>tCK(min), IOL = 0 mA, Page Burst All Banks Activated, tCCD = 1 clk	85	80	mA	1
Auto Refresh Current (4K Cycle)			IDD5	tRC ≥ tRFC(min), All Banks Active	40		mA	2
Self Refresh Current	PASR	TCSR	IDD6	CKE ≤ 0.2V			uA	
	2 Banks	45~85°C			250			
		-25~45°C			200			
	1 Bank	45~85°C			210			
		-25~45°C			180			
Deep Power Down Mode Current			IDD7		10		uA	

Note :

1. Measured with outputs open.
2. Refresh period is 64ms.

Table12: AC Characteristic (AC operation conditions unless otherwise noted)

Parameter		Sym	-6		-75		Unit	Note
			Min	Max	Min	Max		
CLK Cycle Time	CL = 3	tCK3	6.0	1000	7.5	1000	ns	1
	CL = 2	tCK2	10		10			
Access time from CLK (pos. edge)	CL = 3	tAC3		5.5		6		2
	CL = 2	tAC2		8		8		
CLK High-Level Width		tCH	2.5		2.5			3
CLK Low-Level Width		tCL	2.5		2.5			3
CKE Setup Time		tCKS	1.5		2.0			
CKE Hold Time		tCKH	1.0		1.0			
/CS, /RAS, /CAS, /WE, DQM Setup Time		tCMS	1.5		2.0			
/CS, /RAS, /CAS, /WE, DQM Hold Time		tCMH	1.0		1.0			
Address Setup Time		tAS	1.5		2.0			
Address Hold Time		tAH	1.0		1.0			
Data-In Setup Time		tDS	1.5		2.0			
Data-In Hold Time		tDH	1.0		1.0			
Data-Out High-Impedance Time from CLK (pos.edge)	CL = 3	tHZ3		5.5		6		4
	CL = 2	tHZ2		8		8		
Data-Out Low-Impedance Time		tLZ	1.0		1.0			
Data-Out Hold Time (load)		tOH	2.5		2.5			
Data-Out Hold Time (no load)		tOHN	1.8		1.8			
ACTIVE to PRECHARGE command		tRAS	42	100K	45	100K		
PRECHARGE command period		tRP	18		22.5			
ACTIVE bank a to ACTIVE bank a command		tRC	60		67.5			5
ACTIVE bank a to ACTIVE bank b command		tRRD	12		15			
ACTIVE to READ or WRITE delay		tRCD	18		22.5			
READ/WRITE command to READ/WRITE command		tCCD	1		1		CLK	6
WRITE command to input data delay		tDWD	0		0			6
Data-in to PRECHARGE command		tDPL	12		15		ns	7
Data-in to ACTIVE command		tDAL	30		37.5			7
DQM to data high-impedance during READs		tDQZ	2		2		CLK	6
DQM to data mask during WRITEs		tDQM	0		0			6
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2		2			8
Data-out to high-impedance from PRECHARGE command	CL = 3	tROH3	3		3			6
	CL = 2	tROH2	2		2			
Last data-in to burst STOP command		tBDL	1		1			6
Last data-in to new READ/WRITE command		tCDL	1		1			6
CKE to clock disable or power-down entry mode		tCKED	1		1		CLK	9
CKE to clock enable or power-down exit setup mode		tPED	1		1			9
Refresh period (4,096 refresh cycles)		tREF		64		64	ms	
AUTO REFRESH period		tRFC	80		80		ns	5
Exit SELF REFRESH to ACTIVE command		tXSR	80		80			5
Transition time		tT	0.5	1.2	0.5	1.2		

Note :

1. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including tDPL, and PRECHARGE commands). CKE may be used to reduce the data rate.
2. tAC at CL = 3 with no load is 5.5ns and is guaranteed by design. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter.
3. AC characteristics assume tT = 1ns. If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter.
4. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.
5. Parameter guaranteed by design.
6. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
7. Timing actually specified by tDPL plus tRP; clock(s) specified as a reference only at minimum cycle rate
8. JEDEC and PC100 specify three clocks.
9. Timing actually specified by tCKs; clock(s) specified as a reference only at minimum cycle rate.
10. A new command can be given tRC after self refresh exit.

Special Operation for Low Power Consumption

Temperature Compensated Self Refresh

Temperature Compensated Self Refresh allows the controller to program the Refresh interval during SELF REFRESH mode, according to the case temperature of the Low Power SDRAM device. This allows great power savings during SELF REFRESH during most operating temperature ranges. Only during extreme temperatures would the controller have to select a TCSR level that will guarantee data during SELF REFRESH.

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during Self Refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high, because the refresh rate was set to accommodate the higher temperatures. This temperature compensated refresh rate will save power when the DRAM is operating at normal temperatures.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are Two Bank;all two banks, One Bank;bank a. WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Deep Power Down

Deep Power Down is an operating mode to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. Data will not be retained once the device enters Deep Power Down Mode.

This mode is entered by having all banks idle then /CS and /WE held low with /RAS and /CAS held high at the rising edge of the clock, while CKE is low. This mode is exited by asserting CKE high.

Figure7: Deep Power Down Mode Entry

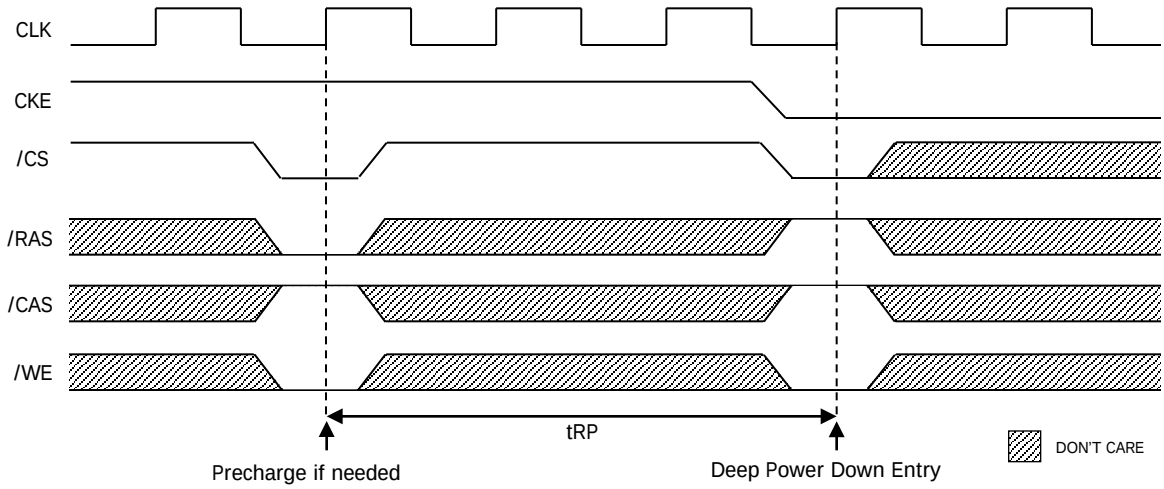
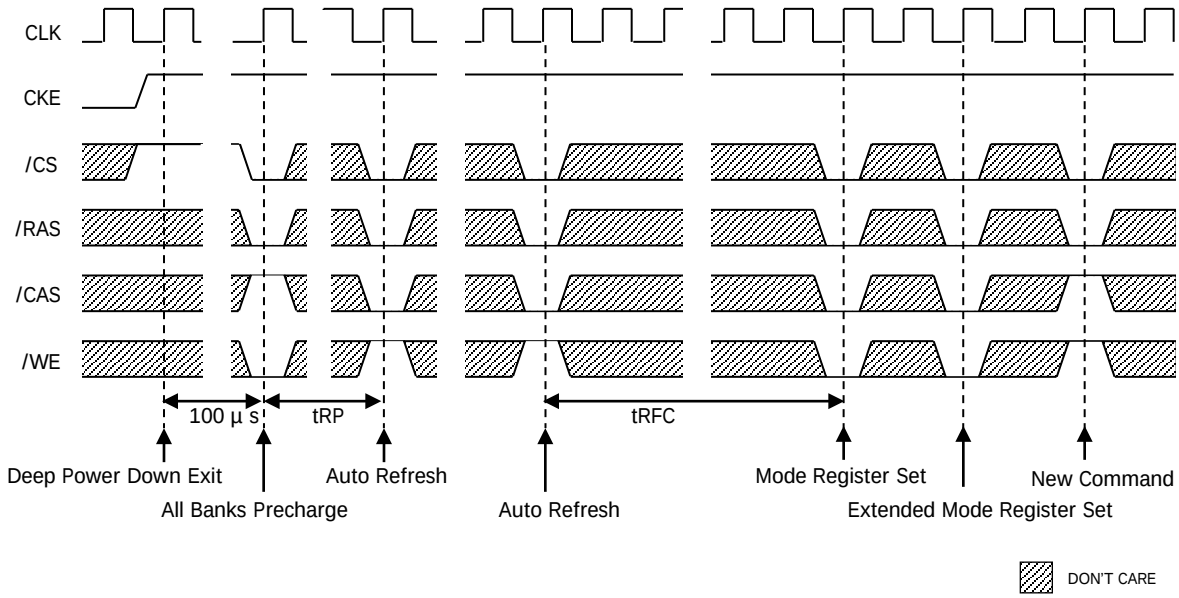


Figure8: Deep Power Down Mode Exit



Ordering Information – VDD = 1.8V

Industrial Range: (-40°C to +85°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
2Mx16	166	6	IS42VM16200D-6BLI	54-ball BGA, Lead-free
	133	7.5	IS42VM16200D-75BLI	54-ball BGA, Lead-free

Ordering Information – VDD = 2.5V

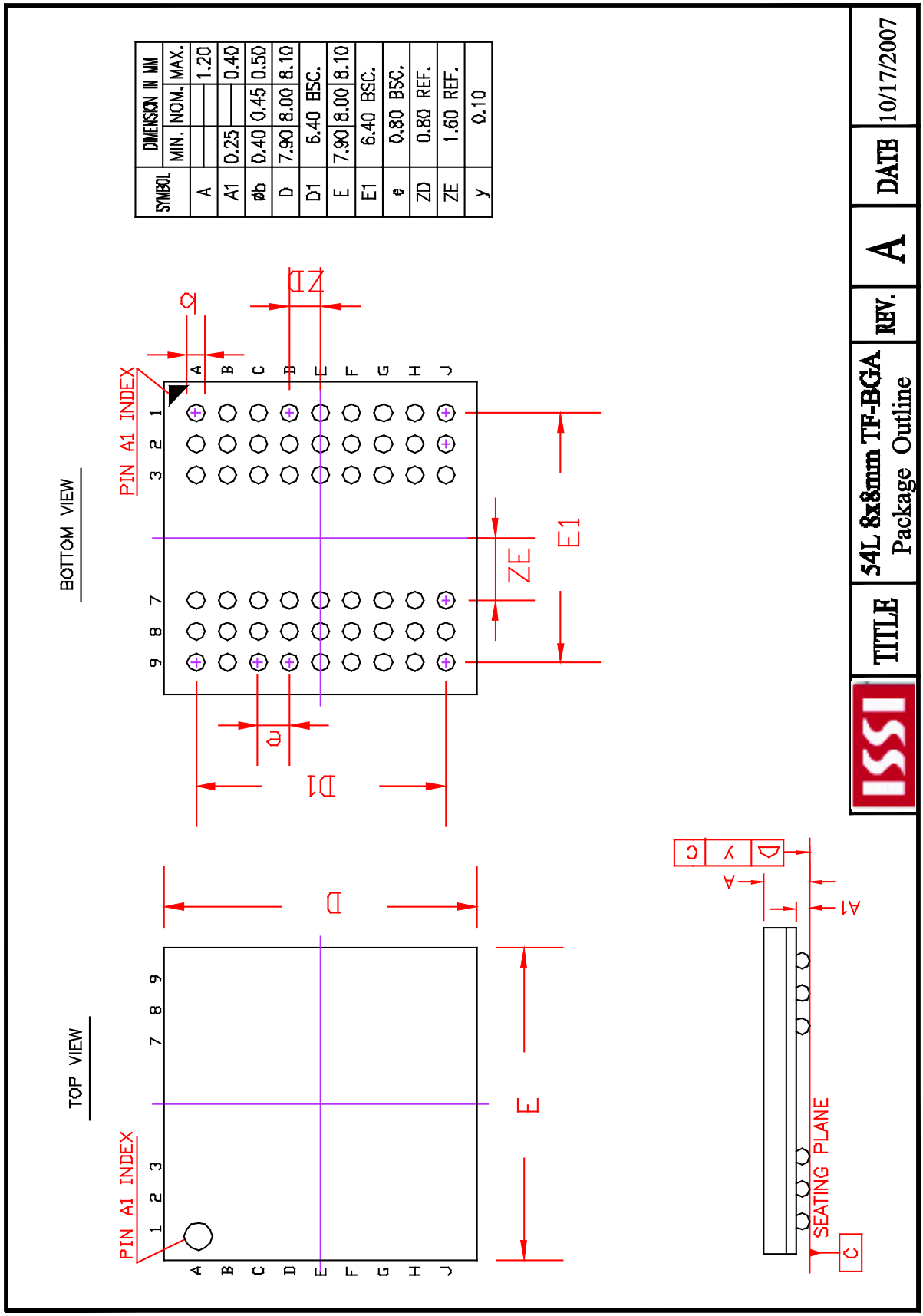
Industrial Range: (-40°C to +85°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
2Mx16	166	6	IS42RM16200D-6BLI	54-ball BGA, Lead-free
	133	7.5	IS42RM16200D-75BLI	54-ball BGA, Lead-free

Ordering Information – VDD = 3.3V

Industrial Range: (-40°C to +85°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
2Mx16	166	6	IS42SM16200D-6BLI	54-ball BGA, Lead-free
	133	7.5	IS42SM16200D-75BLI	54-ball BGA, Lead-free


SYMBOL
DIMENSION IN MM
MIN.
NOM.
MAX.
A
1.20
A1
0.25
0.40
øb
0.40
0.45
0.50
D
7.90
8.00
8.10
D1
6.40 BSC.
E
7.90
8.00
8.10
E1
6.40 BSC.
e
0.80 BSC.
ZD
0.80 REF.
ZE
1.60 REF.
y
0.10
BOTTOM VIEW
PIN A1 INDEX
TOP VIEW
SEATING PLANE
TITLE
54L 8x8mm TF-BGA
Package Outline
REV.
A
DATE
10/17/2007