IS31AP4912

STEREO HEADPHONE DRIVER

January 2016

GENERAL DESCRIPTION

The IS31AP4912 is stereo headphone drivers designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The IS31AP4912 is ideal for small portable electronics where size and cost are critical design parameters.

The IS31AP4912 integrates click-and-pop suppression circuitry and thermal protect circuit. The gain of the amplifier is adjusted via external resistors.

IS31AP4912 is available in UTQFN-12 (2mm × 2mm) packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- No output DC-blocking capacitors
- Supply voltage from 2.7V ~ 5.5V
- Low output noise (7μV)
- High SNR (103dB)
- -95dB PSRR
- Thermal protect circuit
- Integrated click-and-pop suppression circuitry
- UTQFN-12 (2mm × 2mm) package

APPLICATIONS

- Cellular handsets and PDAs
- Notebook PC
- MP3
- Portable gaming

TYPICAL APPLICATION CIRCUIT

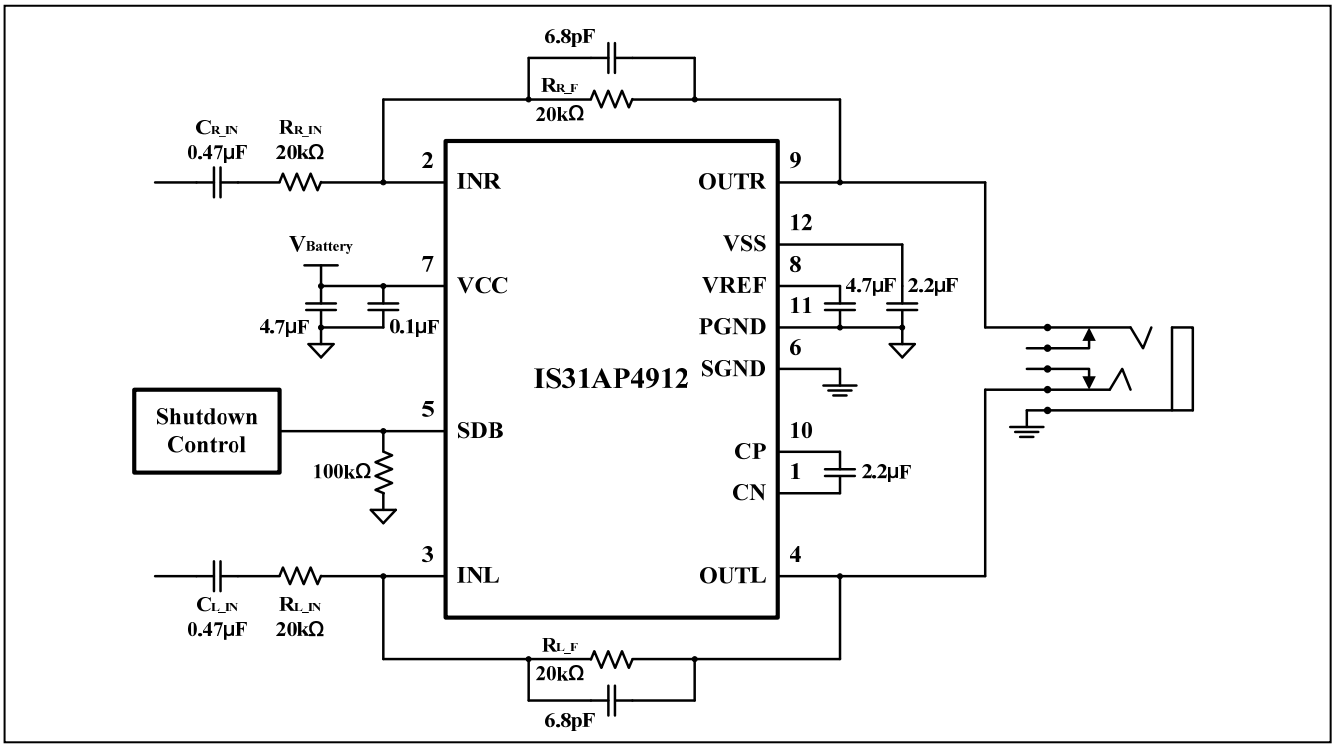
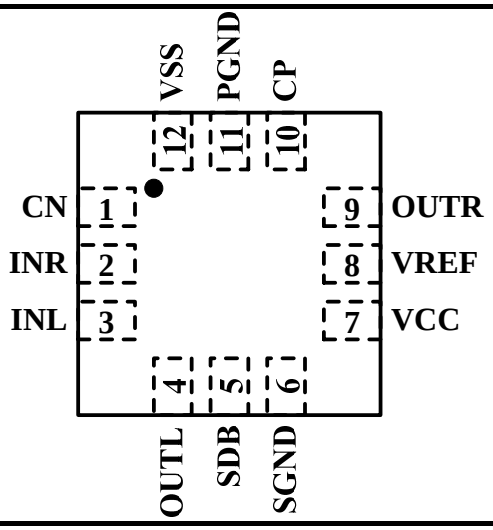


Figure 1 Typical Application Circuit

Note: The SGND and PGND pins of the IS31AP4912 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UTQFN-12	

PIN DESCRIPTION

No.	Pin	Description
1	CN	Charge pump flying capacitor negative terminal.
2	INR	Right channel audio input.
3	INL	Left channel audio input.
4	OUTL	Left channel audio output.
5	SDB	Shutdown control terminal, active low.
6	SGND	Signal Ground.
7	VCC	Supply voltage.
8	VREF	Internal produced supply voltage for charge pump and audio power amplifier.
9	OUTR	Right channel audio output.
10	CP	Charge pump flying capacitor positive terminal.
11	PGND	Power ground.
12	VSS	Output from charge pump.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4912-UTLS2-TR	UTQFN-12, Lead-free	3000

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
Thermal resistance, θ_{JA}	63.1°C/W
ESD (HBM) ESD (CDM)	±8kV ±1kV

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V ~ 5.5V, T_A = 25°C, unless otherwise noted. Typical value is T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent current	No load		3	5.5	mA
I_{SD}	Shutdown current	V_{SDB} = 0V			1	μA
f_{OSC}	Operating frequency			250		kHz
$\|V_{OS}\|$	Output offset voltage	V_{IN} = 0V		1		mV
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.4	V

ELECTRICAL CHARACTERISTICS (NOTE 1)

T_A = 25°C, V_{CC} = 3.6V, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_O	Output power	THD+N = 1%, R_L = 32Ω, f = 1kHz		30		mW
THD+N	Total harmonic distortion plus noise	P_O = 20mW, R_L = 32Ω, f = 1kHz		0.024		%
t_{WU}	Wake-up time from shutdown			39		ms
PSRR	Power supply rejection ratio	V_{P-P} = 200mV, R_L = 32Ω, f = 217Hz		-95		dB
		V_{P-P} = 200mV, R_L = 32Ω, f = 1kHz		-93		dB
V_{NO}	Output voltage noise			7		μV
SNR	Signal-to-noise ratio	P_O = 30mW, THD+N = 0.1%		103		dB

Note 1: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTIC

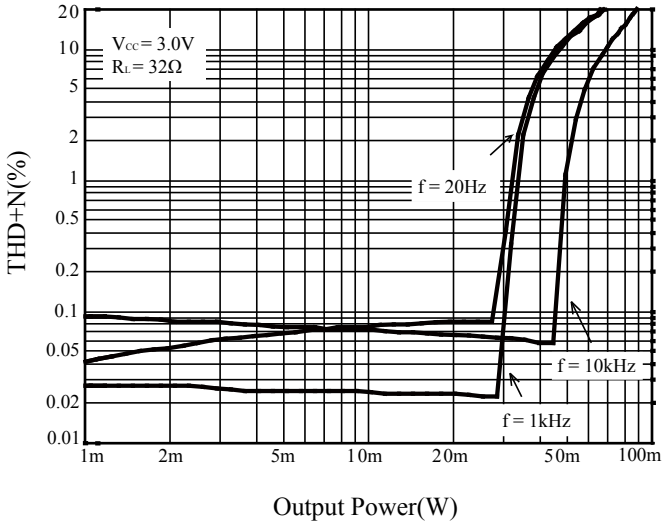


Figure 2 THD+N vs. Output Power

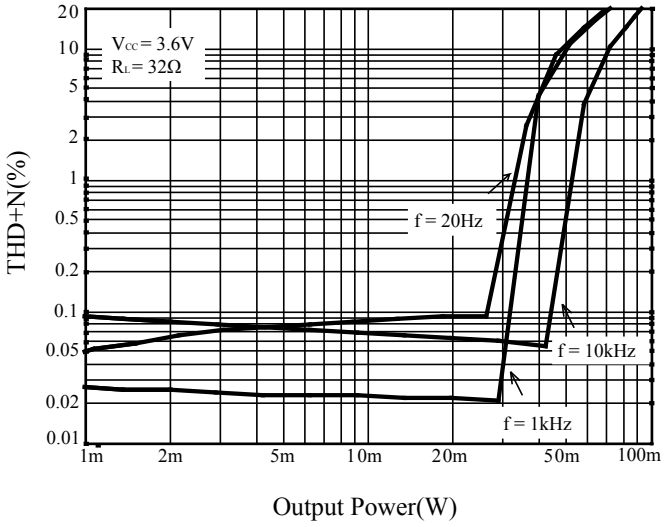


Figure 3 THD+N vs. Output Power

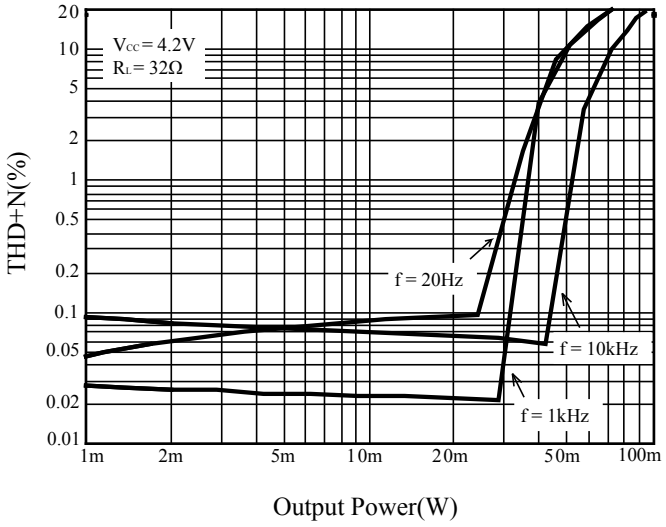


Figure 4 THD+N vs. Output Power

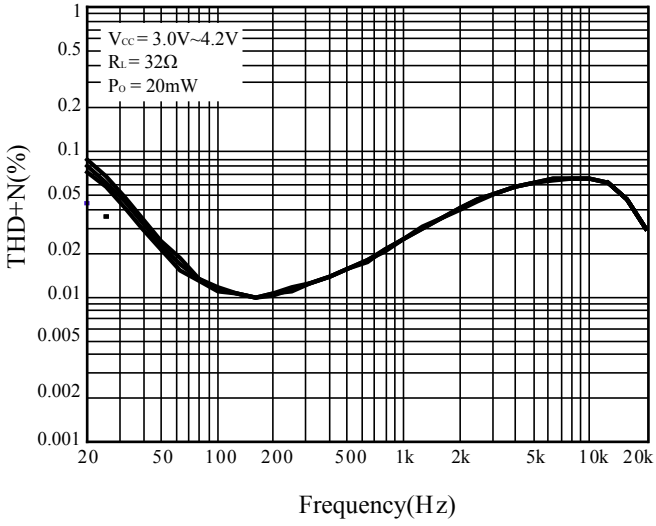


Figure 5 THD+N vs. Frequency

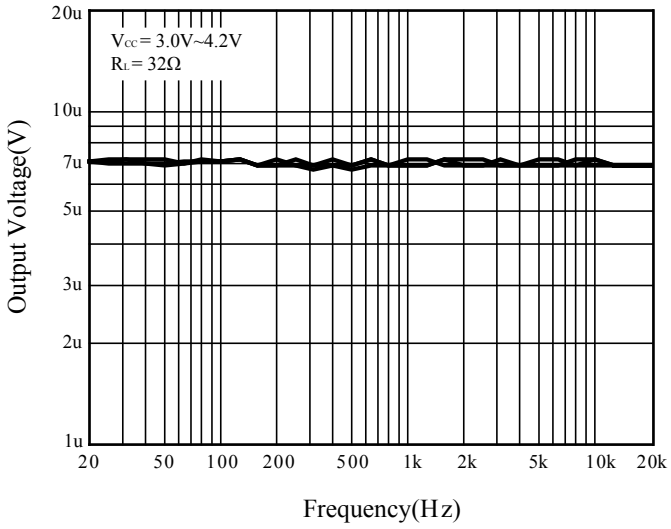


Figure 6 Noise

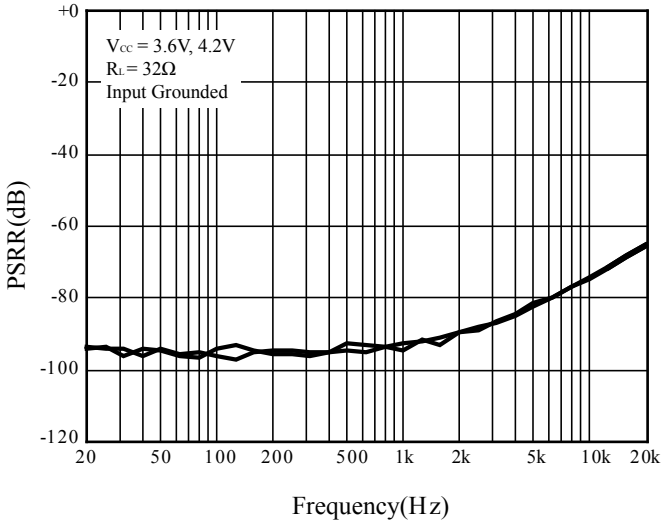
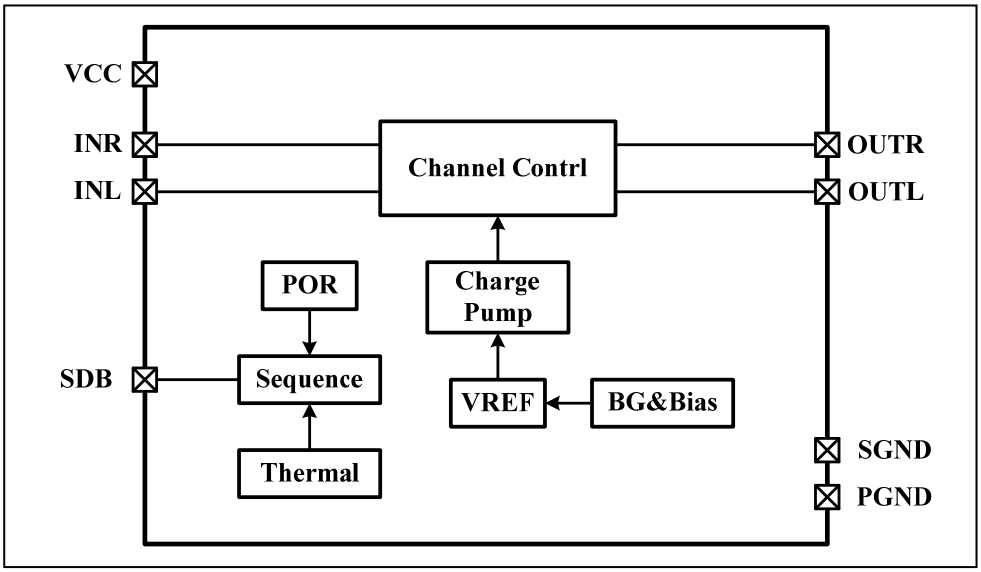


Figure 7 PSRR vs. Frequency

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

CHARGE PUMP CONVERTER

IS31AP4912 integrate a charge pump converter to change input supply voltage (V_{CC}) into a negative voltage providing a 0V reference voltage for output.

The charge pump converter only needs three external components: supply decoupling capacitor, output bypass capacitor and flying capacitor.

Choose low ESR capacitors to ensure the best operating performance and place the capacitors as close as possible to the IS31AP4912.

GAIN SETTING

The input resistors (R_{IN}) and feedback resistors (R_F) set the gain of the amplifier according to Equation (1).

$$Gain = \frac{R_F}{R_{IN}}\left(\frac{V}{V}\right) \qquad (1)$$

For example, in Figure 1:

R_F = 20kΩ, R_{IN} = 20kΩ,

so, $$Gain = \frac{20}{20} = 1\left(\frac{V}{V}\right)$$

Resistor matching is very important in the amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the IS31AP4912 to limit noise injection on the high-impedance nodes.

INPUT CAPACITOR (C_{IN})

The input capacitors and input resistors form a high pass filter with the corner frequency, f_C, determined in Equation (2).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \qquad (2)$$

For example, in Figure 1:

R_{IN} = 20kΩ, C_{IN} = 0.47μF,

so, $$f_c = \frac{1}{2\pi \times 20k\Omega \times 0.47\mu F} \approx 17Hz$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. The capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

DESIGN NOTE

COMPONENT SELECTION

The value and ESR of the output capacitor for charge pump will affect output ripple and transient performance. A X7R or X5R ceramic capacitor in 2.2μF should be recommended. The flying capacitor should use a 2.2μF X7R or X5R ceramic capacitor.

All the capacitors should support at least 10V.

PCB LAYOUT

The decoupling capacitors should be placed close to the VCC pin and the output capacitors should be placed close to the VSS pin. The flying capacitor should be placed close to the CN and CP pins. The input capacitors and input resistors should be placed close to the INR and INL pins and the traces must be parallel to prevent noise. The traces of OUTR and OUTL pins connected to the headphone should be as possible as short and wide. The recommended width is 0.5mm.

Trace width should be at least 0.75mm for the power supply and the ground plane. The SGND and PGND pins of the IS31AP4912 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

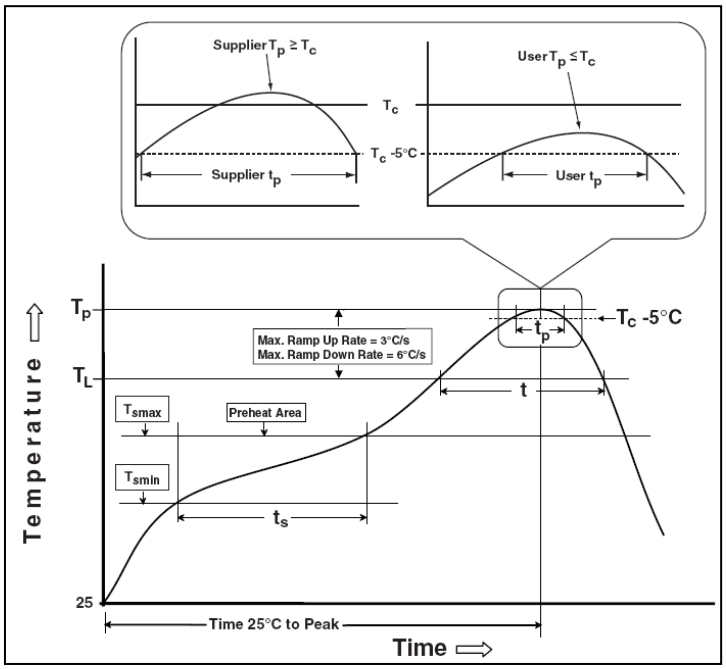
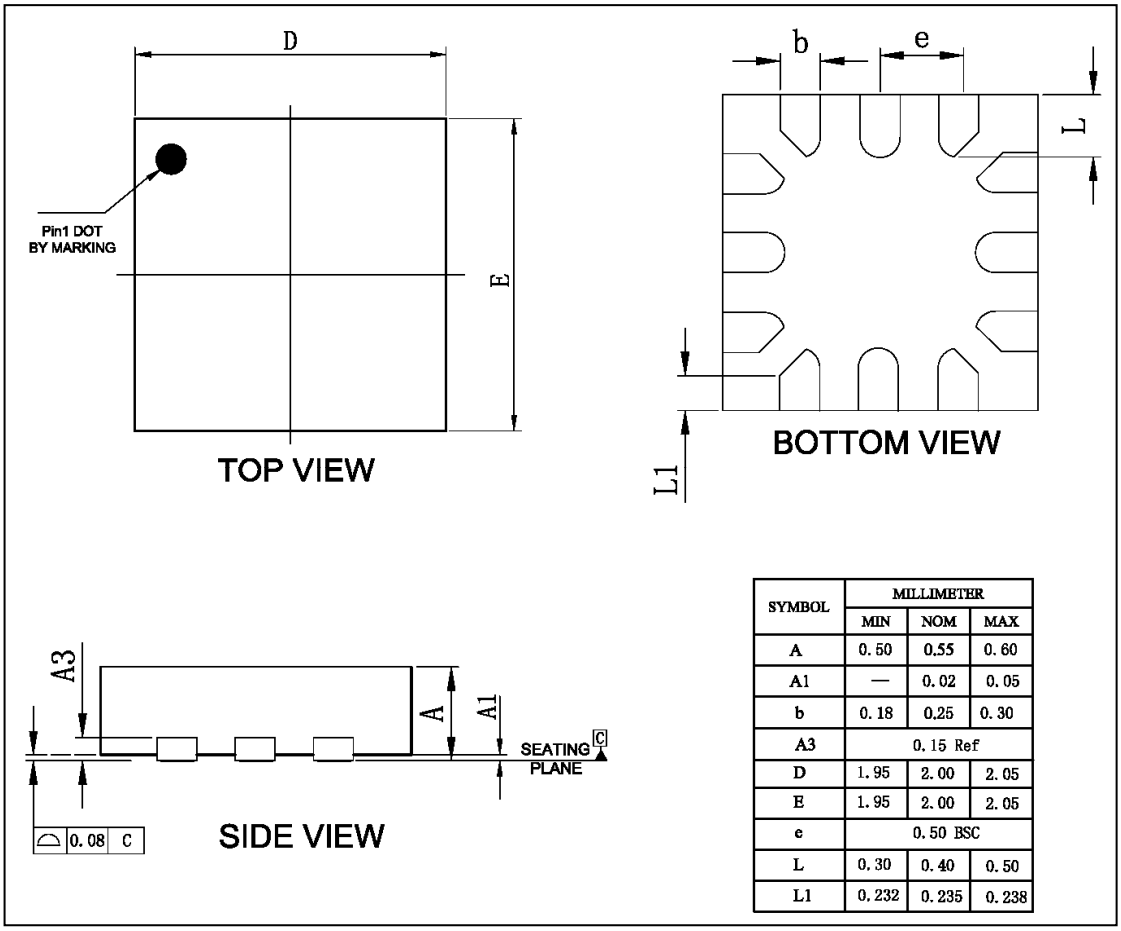


Figure 8 Classification Profile

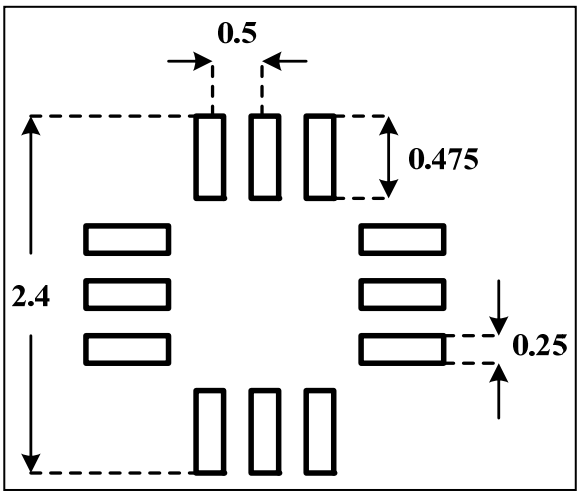
PACKAGING INFORMATION

UTQFN-12



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	—	0.02	0.05
b	0.18	0.25	0.30
A3	0.15 Ref		
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.50 BSC		
L	0.30	0.40	0.50
L1	0.232	0.235	0.238

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.11.17
B	Update POD	2013.06.06
C	1. Add ESD value and θ_{JA} 2. Add land pattern and update POD	2015.12.23