DUAL 2.84W STEREO AUDIO AMPLIFIER PLUS HEADPHONE DRIVER

January 2012

GENERAL DESCRIPTION

The IS31AP4088A is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.84W to a 4Ω load.

To simplify audio system design, the IS31AP4088A combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The IS31AP4088A features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce “clicks and pops” during device turn-on.

APPLICATIONS

- Cell phones, PDA, MP4, PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

KEY SPECIFICATIONS

- P_O at 1% THD+N, V_{DD} = 5V
  R_L = 4Ω ---------- 2.30W (Typ.)
  R_L = 8Ω ---------- 1.38W (Typ.)
- P_O at 10% THD+N, V_{DD} = 5V
  R_L = 4Ω ---------- 2.84W (Typ.)
  R_L = 8Ω ---------- 1.71W (Typ.)
- P_O at 1% THD+N, V_{DD} = 4V
  R_L = 4Ω ---------- 1.40W (Typ.)
  R_L = 8Ω ---------- 0.89W (Typ.)
- Shutdown current ---------- 0.04μA (Typ.)
- Supply voltage range ---------- 2.7V ~ 5.5V
- QFN-16(4mm × 4mm) package

FEATURES

- Suppress “click-and-pop”
- Thermal shutdown protection circuitry
- Stereo headphone amplifier mode
- Micro power shutdown mode

TYPICAL APPLICATION CIRCUIT

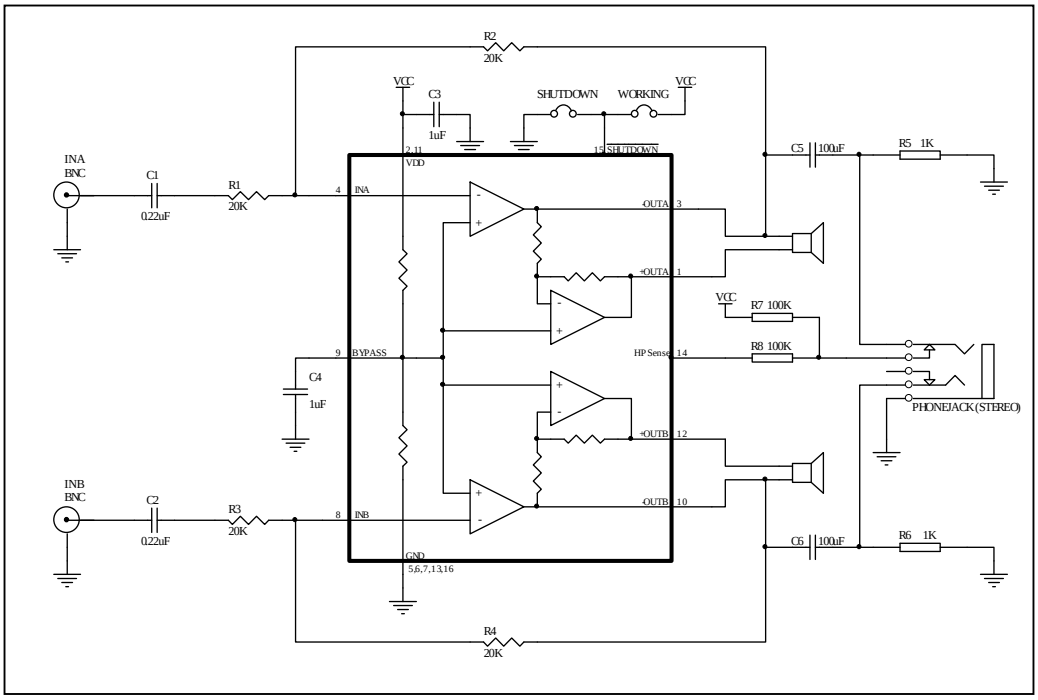
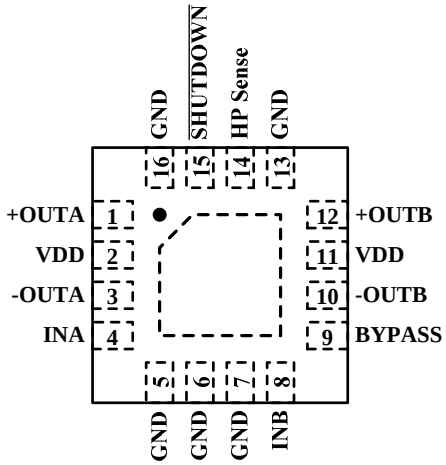


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-16	

PIN DESCRIPTION

No.	Pin	Description
1	+OUTA	Left channel +output.
2,11	VDD	Supply voltage.
3	-OUTA	Left channel –output.
4	INA	Left channel input.
5~7,13,16	GND	GND.
8	INB	Right channel input.
9	Bypass	Bypass capacitor which provides the common mode voltage.
10	-OUTB	Right channel –output.
12	+OUTB	Right channel +output.
14	Hp Sense	Headphone sense control.
15	$\overline{\text{Shutdown}}$	Shut down control, hold low for shutdown mode.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4088A-QFLS2-TR	QFN-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{DD}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	−40°C ~ +85°C
Solder information, Vapor Phase (60s) Infrared (15s)	215°C 220°C

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
V_{DD}	Supply voltage			2.7	V(Min.)
				5.5	V(Max.)
I_{DD}	Quiescent power supply current	Vin = 0V, Io = 0A, BTL Vin = 0V, Io = 0A, SE	5.7 3	7.5 5.5	mA(Max.) mA(max.)
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.036	2	μA(Max.)
V_{IH_SDB}	Shutdown input voltage high			1.4	V(Min.)
V_{IL_SDB}	Shutdown input voltage low			0.4	V(Max.)
V_{IH_HPS}	HP sense input voltage high			3.8	V(Min.)
V_{IL_HPS}	HP sense input voltage low			2.8	V(Max.)
t_{WU}	Turn on time	1μF bypass cap(C4)	113		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN} = 0V	5	30	mV(Max.)
Po	Output power	THD+N = 1%, f = 1kHz, R_L = 8Ω, BTL mode	1.38	1.2	W(Min.)
		THD+N = 10%, f = 1kHz, R_L = 8Ω, BTL mode	1.71	1.5	W(Min.)
		THD+N = 1%, f = 1kHz, R_L = 4Ω, BTL mode	2.30	2.0	W(Min.)
		THD+N = 10%, f = 1kHz, R_L = 4Ω, BTL mode	2.84	2.5	W(Min.)
THD+N	Total harmonic distortion +noise	1kHz, Avd = 2, R_L = 8Ω, Po = 0.4W	0.055		%
PSRR	Power supply rejection Ratio	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	82		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	70		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	80		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	75		dB
X_{talk}	Channel separation	f = 1kHz, C4 = 1μF, BTL mode, 8Ω	-91		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	30		μV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED OPERATION

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
Po	Output power	THD+N = 0.5%,f = 1kHz R_L = 32Ω, SE mode	98.5	83	mW(Min.)
THD+N	Total harmonic distortion+noise	Po = 20mW, 1kHz, R_L = 32Ω	0.013		%
PSRR	Power supply rejection raito	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	84		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	80		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	82		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	80		dB
X_{talk}	Channel separation	f = 1kHz, C6 = 1μF Stereo enhanced control = Low	-68		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	20		μV

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD} = 3V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{DD}	Quiescent power supply current	Vin = 0V, Io = 0A, BTL Vin = 0V, Io = 0A, SE	5 2.6		mA mA
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.02		μA
V_{IH_SDB}	Shutdown input voltage high			1.4	V(min)
V_{IL_SDB}	Shutdown input voltage low			0.4	V(max)
V_{IH_HPS}	HP sense input voltage high			3.8	V(min)
V_{IL_HPS}	HP sense input voltage low			2.8	V(max)
t_{WU}	Turn on time	1μF bypass cap(C4)	120		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{DD} = 3V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN}=0V	2.5		mV
Po	Output power	THD+N = 1%, f = 1kHz,R_L = 8Ω, BTL mode	0.48		W(Min.)
		THD+N = 10%, f = 1kHzR_L = 8Ω, BTL mode	0.6		W(Min.)
		THD+N = 1%, f = 1kHz,R_L = 4Ω, BTL mode	0.78		W(Min.)
		THD+N = 10%, f = 1kHz,R_L = 4Ω, BTL mode	0.97		W(Min.)
THD+N	Total harmonic distortion+noise	1kHz, Avd = 2, R_L = 8Ω, Po = 0.15W	0.078		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	85		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	75		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	84		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	75		dB
X_{talk}	Channel separation	f = 1kHz, C4 = 1μF	-92		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	30		μV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED OPERATION

The following specifications apply for V_{DD} = 3V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
Po	Output power	THD+N = 0.5%, f = 1kHz, R_L = 32Ω	36.7		mW
THD+N	Total harmonic distortion+noise	Po = 20mW, 1kHz, R_L = 32Ω	0.016		%
PSRR	Power supply rejection raito	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C6 = 1μF, R_L = 32Ω	87		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C6 = 1μF, R_L = 32Ω	80		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C6 = 1μF, R_L = 32Ω	82		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C6 = 1μF, R_L = 32Ω	82		dB
X_{talk}	Channel separation	f = 1kHz, C6 = 1μF Stereo enhanced control= Low	-66		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	20		μV

TYPICAL PERFORMANCE CHARACTERISTICS

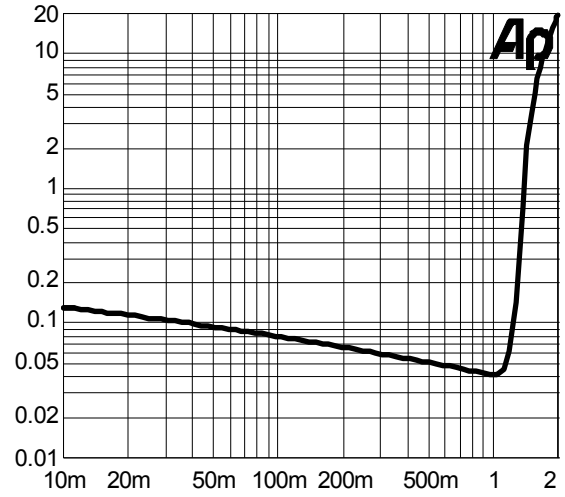


Figure 2 THD+N vs. Output Power 5V, 8Ohm, BTL at f=1kHz

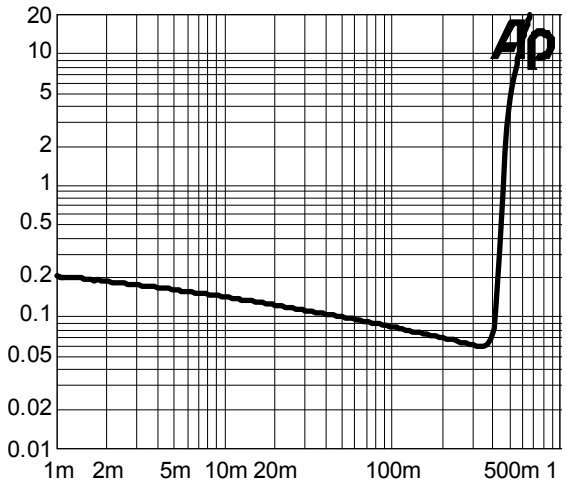


Figure 3 THD+N vs. Output Power 3V, 8Ohm, BTL at f=1kHz

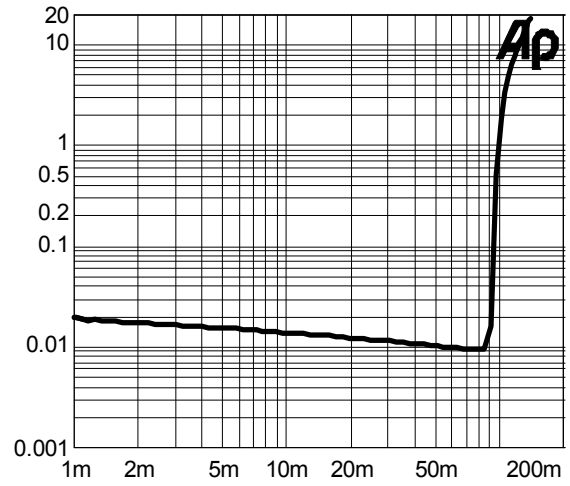


Figure 4 THD+N vs. Output Power SE mode, 5V, 32Ohm, f=1kHz

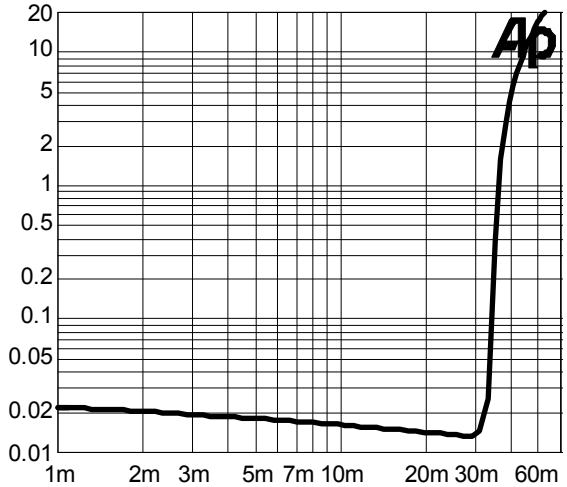


Figure 5 THD+N vs. Output Power SE mode, 3V, 32Ohm, f=1kHz

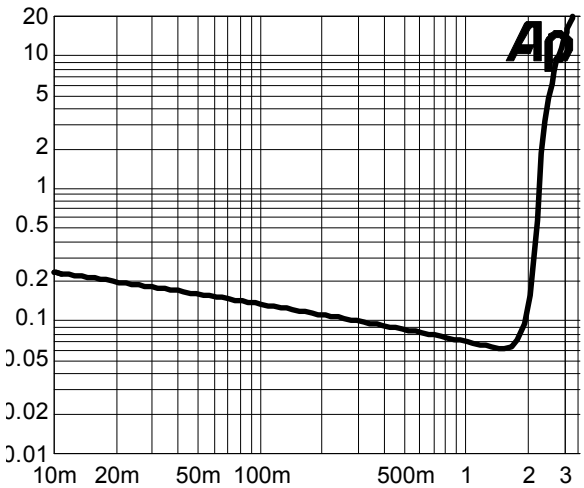


Figure 6 THD+N vs. Output Power

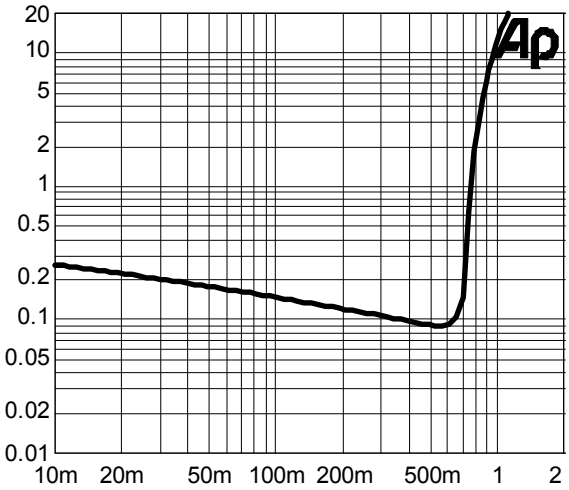


Figure 7 THD+N vs. Output Power BTL mode, 3V, 4Ohm, f=1kHz

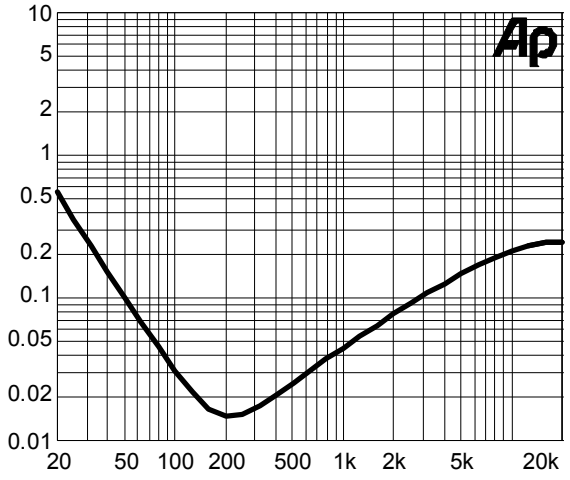


Figure 8 THD+N vs. Frequency BTL mode, 5V, 8Ohm, Po=800mW

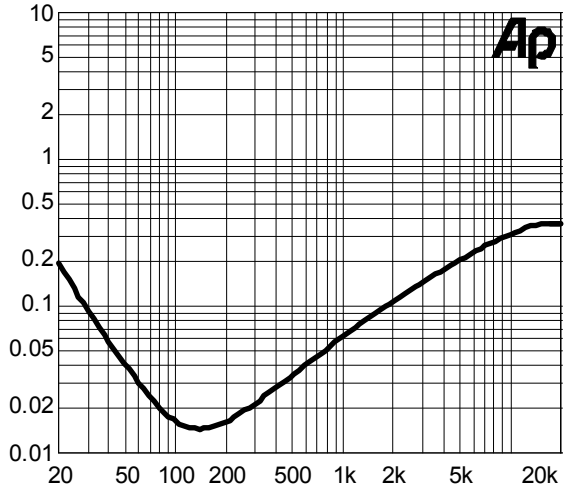


Figure 9 THD+N vs. Frequency BTL mode, 3V, 8Ohm, Po=300mW

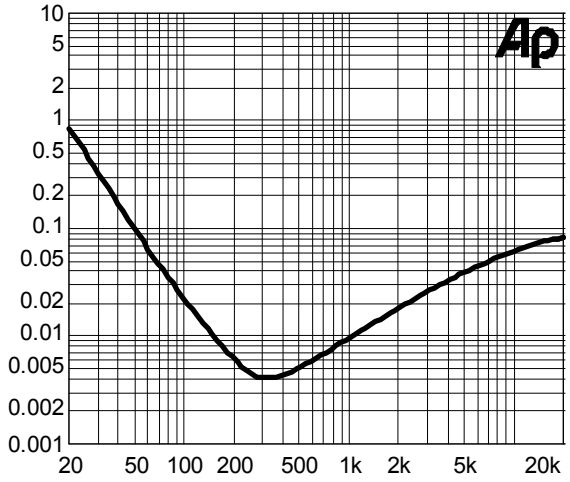


Figure 10 THD+N vs. Frequency SE mode, 5V, 32Ohm, Po=70mW

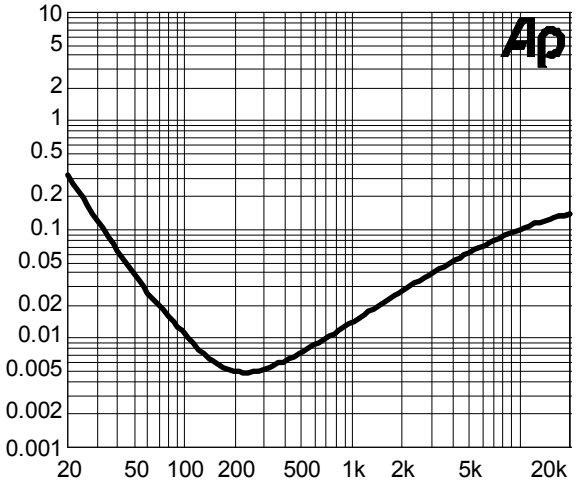


Figure 11 THD+N vs. Frequency SE mode, 3V, 32Ohm, Po=20mW

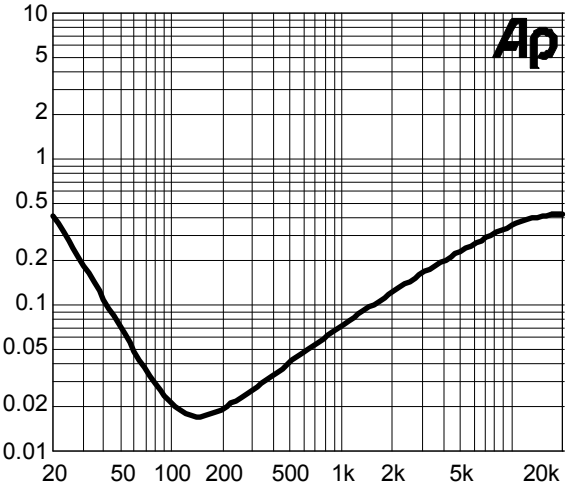


Figure 12 THD+N vs. Frequency BTL mode, 5V, 4Ohm, Po=1W

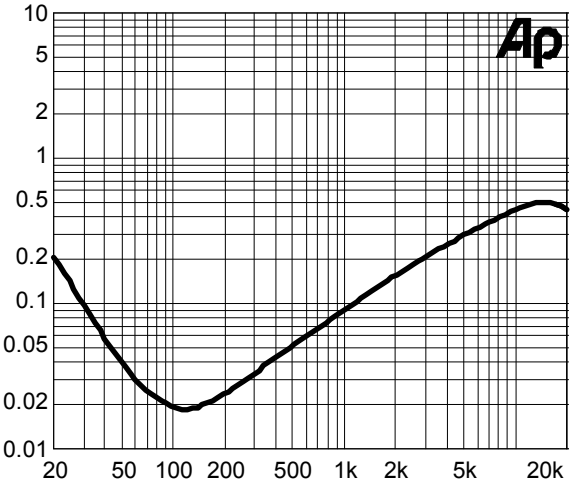


Figure 13 THD+N vs. Frequency BTL mode, 3V, 4Ohm, Po=500mW

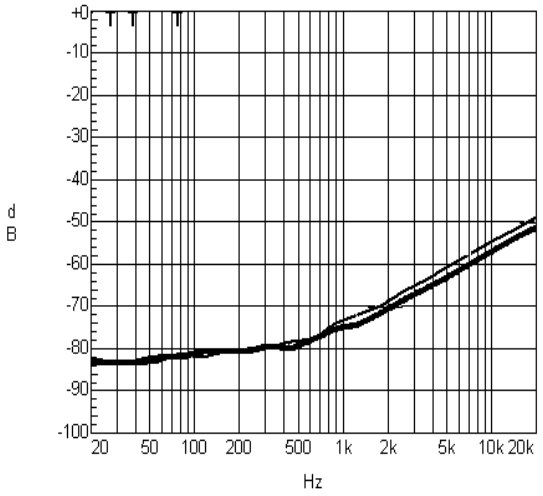


Figure 14 PSRR vs. Freq BTL mode, 5V, 8Ohm, 200mVpp Input terminated

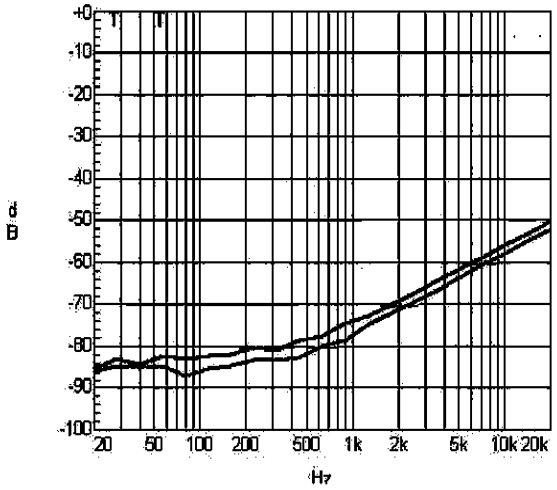


Figure 15 PSRR vs. Freq BTL mode, 3V, 8Ohm, 200mVpp Input terminated

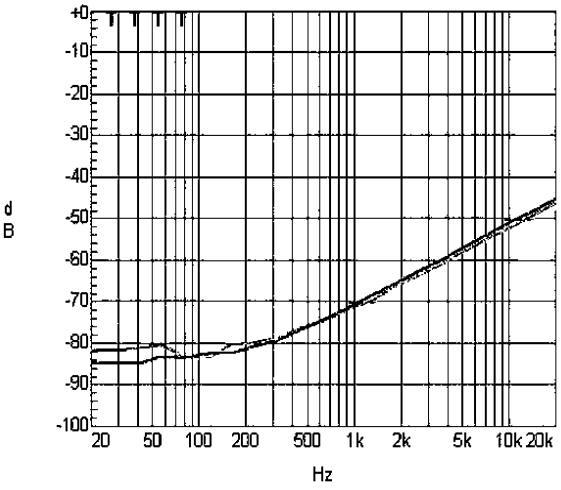


Figure 16 PSRR vs. Freq BTL mode, 5V, 8Ohm, 200mVpp Input unterminated

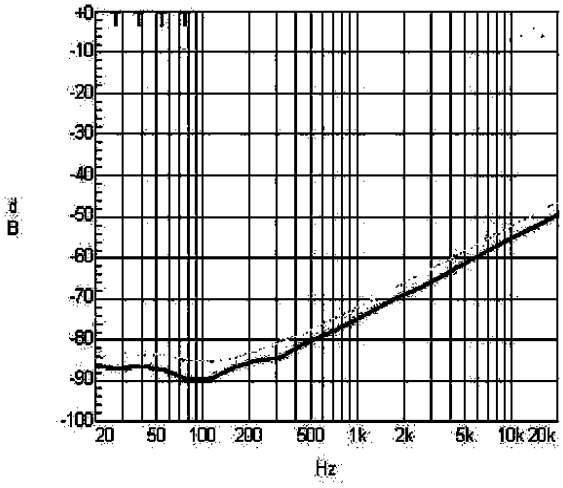


Figure 17 PSRR vs. Freq BTL mode, 3V, 8Ohm, 200mVpp Input unterminated

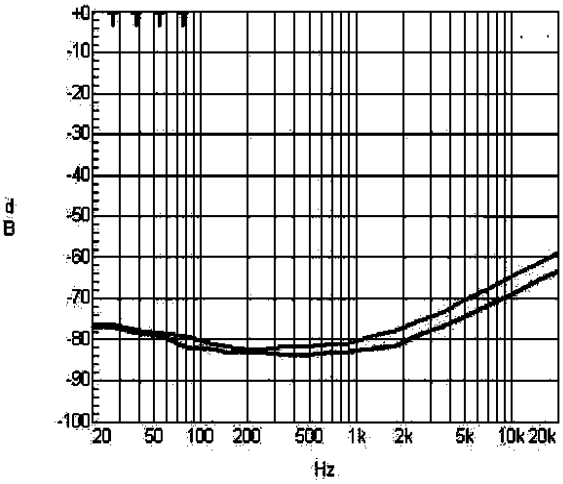


Figure 18 PSRR vs. Freq SE mode, 5V, 32Ohm, 200mVpp Input terminated

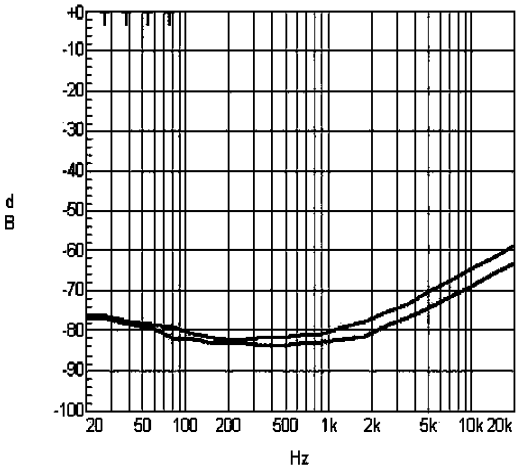


Figure 19 PSRR vs. Freq SE mode, 3V, 32Ohm, 200mVpp Input terminated

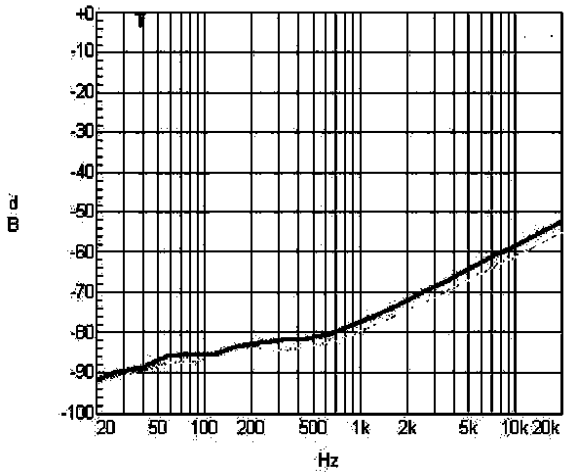


Figure 20 PSRR vs. Freq SE mode, 5V, 32Ohm, 200mVpp Input unterminated

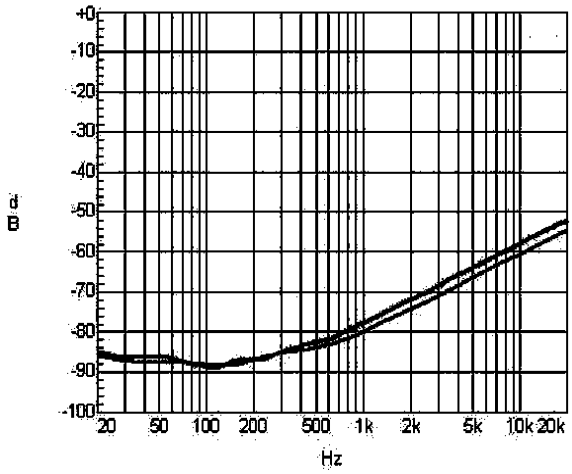


Figure 21 PSRR vs. Freq SE mode, 3V, 32Ohm, 200mVpp Input unterminated

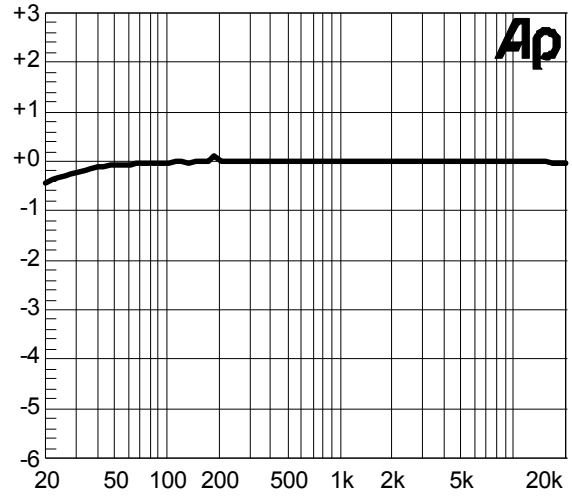


Figure 22 Frequency Response BTL mode, 5V, 8Ohm

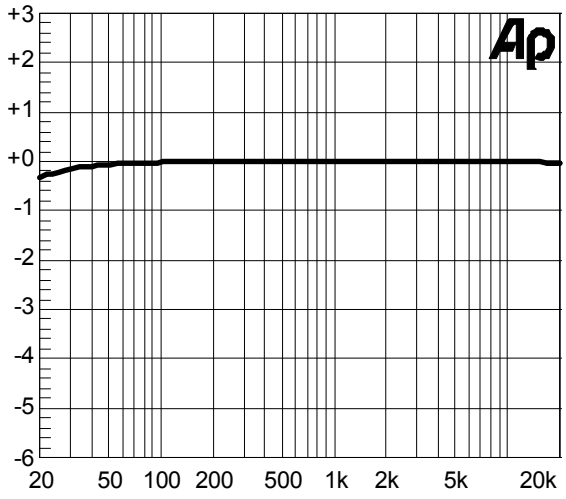


Figure 23 Frequency Response BTL mode, 3V, 8Ohm

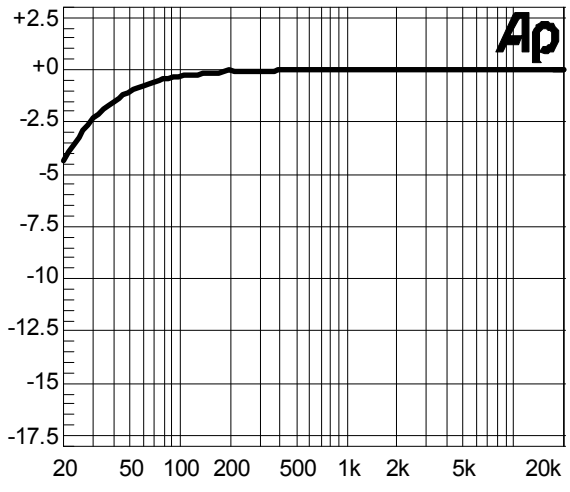


Figure 24 Frequency Response SE mode, 5V, 32Ohm, C5/C6=220uF

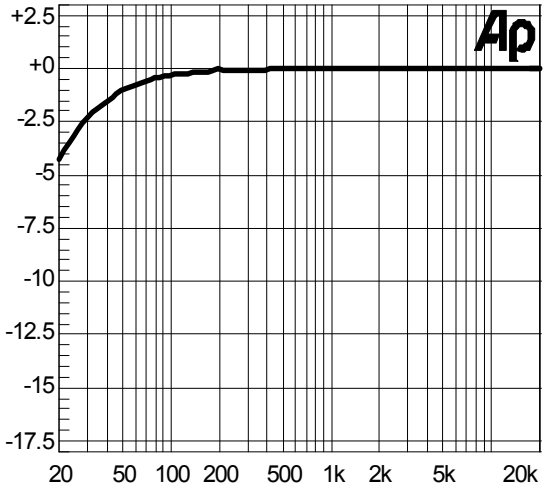


Figure 25 Frequency Response SE mode, 3V, 32Ohm, C5/C6=220uF

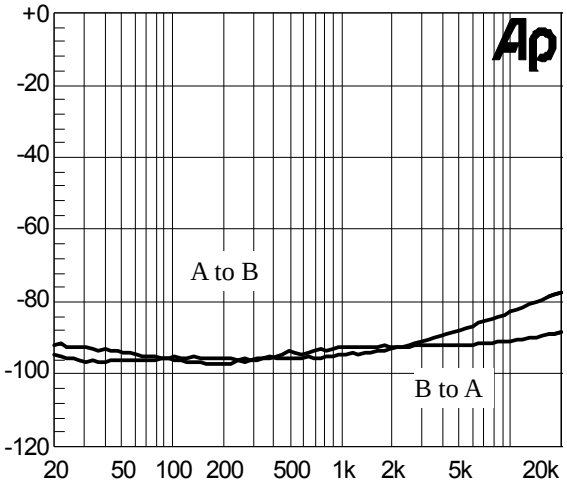


Figure 26 Crosstalk BTL mode, 5V, 8Ohm, Po=1W

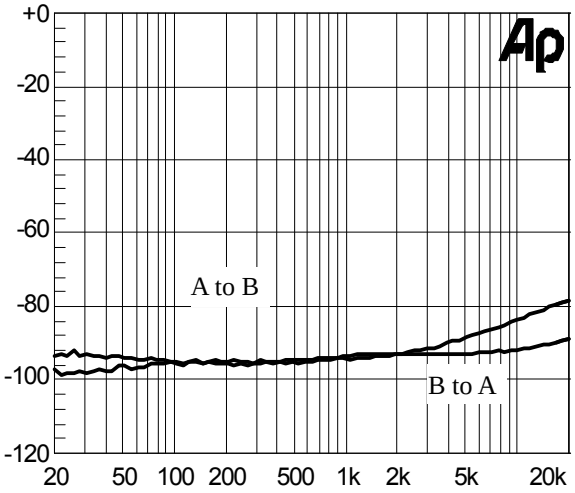


Figure 27 Crosstalk BTL mode, 3V, 8Ohm, Po=0.3W

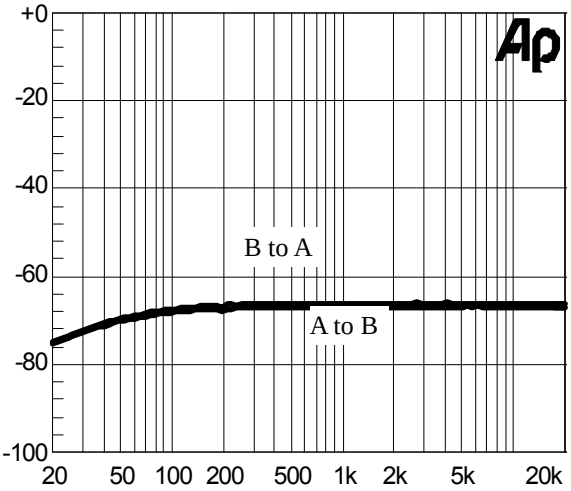


Figure 28 Crosstalk SE mode, 5V, 32Ohm, Po=80mW

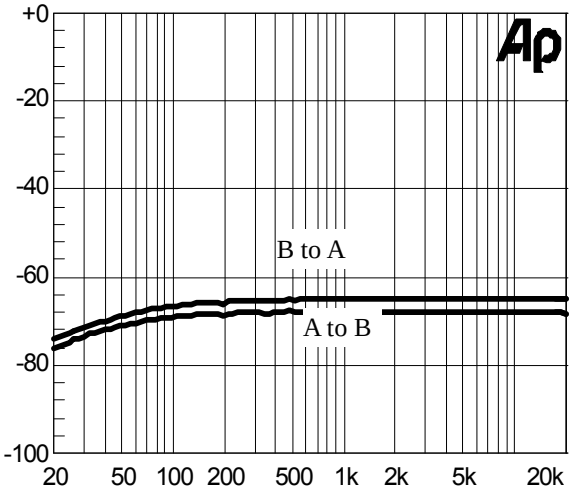


Figure 29 Crosstalk SE mode, 3V, 32Ohm, Po=30mW

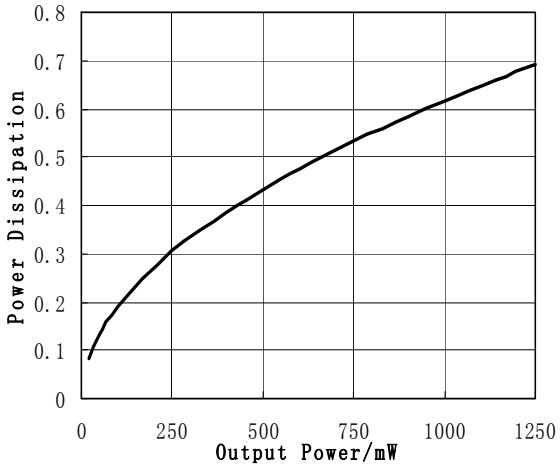


Figure 30 Power Dissipation vs. Output Power BTL mode, 5V, f=1 kHz, RL=8Ohm, THD+N<=1%

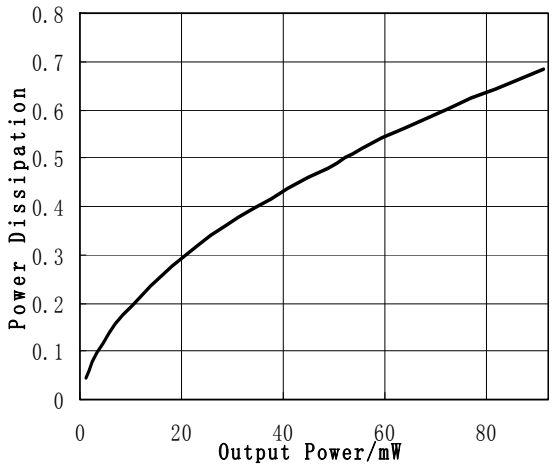


Figure 31 Power Dissipation vs. Output Power SE mode, 5V, f=1 kHz, RL=32Ohm

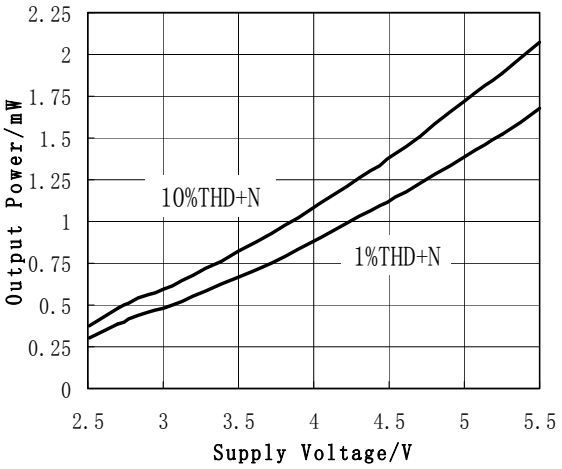


Figure 32 Output Power vs. Power Supply BTL mode, f=1 kHz, RL=8 Ohm

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The IS31AP4088A's QFN (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air.

The QFN package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 2, the IS31AP4088A consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors R2, R4 and input resistors R1 and R3 set the closed-loop gain of Amp A (-out) and Amp B (-out) whereas two internal 20kΩ resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The IS31AP4088A drives a load, such speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 2 shows that Amp A's (-out) output serves as Amp A's (+out) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2\times(Rf/Ri) \qquad (1)$$

or

$$A_{VD} = 2\times(R2/R1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \text{ Single-Ended} \qquad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The IS31AP4088A has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and an 8Ω load, the maximum single ended amplifier power dissipation is 0.63W or 1.23W for BTL mode per channel.

$$P_{DMAX} = 4\times(V_{DD})^2/(2\pi^2 R_L) \text{ Bridge Mode} \qquad (3)$$

The IS31AP4088A's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the Stereo Mode. And in stereo mode, twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \qquad (4)$$

The IS31AP4088A's T_{JMAX} = 150°C. In the QFN package soldered to a DAP pad that expands to a copper area of 5in2 on a PCB, the IS31AP4088A's θ_{JA} is 20°C/W. At any given ambient temperature TA, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging

Equation (4) and substituting P_{DMAX} for $P_{DMAX'}$ results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the IS31AP4088A's maximum junction temperature.

$$T_A = T_{JMAX} - 2\times P_{DMAX}\,\theta_{JA} \qquad (5)$$

For a typical application with a 5V power supply and a 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the QFN package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \qquad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the IS31AP4088A's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load

resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heat sinks such as the Thermally 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the IS31AP4088A's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation.

Keep the length of leads and traces that connect capacitors between the IS31AP4088A's power supply pin and ground as short as possible.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the IS31AP4088A's shutdown function. Activate micro-power shutdown by applying GND to the SHUTDOWN pin. When active, the IS31AP4088A's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.04µA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SHUTDOWN pin. Table 1 shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown.

These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When use a switch, connect an external 100k resistor between the SHUTDOWN pin and GND. Select normal amplifier operation by closing the switch. Opening the switch sets the SHUTDOWN pin to GND through the 100k resistor, which activates the micro power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Shutdown Pin	Headphone Jack Sense Pin	Operational Shutdown Mode
Logic High	Low(HP not Plugged in)	Bridged /BTL
Logic High	High(HP Plugged in)	Single Ended
Logic Low	Don't care	Micro Power Shutdown

Applying a logic level to the IS31AP4088A's HP Sense headphone control pin turns off Amp A (+out) and Amp B (+out) muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 33 shows the implementation of the IS31AP4088A's headphone control function. With no headphones connected to the headphone jack, the R5-R8 voltage divider sets the voltage applied to the HP Sense pin (pin 14) at approximately 50mV. This 50mV enables Amp A (+out) and Amp B (+out) placing the IS31AP4088A in bridged mode operation.

While the IS31AP4088A operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single ended trigger. Connecting headphones to the Headphone jack disconnects the headphone jack contact pin from −OUTA and allows R7. to pull the HP Sense pin up to $V_{DD.}$

This enables the headphone function, turns off Amp A (+out) and Amp B (+out) which mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R5 and R6. These resistors have negligible effect on the

IS31AP4088A's output drive capability since the typical impedance of headphones is 32Ω.

Figure 33 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return.

A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones.

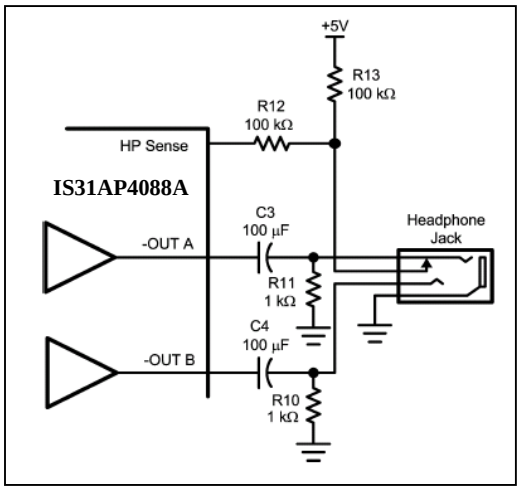


Figure 33 Headphone Circuit

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the IS31AP4088A's performance requires properly selecting external components. Though the IS31AP4088A operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The IS31AP4088A is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio.

These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS ($2.83V_{P-P}$). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C1 and C2) in Figure 2. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor. Besides effecting system cost and size, C1 and C2 have an effect on the IS31AP4088A's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, R2 and R8. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

A shown in Figure 2, the input resistors (R1, 4, 5, and 6) and the input capacitors, C1 and C2 produce a −3dB high pass filter cutoff frequency that is found using Equation (7).

$$F_{-3dB} = 1/2\pi R_{in}C_{in} = 1/2\pi\ R1C1 \qquad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C1, using Equation (7) is 0.053µF. The 0.33µF C1 shown in Figure 1 allows the IS31AP4088A to drive high efficiency, full range speaker whose response extends below 30Hz.

BYPASS CAPACITOR VALUE SELECTION

Besides minimizing the input capacitor size, careful consideration should be paid to value of C6, the capacitor connected to the BYPASS pin. Since C6 determines how fast the IS31AP4088A settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the IS31AP4088A's outputs ramp to their quiescent DC voltage (nominally 1/2 VDD), the smaller the turn-on pop. Choosing C6 equal to 1.0µF along with a small value of C1 (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C1 no larger than necessary for the desired bandwidth helps minimize clicks and pops. Connecting a 1µF capacitor, C6, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The IS31AP4088A contains circuitry that minimizes turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the

device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C6 alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C6 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C6 increases, the turn-on time increases. There is a linear relationship between the size of C6 and the turn-on time. Here are some typical turn-on times for various values of C6 (all tested at V_{DD} = 5V):

C6	T_{ON}
0.01μF	13ms
0.1μF	26ms
0.22μF	44ms
0.47μF	68ms
1.0μF	113ms

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} on and off may not allow the capacitors to fully discharge, which may cause "click-and-pop".

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load. The following are the desired operational parameters:

Power Output: 1WRMS

Load Impedance: 8Ω

Input Level: 1Vrms

Input Impedance: 20kΩ

Bandwidth: 100Hz−20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation (8). The result is in Equation (9).

$$V_{OUTPEAK} = \sqrt{(2R_L P_O)} \quad (8)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (9)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.35V for a 1W output at 1% THD+N. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the IS31AP4088A to produce peak output power in excess of 1.2W at 5V of VDD and 1% THD+N without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the Power Dissipation section.

After satisfying the IS31AP4088A's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (10).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (10)$$

Thus, a minimum gain of 2.83 allows the IS31AP4088A's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain (non Stereo Enhanced mode) is set using the input (R1 and R9) and feedback resistors R2 and R8. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R2/R1 = A_{VD}/2 \quad (11)$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz$$

and an

$$f_H = 20kHz \times 5 = 100kHz.$$

As mentioned in the External Components section, R1 and C1 create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using Equation (12).

$$C1 \geq 1/(2\pi R1 f_L) \quad (12)$$

The result is

$$1/(2\pi \times 20k\Omega \times 20Hz) = 0.398\mu F$$

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100 kHz in this example) and the differential gain, A_{VD}, determines the upper pass band response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300 kHz. This is less than the IS31AP4088A's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that

require more differential gain while avoiding performance-restricting bandwidth limitations.

STEREO ENHANCED STEREO ENHANCEMENT

The IS31AP4088A features a Stereo Enhanced audio enhancement effect that widens the perceived soundstage from a stereo audio signal.

The Stereo Enhanced audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network, Shown in figure 2, is required to enable the Stereo Enhanced effect. The amount of the Stereo Enhanced effect is set by the R5 and C7 or Cadj. Decreasing the value of R5 will increase the Stereo Enhanced effect. Increasing the value of the capacitors (C7 or Cadj) will decrease the low cutoff frequency at which the Stereo Enhanced effect starts to occur, as shown by Equation 13.

$$F_{(-3dB)} = 1 / 2\pi R5 \times Cadj \qquad (13)$$

The amount of perceived Stereo Enhanced is also dependent on many other factors such as speaker placement and the distance to the listener. Therefore, it is recommended that the user try various values of R5 and Cadj to get a feel for how the Stereo Enhanced effect works in the application. There is not a “right or wrong” for the effect, it is merely what is most pleasing to the individual user. Take note that R3 and R4 replace R2, and R7 and R6 replace R8 when Stereo Enhanced mode is enabled.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

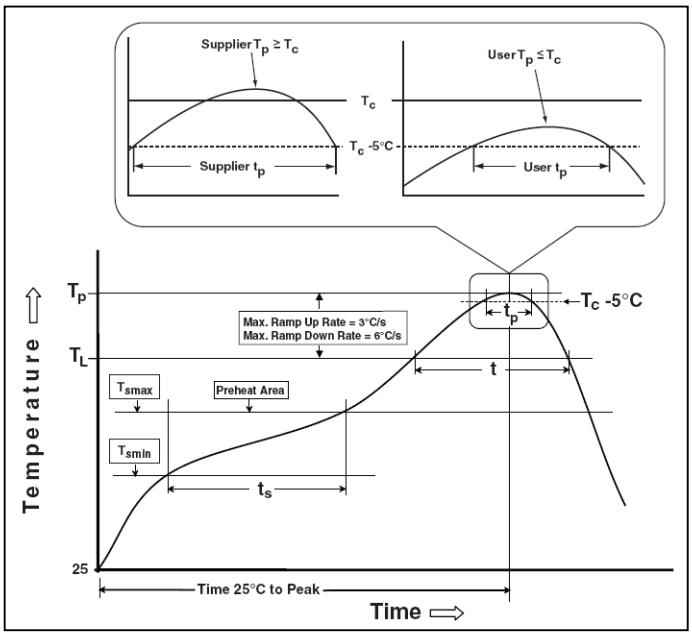
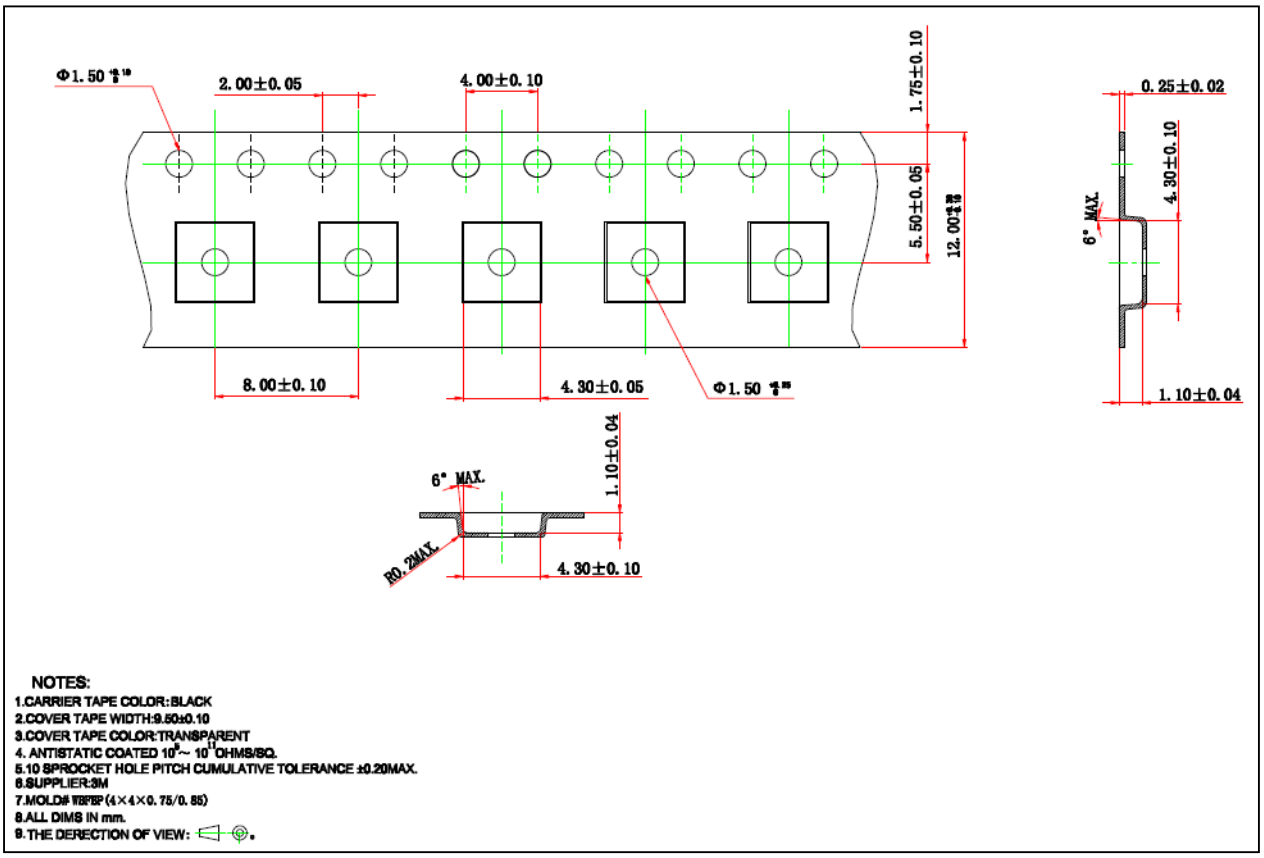


Figure 34 Classification Profile

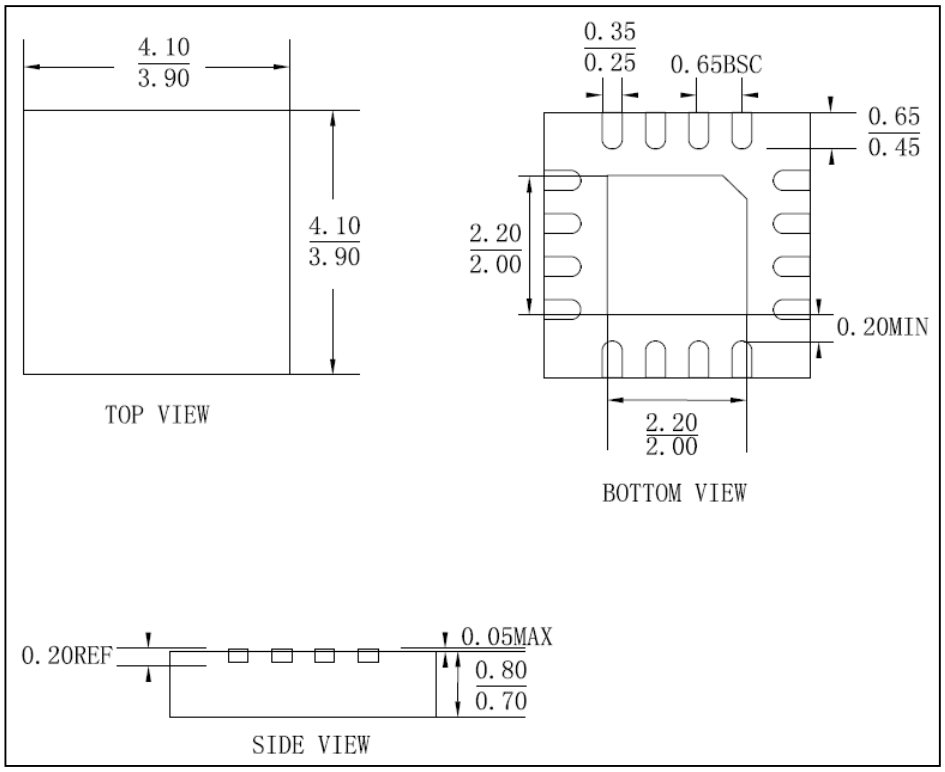
TAPE AND REEL INFORMATION



NOTES:
1.CARRIER TAPE COLOR:BLACK
2.COVER TAPE WIDTH:9.50±0.10
3.COVER TAPE COLOR:TRANSPARENT
4. ANTISTATIC COATED 10^{6}~ 10^{11}OHMS/SQ.
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
6.SUPPLIER:3M
7.MOLD# W8FEP(4×4×0.75/0.85)
8.ALL DIMS IN mm.
9.THE DERECTION OF VIEW:

PACKAGE INFORMATION

QFN-16



Note: All dimensions in millimeters unless otherwise stated.