IS31AP2111

2×20W STEREO/1×40W MONO DIGITAL (I2S) AUDIO AMPLIFIER WITH 20 BANDS EQ FUNCTIONS

November 2015

GENERAL DESCRIPTION

The IS31AP2111 is a digital I2S interface audio amplifier capable of driving a pair of 8Ω speakers at 20W when operating from a 24V supply. Due to its Class-D output drive stage; it can operate without an external heat-sink or fan.

The IS31AP2111 integrates advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I2C control interface.

Robust protection circuits are provided to protect the IS31AP2111 from damage due to accidental or erroneous operating conditions. Because of its digital design, the IS31AP2111 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart. It has a robust anti-pop circuit for pop free operation during power ON. It integrates protection features for short circuit and over temperature.

The IS31AP2111 is available in a thermally enhanced eTSSOP-24 package.

APPLICATIONS

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

FEATURES

- 16/18/20/24-bits input with I2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  speaker: 99dB (PSNR), 104dB (DR) @24V
- Multiple sampling frequencies (F_S)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  - 64x~1024x F_S for 32kHz / 44.1kHz / 48kHz
  - 64x~512x F_S for 64kHz / 88.2kHz / 96kHz
  - 64x~256x F_S for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for speaker driver
- speaker output power at 24V
  - 10W × 2CH into 8Ω @0.24% THD+N for stereo
  - 20W × 2CH into 8Ω @0.38% THD+N for stereo
  - 40W × 1CH into 4Ω @0.12% THD+N for mono
- Sound processing including:
  - 20 bands parametric speaker EQ
  - Volume control (+24dB ~ -103dB, 0.125dB/step),
  - Dynamic range control (DRC)
  - Dual band dynamic range control
  - Power clipping
  - 3D surround sound
  - Channel mixing
  - Noise gate with hysteresis window
  - Bass/Treble tone control
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode

TYPICAL APPLICATION CIRCUIT

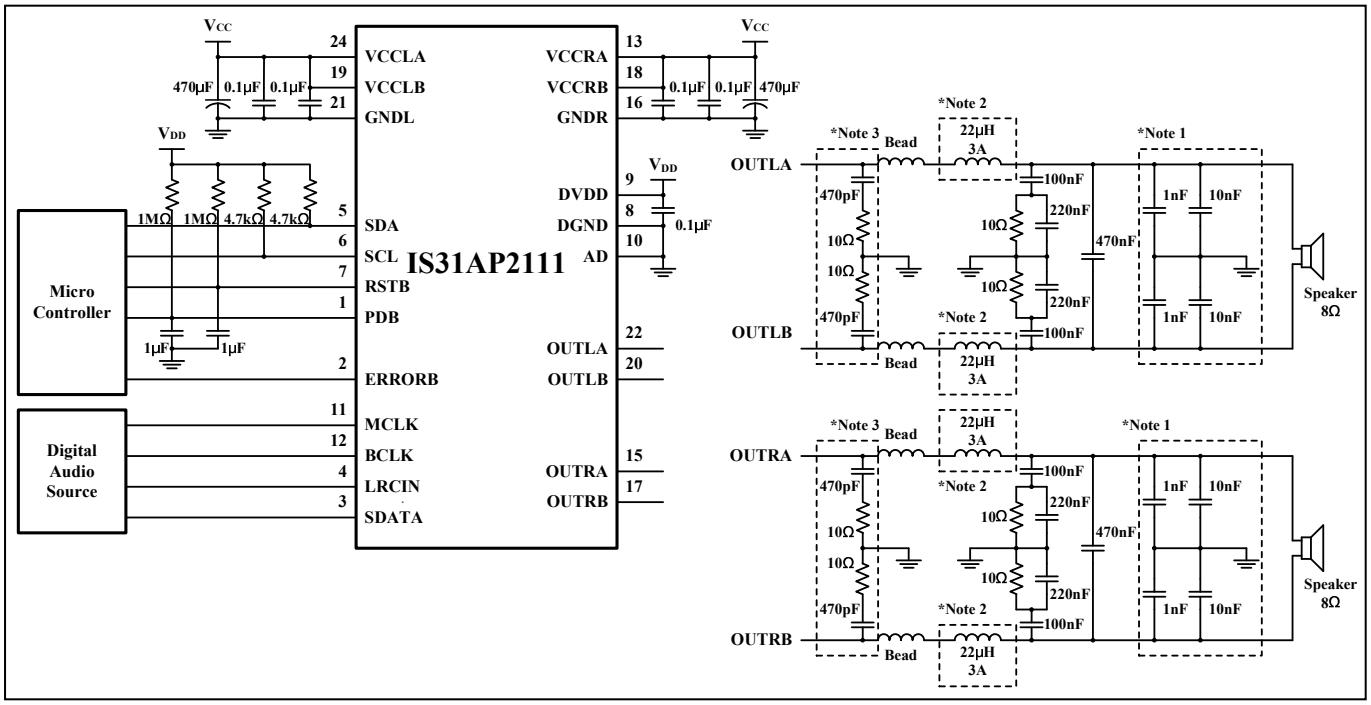


Figure 1 Typical Application Circuit (for BTL Stereo, Single-ended Input)

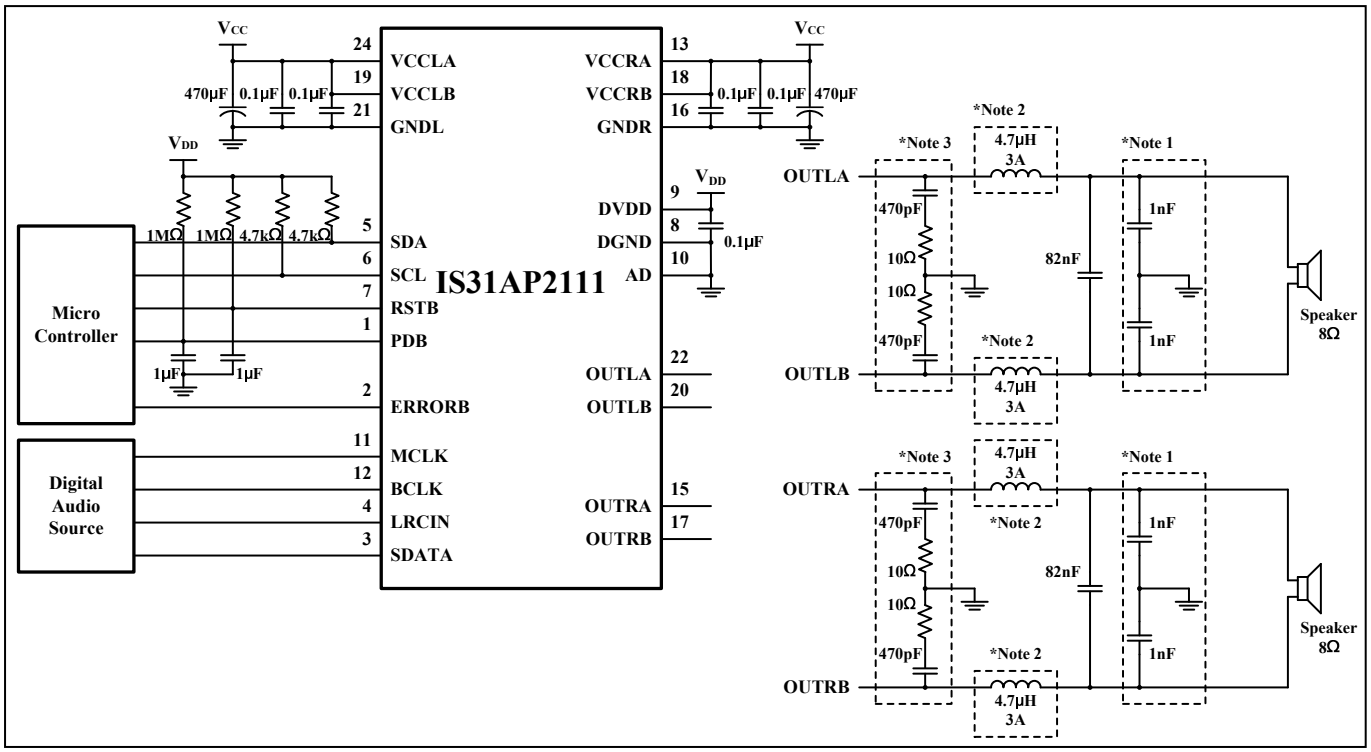


Figure 2 Typical Application Circuit (Economic Type, Moderate EMI Suppression)

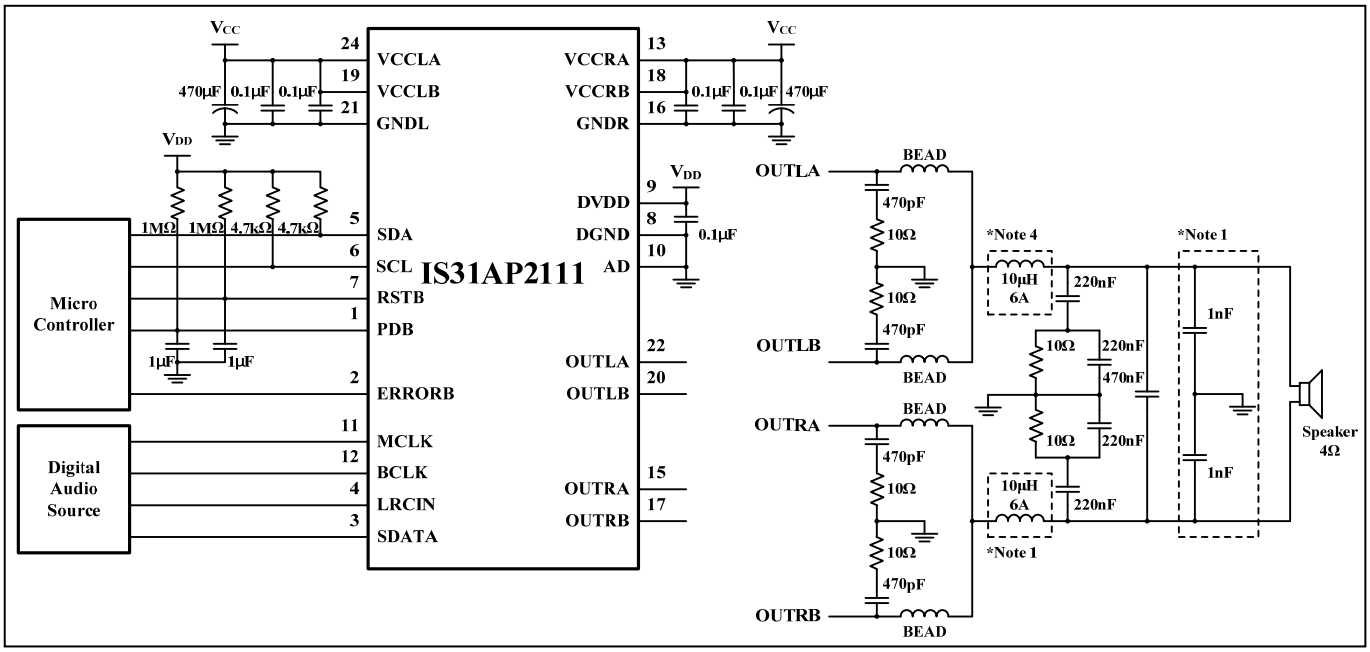


Figure 3 Typical Application Circuit (for Mono)

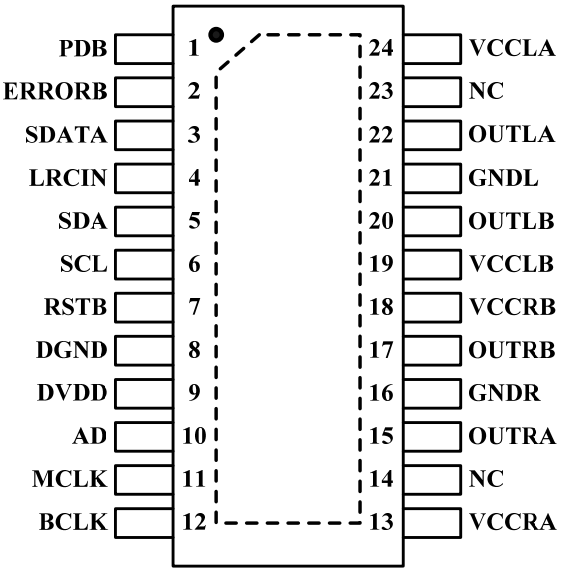
Note 1: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 2: When concerning about short-circuit protection, it is suggested using the choke with its I_{DC} larger than 5A.

Note 3: The snubber circuit can be removed while the V_{CC} ≤20V.

Note 4: When concerning about short-circuit protection, it is suggested using the choke with its I_{DC} larger than 10A.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-24	

PIN DESCRIPTION

No.	Pin	Description	Characteristics
1	PDB	Power down, low active.	Schmitt trigger TTL input buffer
2	ERRORB	Error status, low active.	Open-drain output
3	SDATA	I2S serial audio data input.	Schmitt trigger TTL input buffer
4	LRCIN	Left/Right clock input (F_S).	Schmitt trigger TTL input buffer
5	SDA	I2C serial data.	Schmitt trigger TTL input buffer
6	SCL	I2C serial clock input.	Schmitt trigger TTL input buffer
7	RSTB	Reset, low active.	Schmitt trigger TTL input buffer
8	DGND	Digital ground.	
9	DVDD	Digital power.	
10	AD	I2C select address.	Schmitt trigger TTL input buffer
11	MCLK	Master clock input.	Schmitt trigger TTL input buffer
12	BCLK	Bit clock input ($64F_S$).	Schmitt trigger TTL input buffer
13	VCCRA	Right channel supply A.	
14, 23	NC	No connection.	
15	OUTRA	Right channel output A.	
16	GNDR	Right channel ground.	
17	OUTRB	Right channel output B.	
18	VCCRB	Right channel supply B.	
19	VCCLB	Left channel supply B.	
20	OUTLB	Left channel output B.	
21	GNDL	Left channel ground.	
22	OUTLA	Left channel output A.	
24	VCCLA	Left channel supply A.	
	Thermal Pad	Connect to GND.	

ORDERING INFORMATION

Industrial Range: 0°C to +70°C

Order Part No.	Package	QTY
IS31AP2111-ZLS1-TR	eTSSOP-24, Lead-free	2500/Reel
IS31AP2111-ZLS1		62/Tube

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

Supply for driver stage (VCCR, VCCL), V_{CC}	−0.3V ~ +30V
Supply for digital circuit (DVDD), V_{DD}	−0.3V ~ +3.6V
Input voltage (SDA,SCL,RSTB,PDB,ERRORB,MCLK, BCLK,LRCIN,SDATA), V_{IN}	−0.3V ~ +3.6V
Thermal resistance, θ_{JA}	32.8°C/W
Junction temperature range, T_J	0°C ~ 150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
ESD (HBM) ESD (CDM)	±2kV ±1kV

Note:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply for driver stage to VCCR/L		7		26	V
V_{DD}	Supply for digital circuit		3.15		3.45	V
T_J	Junction operating temperature		0		125	°C
T_A	Ambient operating temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=24V, T_A=25°C, R_L=8Ω (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{PDH}	VCC supply current during power down	V_{CC} = 24V		4	200	μA
I_{PDL}	DVDD supply current during power down	V_{DD} = 3.3V		3.6	10	μA
V_{UVH_HV}	Under voltage disabled (For VCC)			10.2		V
V_{UVL_HV}	Under voltage enabled (For VCC)			9.2		V
V_{UVH_LV}	Under voltage disabled (For DVDD)			2.9		V
V_{UVL_LV}	Under voltage enabled (For DVDD)			2.8		V
$R_{DS(ON)}$	Static drain-to-source ON-state resistor, PMOS	V_{CC} =24V, I_D = 500mA		245		mΩ
	Static drain-to-source ON-state resistor, NMOS			150		
I_{SC}	L/R channel over-current protection	V_{CC} =24V (Note 1)		5.1		A
	Mono channel over-current protection			10		
T_S	Junction temperature for driver shutdown			158		°C
	Temperature hysteresis for recovery from shutdown			33		°C
Logic Electrical Characteristics						
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{OH}	High level output voltage		2.4			V
V_{OL}	Low level output voltage				0.4	V
C_{IN}	Input capacitance			6.4		pF

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=24V, V_{DD} = 3.3V, f_S = 48kHz, R_L=8Ω with passive LC lowpass filter (L= 22μH, R_{DC}= 0.12Ω, C=470nF), input is 1kHz sinewave, volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_O	RMS output power	THD+N=0.38%, +8dB volume (Note 2)		20		W
THD+N	Total harmonic distortion + noise	P_O = 10W		0.24		%
V_{NO}	Output noise	20Hz ~ 20kHz (Note 3)		179		μV
SNR	Signal-to-noise ratio	+8dB volume, input level is -9dB (Note 3)		99		dB
DR	Dynamic range	+8dB volume, input level is -68dB (Note 3)		104		dB
PSRR	Power supply ripple rejection	V_{RIPPLE} = 1V_{RMS} at 1kHz		-68		dB
	Channel separation	1W @1kHz		-85		dB

I2C DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Serial-Clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	4.7		1.3		μs
$t_{HD, STA}$	Hold time (repeated) START condition	4.0		0.6		μs
$t_{SU, STA}$	Repeated START condition setup time	4.7		0.6		μs
$t_{SU, STO}$	STOP condition setup time	4.0		0.6		μs
$t_{HD, DAT}$	Data hold time	0	3.45	0	0.9	μs
$t_{SU, DAT}$	Data setup time	250		100		ns
t_{LOW}	SCL clock low period	4.7		1.3		μs
t_{HIGH}	SCL clock high period	4.0		0.6		μs
t_R	Rise time of both SDA and SCL signals, receiving		1000	20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving		300	20+0.1C_b	300	ns
C_b	Capacitive load for each bus line		400		400	pF
V_{NL}	Noise margin at the low level for each connected device (including hysteresis)	0.1V_{DD}		0.1V_{DD}		V
V_{NH}	Noise margin at the high level for each connected device (including hysteresis)	0.2V_{DD}		0.2V_{DD}		V

I2S DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{LR}	LRCIN period ($1/F_S$)		10.41		31.25	μs
t_{BL}	BCLK rising edge to LRCIN edge		50			ns
t_{LB}	LRCIN edge to BCLK rising edge		50			ns
t_{BCC}	BCLK period ($1/64F_S$)		162.76		488.3	ns
t_{BCH}	BCLK pulse width high		81.38		244	ns
t_{BCL}	CBLK pulse width low		81.38		244	ns
t_{DS}	SDATA set up time		50			ns
t_{DH}	SDATA hold time		50			ns

Note 1: Speaker over-current protection is only effective when speaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Note 2: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

Note 3: Measured with A-weighting filter.

Note 4: Guaranteed by design.

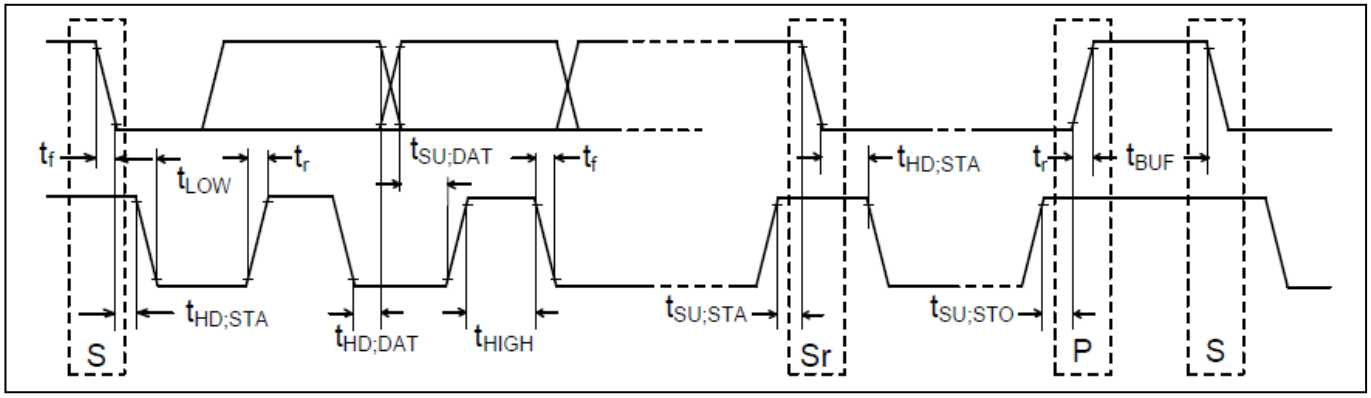


Figure 4 I2C Timing

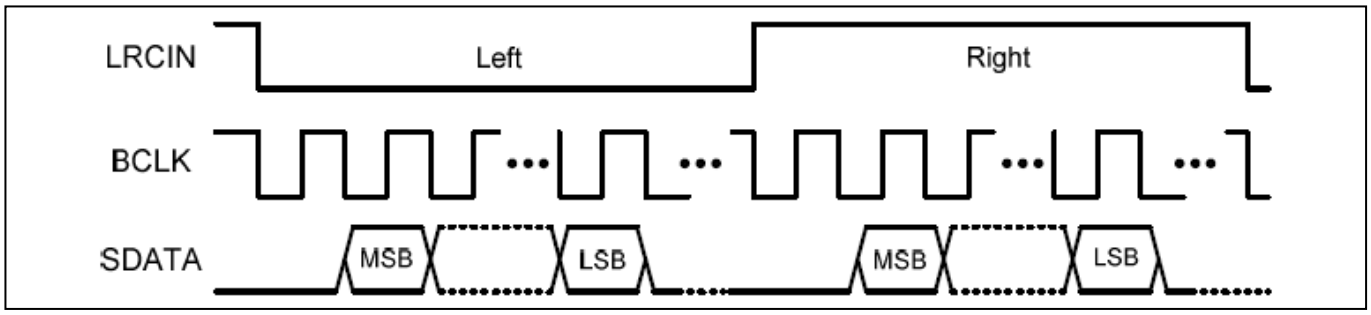


Figure 5 I2S

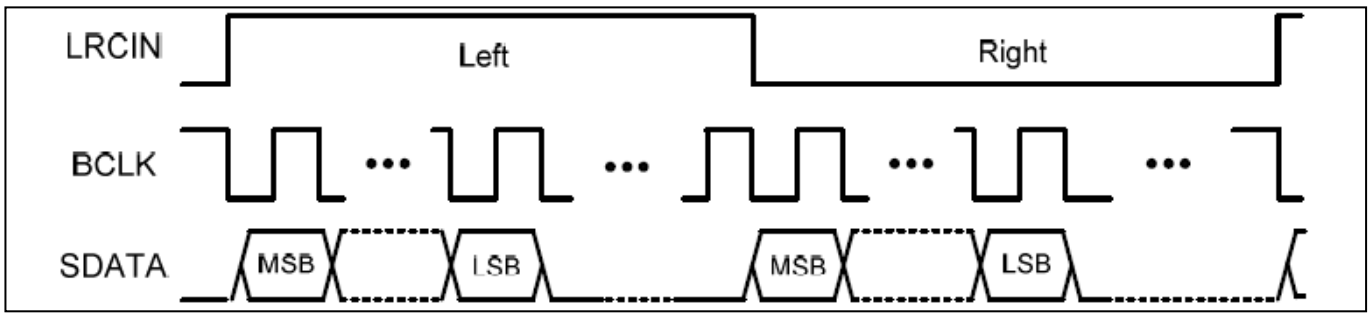


Figure 6 Left-Alignment

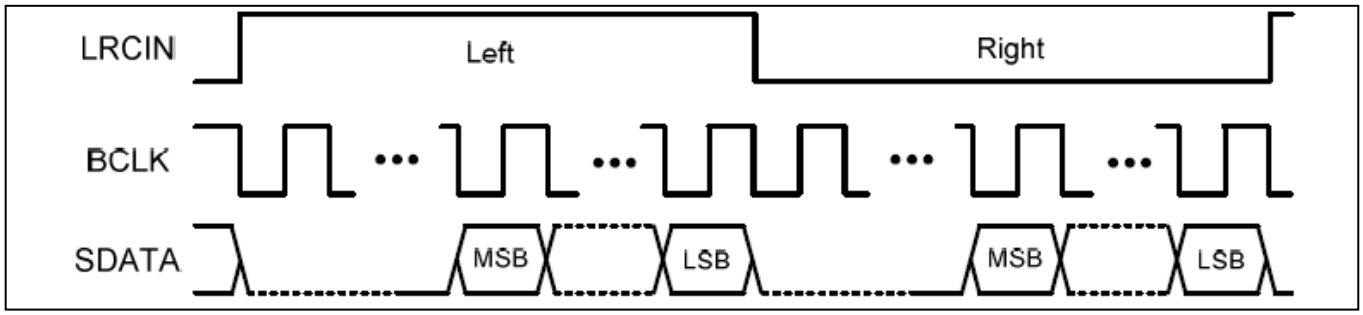


Figure 7 Right-Alignment

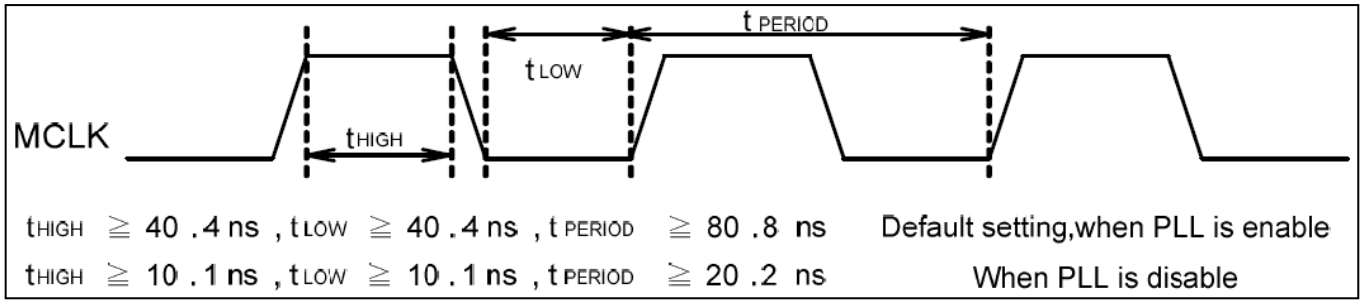


Figure 8 System Clock Timing

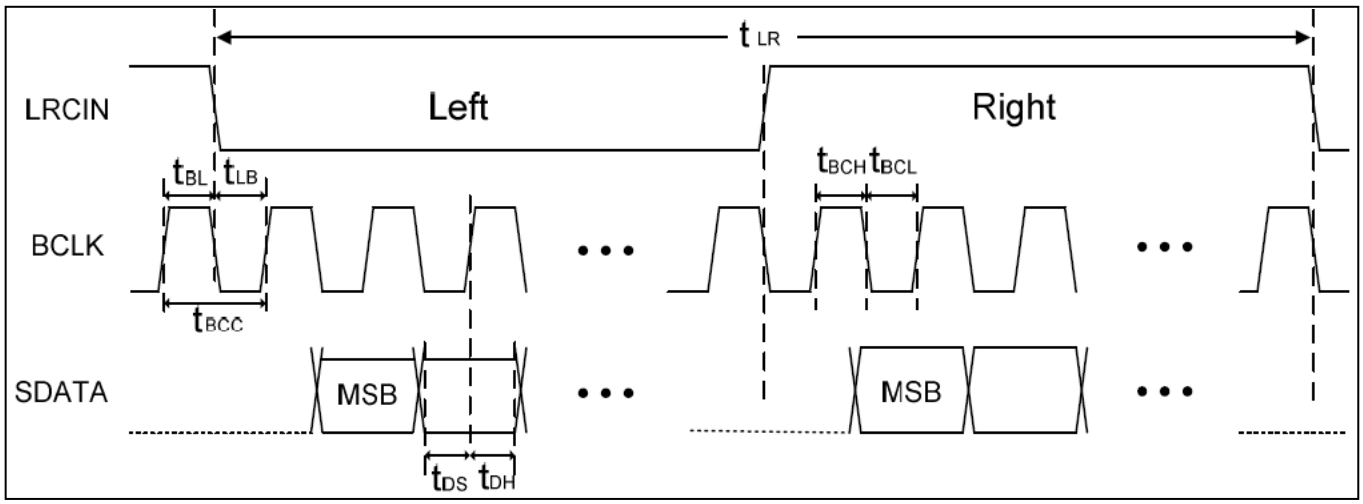


Figure 9 Timing Relationship (Using I2S format as an example)

TYPICAL PERFORMANCE CHARACTERISTICS

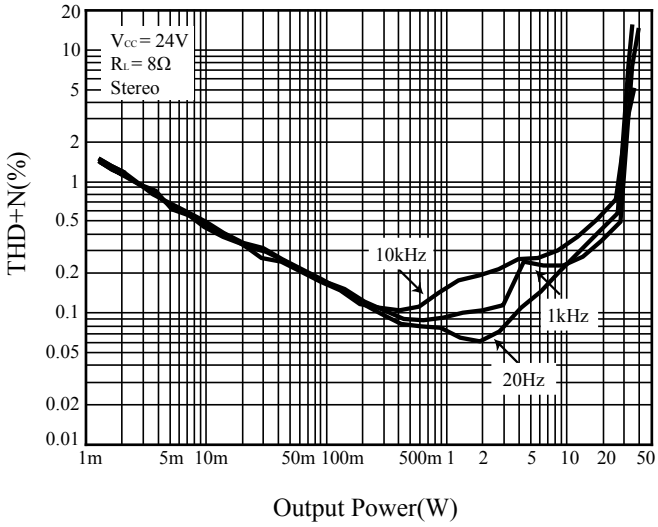


Figure 10 THD+N vs. Output Power

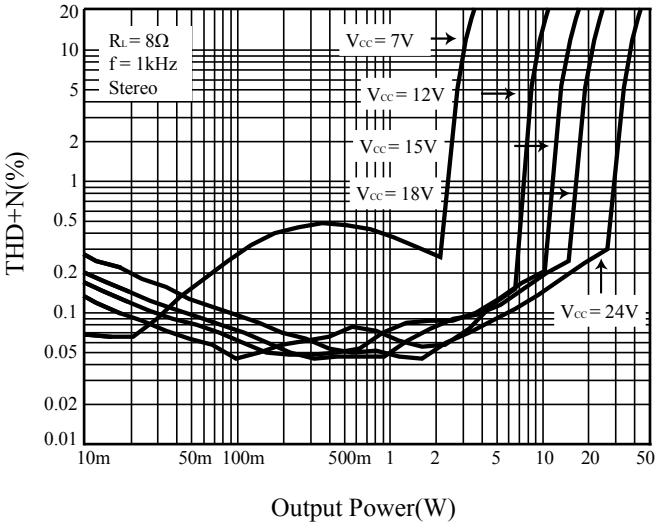


Figure 11 THD+N vs. Output Power

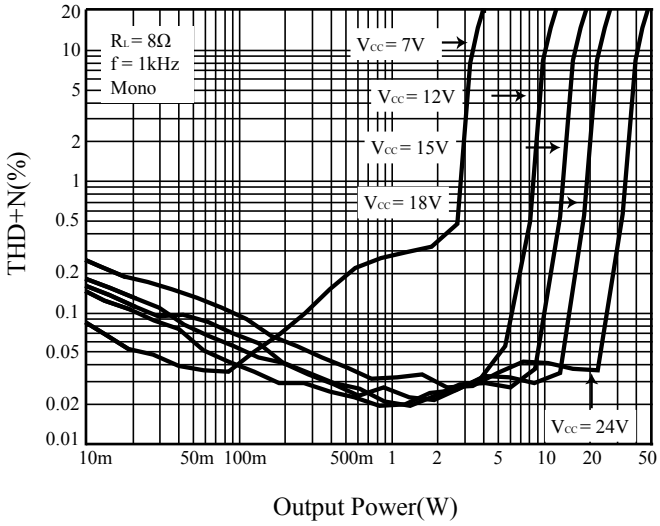


Figure 12 THD+N vs. Output Power

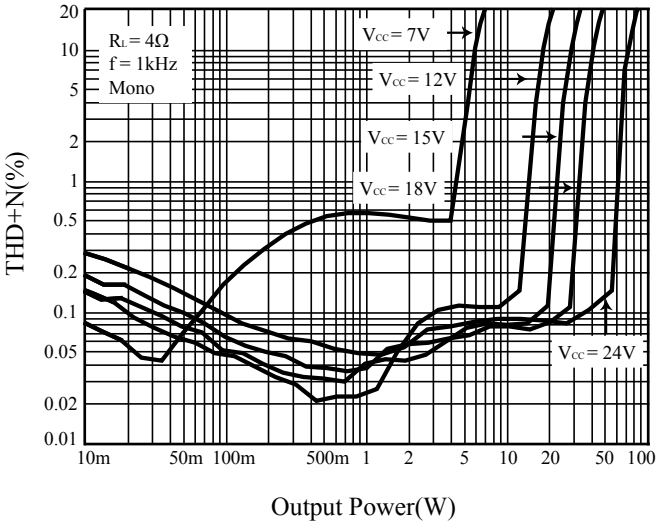


Figure 13 THD+N vs. Output Power

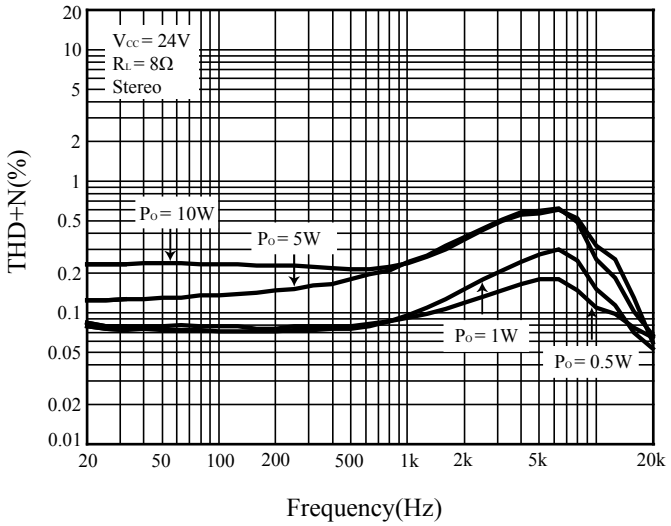


Figure 14 THD+N vs. Frequency

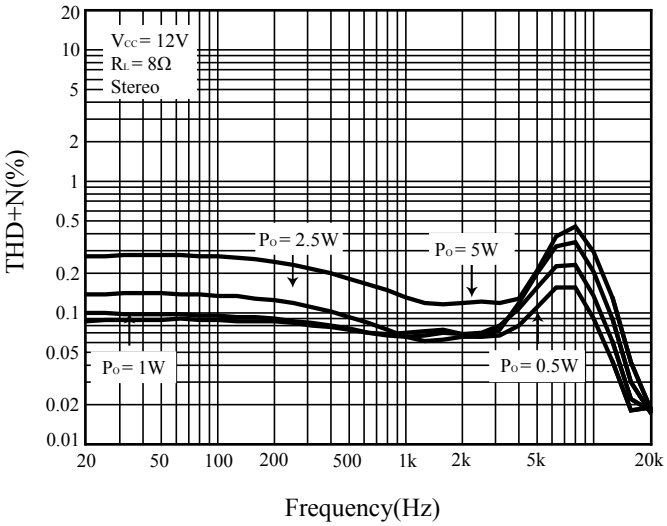


Figure 15 THD+N vs. Frequency

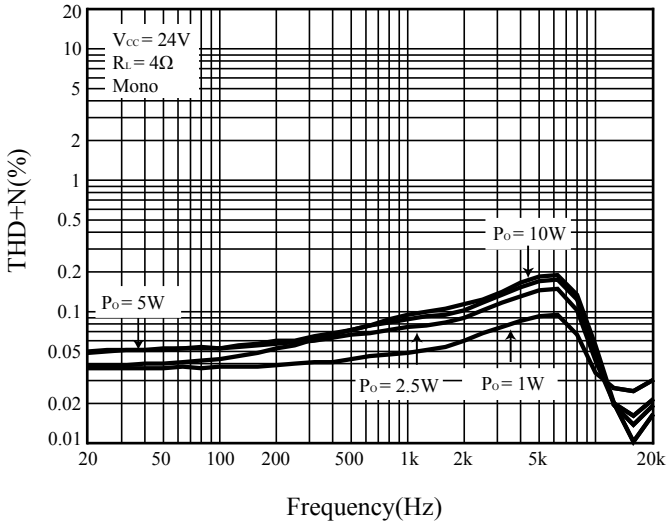


Figure 16 THD+N vs. Frequency

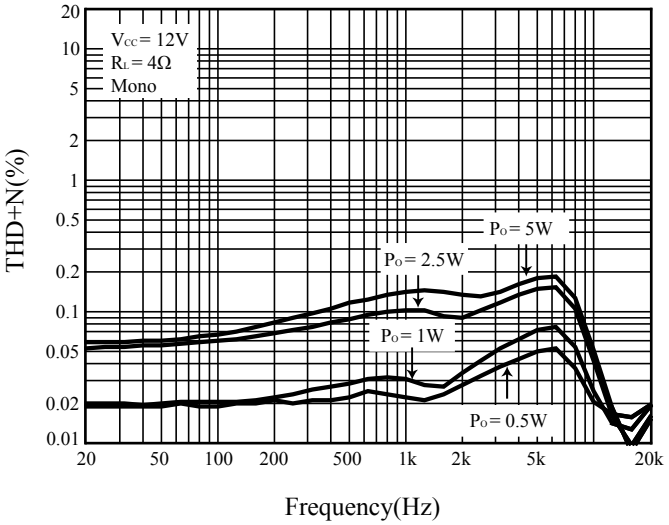


Figure 17 THD+N vs. Frequency

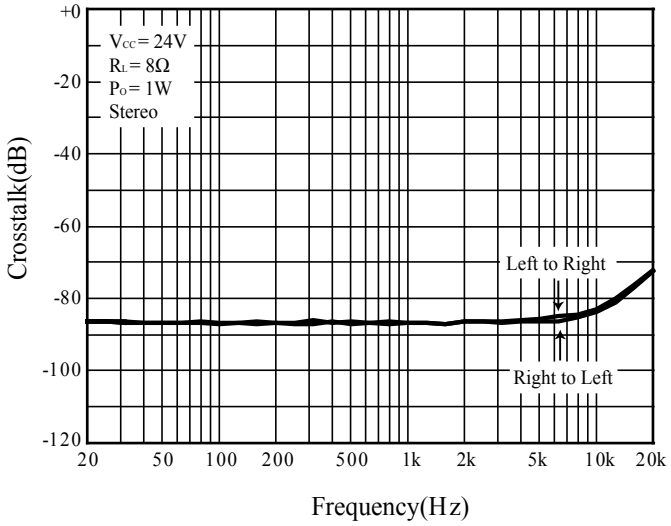


Figure 18 Cross-Talk

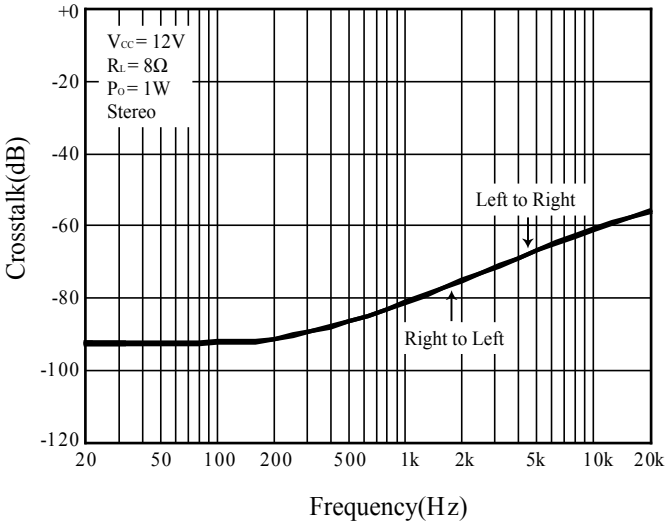


Figure 19 Cross-Talk

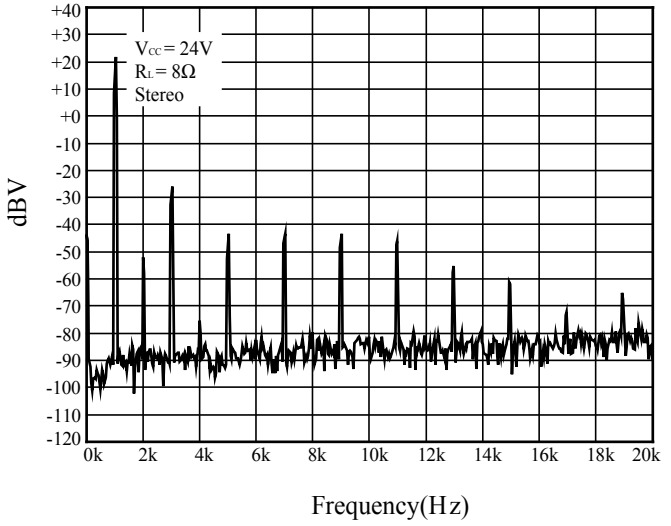


Figure 20 Spectrum at Peak SNR at -1dB Signal Input

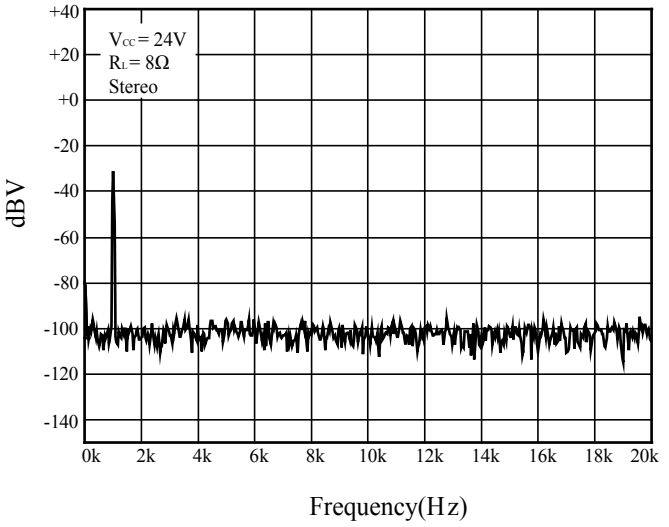


Figure 21 Spectrum at -60dB Signal Input Level

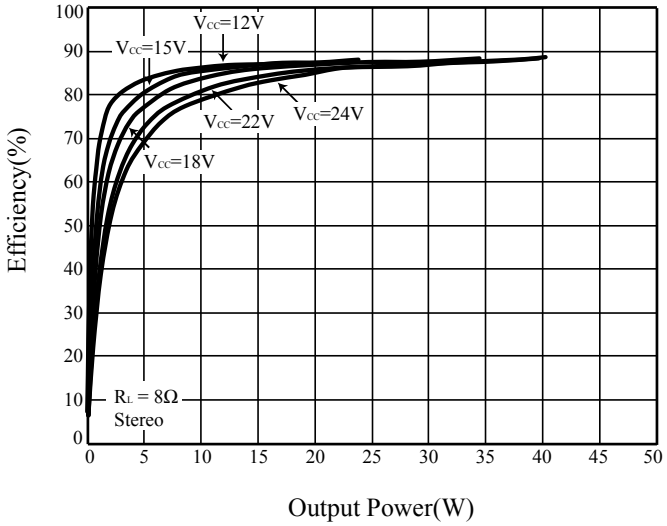


Figure 22 Efficiency vs. Total Output Power (Without Power Saving Mode)

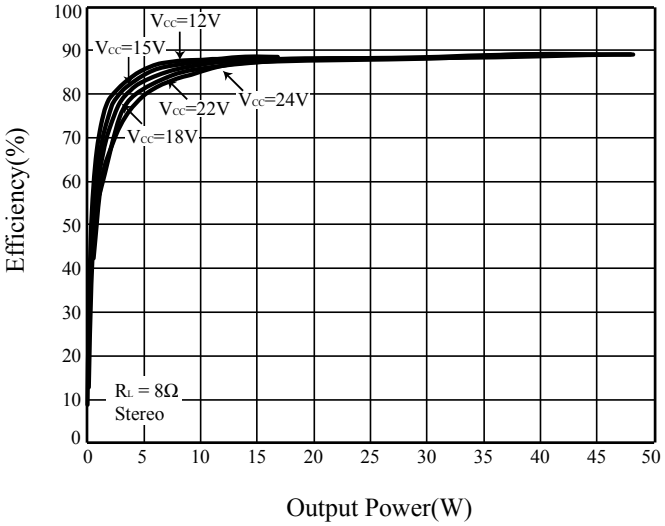


Figure 23 Efficiency vs. Total Output Power (With Power Saving Mode)

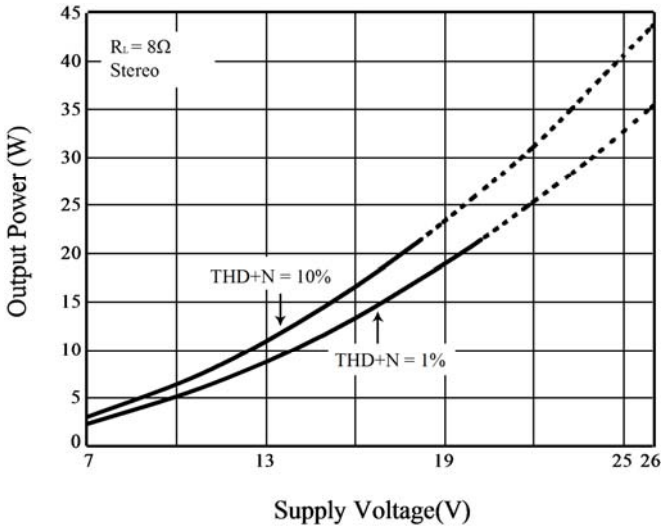


Figure 24 Output Power vs. Supply voltage

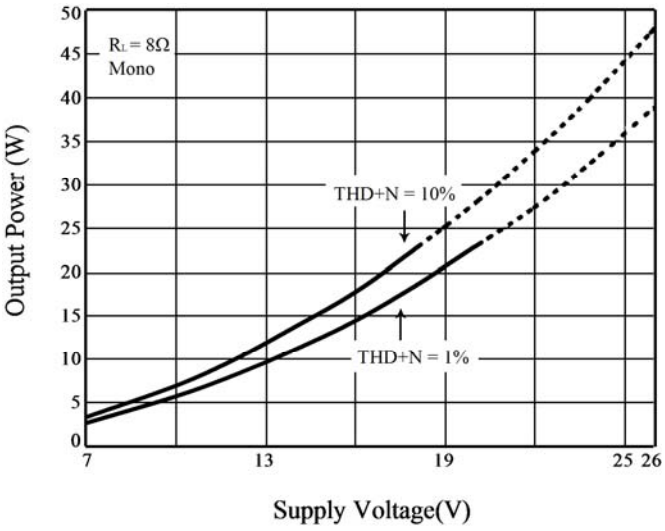


Figure 25 Output Power vs. Supply voltage

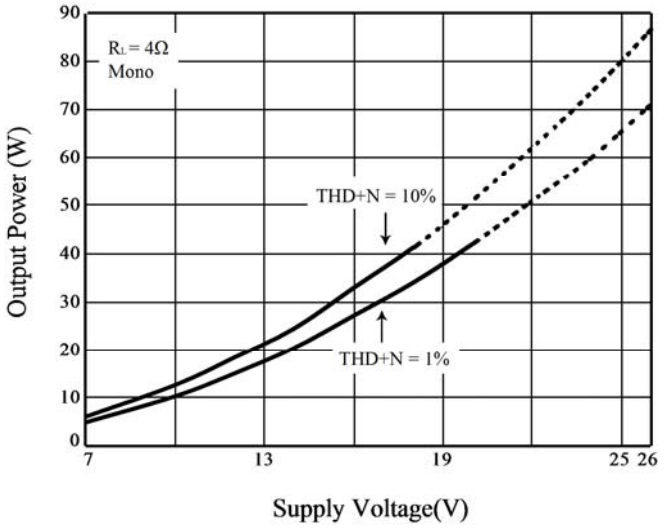


Figure 26 Output Power vs. Supply voltage

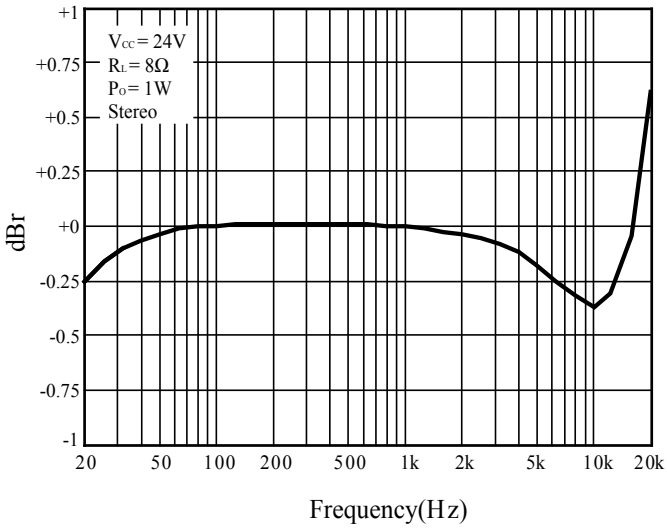


Figure 27 Frequency Response

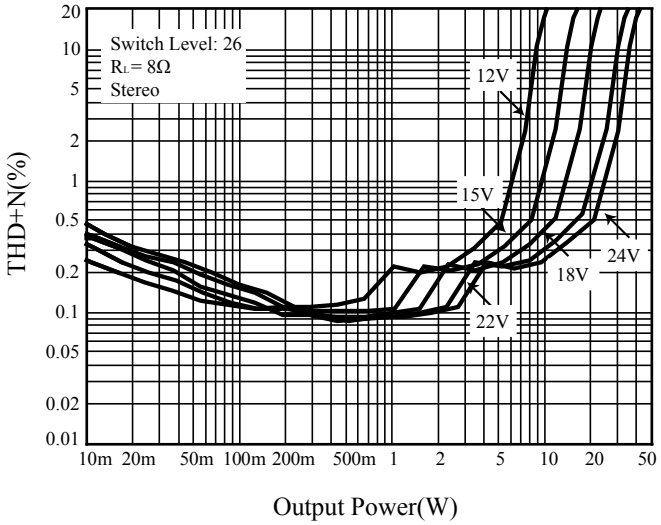
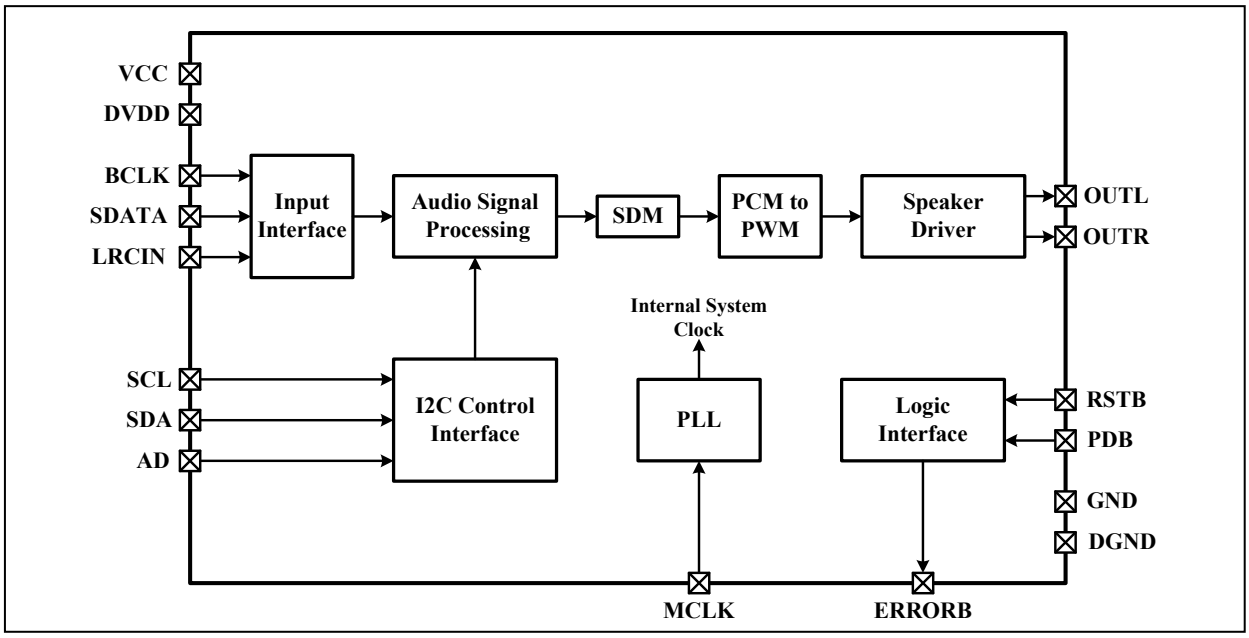


Figure 28 THD+N vs. Output Power

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

OPERATION MODES

Without I2C Control

The default settings, Bass, Treble, EQ, Volume, DRC are applied to register table content when using the IS31AP2111 without I2C control. For more information about default settings, please refer to the Default Column of Table 4 (Register Function).

As default state is mute, customers should send a de-mute command via I2C to enable the system.

With I2C Control

When using I2C control, user can program suitable parameters into the IS31AP2111 to enable or enhance specific operation features. Please refer to the register table section (Table 5 ~ Table 25) to get the more detail.

INTERNAL PLL

The IS31AP2111 has an integrated PLL to derive a synchronized internal clock (Fs) from the master clock (MCLK) input.

F_S	MCLK/FS Setting Ratio for PLL	MCLK Frequency	Multiple Edge Evaluation for Master Clock	PWM Career Frequency
48kHz	256x	12.288MHz	4x	384kHz
44.1kHz	256x	11.289MHz	4x	352.8kHz
32kHz	256x	8.192MHz	4x	256kHz

DEFAULT VOLUME

The default volume level of the IS31AP2111 is +2.0dB, and the default state is muted. Please give a de-mute command via I2C to enable the volume when the whole system is stable. For more detailed information, please refer to the register table section Table 7 (State Control 3 Register).

RESET

When a logic LOW is applied to the RSTB pin, the IS31AP2111 will clear the stored data and reset the register table to their default values. The IS31AP2111 will exit the reset state at the 256th MCLK cycle after the RSTB pin is raised to high.

POWER DOWN CONTROL

The IS31AP2111 has a built-in volume fade-in/fade-out design for power down and mute function. The relative power down timing diagrams for speakers are shown in Figure 29 and 30.

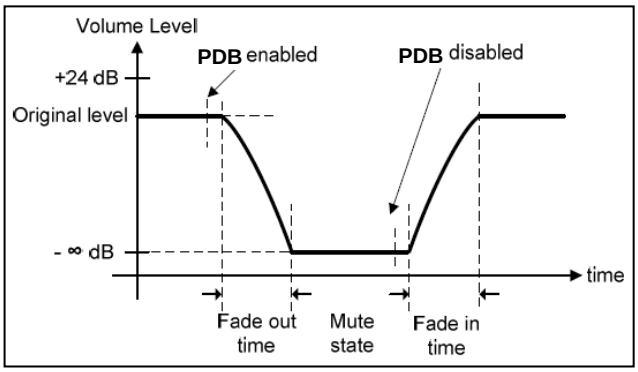


Figure 29 Power Down Timing Diagrams With Mute

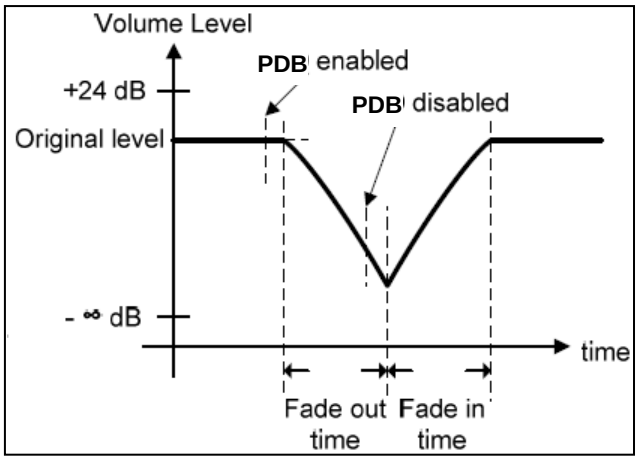


Figure 30 Power Down Timing Diagrams

$$t_{FADE} = \left| 10^{\frac{Target(dB)}{20}} - 10^{\frac{Original(dB)}{20}} \right| \times 128 \times (1/96kHz)$$

The volume level will be decreased to -∞dB in several LRCIN (Left/Right clock) cycles. Once the fade-out procedure has completed, the IS31AP2111 will turn off the power stages, stop the clock signals (MCLK, BCLK) from feeding into the digital circuit and turn off the internal analog circuit current. When PDB pin is pulled low, the IS31AP2111 requires t_{FADE} time to finish the above proceduresbefore entering the power down state. The IS31AP2111 will not accept programming commands while it is in the power down state. During power down, all the register table settings are kept until DVDD power is removed.

If cancel the power down function within fade-out procedure, the IC will enter into fade-in after few

delay time (Figure 30). In addition, the IS31AP2111 will power the internal analog circuit and pass the clock signals (MCLK, BCLK) to the digital circuits. Then, the IS31AP2111 will return to its normal operation without powering down.

SELF-PROTECTION CIRCUITS

The IS31AP2111 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

Thermal Protection

When the internal junction temperature increases to greater than 158°C, the power stages will be turned off. Normal operation will begin once the device temperature cools to 125°C.The temperature values may vary by +/- 10%.

Short-Circuit Protection

The short-circuit protection circuit protects the output stage when the speaker wires are shorted to each other or GND/VDD. During normal 24V stereo operation, the current flowing through the power stage should be less than 5.1A. If an over-temperature or short-circuit condition (current greater than 5.1A) occurs, the open-drain ERRORB pin will be pulled low and latched into ERROR state and the output stages are disabled.

Once the over-temperature or short-circuit condition is removed, the IS31AP2111 will exit the ERROR state when one of the following conditions are met: (1) RSTB pin is pulled low, (2) PDB pin is pulled low, or (3) Master mute is enabled through the I2C interface.

Under-Voltage Protection

If the V_{DD} voltage is lower than 2.8V, the IS31AP2111 will turn off its speaker power stages and disable the digital processing section. The IS31AP2111 will return to normal operation When the V_{DD} supply increases above 2.9V.

ANTI-POP DESIGN

The device generates control signals which suppresses pop sounds during initial power on/off, power down/up, mute, and volume level changes.

3D SURROUND SOUND

The IS31AP2111 includes virtual surround sound technology for stereo signals inputs.

POWER ON SEQUENCE

At power up, the IS31AP2111's default volume setting is muted, so a de-mute command needs to be sent via the I2C interface once the device has completely powered up and stable.

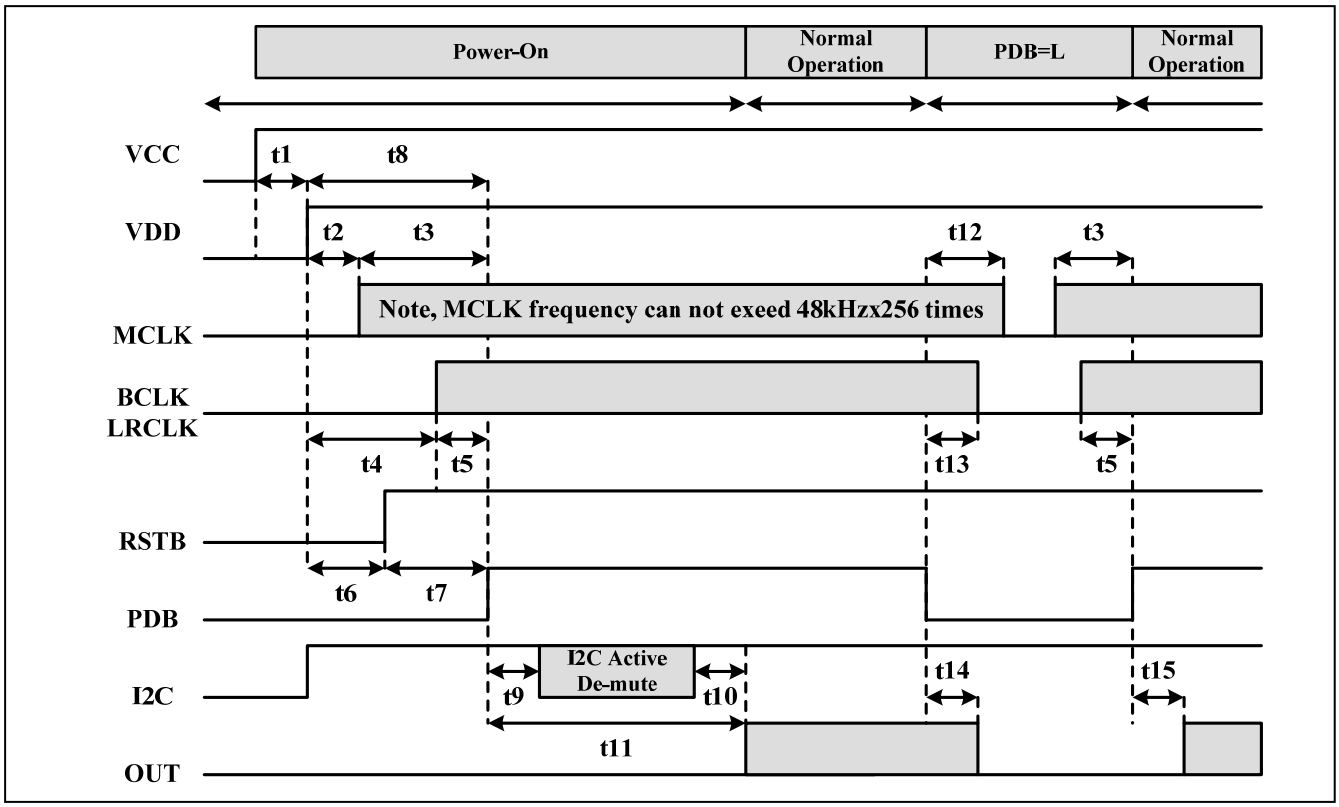


Figure 31 Power On Sequence

Table 2 Power On Sequence

Symbol	Condition	Min.	Max.	Unit
t1		0	-	ms
t2		0	-	ms
t3		10	-	ms
t4		0	-	ms
t5		10	-	ms
t6		10	-	ms
t7		0	-	ms
t8		200	-	ms
t9		20	-	ms
t10		-	0.1	ms
t11		-	0.1	ms
t12		25	-	ms
t13		25	-	ms
t14		-	22	ms
t15	DEF=L or H	-	0.1	ms

POWER OFF SEQUENCE

Hereunder is IS31AP2111's power off sequence.

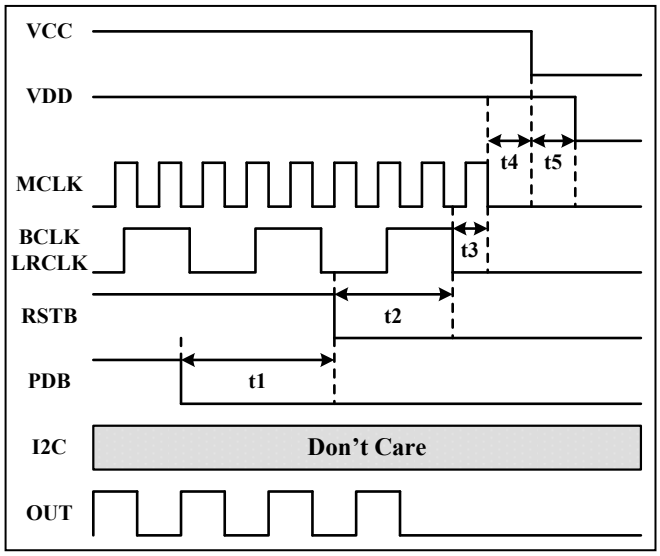


Figure 32 Power Off Sequence

Table 3 Power Off Sequence

Symbol	Min.
t1	35ms
t2	0.1ms
t3	0ms
t4	1ms
t5	1ms

I2C-BUS TRANSFER PROTOCOL

I2C INTERFACE

The IS31AP2111 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31AP2111 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A3 is decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write only):

Bit	A7:A4	A3	A2:A1	A0
Value	0110	AD	00	0/1

AD connected to GND, AD = 0;
AD connected to VCC, AD = 1;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31AP2111.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31AP2111's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31AP2111 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31AP2111, the register address byte is sent, most significant bit first. IS31AP2111 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31AP2111 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31AP2111 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31AP2111 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31AP2111 to the master (Figure 35).

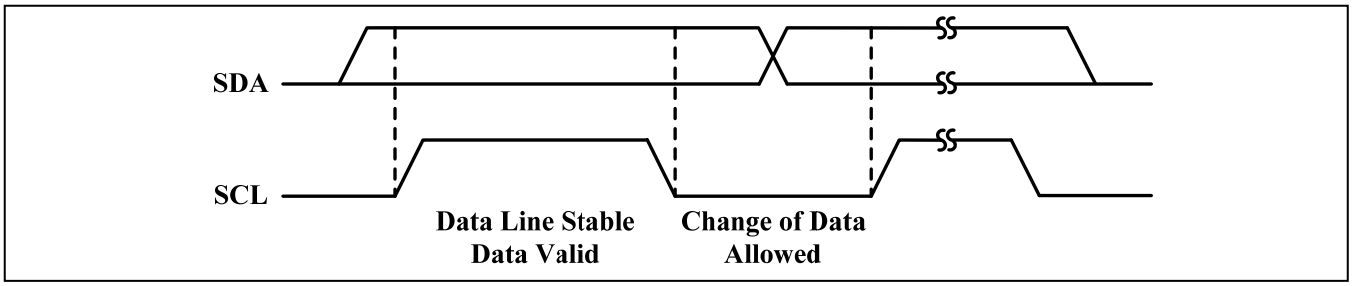


Figure 33 Bit Transfer

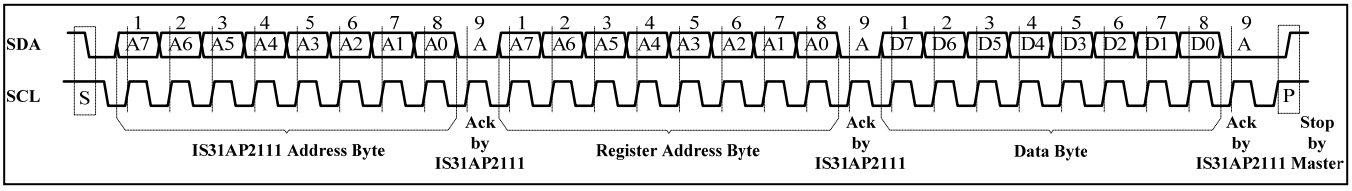


Figure 34 Writing to IS31AP2111

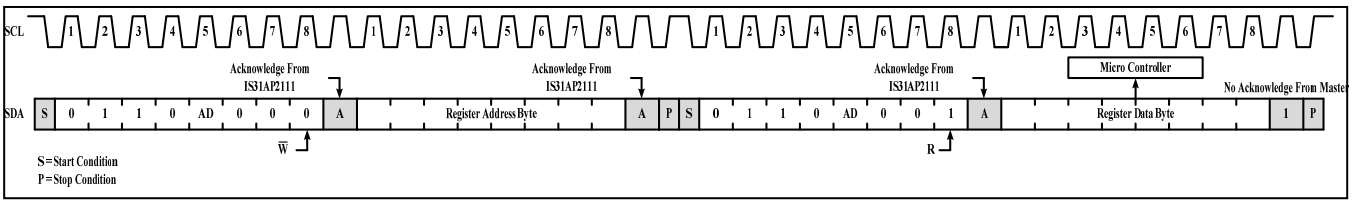
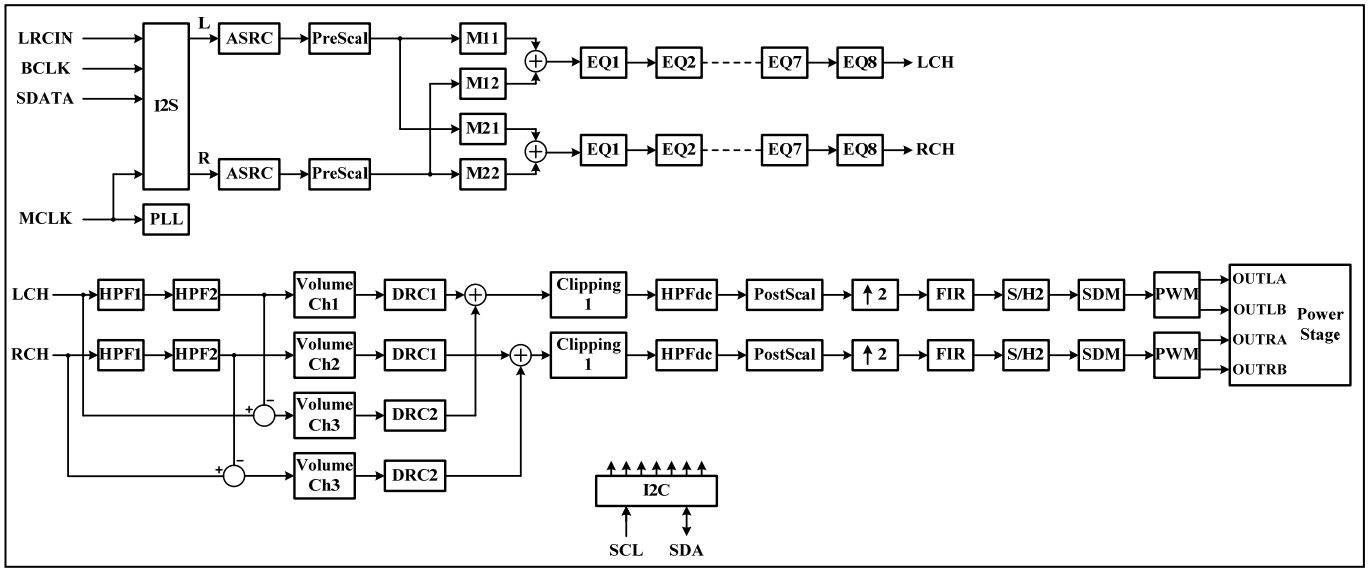


Figure 35 Reading from IS31AP2111

REGISTER DEFINITIONS

The IS31AP2111's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

Dual Band DRC Enable



Dual Band DRC Disable

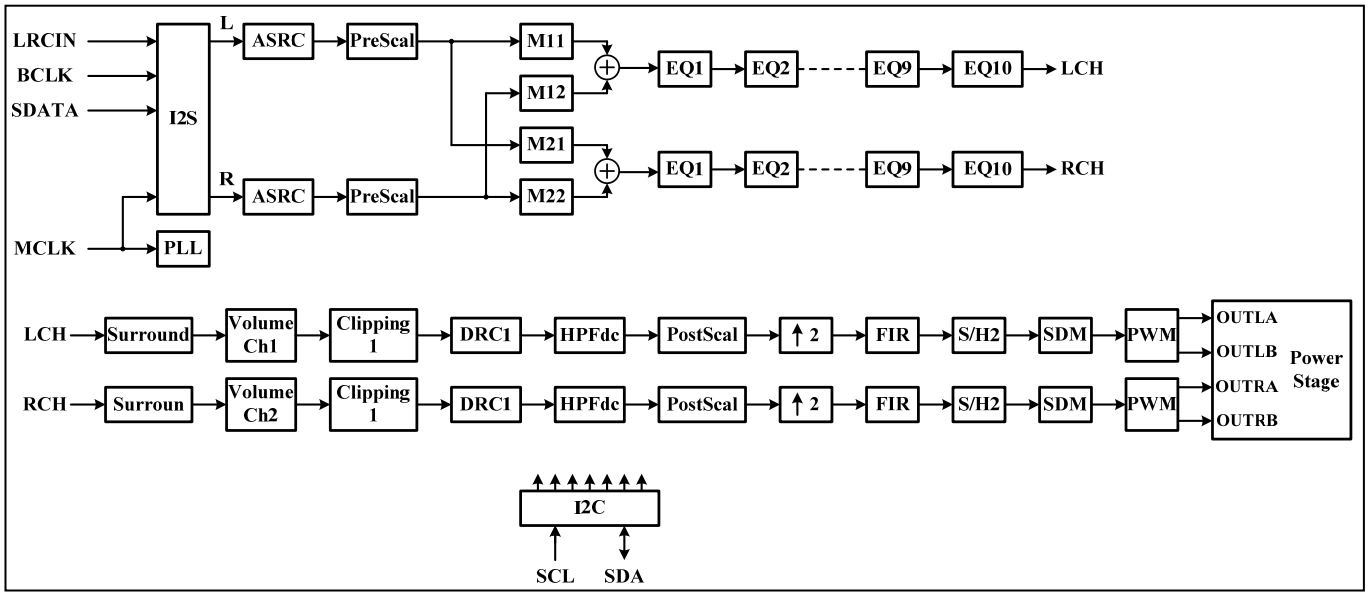


Table 4 Register Function

Address	Name	Table	Default
00h	State Control 1 Register	5	000x 0000
01h	State Control 2 Register	6	xx00 0000
02h	State Control 3 Register	7	xxxx 111x
03h	Master Volume Control Register	8	0001 1000
04h~06h	Channel 1~3 Volume Register	9	0001 0100
07h,08h	Bass/Treble Tone Register	10	xxx1 0000
09h	Reserved (Note)	-	-
0Ah	State Control 4 Register	11	1001 0000
0Bh~0Ch	Channel 1~2 Configuration Register	12	xxx1 0000
0Dh	Reserved	-	-
0Eh	DRC Limiter Attack/Release Rate Register	13	0110 1010
0Fh~10h	Reserved (Note)	-	-
11h	State Control 5 Register	14	xx11 x010
12h	VCC Under Voltage Selection Register	15	1xxx 0001
13h	Noise Gate Gain Register	16	xxx0 xx00
14h	Coefficient RAM Base Address Register	17	x000 0000
15h~23h	User-Defined Coefficients Register	18~22	-
24h	Coefficients Control Register	23	xxxx 0000
25h~29h	Reserved (Note)	-	-
2Ah	Power Saving Mode Switching Level Register	24	0000 1101
2Bh	Volume Fine Tune Register	25	0011 1111

Note: The reserved registers are not allowed to write any bits in them, or the IC will be abnormal.

Table 5 00h State Control 1 Register

Bit	D7:D5	D4	D3
Name	IF	-	PWML_X
Default	000	x	0
Bit	D2	D1	D0
Name	PWMR_X	LV_UVSEL	LREXC
Default	0	0	0

IS31AP2111 supports multiple serial data input formats including I2S, Left-alignment and Right-alignment. These formats are selected by users via D7~D5 of address 00h. The left/right channels can be exchanged to each other by programming to address 00h/D0, LREXC.

IF Input Format
000 I2S 16-24 bits
001 Left-alignment 16-24 bits
010 Right-alignment 16 bits
011 Right-alignment 18 bits
100 Right-alignment 20 bits
101 Right-alignment 24 bits
Others Not available

PWML_X OUTLA/B exchange
0 No exchange
1 Exchange

PWMR_X OUTRA/B exchange
0 No exchange
1 Exchange

LV_UVSEL LV Under Voltage Selection
0 2.8V
1 3.1V

LREXC Left/Right Channel Exchanged
0 No exchange
1 Left/Right exchange

Table 6 01h State Control 2 Register

Bit	D7:D6	D5:D4	D3:D0
Name	-	FS	PMF
Default	xx	00	0000

IS31AP2111 has a built-in PLL and multiple MCLK/Fs ratios are supported. Detail setting is shown in the following table.

FS	Sampling Frequency
00	32/44.1/48kHz
01	64/88.2/96kHz
1x	128/176.4/192kHz

PMF	Multiple MCLK/FS Ratio Setting
0000	1024x(FS=00)/ 512x(FS=01)/ 256x(FS=1x)
0001	64x
0010	128x
0011	192x
0100	256x
0101	384x (Not available when FS=1x)
0110	512x (Not available when FS=1x)
0111	576x (Not available when FS=01,1x)
1000	768x (Not available when FS=01,1x)
1001	1024x (Not available when FS=01,1x)
Others	Not available

Note: The FS × PMF should be lower than 49.152MHz, or the system will be error.

Table 7 02h State Control 3 Register

Bit	D7:D4	D3	D2:D1	D0
Name	-	MUTE	CM1:CM2	-
Default	xxxx	1	11	x

IS31AP2111 has mute function including master mute and channel mute. When master mute is enabled, all 2 processing channels are muted. User can mute these 2 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

MUTE	Master Mute
0	All channel not muted
1	All channel muted

CMx	Channel x Mute
0	Channel x not muted
1	Channel x muted

Table 8 03h Master Volume Control Register

Bit	D7:D0
Name	MV
Default	0001 1000

IS31AP2111 supports both master-volume (03h Register) and channel-volume control (04h, 05h and 06h Registers) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B. -103dB ≦ Total volume (Level A + Level B) ≦ +24dB.

MV	Master Volume
0000 0000	+12.0dB
0000 0001	+11.5dB
0000 0010	+11.0dB
…	
0001 1000	0dB
…	
1110 0110	-103.0dB
1110 0111	-∞
Others	-∞

Table 9 04h~06h Channel 1~3 Volume Registers

Bit	D7:D0
Name	CxV
Default	0001 0100

CxV	Channel x Volume
0000 0000	+12.0dB
0000 0001	+11.5dB
…	
0001 0100	+2dB
…	
1110 0110	-103.0dB
1110 0111	-∞
Others	-∞

Table 10 07h/08h Bass/Treble Tone Registers

Bit	D7:D5	D6:D0
Name	-	BTC/TTC
Default	xxx	10000

Last two sets of EQ can be programmed as bass/treble tone boost and cut. When, 0Ah Register, D6, BTE is set to high, the EQ-7 and EQ-8 will perform as bass and treble respectively. The -3dB corner frequency of bass is 360Hz, and treble is 7kHz. The gain range for both filters is +12db ~ -12dB with 1dB per step.

BTC/TTC	Bass/Treble Gain Setting
00000	+12dB
…	
00100	+12dB
00101	+11dB
…	
10000	0dB
10001	-1dB
…	
111xx	-12dB

Table 11 0Ah State Control 4 Register

Bit	D7	D6	D5	D4
Name	SRBP	BTE	TBDRCE	NGE
Default	1	0	0	1
Bit	D3	D2	D1	D0
Name	EQL	PSL	DSPB	HPB
Default	0	0	0	0

The IS31AP2111 provides several DSP setting as following.

SRBP Surround Bypass
0 Surround enable
1 Surround bypass

BTE Bass/Treble Selection Bypass
0 Bass/treble disable
1 Bass/treble enable

TBDRCE Two Band DRC Enable
0 Two band DRC disable
1 Two band DRC enable

NGE Noise Gate Enable
0 Noise gate disable
1 Noise gate enable

EQL EQ Link
0 Each channel uses individual EQ
1 Channel-2 uses channel-1 EQ

PSL Post-Scale Link
0 Each channel uses individual post-scale
1 Use channel-1 post-scale

DSPB EQ Bypass
0 EQ enable
1 EQ bypass

HPB DC Blocking HPF Bypass
0 HPF DC enable
1 HPF DC bypass

Table 12 0Bh~0Ch Channel 1~2 Configuration Registers

Bit	D7:D5	D4	D3
Name	-	CxDRCM	CxPCBP
Default	xxx	1	0
Bit	D2	D1	D0
Name	CxDRCBP	-	CxVBP
Default	0	x	0

The IS31AP2111 can configure each channel to enable or bypass DRC and channel volume and select the limiter set. IS31AP2111 support two mode of DRC, RMS and PEAK detection which can be selected via D4.

CxDRCM Channel 1/2 DRC Mode
0 Peak detection
1 RMS detection

CxPCBP Channel 1/2 Power Clipping Bypass
0 Channel 1/2 PC enable
1 Channel 1/2 PC bypass

CxDRCBP Channel 1/2 DRC Bypass
0 Channel 1/2 DRC enable
1 Channel 1/2 DRC bypass

CxVBP Channel 1/2 Volume Bypass
0 Channel 1/2's master volume operation
1 Channel 1/2's master volume bypass

Table 13 0Eh DRC Limiter Attack/Release Rate Register

Bit	D7:D5	D6:D0
Name	LA	LR
Default	0110	1010

The IS31AP2111 defines a set of limiter. The attack/release rates are defines as following table.

LA	DRC Attack Rate
0000	3dB/ms
0001	2.667dB/ms
0010	2.182dB/ms
0011	1.846dB/ms
0100	1.333dB/ms
0101	0.889dB/ms
0110	0.4528dB/ms
0111	0.2264dB/ms
1000	0.15dB/ms
1001	0.1121dB/ms
1010	0.0902dB/ms
1011	0.0752dB/ms
1100	0.0645dB/ms
1101	0.0563dB/ms
1110	0.0501dB/ms
1111	0.0451dB/ms

LR	DRC Release Rate
0000	0.5106dB/ms
0001	0.1371dB/ms
0010	0.0743dB/ms
0011	0.0499dB/ms
0100	0.0360dB/ms
0101	0.0299dB/ms
0110	0.0264dB/ms
0111	0.0208dB/ms
1000	0.0198dB/ms
1001	0.0172dB/ms
1010	0.0147dB/ms
1011	0.0137dB/ms
1100	0.0134dB/ms
1101	0.0117dB/ms
1110	0.0112dB/ms
1111	0.0104dB/ms

Table 14 11h State Control 5 Register

Bit	D7:D6	D5	D4	D3
Name	-	SW_RSTB	LVUV_FADE	-
Default	xx	1	1	x

Bit	D2	D1	D0
Name	DIS_MCLK_DET	QT_EN	PWM_SEL
Default	0	1	0

The IS31AP2111 provides several DSP setting as following.

SW_RSTB	Software Reset
0	Reset
1	Normal operation

LVUV_FADE	Low Under Voltage Fade
0	No fade
1	fade

DIS_MCLK_DET	Disable MCLK Detect Circuit
0	Enable MCLK detect circuit
1	Disable MCLK detect circuit

QT_EN	Power Saving Mode
0	Disable
1	Enable

PWM_SEL	PWM Modulation
0	Qua-ternary
1	Ternary

Table 15 12h VCC Under Voltage Selection Register

Bit	D7	D6:D4	D3:D0
Name	Dis_HVUV	-	HV_UVSEL
Default	1	xxx	0001

IS31AP2111 can disable HV under voltage detection via D7. IS31AP2111 support multi-level HV under voltage detection via D3~ D0, using this function, IS31AP2111 will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

Dis_HVUV	Disable HV Under Voltage Selection
0	Enable
1	Disable

HV_UVSEL	UV Detection Level
0000	8.2V
0001	9.7V
0011	13.2V
0100	15.5V
1100	19.5V
Others	9.7V

Table 16 13h Noise Gate Gain Register

Bit	D7:D5	D4
Name	-	DIS_NG_FADE
Default	xxx	0
Bit	D3:D2	D1:D0
Name	-	NG_GAIN
Default	xx	00

IS31AP2111 provide noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via D1~ D0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via D4.

DIS_NG_FADE	Disable Noise Gate Fade
0	Fade
1	No fade

NG_GAIN	Noise Gate Gain
00	x1/8
01	x1/4
10	x1/2
11	Mute

Table 17 14h Coefficient RAM Base Address Register

Bit	D7	D6:D0
Name	-	CFA
Default	x	000 0000

An on-chip RAM in IS31AP2111 stores user-defined EQ and mixing coefficients. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (14h), five sets of registers (15h ~ 23h) of three consecutive 8-bit entries for each 24-bit coefficient, and one control register (24h) to control access of the coefficients in the RAM.

CFA Coefficient RAM Base Address

Table 18 15h~17h User-Defined Coefficients Registers (Top/Middle/Bottom 8-bits of coefficients A1)

Bit	D7:D0
Name	C1B
Default	-

Table 19 18h~1Ah User-Defined Coefficients Registers (Top/Middle/Bottom 8-bits of coefficients A2)

Bit	D7:D0
Name	C2B
Default	-

Table 20 1Bh~1Dh User-Defined Coefficients Registers (Top/Middle/Bottom 8-bits of coefficients A1)

Bit	D7:D0
Name	C3B
Default	-

Table 21 1Eh~20h User-Defined Coefficients Registers (Top/Middle/Bottom 8-bits of coefficients B2)

Bit	D7:D0
Name	C4B
Default	-

Table 22 21h~23h User-Defined Coefficients Registers (Top/Middle/Bottom 8-bits of coefficients A0)

Bit	D7:D0
Name	C5B
Default	-

Table 23 24h Coefficients Control Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	RA	R1	WA	W1
Default	xxxx	0	0	0	0

RA	Enable Of Reading A Set Of Coefficients From RAM
0	Read complete
1	Read enable

R1	Enable Of Reading A Single Coefficients From RAM
0	Read complete
1	Read enable

WA Enable Of Writing A Set Of Coefficients To RAM
0 Write complete
1 Write enable

W1 Enable Of Writing A Single Coefficient To RAM
0 Write complete
1 Write enable

Table 24 2Ah Power Saving Mode Switching Level Register

Bit	D7:D5	D4:D0
Name	QT_SW_WINDOW	QT_SW_LEVEL
Default	000	01101

If the PWM exceeds the programmed switching power level (default 26×40ns), the modulation algorithm will change from quaternary into power saving mode. It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level - power saving mode hysteresis window, the modulation algorithm will change back to quaternary modulation.

QT_SW_WINDOW Power Saving Mode Hysteresis Window
000 2
001 3
010 4
011 5
100 6
101 7
110 8
111 9

QT_SW_LEVEL Switching Level
00000 4
00001 4
00010 6
…
01101 26
…
11111 62

Table 25 2Bh Volume Fine Tune Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	MV_FT	C1V_FT	C2V_FT	-
Default	00	11	11	11

IS31AP2111 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

MV_FT Master Volume Fine Tune
00 0dB
01 -0.125dB
10 -0.25dB
11 -0.375dB

C1V_FT Channel 1 Volume Fine Tune
00 0dB
01 -0.125dB
10 -0.25dB
11 -0.375dB

C2V_FT Channel 2 Volume Fine Tune
00 0dB
01 -0.125dB
10 -0.25dB
11 -0.375dB

RAM ACCESS

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read A Single Coefficient From RAM:

1. Write 7-bit of address to I2C address-0X14
2. Write 1 to R1 bit in address-0X24
3. Read top 8-bits of coefficient in I2C address-0X15
4. Read middle 8-bits of coefficient in I2C address-0X16
5. Read bottom 8-bits of coefficient in I2C address-0X17

Read A Set Of Coefficients From RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write 1 to RA bit in address-0X24
3. Read top 8-bits of coefficient A1 in I2C address-0X15
4. Read middle 8-bits of coefficient A1in I2C address-0X16
5. Read bottom 8-bits of coefficient A1 in I2C address-0X17
6. Read top 8-bits of coefficient A2 in I2C address-0X18
7. Read middle 8-bits of coefficient A2 in I2C address-0X19
8. Read bottom 8-bits of coefficient A2 in I2C address-0X1A
9. Read top 8-bits of coefficient B1 in I2C address-0X1B
10. Read middle 8-bits of coefficient B1 in I2C address-0X1C

11. Read bottom 8-bits of coefficient B1 in I2C address-0X1D
12. Read top 8-bits of coefficient B2 in I2C address-0X1E
13. Read middle 8-bits of coefficient B2 in I2C address-0X1F
14. Read bottom 8-bits of coefficient B2 in I2C address-0X20
15. Read top 8-bits of coefficient A0 in I2C address-0X21
16. Read middle 8-bits of coefficient A0 in I2C address-0X22
17. Read bottom 8-bits of coefficient A0 in I2C address-0X23

Write A Single Coefficient From RAM:

1. Write 7-bis of address to I2C address-0X14
2. Write top 8-bits of coefficient in I2C address-0X15
3. Write middle 8-bits of coefficient in I2C address-0X16
4. Write bottom 8-bits of coefficient in I2C address-0X17
5. Write 1 to W1 bit in address-0X24

Write A Set Of Coefficients From RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write top 8-bits of coefficient A1 in I2C address-0X15
3. Write middle 8-bits of coefficient A1 in I2C address-0X16
4. Write bottom 8-bits of coefficient A1 in I2C address-0X17
5. Write top 8-bits of coefficient A2 in I2C address-0X18
6. Write middle 8-bits of coefficient A2 in I2C address-0X19
7. Write bottom 8-bits of coefficient A2 in I2C address-0X1A
8. Write top 8-bits of coefficient B1 in I2C address-0X1B
9. Write middle 8-bits of coefficient B1 in I2C address-0X1C
10. Write bottom 8-bits of coefficient B1 in I2C address-0X1D
11. Write top 8-bits of coefficient B2 in I2C address-0X1E
12. Write middle 8-bits of coefficient B2 in I2C address-0X1F
13. Write bottom 8-bits of coefficient B2 in I2C address-0X20
14. Write top 8-bits of coefficient A0 in I2C address-0X21
15. Write middle 8-bits of coefficient A0 in I2C address-0X22
16. Write bottom 8-bits of coefficient A0 in I2C address-0X23
17. Write 1 to WA bit in address-0X24

Note: the read and write operation on RAM coefficients works only if LRCIN (Pin 15) switching on rising edge. And, before each writing operation, it is necessary to read the address-0X24 to confirm whether RAM is writable current in first. If the logic of W1 or WA is high, the coefficient writing is prohibited.

USER-DEFINED EQUALIZER

The IS31AP2111 provides 20 parametric Equalizer (EQ). Users can program suitable coefficients via I2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H_{(z)} = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.21. i.e., 3-bits for integer (MSB is the sign bit) and 21-bits for mantissa. Each coefficient range is from 0x800000 (-4) to 0x7FFFFF (+3.999999523). These coefficients are stored in User Defined RAM and are referenced in following manner:

CHxEQyA0=A0

CHxEQyA1=A1

CHxEQyA2=A2

CHxEQyB1=-B1

CHxEQyB2=-B2

Where *x* and *y* represents the number of channel and the band number of EQ equalizer.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x200000 which represents 1.

MIXER

The IS31AP2111 provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x800000 (-1) to 0x7FFFFF (0.9999998808). The function block diagram is as following figure:

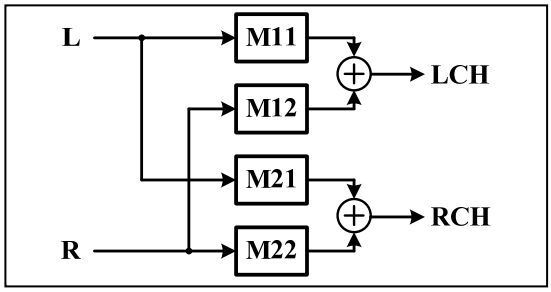


Figure 36 Mixer Function Block Diagram

PRE-SCALE

For each audio channel, IS31AP2111 can scale input signal level prior to EQ processing which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x7FFFFF. Programming of RAM is described in RAM access.

POST-SCALE

The IS31AP2111 provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 24-bit signed fractional multiplier. The post-scaling factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x7FFFFF. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

POWER CLIPPING

The IS31AP2111 provides power clipping function to avoid excessive signal that may destroy loud speaker. The power clipping level is defined by 24-bit representation and is stored in RAM address 0X6F. The following table shows the power clipping level's numerical representation.

Table 26 Sample Calculation For Power Clipping

Max. Amplitude	dB	Linear	Decimal	Hex (3.21 Format)
V_{CC}	0	1	2097152	200000
$V_{CC}\times0.707$	-3	0.707	1484574	16A71E
$V_{CC}\times0.5$	-6	0.5	1048576	100000
$V_{CC}\times L$	x	$L=10^{(x/20)}$	$D=2097152\times L$	H= dec2hex(D)

ATTACK THRESHOLD FOR DYNAMIC RANGE CONTROL (DRC)

The IS31AP2111 provides dynamic range control (DRC) function. When the input exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Attack threshold is defined by 24-bit representation and is stored in RAM address 0X71 and 0X72.

RELEASE THRESHOLD FOR DYNAMIC RANGE CONTROL (DRC)

After IS31AP2111 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Release threshold is defined by 24-bit representation and is stored in RAM address 0X73 and 0X74. The following table shows the attack and release threshold's numerical representation.

Table 27 Sample Calculation For Attack And Release Threshold

Power	dB	Linear	Decimal	Hex (3.21 Format)
(V_{CC}^2)/R	0	1	2097152	200000
(V_{CC}^2)/2R	-3	0.5	1048576	100000
(V_{CC}^2)/4R	-6	0.25	524288	80000
(V_{CC}^2)/R $\times$L	x	$L=10^{(x/10)}$	$D=2097152\times L$	H= dec2hex(D)

To best illustrate the dynamic range control, please refer to the following figure.

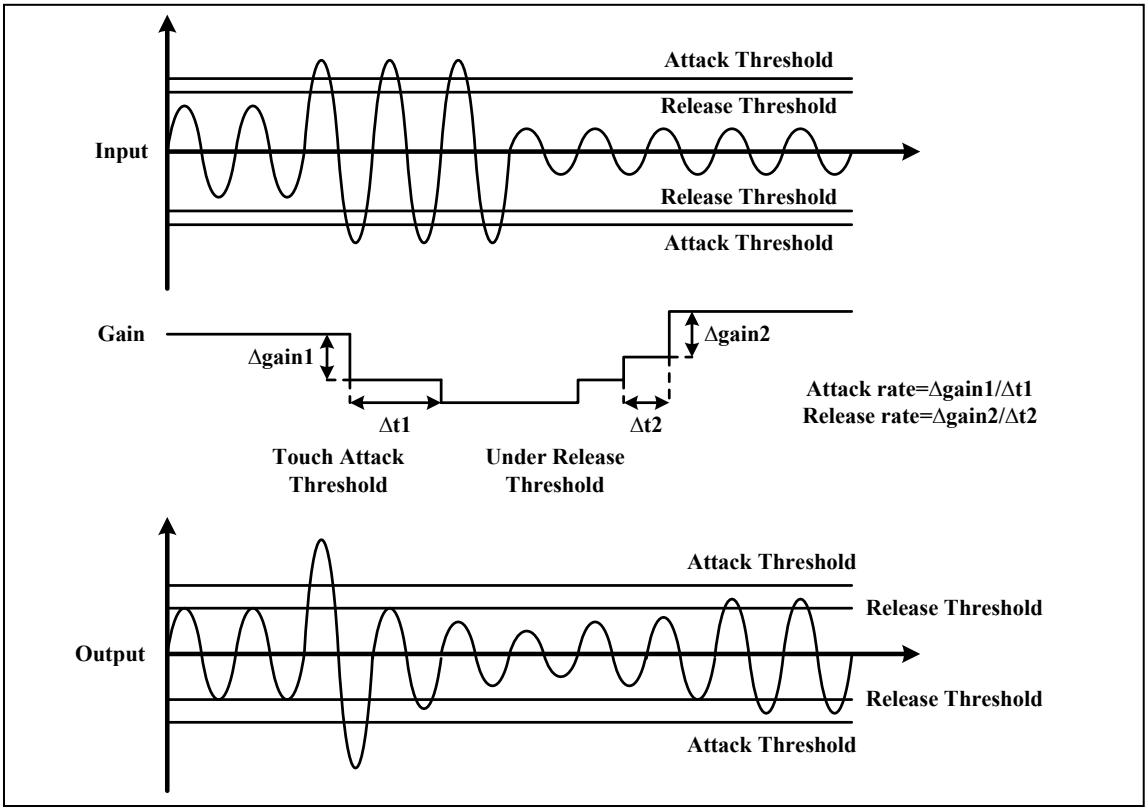


Figure 37 Attack And Release Threshold

NOISE GATE ATTACK LEVEL

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation and is stored in RAM address 0X75.

NOISE GATE RELEASE LEVEL

After entering the noise gating status, the noise gain will be removed whenever IS31AP2111 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation and is stored in RAM address 0X76. The following table shows the noise gate attack and release threshold level's numerical representation.

Table 28 Sample Calculation For Noise Gate Attack And Release Level

Input Amplitude	Linear	Decimal	Hex (1.23 Format)
0dB	1	8388607	7FFFFF
-100dB	10^{-5}	83	53
-110dB	$10^{-5.5}$	26	1A
xdB	L= $10^{(x/20)}$	D= 2097152×L	H= dec2hex(D)

DRC ENERGY COEFFICIENT

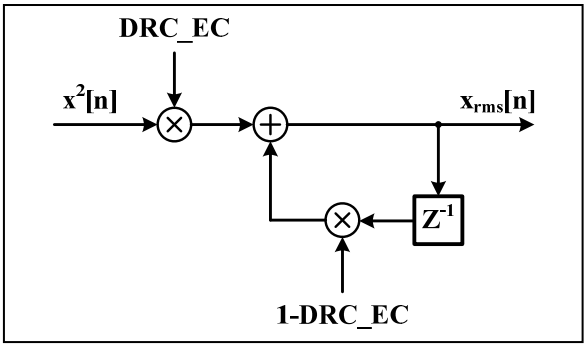


Figure 38 Digital Processing Of Calculating RMS Signal Power

The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Energy coefficient is defined by 24-bit representation and is stored in RAM address 0X77 and 0X78. The following table shows the DRC energy coefficient numerical representation.

Table 29 Sample Calculation For DRC Energy Coefficient

DRC Energy Coefficient	dB	Linear	Decimal	Hex (1.23 Format)
1	0	1	8388607	7FFFFF
1/256	-48.2	1/256	524288	80000
1/1024	-60.2	1/1024	131072	20000
L	x	$L=10^{(x/20)}$	D= 2097152×L	H= dec2hex(D)

THE USER DEFINED RAM

The contents of user defined RAM is represented in following table.

Table 30 User Defined RAM

Address	Name	Coefficient	Default	Address	Name	Coefficient	Default
0x00	Channel 1 EQ1	CH1EQ1A1	0x000000	0x32	Channel 2 EQ1	CH2EQ1A1	0x000000
0x01		CH1EQ1A2	0x000000	0x33		CH2EQ1A2	0x000000
0x02		CH1EQ1B1	0x000000	0x34		CH2EQ1B1	0x000000
0x03		CH1EQ1B2	0x000000	0x35		CH2EQ1B2	0x000000
0x04		CH1EQ1A0	0x200000	0x36		CH2EQ1A0	0x200000
0x05	Channel 1 EQ2	CH1EQ2A1	0x000000	0x37	Channel 2 EQ2	CH2EQ2A1	0x000000
0x06		CH1EQ2A2	0x000000	0x38		CH2EQ2A2	0x000000
0x07		CH1EQ2B1	0x000000	0x39		CH2EQ2B1	0x000000
0x08		CH1EQ2B2	0x000000	0x3A		CH2EQ2B2	0x000000
0x09		CH1EQ2A0	0x200000	0x3B		CH2EQ2A0	0x200000
0x0A	Channel 1 EQ3	CH1EQ3A1	0x000000	0x3C	Channel 2 EQ3	CH2EQ3A1	0x000000
0x0B		CH1EQ3A2	0x000000	0x3D		CH2EQ3A2	0x000000
0x0C		CH1EQ3B1	0x000000	0x3E		CH2EQ3B1	0x000000
0x0D		CH1EQ3B2	0x000000	0x3F		CH2EQ3B2	0x000000
0x0E		CH1EQ3A0	0x200000	0x40		CH2EQ3A0	0x200000
0x0F	Channel 1 EQ4	CH1EQ4A1	0x000000	0x41	Channel 2 EQ4	CH2EQ4A1	0x000000
0x10		CH1EQ4A2	0x000000	0x42		CH2EQ4A2	0x000000
0x11		CH1EQ4B1	0x000000	0x43		CH2EQ4B1	0x000000
0x12		CH1EQ4B2	0x000000	0x44		CH2EQ4B2	0x000000
0x13		CH1EQ4A0	0x200000	0x45		CH2EQ4A0	0x200000
0x14	Channel 1 EQ5	CH1EQ5A1	0x000000	0x46	Channel 2 EQ5	CH2EQ5A1	0x000000
0x15		CH1EQ5A2	0x000000	0x47		CH2EQ5A2	0x000000
0x16		CH1EQ5B1	0x000000	0x48		CH2EQ5B1	0x000000
0x17		CH1EQ5B2	0x000000	0x49		CH2EQ5B2	0x000000
0x18		CH1EQ5A0	0x200000	0x4A		CH2EQ5A0	0x200000
0x19	Channel 1 EQ6	CH1EQ6A1	0x000000	0x4B	Channel 2 EQ6	CH2EQ6A1	0x000000
0x1A		CH1EQ6A2	0x000000	0x4C		CH2EQ6A2	0x000000
0x1B		CH1EQ6B1	0x000000	0x4D		CH2EQ6B1	0x000000
0x1C		CH1EQ6B2	0x000000	0x4E		CH2EQ6B2	0x000000
0x1D		CH1EQ6A0	0x200000	0x4F		CH2EQ6A0	0x200000

Table 30 User Defined RAM (Continues)

Address	Name	Coefficient	Default	Address	Name	Coefficient	Default
0x1E	Channel 1 EQ7	CH1EQ7A1	0x000000	0x50	Channel 2 EQ7	CH2EQ7A1	0x000000
0x1F		CH1EQ7A2	0x000000	0x51		CH2EQ7A2	0x000000
0x20		CH1EQ7B1	0x000000	0x52		CH2EQ7B1	0x000000
0x21		CH1EQ7B2	0x000000	0x53		CH2EQ7B2	0x000000
0x22		CH1EQ7A0	0x200000	0x54		CH2EQ7A0	0x200000
0x23	Channel 1 EQ8	CH1EQ8A1	0x000000	0x55	Channel 2 EQ8	CH2EQ8A1	0x000000
0x24		CH1EQ8A2	0x000000	0x56		CH2EQ8A2	0x000000
0x25		CH1EQ8B1	0x000000	0x57		CH2EQ8B1	0x000000
0x26		CH1EQ8B2	0x000000	0x58		CH2EQ8B2	0x000000
0x27		CH1EQ8A0	0x200000	0x59		CH2EQ8A0	0x200000
0x28	Channel 1 EQ9	CH1EQ9A1	0x000000	0x5A	Channel 2 EQ9	CH2EQ9A1	0x000000
0x29		CH1EQ9A2	0x000000	0x5B		CH2EQ9A2	0x000000
0x2A		CH1EQ9B1	0x000000	0x5C		CH2EQ9B1	0x000000
0x2B		CH1EQ9B2	0x000000	0x5D		CH2EQ9B2	0x000000
0x2C		CH1EQ9A0	0x200000	0x5E		CH2EQ9A0	0x200000
0x2D	Channel 1 EQ10	CH3EQ1A1	0x000000	0x5F	Channel 2 EQ10	CH3EQ2A1	0x000000
0x2E		CH3EQ1A2	0x000000	0x60		CH3EQ2A2	0x000000
0x2F		CH3EQ1B1	0x000000	0x61		CH3EQ2B1	0x000000
0x30		CH3EQ1B2	0x000000	0x62		CH3EQ2B2	0x000000
0x31		CH3EQ1A0	0x200000	0x63		CH3EQ2A0	0x200000

Table 30 User Defined RAM (Continues)

Address	Name	Coefficient	Default
0x64	Channel 1 Mixer1	M11	0x7FFFFF
0x65	Channel 1 Mixer2	M12	0x000000
0x66	Channel 2 Mixer1	M21	0x000000
0x67	Channel 2 Mixer2	M22	0x7FFFFF
0x68~0x69	Reserve	Reserve	-
0x6A	Channel 1 Prescale	C1PRS	0x7FFFFF
0x6B	Channel 2 Prescale	C2PRS	0x7FFFFF
0x6C	Channel 1 Postscale	C1POS	0x7FFFFF
0x6D	Channel 2 Postscale	C2POS	0x7FFFFF
0x6E	Reserve	Reserve	-
0x6F	CH1.2 Power Clipping	PC1	0x200000
0x70	Reserve	Reserve	-
0x71	CH1.2 DRC Attack Threshold	DRC1_ATH	0x200000
0x72	CH1.2 DRC Release Threshold	DRC1_RTH	0x80000
0x73	CH3 DRC Attack Threshold	DRC2_ATH	0x200000
0x74	CH3 DRC Release Threshold	DRC2_RTH	0x80000
0x75	Noise Gate Attack Level	NGAL	0x0001A
0x76	Noise Gate Release Level	NGRL	0x000053
0x77	DRC1 Energy Coefficient	DRC1_EC	0x8000
0x78	DRC2 Energy Coefficient	DRC2_EC	0x2000

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

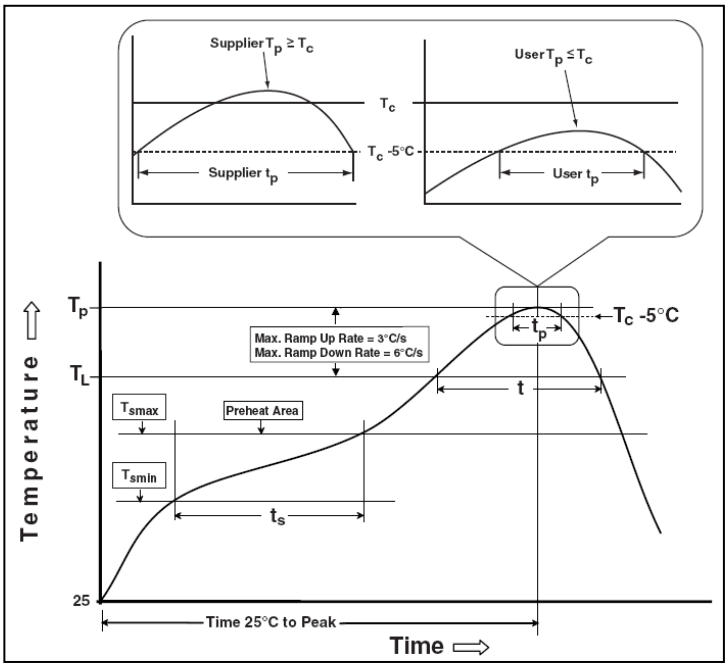
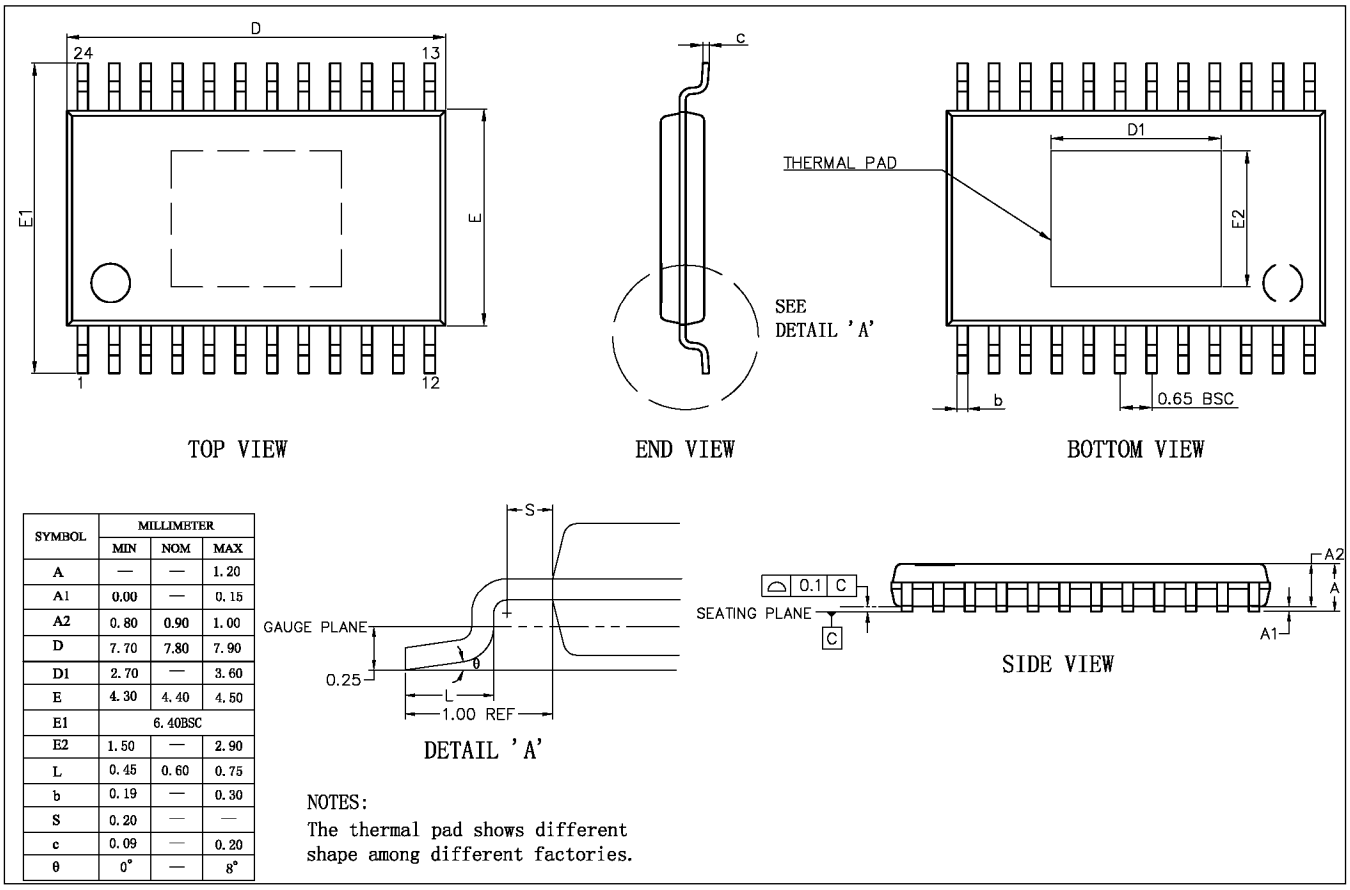


Figure 39 Classification Profile

PACKAGE INFORMATION

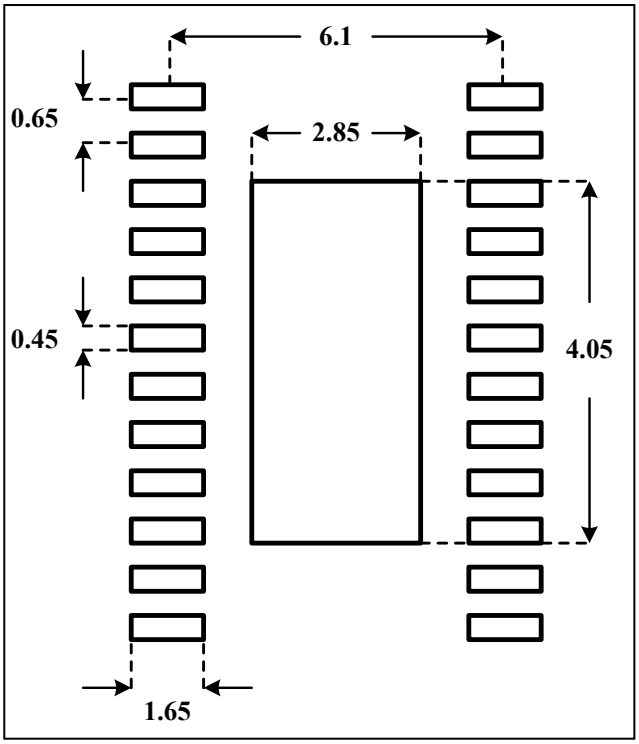
eTSSOP-24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.00
D	7.70	7.80	7.90
D1	2.70	—	3.60
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	2.90
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2015.06.12
B	1. Add mono mode 2. Update EC table 3. Add performance figures	2015.10.20