IS25LQ025B
IS25LQ512B
IS25LQ010B
IS25LQ020B
IS25LQ040B

256K/512K/1M/2M/4MBIT
3V QUAD SERIAL FLASH MEMORY WITH MULTI-I/O SPI

256K/512K/1M/2M/4MBIT
3V QUAD SERIAL FLASH MEMORY WITH MULTI-I/O SPI

FEATURES

- **Industry Standard Serial Interface**
  - IS25LQ040B: 4Mbit/ 512Kbyte
  - IS25LQ020B: 2Mbit/ 256Kbyte
  - IS25LQ010B: 1Mbit/ 128Kbyte
  - IS25LQ512B: 512Kbit/ 64Kbyte
  - IS25LQ025B: 256Kbit/ 32Kbyte
  - 256-bytes per Programmable Page Standard
  - Standard SPI/Dual/Quad Multi-I/O SPI
  - Supports Serial Flash Discoverable Parameters (SFDP)
- **High Performance Serial Flash (SPI)**
  - 104 MHz SPI/Dual/Quad Multi-I/O SPI
  - 416 MHz equivalent Quad SPI
  - 52MB/S Continuous Data Throughput
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous data read with Byte Wrap around
  - Allows XIP operations (execute in place)
  - Outperforms X16 Parallel Flash
- **Flexible & Cost Efficient Memory Architecture**
  - Uniform 4Kbyte Sectors or 32/64Kbyte Blocks
  - Flexible 4, 32, 64Kbyte, or Chip Erase
  - Standard Page Program 1 to 256 bytes
  - Program/Erase Suspend and Resume
- **Low Power with Wide Temp. Ranges**
  - Single 2.3V to 3.6V Voltage Supply
  - 10 mA Active Read Current
  - 8 µA Standby Current
  - Deep Power Down
  - Temp Grades:
    Extended: -40°C to +105°C
    V Grade: -40°C to +125°C
    Auto Grade: -40°C to +125°C
- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - 4x256-Byte dedicated security area with user-lockable bits, (OTP) One Time Programmable Memory
  - 128 bit Unique ID for each device
- **Industry Standard Pin-out & Pb-Free Packages**[1]
  - JB = 8-pin SOIC 208mil
  - JN = 8-pin SOIC 150mil
  - JD = 8-pin TSSOP 150mil
  - JV = 8-pin VVSOP 150mil
  - JK = 8-contact WSON 6x5mm
  - JU = 8-contact USON 2x3mm
  - KGD (call factory)

  Note1: IS25LQ040B (not available in JD)

GENERAL DESCRIPTION

The IS25LQ025/512/010/020/040B (256K/512K/1M/2M/4Mbit) Serial Flash memory offers a storage solution with flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" is for systems that have limited space, pins, and power. The IS25LQ025/512/010/020/040B is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which also serve as multi-function I/O pins in Dual and Quad modes (see pin descriptions). The IS25xQ series of Flash is ideal for code shadowing to RAM, execute in place (XIP) operations, and storing non-volatile data.

The memory array is organized into programmable pages of 256-bytes each. The IS25LQ025/512/010/020/040B supports page program mode where 1 to 256 bytes of data can be programmed into the memory with one command. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sectors and blocks allow greater flexibility for a variety of applications requiring solid data retention.

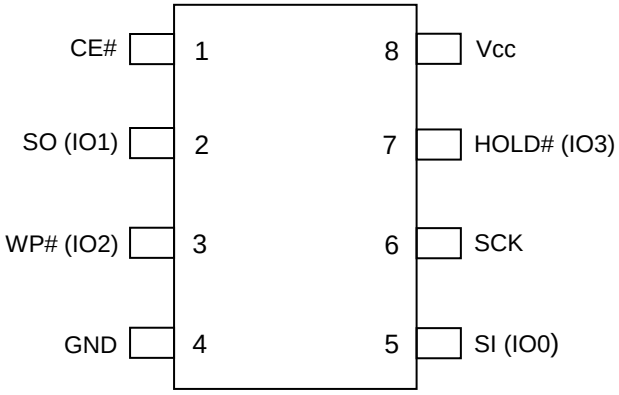
The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad output (SPI), and Dual/Quad I/O (SPI). Clock frequencies of up to 104MHz for all read modes allow for equivalent clock rates of up to 416MHz (104MHz x 4) allowing up to 52MBytes/S of throughput. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access for a XIP (execute in place) operation. The IS25LQ025/512/010/020/040B is manufactured using industry leading non-volatile memory technology and offered in industry standard lead-free packages. See Ordering Information for the density and package combinations available.

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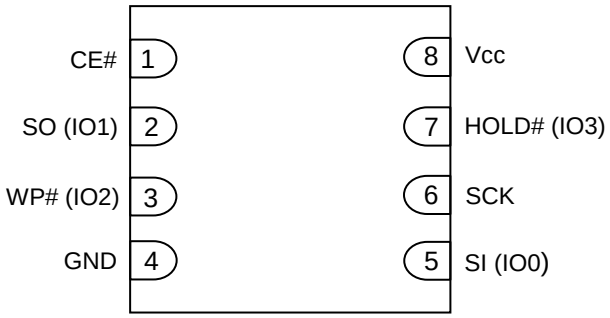
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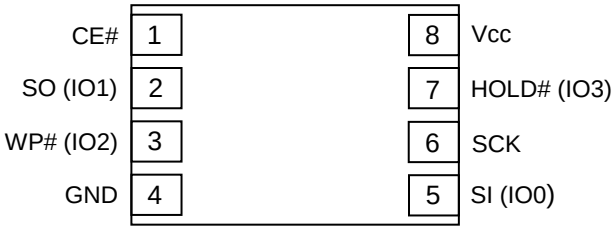
1. PIN CONFIGURATION



8-pin SOIC 208mil (Package: JB)
8-pin SOIC 150mil (Package: JN)
8-pin TSSOP 150mil (Package: JD)
8-pin VVSOP 150mil (Package: JV)



8-contact WSON 6x5mm (Package: JK)

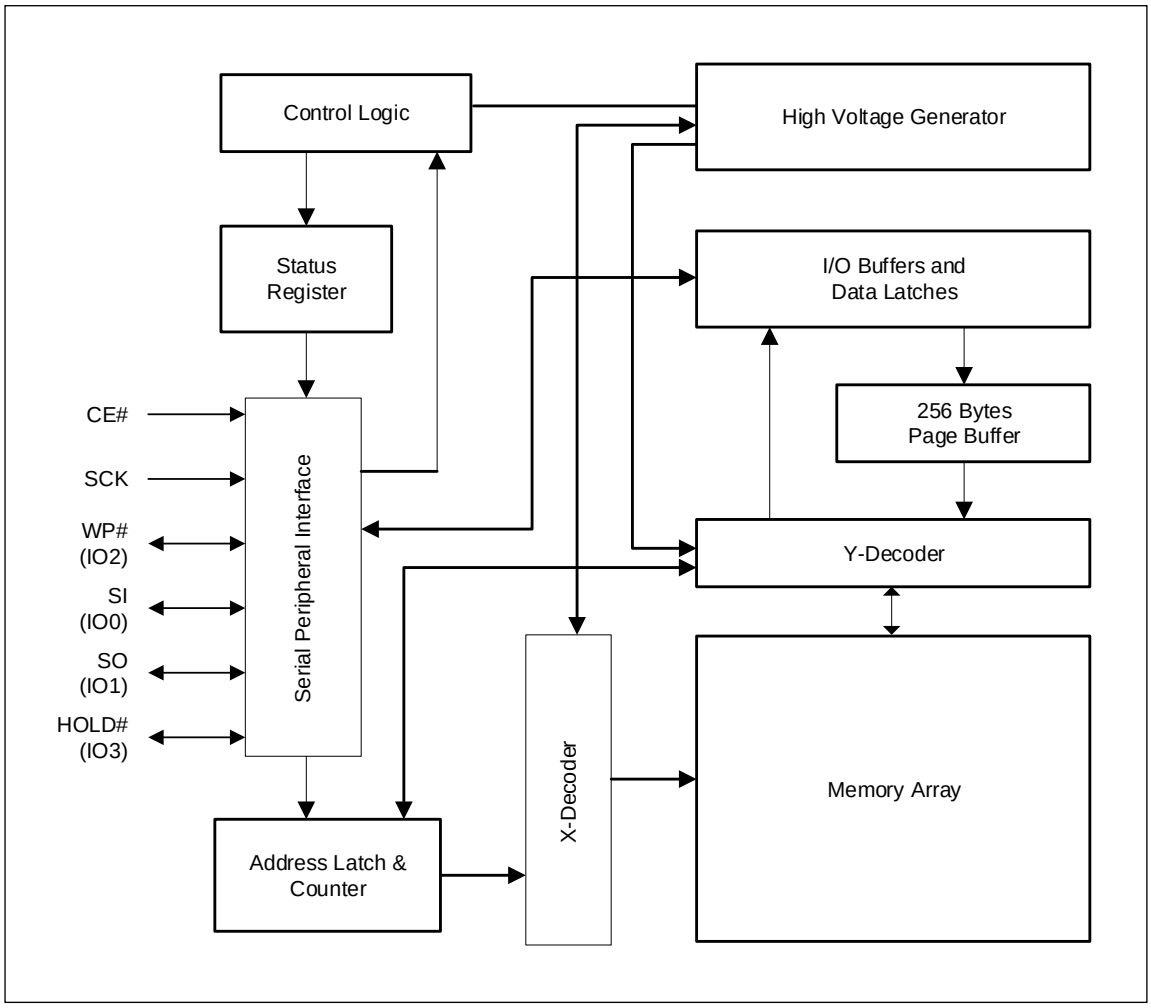


8-contact USON 2x3mm (Package: JU)

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to "1" and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP**#** high. When the SRWD is set to "0", the Status Register is not write-protected regardless of WP# state. When the QE bit is set to "1", the WP**#** pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3)	INPUT/OUTPUT	**Hold/Serial Data IO (IO3):** Pauses serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set to "1", HOLD**#** pin is not available since it becomes IO3. The HOLD# pin allows the device to be paused while it is selected. The HOLD# pin is active low. When HOLD# is in a low state, and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. When the QE bit of Status Register is set for Quad I/O, the HOLD# pin function is not available and becomes IO3 for Multi-I/O SPI mode.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled "NC" stand for "No Connect" and should be left uncommitted.

3. BLOCK DIAGRAM



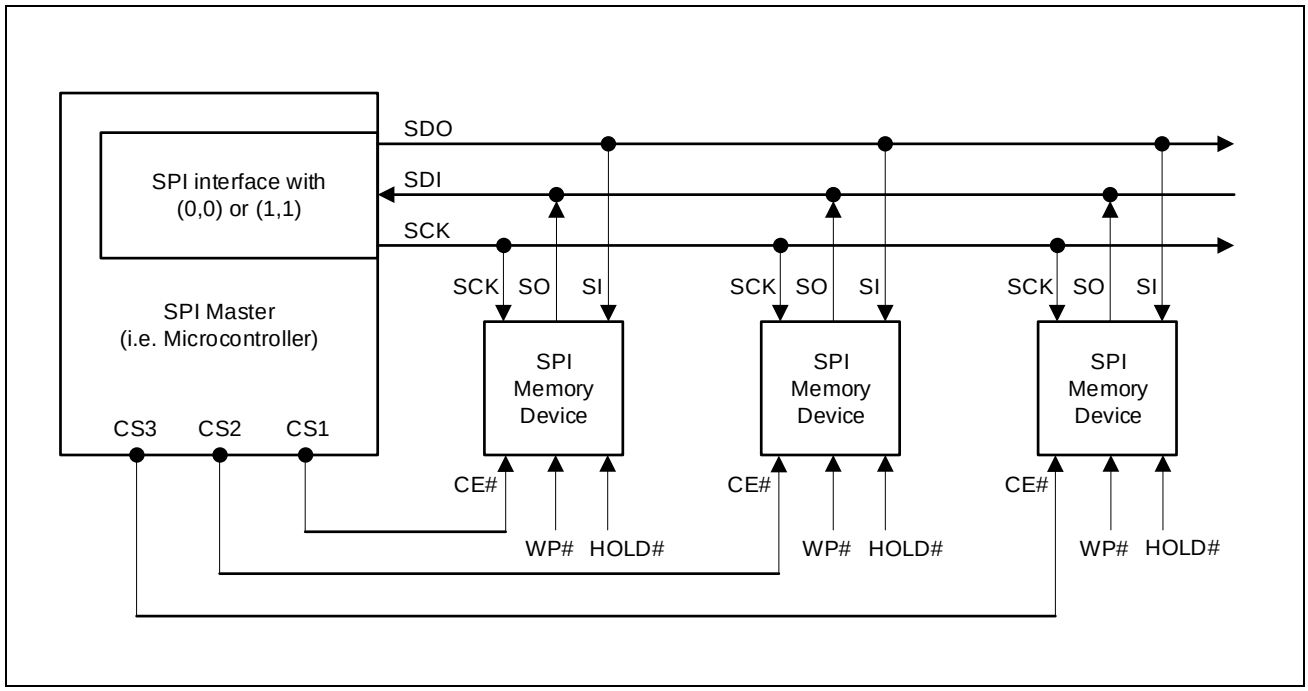
4. SPI MODES DESCRIPTION

Multiple IS25LQ025/512/010/020/040B devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1 the devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

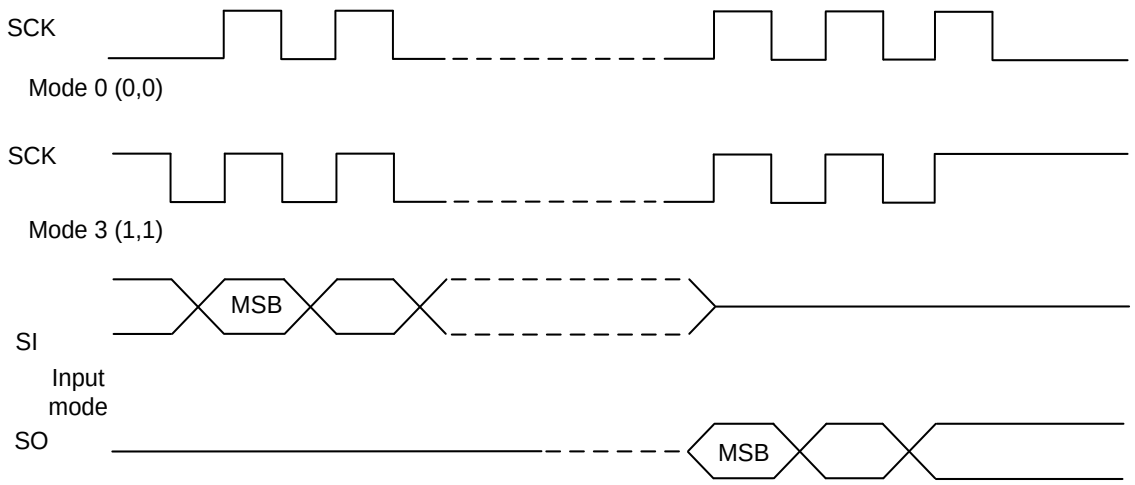
The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 for SPI mode. In SPI mode, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:
1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven high or low as necessary.
2. SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during Multi-IO mode.

Figure 4.2 SPI Mode Support



5. SYSTEM CONFIGURATION

The IS25LQ025/512/010/020/040B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) microcontrollers or any SPI interface-equipped system controllers.

The memory array of IS25LQ025/512/010/020/040B is divided into uniform 4Kbyte sectors or uniform 32/64Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 and Table 5.2 illustrate the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses of IS25LQ025/512/010B

Memory Density			Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
256 Kbit			Block 0	Block 0	Sector 0	4	000000h - 000FFFh
					Sector 1	4	001000h - 001FFFh
					:	:	:
					Sector 7	4	007000h - 007FFFh
	512 Kbit			Block 1	Sector 8	4	008000h - 008FFFh
					Sector 9	4	009000h - 009FFFh
					:	:	:
					Sector 15	4	00F000h - 00FFFFh
		1 Mbit	Block 1	Block 2	Sector 16	4	010000h - 010FFFh
					Sector 17	4	011000h - 011FFFh
					:	:	:
					Sector 23	4	017000h - 017FFFh
				Block 3	Sector 24	4	018000h - 018FFFh
					Sector 25	4	019000h - 019FFFh
					:	:	:
					Sector 31	4	01F000h – 01FFFFh

Table 5.2 Block/Sector Addresses of IS25LQ020/040B

Memory Density		Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
2 Mbit	4 Mbit	Block 0	Block 0	Sector 0	4	000000h - 000FFFh
				:	:	:
			Block 1	:	:	:
				Sector 15	4	00F000h - 00FFFFh
		Block 1	Block 2	Sector 16	4	010000h - 010FFFh
				:	:	:
			Block 3	:	:	:
				Sector 31	4	01F000h - 01FFFFh
		Block 2	Block 4	Sector 32	4	020000h - 020FFFh
				:	:	:
			Block 5	:	:	:
				Sector 47	4	02F000h - 02FFFFh
		Block 3	Block 6	Sector 48	4	030000h - 030FFFh
				:	:	:
			Block 7	:	:	:
				Sector 63	4	03F000h - 03FFFFh
		Block 4	Block 8	Sector 64	4	040000h - 040FFFh
				:	:	:
			Block 9	:	:	:
				Sector 79	4	04F000h - 04FFFFh
		Block 5	Block 10	Sector 80	4	050000h - 050FFFh
				:	:	:
			Block 11	:	:	:
				Sector 95	4	05F000h - 05FFFFh
		Block 6	Block 12	Sector 96	4	060000h - 060FFFh
				:	:	:
			Block 13	:	:	:
				Sector 111	4	06F000h - 06FFFFh
		Block 7	Block 14	Sector 112	4	070000h - 070FFFh
				:	:	:
			Block 15	:	:	:
				Sector 127	4	07F000h - 07FFFFh

6. REGISTERS

The IS25LQ025/512/010/020/040B has two sets of Registers: Status, Function.

6.1. STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Tables 6.1 & 6.2.

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R	Volatile
Bit 2	BP0	Block Protection Bit: (See Tables 6.4 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Non-Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Non-Volatile
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Non-Volatile

The BP0, BP1, BP2, BP3 and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP2, BP1, BP0, and SRWD bits were set to “0” at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for write Status or Function Register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled and all write operations described in Table 6.3 are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically be reset after the completion of any write operation.

Table 6.3 Instructions requiring WREN instruction ahead

Instructions must be preceded by the WREN instruction		
Name	**Hex Code**	**Operation**
PP	02h	Input Page Program
PPQ	32h/38h	Quad Input Page Program
SER	D7h/20h	Sector Erase
BER32 (32Kb)	52h	Block Erase 32K
BER64 (64Kb)	D8h	Block Erase 64K
CER	C7h/60h	Chip Erase
WRSR	01h	Write Status Register
WRFR	42h	Write Function Register
IRP	62h	Program Information Row

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Tables 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP**#** is pulled low (V_{IL}), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the Status Register that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD# pin is tied directly to the power supply.

Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits.

Status Register Bits				Protected Memory Area			
BP3	**BP2**	**BP1**	**BP0**	**4 Mbit**	**2 Mbit**	**1 Mbit**	**512K and 256K**
0	0	0	0	None	None	None	None
0	0	0	1	1 block : 7	1 block : 3	1 block : 1	All Blocks
0	0	1	0	2 blocks : 6 - 7	2 blocks : 2 - 3	All Blocks	
0	0	1	1	4 blocks : 4 - 7	All Blocks		
0	1	0	0	All Blocks			
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0	4 blocks 0 - 3			
1	1	0	1	2 blocks : 0 - 1	2 blocks : 0 - 1		
1	1	1	0	1 block : 0	1 block : 0	1 block : 0	
1	1	1	1	None	None	None	None

6.2. FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and 6.6.

Table 6.5 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0	ESUS	PSUS	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Table 6.6 Function Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	Reserved	Reserved	R	Non-Volatile
Bit 1	Reserved	Reserved	R	Non-Volatile
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	Volatile
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
Bit 4	IR Lock 0	Lock the information row 0: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Non-Volatile
Bit 5	IR Lock 1	Lock the information row 1: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Non-Volatile
Bit 6	IR Lock 2	Lock the information row 2: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Non-Volatile
Bit 7	IR Lock 3	Lock the information row 3: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Non-Volatile

Note: Function Register bits are only One Time Programmable (OTP) and cannot be modified.

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to “1” after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to “0”.

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is “1” after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to “0”.

IR lock bit 0 ~ 3: The information row lock bits are programmable. If the bit set to “1”, it can’t be programmed.

7. PROTECTION MODE

The IS25LQ025/512/010/020/040B supports hardware and software write-protection mechanisms.

7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, QE, and SRWD in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage (V_{WI}) is specified in the section 9.7 POWER-UP AND POWER-DOWN. All write sequence will be ignored when Vcc drops to V_{WI}.

Table 7.1 Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Note: Before the execution of any program, erase or write Status Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

7.2 SOFTWARE WRITE PROTECTION

The IS25LQ025/512/010/020/040B also provides a software write protection feature. The Block Protection (BP3, BP2, BP1, and BP0) bits allow part or the whole memory area to be write-protected.

8. DEVICE OPERATION

The IS25LQ025/512/010/020/040B utilizes an 8-bit instruction register. Refer to Table 8.1. Instruction Set for details on Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first_on Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in to end the operation.

Table 8.1 Instruction Set

Instruction Name	Hex Code	Operation		Mode	Maximum Frequency
RD	03h	Read Data Bytes from Memory at Normal Read Mode		SPI	33MHz
FR	0Bh	Read Data Bytes from Memory at Fast Read Mode		SPI	104MHz
FRDIO	BBh	Fast Read Dual I/O		SPI	104MHz
FRDO	3Bh	Fast Read Dual Output		SPI	104MHz
FRQIO	EBh	Fast Read Quad I/O		SPI	104MHz
FRQO	6Bh	Fast Read Quad Output		SPI	104MHz
PP	02h	Page Program Data Bytes Into Memory		SPI	104MHz
PPQ	32h/38h	Page Program Data Bytes Into Memory with Quad interface		SPI	104MHz
SER	D7h/20h	Sector Erase 4KB		SPI	104MHz
BER32 (32Kbyte)	52h	Block Erase 32KB	IS25LQ010/020/040B	SPI	104MHz
BER64 (64Kbyte)	D8h	Block Erase 64KB		SPI	104MHz
BER32 (32Kbyte)	52h/D8h	Block Erase 32KB	IS25LQ025/512B	SPI	104MHz
BER64 (64Kbyte)	NA	Block Erase 64KB		SPI	104MHz
CER	C7h/60h	Chip Erase		SPI	104MHz
WREN	06h	Write Enable		SPI	104MHz
WRDI	04h	Write Disable		SPI	104MHz
RDSR	05h	Read Status Register		SPI	104MHz
WRSR	01h	Write Status Register		SPI	104MHz
RDFR	48h	Read Function Register		SPI	104MHz
WRFR	42h	Write Function Register		SPI	104MHz
PERSUS	75h/B0h	Suspend during the program/erase		SPI	104MHz
PERRSM	7Ah/30h	Resume program/erase		SPI	104MHz
DP	B9h	Deep power down mode		SPI	104MHz
RDID, RDPD	ABh	Read Manufacturer and Product ID/release Deep power down		SPI	104MHz
RDUID	4Bh	Read Unique ID Number		SPI	104MHz
RDJDID	9Fh	Read Manufacturer and Product ID by JEDEC ID Command		SPI	104MHz
RDMDID	90h	Read Manufacturer and Device ID		SPI	104MHz
RDSFDP	5Ah	SFDP Read		SPI	104MHz
RSTEN	66h	Software reset enable		SPI	104MHz
RST	99h	Reset		SPI	104MHz

Instruction Name	Hex Code	Operation	Mode	Maximum Frequency
IRP	62h	Program Information Row	SPI	104MHz
IRRD	68h	Read Information Row	SPI	104MHz

8.1 READ DATA OPERATION (RD, 03h)

The Read Data (RD) instruction is used to read memory contents of the IS25LQ025/512/010/020/040B at a maximum frequency of 33MHz.

The RD instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MSB} (most significant bit) - A_0 are decoded. The remaining bits (A23 – A_{MSB+1}) are ignored. The first byte address can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

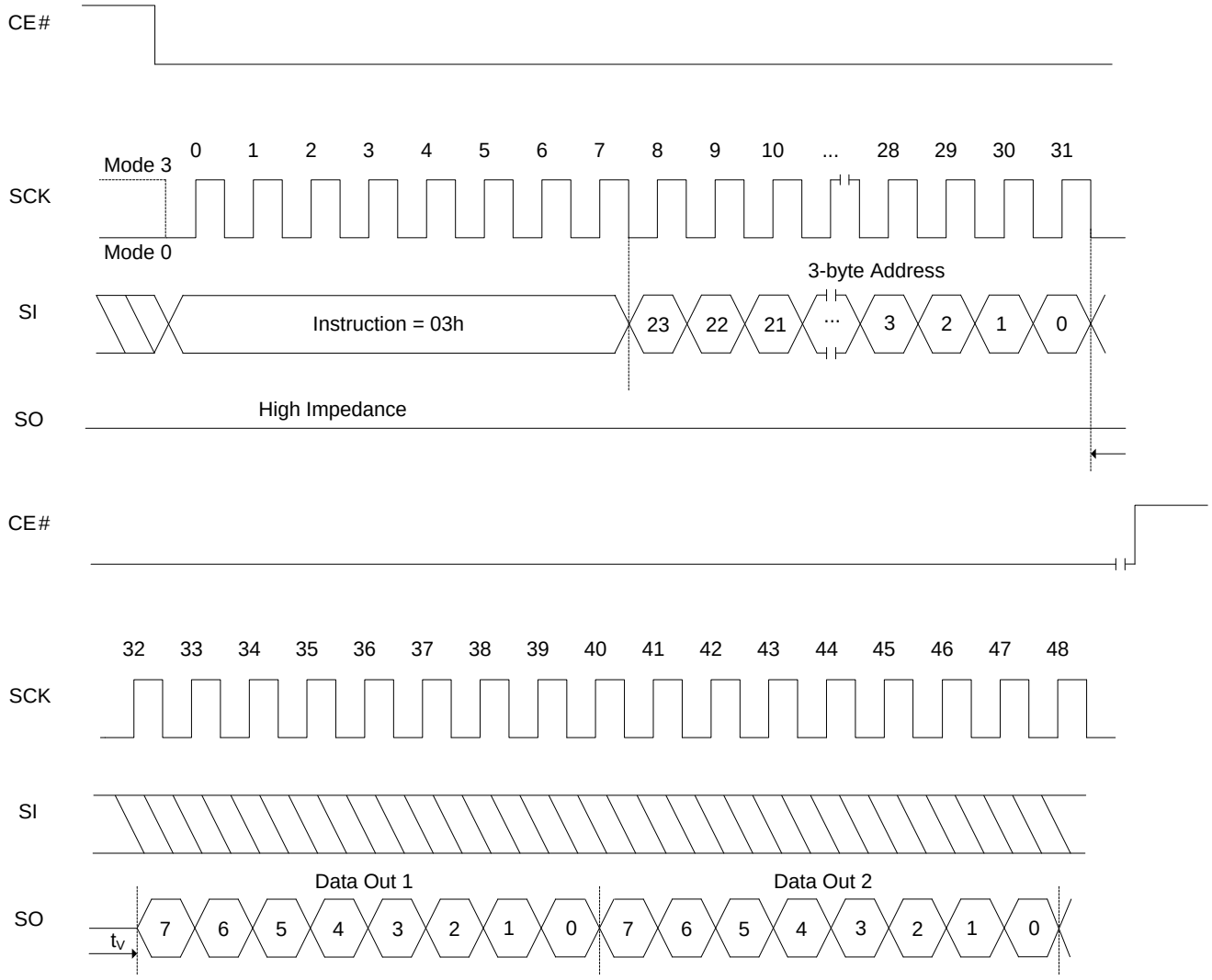
The first byte data (D7 - D0) address is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one RD instruction. The address is automatically incremented after each byte of data is shifted out. The RD operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous RD instruction.
If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Table 8.2 Address Key

Address	IS25LQ040B	IS25LQ020B	IS25LQ010B	IS25LQ512B	IS25LQ025B
A_{MSB}–A_0	A18-A0 (A23-A19=X)	A17-A0 (A23-A18=X)	A16-A0 (A23-A17=X)	A15-A0 (A23-A16=X)	A14-A0 (A23-A15=X)

Note: X=Don't Care

Figure 8.1 Read Data Sequence



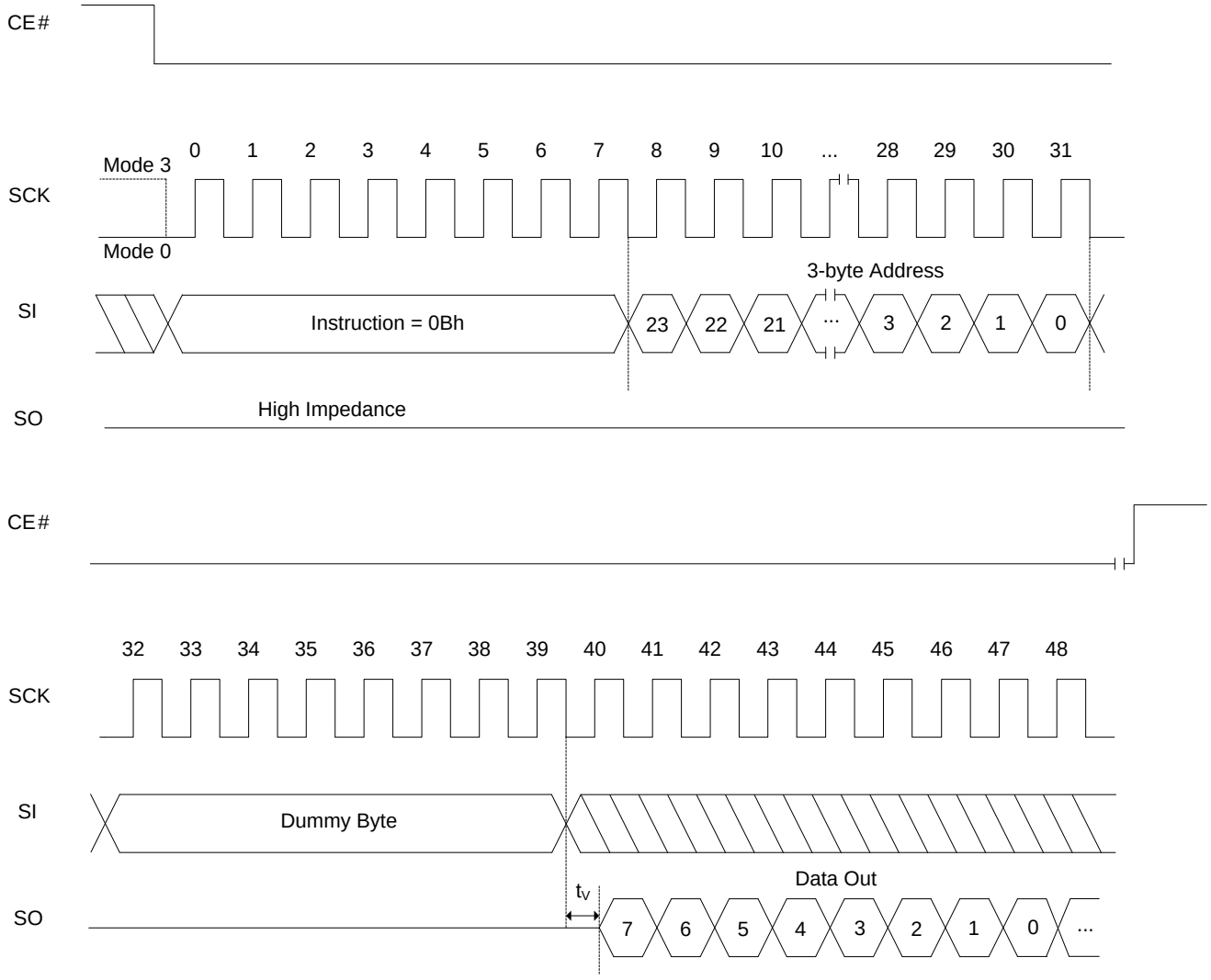
8.2 FAST READ DATA OPERATION (FR, 0Bh)

The Fast Read instruction is used to read memory data at up to a 104MHZ clock.

The Fast Read instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte from the address is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single Fast Read instruction. The Fast Read instruction is terminated by driving CE# high (VIH). If a Fast Read instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.2 Fast Read Data Sequence



8.3 HOLD OPERATION

HOLD# is used in conjunction with CE# to select the IS25LQ025/512/010/020/040B. When the device is selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to SO will be ignored while SO is in the high impedance state.

Timing graph can be referenced in AC Parameters Figure 9.3

8.4 FAST READ DUAL I/O OPERATION (FRDIO, BBh)

The FRDIO instruction allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

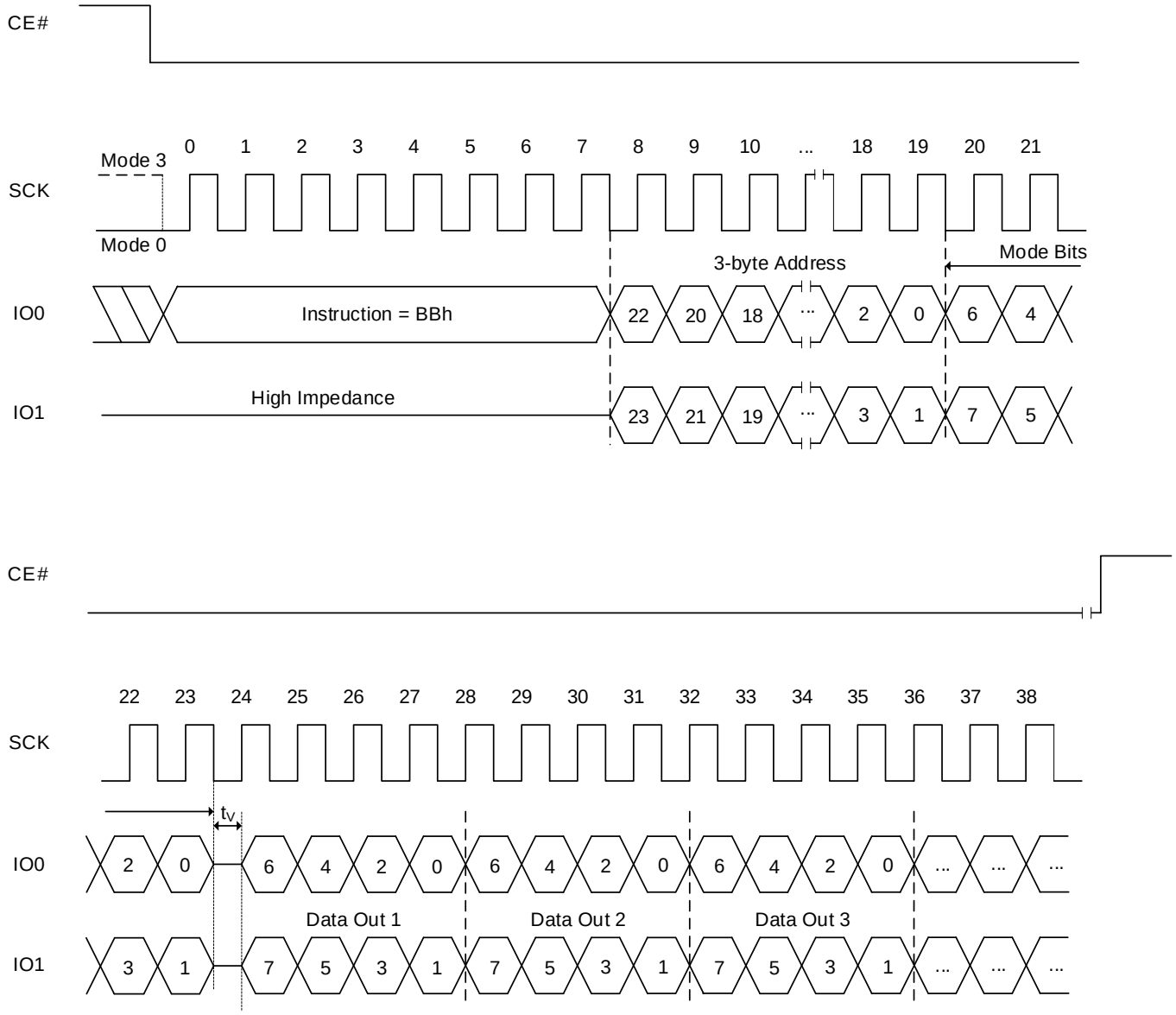
The FRDIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO1 and IO0 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and continue to shift in alternating on the two lines. If AXh (X: don't care) is input for the mode byte, the device will enter AX read mode. In the AX read mode, the next instruction expected from the device will be another FRDIO instruction and will not need the BBh instruction code so that it saves cycles as described in Figure 8.4. If the following mode byte is not set to AXh, the device will exit AX read mode. To avoid any I/O contention problem, X should be Hi-Z.

Once address and mode byte are input the device will read out data at the specified address. The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO1, while simultaneously the second bit is output on IO0. Figure 8.3 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

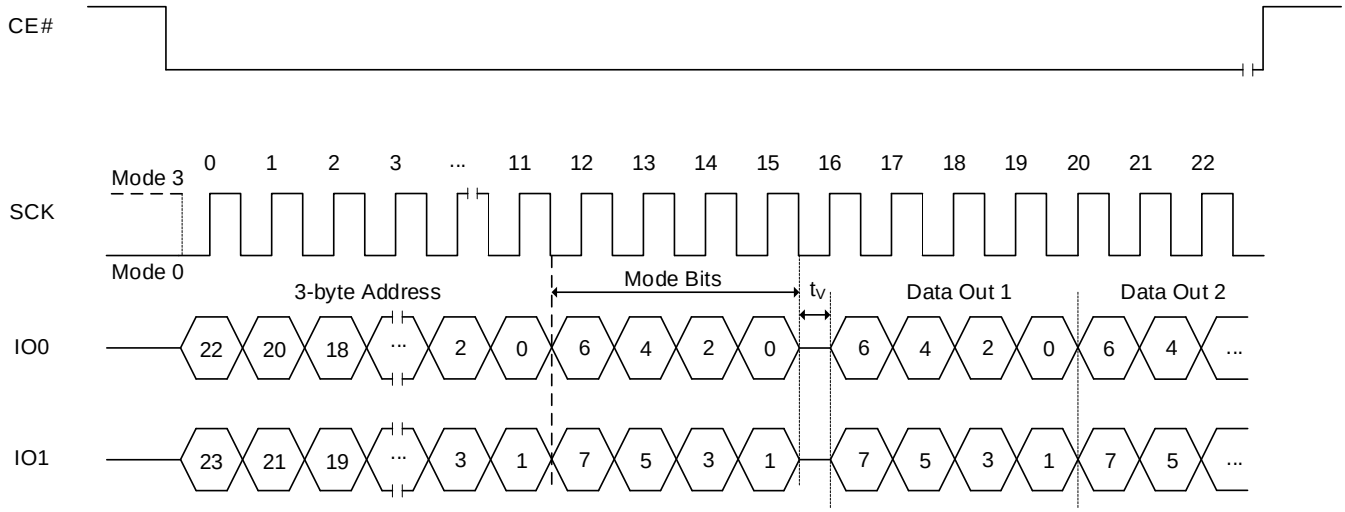
If a FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.3 Fast Read Dual I/O Sequence (with command decode cycles)



Note: If the mode bits=AXh (X is don't care), it can execute the AX read mode (without command). Anything but AXh in the mode byte cycle will keep the same sequence.

Figure 8.4 Fast Read Dual I/O Sequence (without command decode cycles)



Notes:
1. **If the mode bits=AXh (X: don't care), it will keep executing the AX read mode (without command). When the mode bits are different from AXh (X: don't care), the device will exit the AX read operation.**
2. **To avoid I/O contention, X should be Hi-Z.**

8.5 FAST READ DUAL OUTPUT OPERATION (FRDO, 3BH)

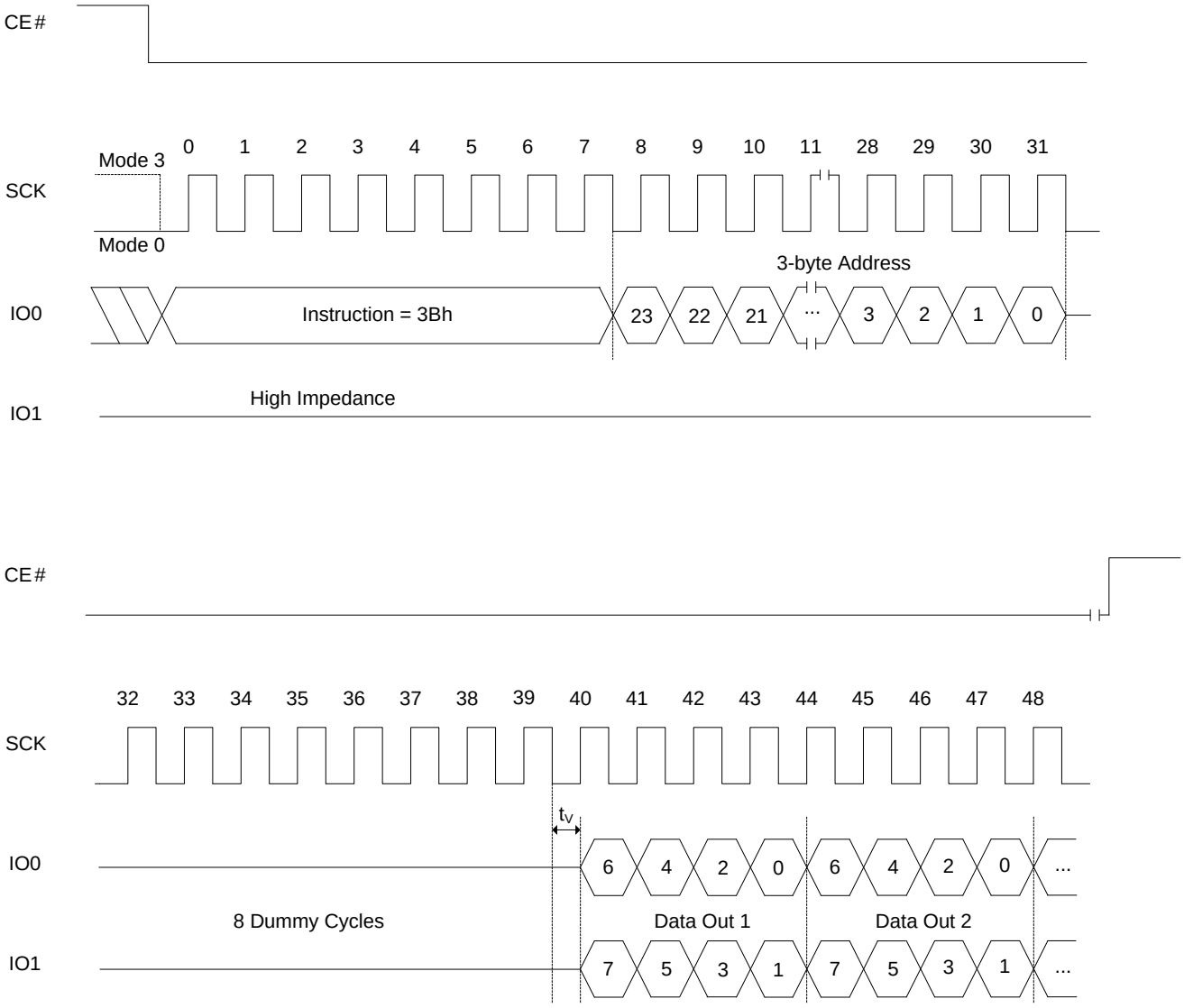
The FRDO instruction is used to read memory data on two output pins each at up to a 104MHZ clock.

The FRDO instruction code is followed by three address bytes (A23 – A0) and a dummy byte (8 clocks), transmitted via the IO0 line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency fCT, during the falling edge of SCK. The first bit (MSB) is output on IO1. Simultaneously the second bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving CE# high (VIH).

If a FRDO instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.5 Fast Read Dual-Output Sequence



8.6 FAST READ QUAD OUTPUT (FRQO, 6Bh)

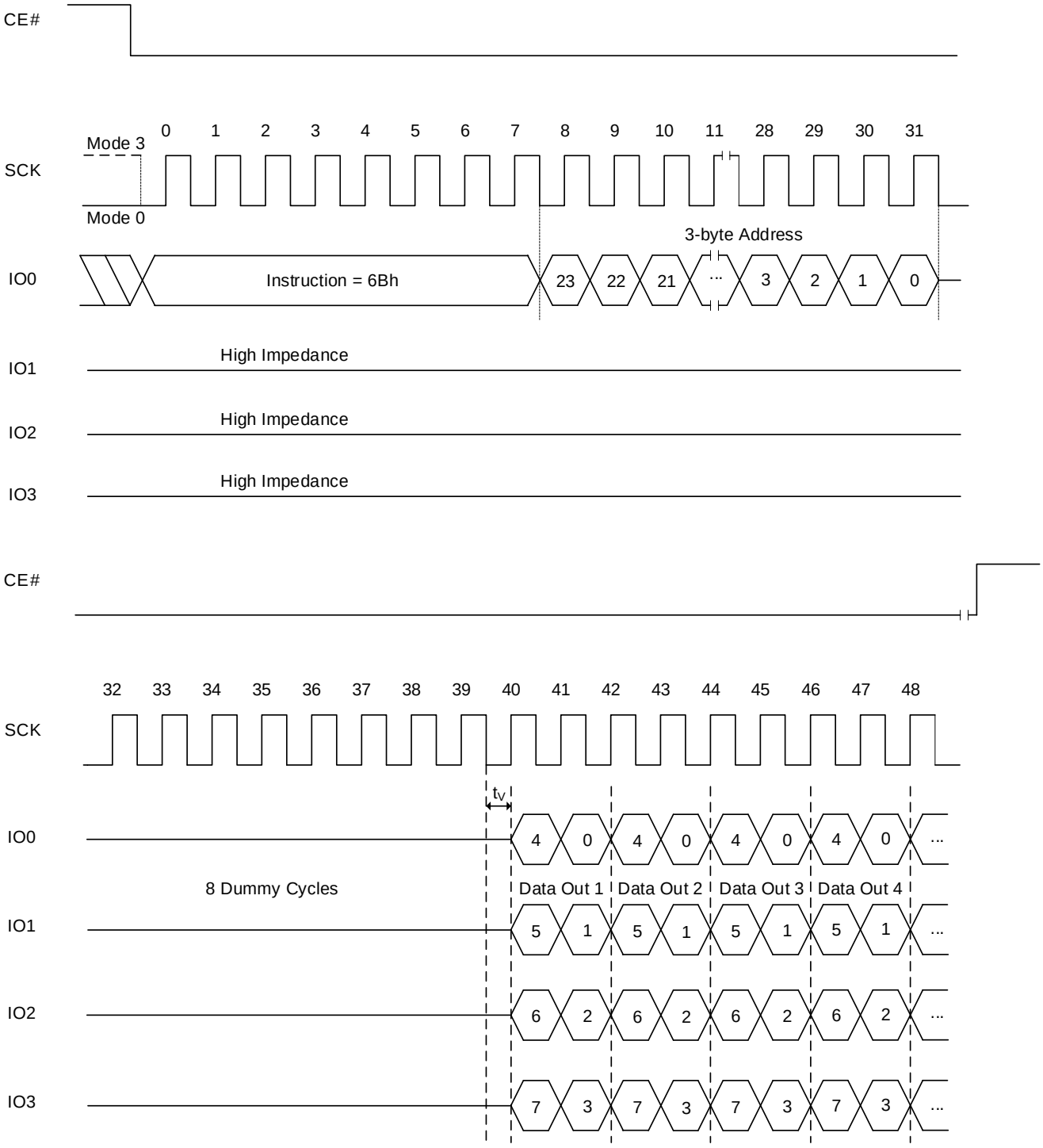
The FRQO instruction is used to read memory data on four output pins each at up to a 104 MHz clock.

The FRQO instruction code is followed by three address bytes (A23 – A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO3, IO2, IO1, and IO0 lines, with each group of four bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQO instruction. FRQO instruction is terminated by driving CE# high (VIH).

If a FRQO instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.6 Fast Read Quad-Output Sequence



8.7 FAST READ QUAD I/O OPERATION (FRQIO, EBh)

The FRQIO instruction allows the address bits to be input four bits at a time. This may allow for code to be executed directly from the SPI in some applications.

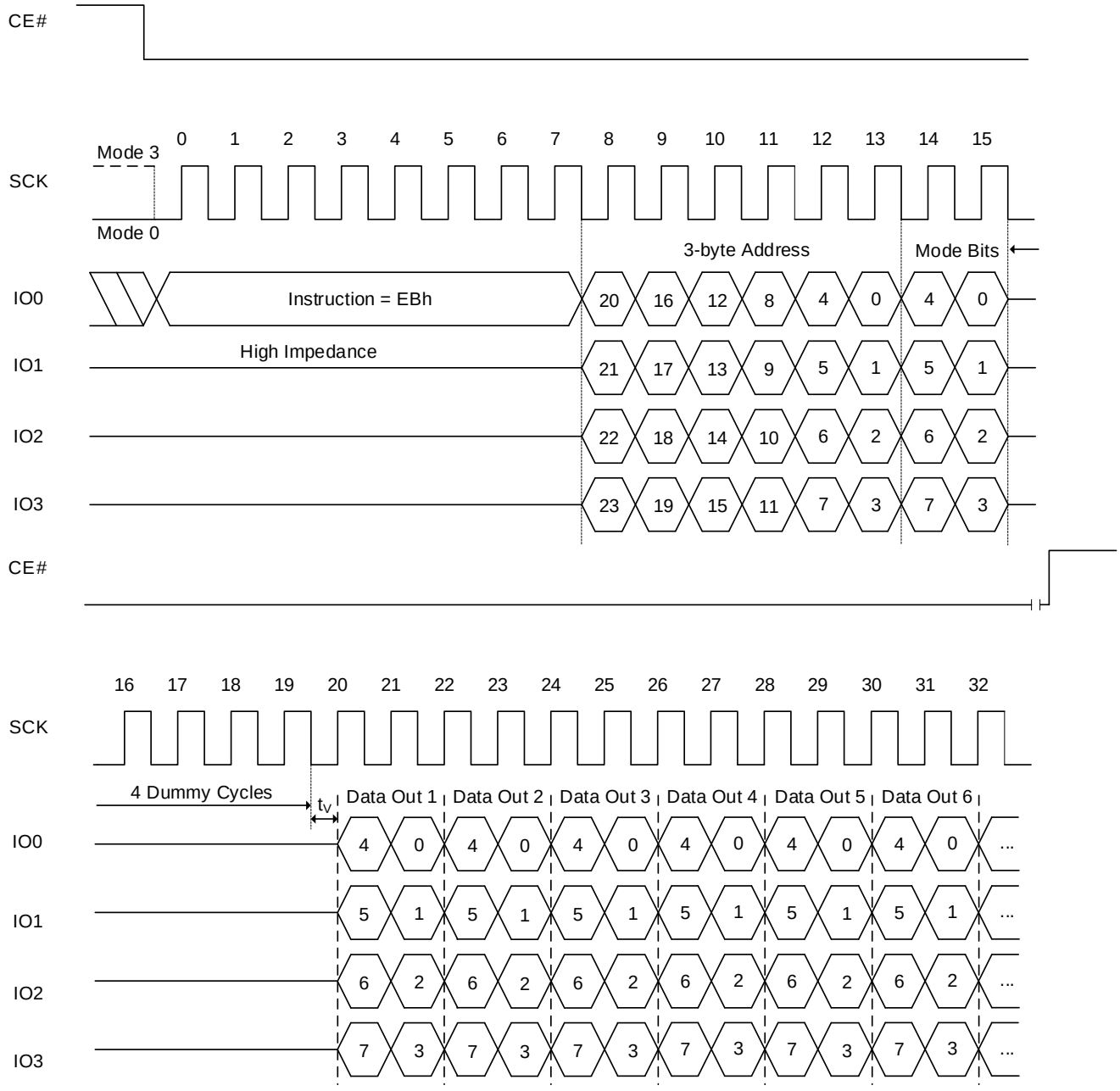
The FRQIO instruction code is followed by three address bytes (A23 – A0), a mode byte, and 4 dummy cycles, transmitted via the IO3, IO2, IO0 and IO1 lines, with each group of four bits latched-in during the rising edge of SCK. The address of MSB inputs on IO3, the next bit on IO2, the next bit on IO1, the next bit on IO0, and continue to shift in alternating on the four. The mode byte contains the value AXh, where X is a "don't care" value. After four dummy clocks, the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each group of four bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc. Figure 8.7 illustrates the timing sequence.

If the mode byte is AXh, the AX read mode is enabled. In the mode, the device expects that the next operation will be another FRQIO and subsequent FRQIO execution skips command code. It saves command cycles as described in Figure 8.8. The device will remain in this mode until the mode byte is different from AXh.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQIO instruction. FRQIO instruction is terminated by driving CE# high (V_{IH}).

If a FRQIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.7 Fast Read Quad I/O Sequence (with command decode cycles)



Note: If the mode bits=AXh (X is don't care), it can execute the AX read mode (without command). Anything but AXh in the mode byte cycle will keep the same sequence.

8.8 PAGE PROGRAM OPERATION (PP, 02h)

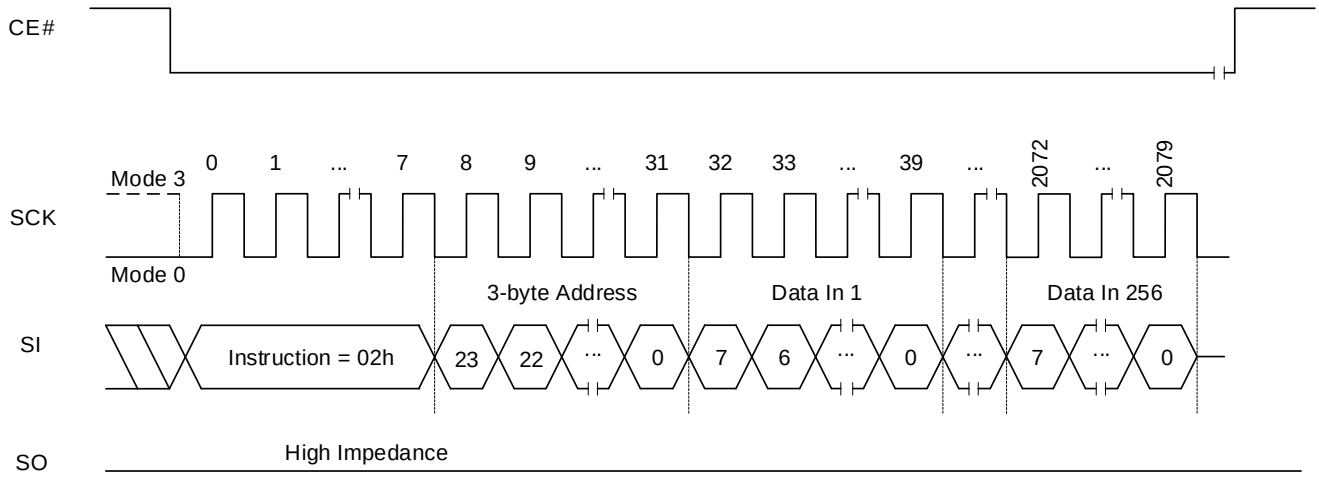
The Page Program (PP) instruction allows up to 256 bytes data to be programmed into memory in a single operation. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP2, BP1, BP0) bits. The PP instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of PP instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PP instruction code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PP instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. A byte cannot be reprogrammed without first erasing the whole sector or block.

Figure 8.8 Page Program Sequence



8.9 QUAD INPUT PAGE PROGRAM OPERATION (PPQ, 32h/38h)

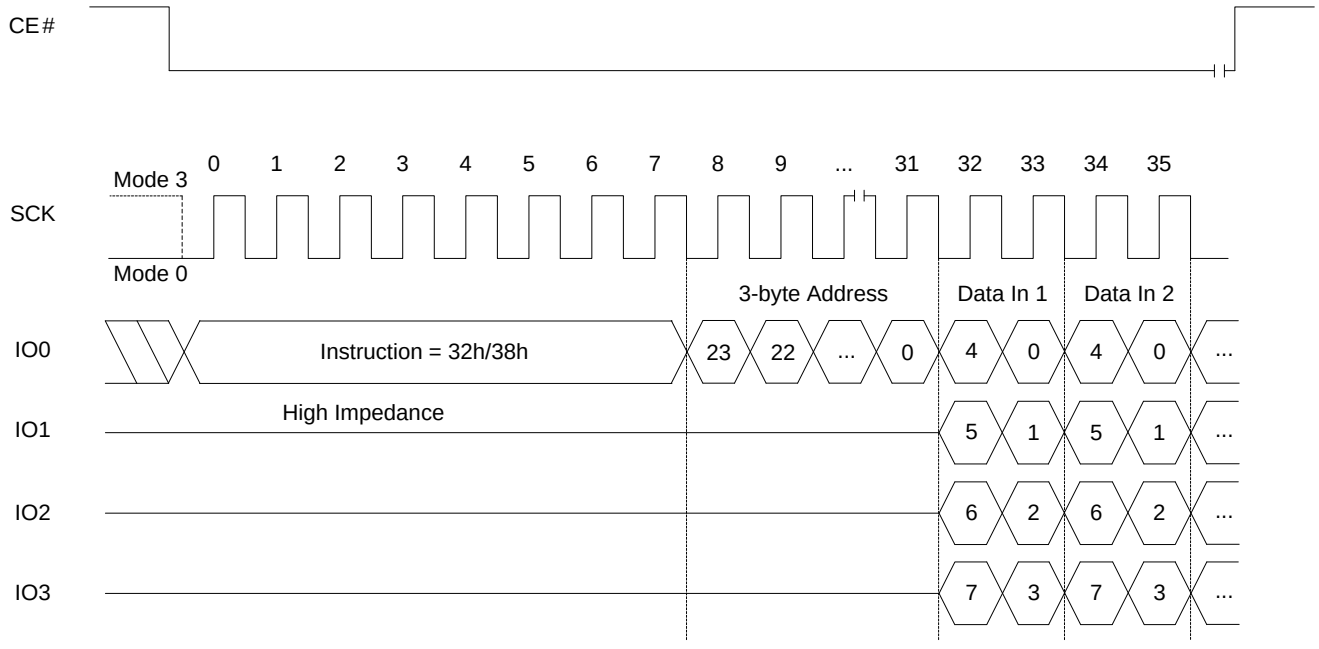
The Quad Input Page Program instruction allows up to 256 bytes data to be programmed into memory in a single operation with four pins (IO0, IO1, IO2 and IO3). The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A Quad Input Page Program instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of Quad Input Page Program instruction, the QE bit in the Status Register must be set to "1" and the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The Quad Input Page Program instruction code, three address bytes and program data (1 to 256 bytes) are input via the four pins (IO0, IO1, IO2 and IO3). Program operation will start immediately after the CE# is brought high, otherwise the Quad Input Page Program instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. A byte cannot be reprogrammed without first erasing the whole sector or block.

Figure 8.9 Quad Input Page Program Operation



8.10 ERASE OPERATION

The memory array of the IS25LQ025/512/010/020/040B is organized into uniform 4Kbyte sectors or 32/64Kbyte uniform blocks (a block consists of sixteen adjacent sectors).

Before a byte is reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to "1"). In order to erase the device, there are three erase instructions available: Sector Erase (SER), Block Erase (BER) and Chip Erase (CER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase or chip erase operation can be executed prior to any programming operation.

8.11 SECTOR ERASE OPERATION (SER, D7h/20h)

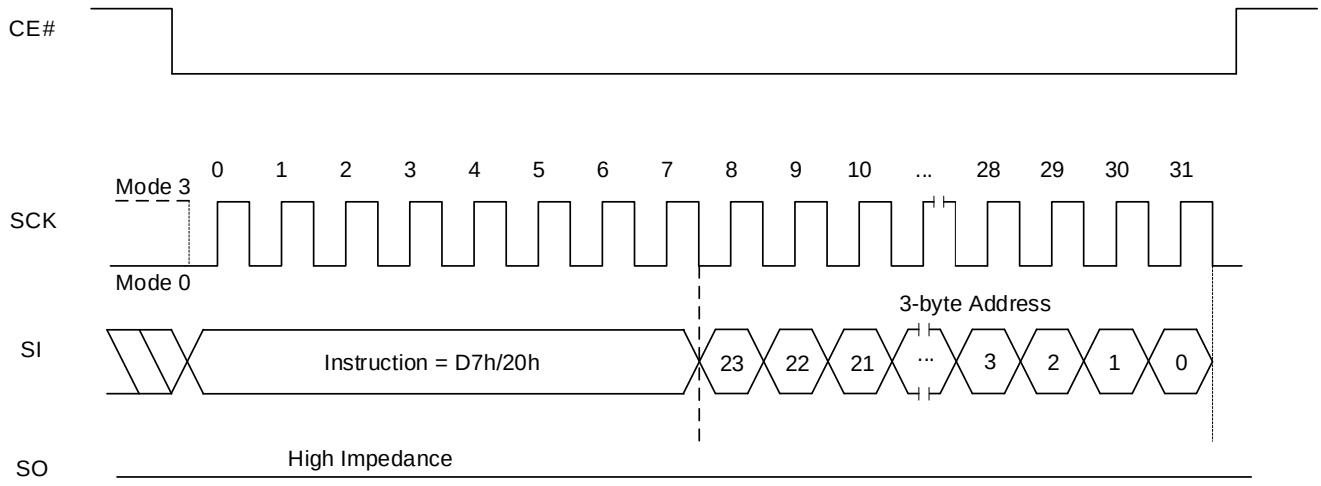
A Sector Erase (SER) instruction erases a 4Kbyte sector. Before the execution of a SER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is reset automatically after the completion of sector an erase operation.

A SER instruction is entered, after CE# is pulled low to select the device and stays low during the entire instruction sequence. The SER instruction code, and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 8.10 for the Sector Erase Sequence.

During an erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR instruction.

If the WIP bit is "1", the erase operation is still in progress. If the WIP bit is "0", the erase operation has been completed.

Figure 8.10 Sector Erase Sequence



8.12 BLOCK ERASE OPERATION (BER32K:52h, BER64K:D8h)

A Block Erase (BER) instruction erases a 32/64Kbyte block of the IS25LQ025/512/010/020/040B. Before the execution of a BER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

The BER instruction code and three address bytes are input via SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 8.11-8.12 for the Block Erase Sequence.

Figure 8.11 Block Erase (64k) Sequence

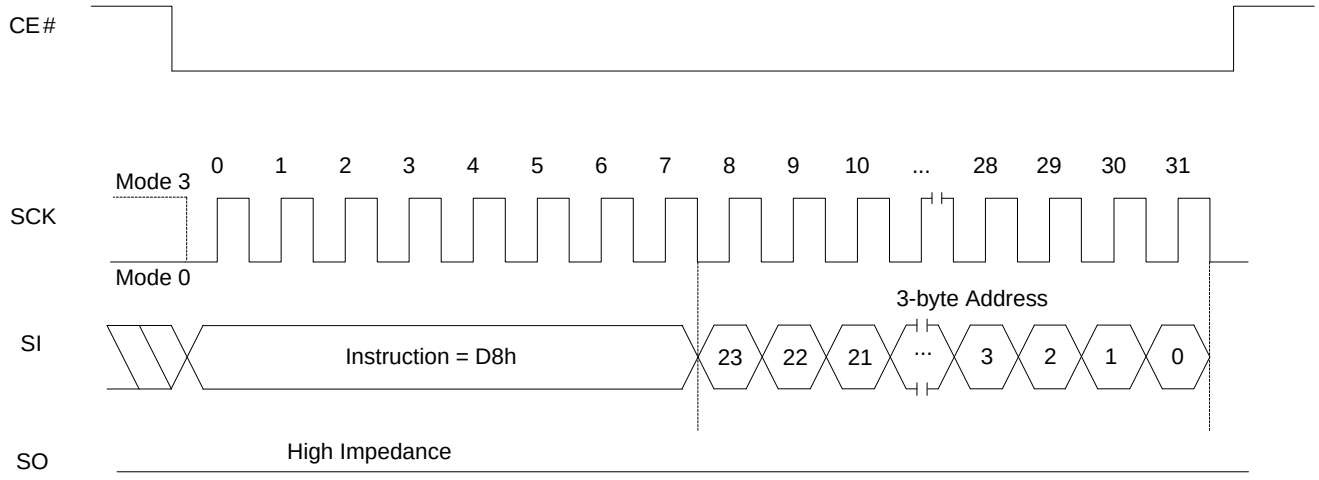
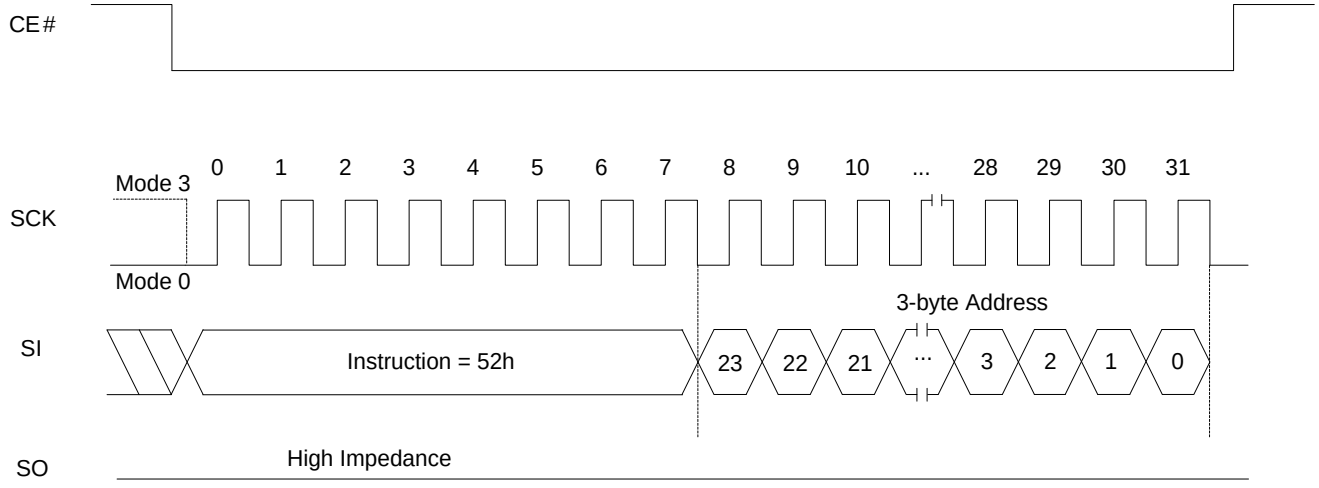


Figure 8.12 Block Erase (32K) Sequence

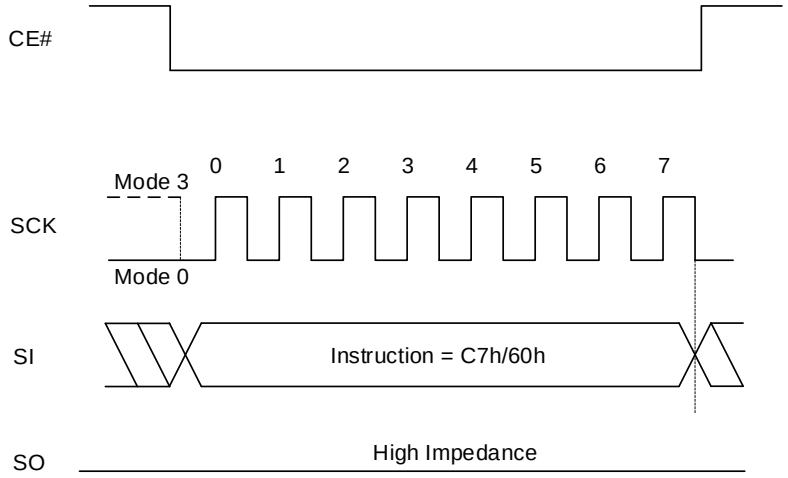


8.13 CHIP ERASE OPERATION (CER, C7h/60h)

A Chip Erase (CER) instruction erases the entire memory array of a IS25LQ025/512/010/020/040B. Before the execution of CER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after completion of a chip erase operation.

The CER instruction code is input via the SI. Erase operation will start immediately after CE# is pulled high, otherwise the CER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing.

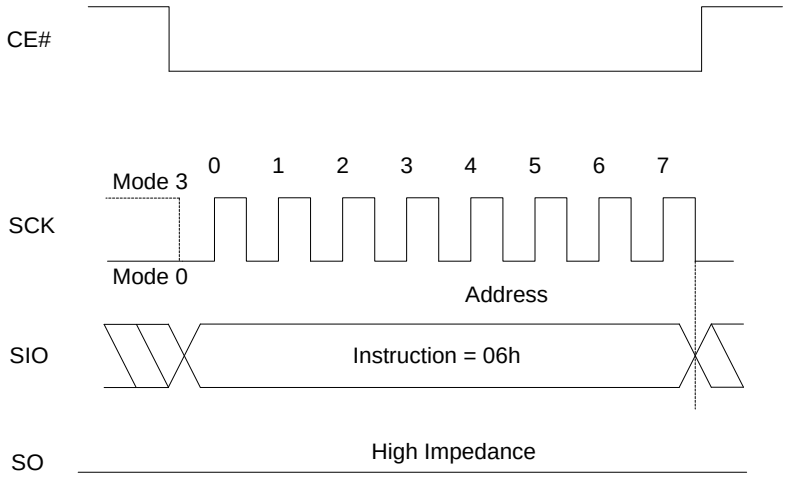
Figure 8.13 Chip Erase Sequence



8.14 WRITE ENABLE OPERATION (WREN, 06h)

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit is reset to the write-protected state after power-up. The WEL bit must be write enabled before any write operation, including Sector Erase, Block Erase, Chip Erase, Page Program, Write Status Register, and Write Function Register operations. The WEL bit will be reset to the write-protected state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

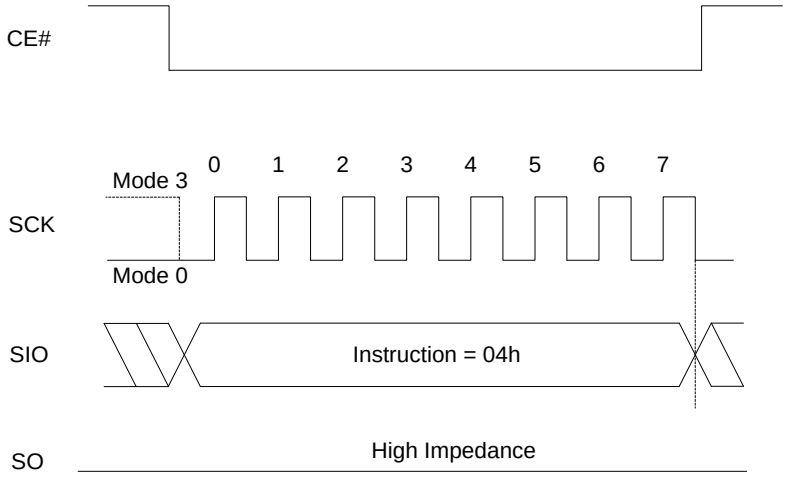
Figure 8.14 Write Enable Sequence



8.15 WRITE DISABLE OPERATION (WRDI, 04h)

The Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction, since the WEL bit is automatically reset.

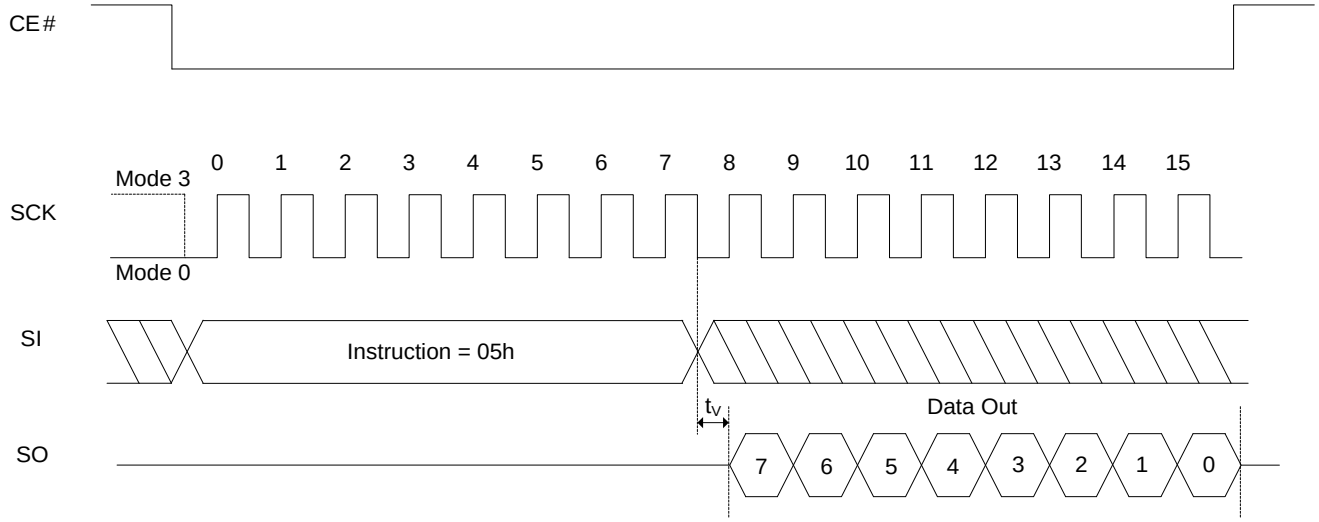
Figure 8.15 Write Disable Sequence



8.16 READ STATUS REGISTER OPERATION (RDSR, 05h)

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write Status Register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of Status Register.

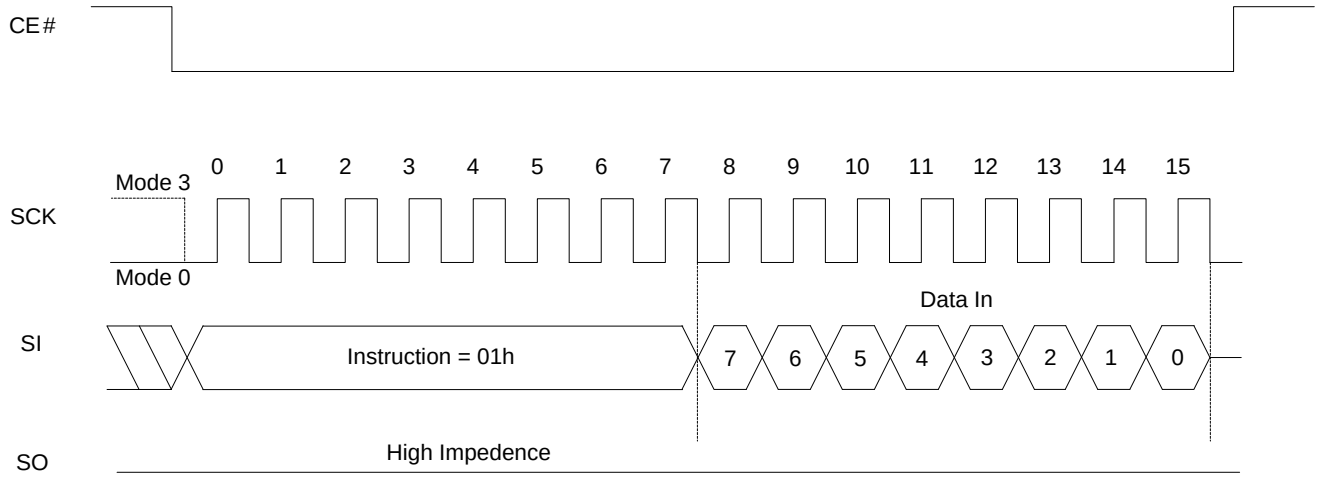
Figure 8.16 Read Status Register Sequence



8.17 WRITE STATUS REGISTER OPERATION (WRSR, 01h)

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and Status Register write protection features by writing “0”s or “1”s into the non-volatile BP3, BP2, BP1, BP0, QE and SRWD bits.

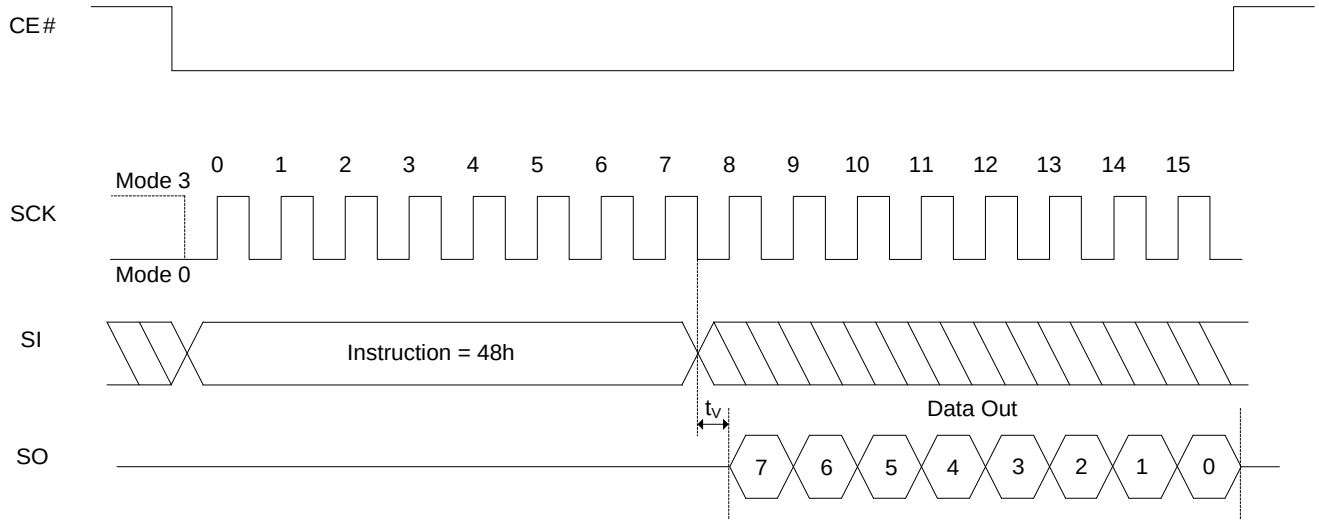
Figure 8.17 Write Status Register Sequence



8.18 READ FUNCTION REGISTER OPERATION (RDFR, 48h)

The Read Function Register (RDFR) instruction provides access to the Erase/Program suspend register. During the execution of a program, erase or write Status Register suspend, which can be used to check the suspend status.

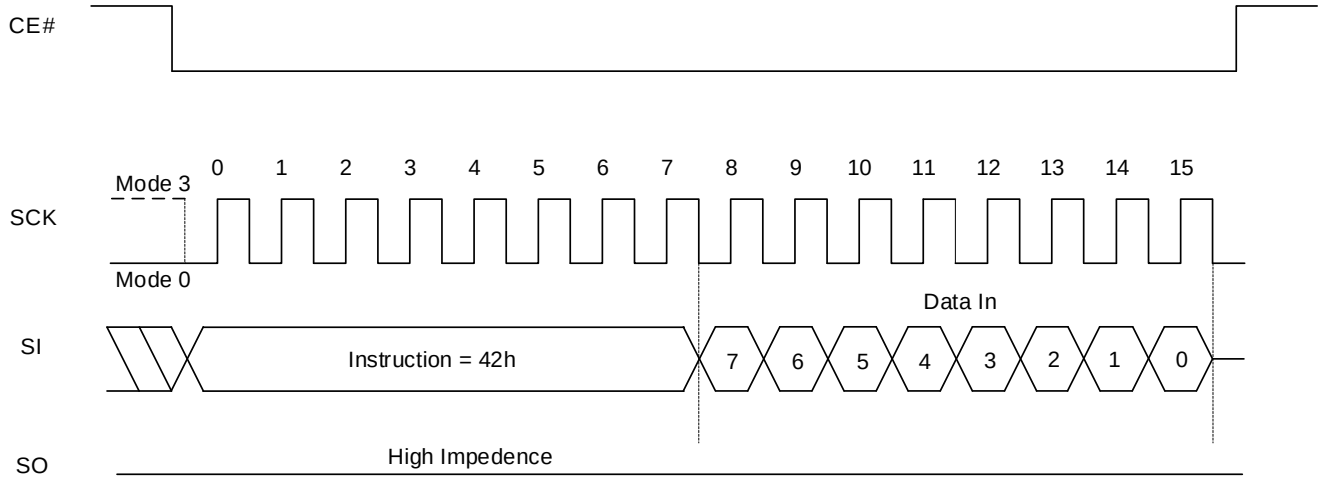
Figure 8.18 Read Function Register Sequence



8.19 WRITE FUNCTION REGISTER OPERATION (WRFR, 42h)

The Write Function Register (WRFR) instruction allows the user to lock the information row by bit 0. (IR lock)

Figure 8.19 Write Function Register Sequence



8.20 PROGRAM/ERASE SUSPEND & RESUME

The device allows the interruption of Sector-Erase, Block-Erase or Page-Program operations to conduct other operations. 75h/B0h command for suspend and 7Ah/30h for resume will be used. Function Register bit2 (PSUS) and bit3 (ESUS) are used to check whether or not the device is in suspend mode.

Suspend to read ready timing: 100µs.
Resume to another suspend timing: 400µs (recommendation).

PROGRAM/ERASE SUSPEND DURING SECTOR-ERASE OR BLOCK-Erase (PERSUS 75h/B0h)
The Program/Erase Suspend allows the interruption of Sector Erase and Block Erase operations. After the Program/Erase Suspend, WEL bit will be disabled, therefore only read related, resume and reset commands can be accepted (Refer to Table 8.3 for more detail).

To execute the Program/Erase Suspend operation, the host drives CE# low, sends the Program/Erase Suspend command cycle (75h/B0h), then drives CE# high. The Function Register indicates that the erase has been suspended by changing the ESUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit in the Status Register or wait the specified time t_{SUS}. When ESUS bit is issued, the Write Enable Latch (WEL) bit will be reset.

PROGRAM/ERASE SUSPEND DURING PAGE PROGRAMMING (PERSUS 75h/B0h)
The Program/Erase Suspend allows the interruption of all program operations. After the Program/Erase Suspend command, WEL bit will be disabled, therefore only read related, resume and reset commands can be accepted (Refer to Table 8.3 for more detail).

To execute the Program/Erase Suspend operation, the host drives CE# low, sends the Program/Erase Suspend command cycle (75h/B0h), then drives CE# high. The Function Register indicates that the programming has been suspended by changing the PSUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit in the Status Register or wait the specified time t_{SUS}.

PROGRAM/ERASE RESUME (PERRSM 7A/30h)
The Program/Erase Resume restarts a Program or Erase command that was suspended, and changes the suspend status bit in the Function Register (ESUS or PSUS bits) back to "0". To execute the Program/Erase Resume operation, the host drives CE# low, sends the Program/Erase Resume command cycle (7Ah/30h), then drives CE# high. A cycle is two nibbles long, most significant nibble first. To determine if the internal, self-timed Write operation completed, poll the WIP bit in the Status Register, or wait the specified time t_{SE}, t_{BE} or t_{PP} for Sector Erase, Block Erase, or Page Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times t_{SE}, t_{BE} or t_{PP}.

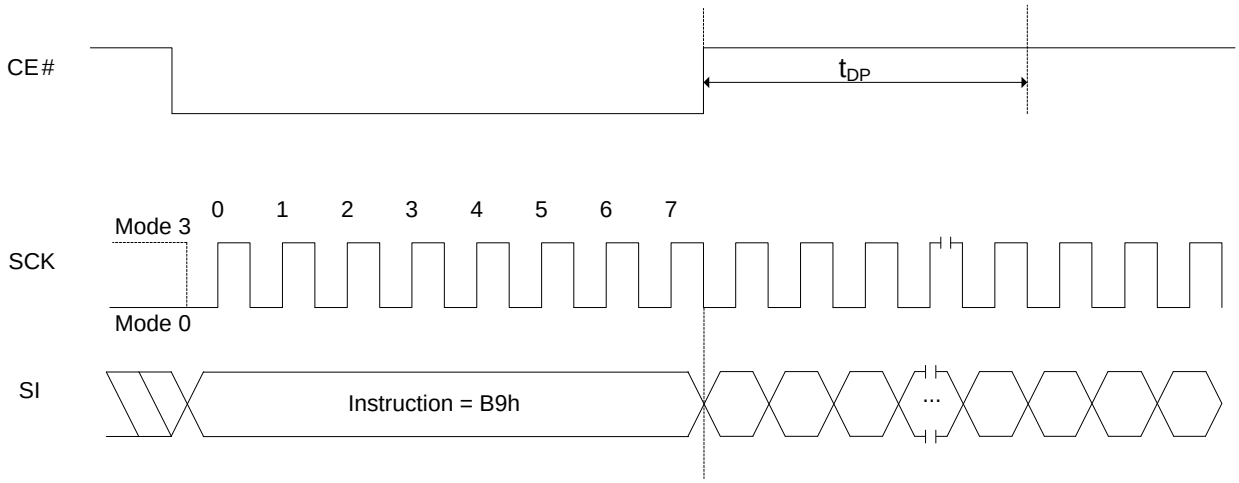
Table 8.3 Instructions accepted during Suspend

Operation Suspended	Instruction Allowed		
	Name	**Hex Code**	**Operation**
Program or Erase	RD	03h	Read Data Bytes from Memory at Normal Read Mode
Program or Erase	FR	0Bh	Read Data Bytes from Memory at Fast Read Mode
Program or Erase	FRDIO	BBh	Fast Read Dual I/O
Program or Erase	FRDO	3Bh	Fast Read Dual Output
Program or Erase	FRQIO	EBh	Fast Read Quad I/O
Program or Erase	FRQO	6Bh	Fast Read Quad Output
Program or Erase	RDSR	05h	Read Status Register
Program or Erase	RDFR	48h	Read Function Register
Program or Erase	PERRSM	7Ah/30h	Resume program/erase
Program or Erase	RDID	ABh	Read Manufacturer and Product ID
Program or Erase	RDUID	4Bh	Read Unique ID Number
Program or Erase	RDJDID	9Fh	Read Manufacturer and Product ID by JEDEC ID Command
Program or Erase	RDMDID	90h	Read Manufacturer and Device ID
Program or Erase	RDSFDP	5Ah	SFDP Read
Program or Erase	RSTEN	66h	Software reset enable
Program or Erase	RST	99h	Reset (Only along with 66h)
Program or Erase	IRRD	68h	Read Information Row

8.21 DEEP POWER DOWN (DP, B9h)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (enter into Power-Down mode), the standby current is reduced from I_{sb1} to I_{sb2}). During the Power-down mode, the device is not active and all Write/Program/Erase instructions are ignored. The instruction is initiated by driving the CE# pin low and shifting the instruction code "B9h" as show in the figure 8.20. The CE# pin must be driven high after the instruction has been latched. If this is not done the Power-Down will not be executed. After CE# pin driven high, the power-down state will be entered within the time duration of t_{DP}. While in the power-down state only the Release from Power-down / RDID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. It can support in SPI and Multi-IO mode.

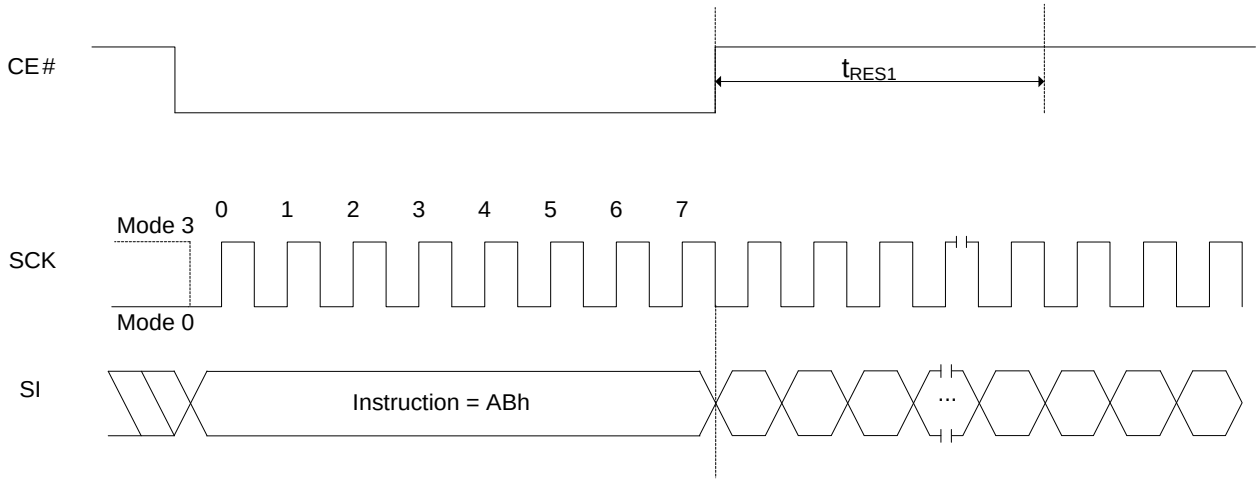
Figure 8.20 Enter Deep Power Down Mode Operation. (SPI)



8.22 RELEASE DEEP POWER DOWN (RDPD, ABh)

The Release from Power-down /read Device ID instruction is a multi-purpose instruction. To release the device from the power-down state Mode, the instruction is issued by driving the CE# pin low, shifting the instruction code “ABh” and driving CE# high as shown in Figure 8.21.
Release from power-down will take the time duration of t_{RES1} before the device will resume normal operation and other instructions are accepted. The CE# pin must remain high during the t_{RES1} time duration. If the Release from Power-down / RDID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.21 Release Power Down Sequence (SPI)



8.23 READ PRODUCT IDENTIFICATION (RDID, ABh)

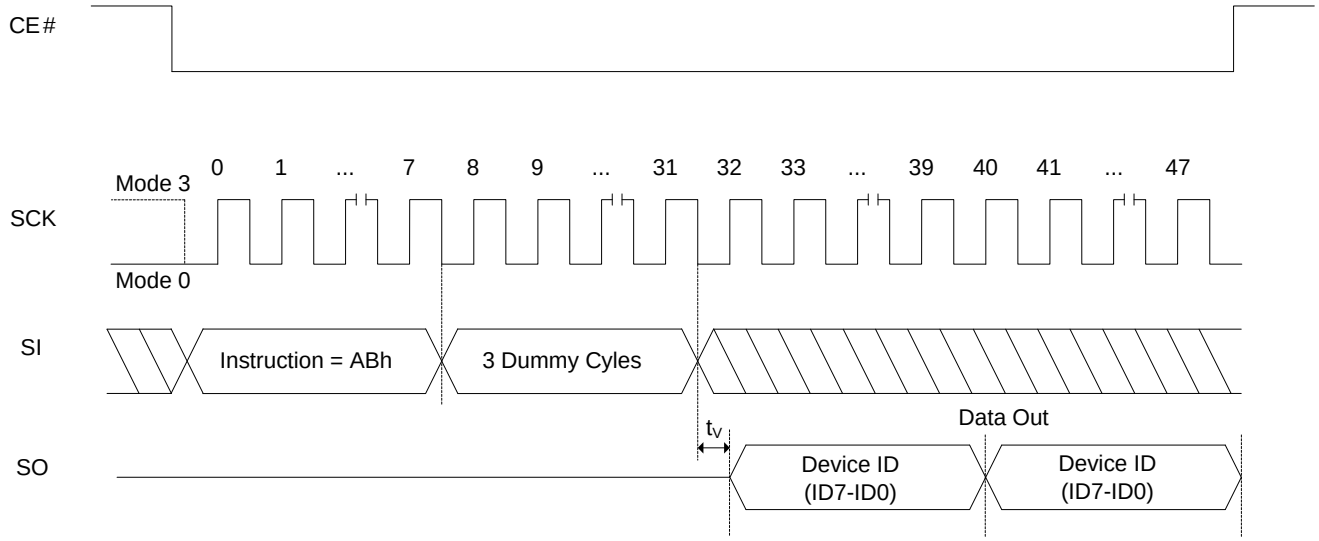
The Release from Power-down /read Device ID instruction is a multi-purpose instruction. It can support both SPI and Multi-IO mode. The Read Product Identification (RDID) instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions.

The RDID instruction code is followed by three dummy bytes, each bit being latched-in on SI during the rising SCK edge. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDID instruction is ended by CE# going high. The Device ID for ABh outputs repeatedly if additional clock cycles are continuously sent on SCK while CE# is at low.

Table 8.4 Product Identification

Manufacturer ID		**(MF7-MF0)**	
ISSI Serial Flash		9Dh	
Instruction	**ABh**	**90h**	**9Fh**
Device Density	Device ID (ID7-ID0)		Device Type + Capacity (ID15-ID0)
4Mb	12h		4013h
2Mb	11h		4012h
1Mb	10h		4011h
512K	05h		4010h
256K	02h		4009h

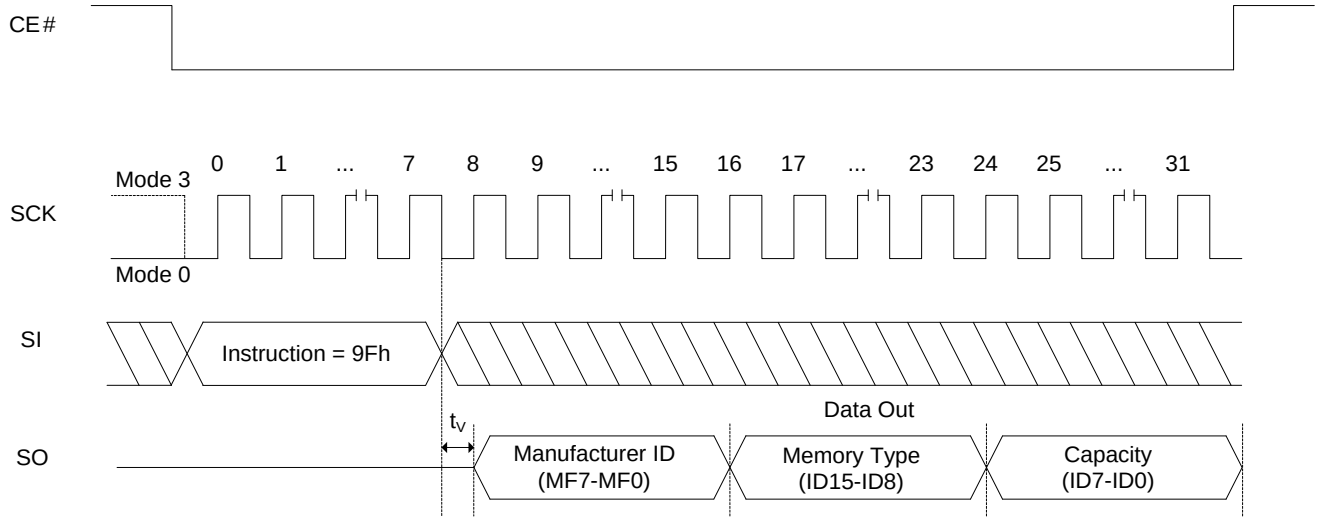
Figure 8.22 Read Product Identification Sequence



8.24 READ PRODUCT IDENTIFICATION BY JEDEC ID OPERATION (RDJDID, 9Fh)

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of devices. Refer to Table 8.4 Product Identification for Manufacturer ID and Device ID. After the JEDEC ID READ command (9Fh) is input, the Manufacturer ID is shifted out on SO with the MSB first, followed by the Device Type and Density ID15-ID0 (9Fh Device ID); each bit is shifted out during the falling edge of SCK. If CE# stays low after the last bit of the Device ID is shifted out, the Manufacturer ID and Device (Type/Capacity) IDs will loop until CE# is pulled high.

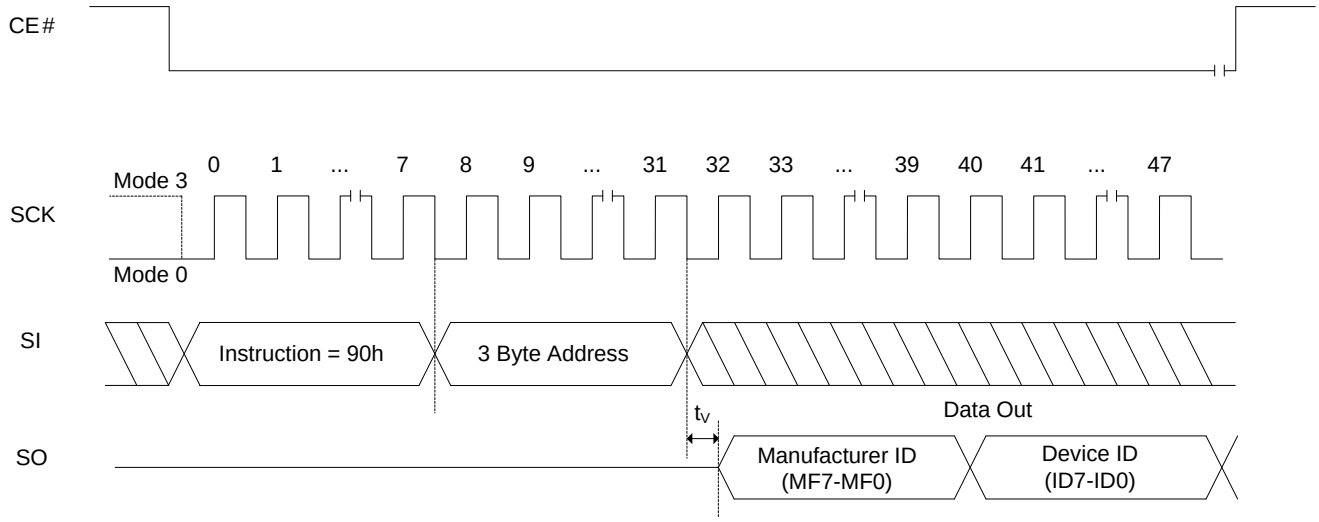
Figure 8.23 Read Product Identification by JEDEC ID Read Sequence



8.25 READ DEVICE MANUFACTURER AND DEVICE ID OPERATION (RDMDID, 90h)

The Read Product Identification (RDID) instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 8.4 Product Identification for manufacturer ID and device ID. The RDID instruction code is followed by two dummy bytes and one byte address (A7~A0), each bit being latched-in on SI during the rising edge of SCK. If one byte address is initially set to A0 = 0, then the manufacturer ID is shifted out on SO with the MSB first, then the Device ID for 90h, with each bit being shifted out during the falling edge of SCK. If one byte address is initially set to A0 = 1, then device ID1 will be read first, followed Manufacturer ID. The manufacturer and device ID can be read continuously alternating between the two until CE# is driven high.

Figure 8.24 Read Product Identification by RDMDID Read Sequence



Notes:

1. **ADDRESS A0 = 0, will output the 1-byte Manufacture ID (MF7-MF0) → 1-byte device (ID7-ID0)**
   ADDRESS A0 = 1, will output the 1-byte device (ID7-ID0) → 1-byte Manufacture ID (MF7-MF0)
2. **The Manufacture and Device ID can be read continuously and will alternate from one to the other until CE# pin is pulled high.**

8.26 READ UNIQUE ID NUMBER (RDUID, 4Bh)

The Read Unique ID Number (RDUID) instruction accesses a factory-set read-only 16-byte number that is unique to the device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The RDUID instruction is instated by driving the CE# pin low and shifting the instruction code (4Bh) followed by 3 address bytes and a dummy byte. After which, the 16-byte ID is shifted out on the falling edge of SCK as shown below.

Note: 16-byte of data will repeat as long as CE# is low and SCK is toggling.

Figure 8.25 Read Product Identification Sequence

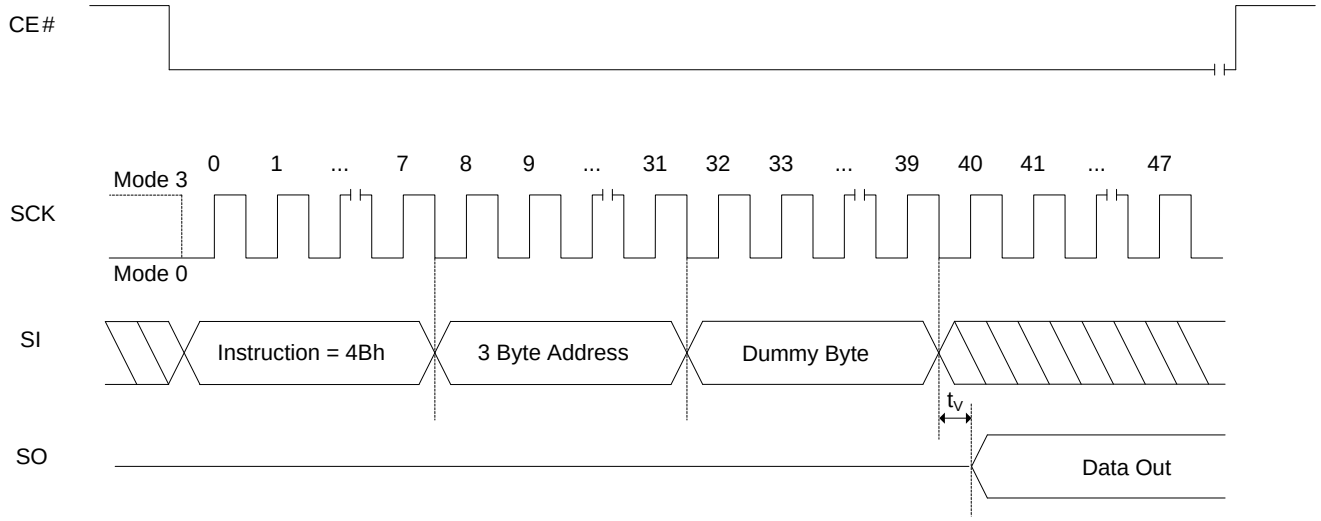


Table 8.5 Unique ID Addressing

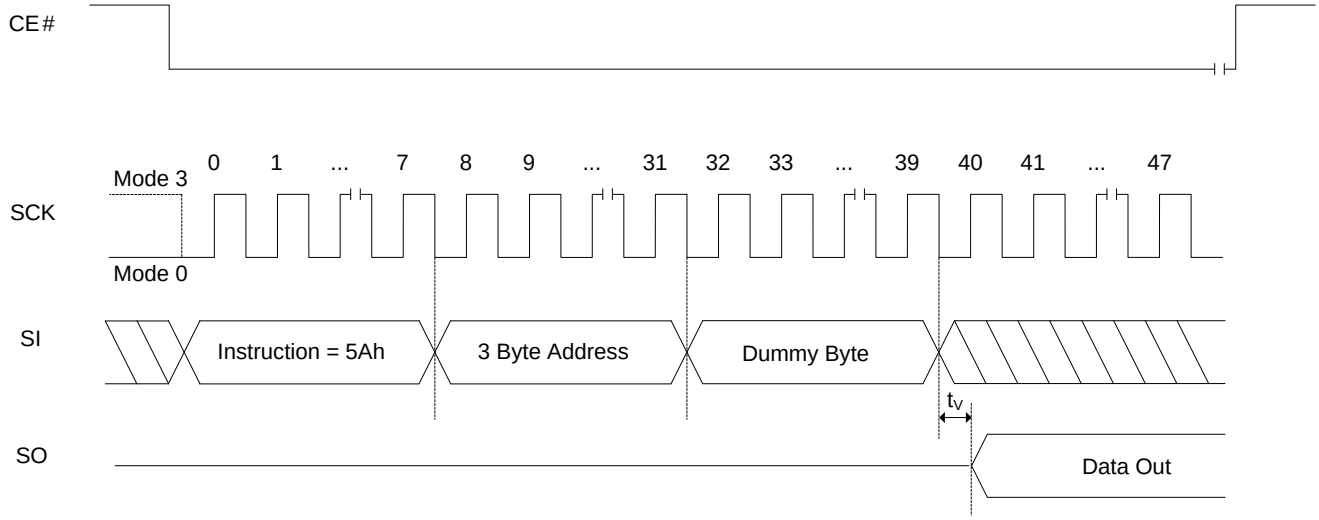
A[23:16]	A[15:9]	A[8:4]	A[3:0]
XXh	XXh	00h	0h Byte address
XXh	XXh	00h	1h Byte address
XXh	XXh	00h	2h Byte address
XXh	XXh	00h	⋮
XXh	XXh	00h	Fh Byte address

8.27 READ SFDP OPERATION (RDSFDP, 5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial Flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. For more details please refer to the JEDEC Standard JESD216A (Serial Flash Discoverable Parameters).

The sequence of issuing RDSFDP instruction is same as Fast Read instruction: CE# goes low → send RDSFDP instruction (5Ah) → send 3 address bytes on SI pin → send 1 dummy byte on SI pin → read SFDP code on SO → to end RDSFDP operation can use CE# high at any time during data out. Refer to ISSI's Application note for SFDP table. The data at the addresses that are not specified in SFDP table are undefined.

Figure 8.26 RDSFDP COMMAND (Read SFDP) OPERATION



8.28 SOFTWARE RESET (RESET-ENABLE (RSTEN, 66h) AND RESET (RST, 99h)

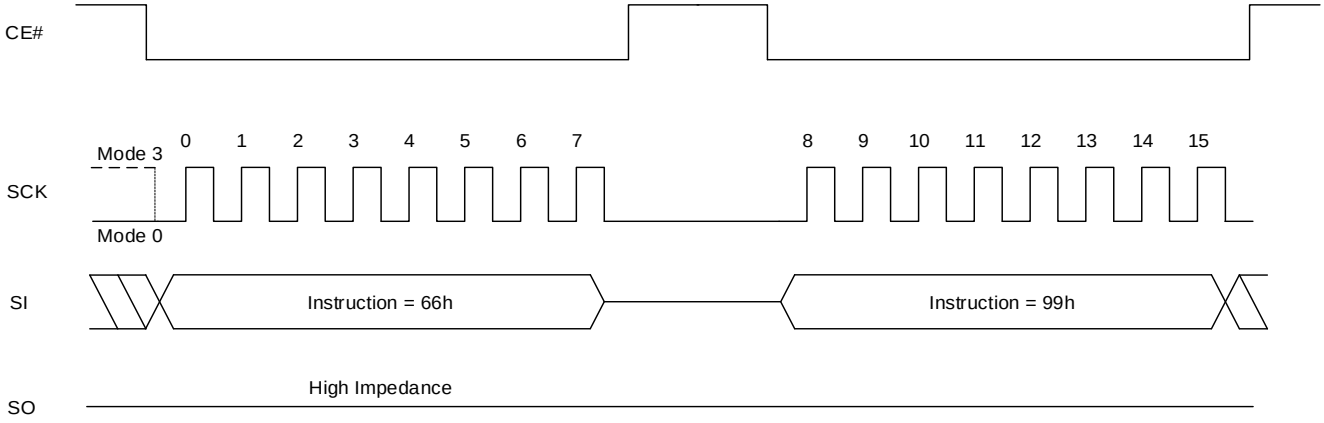
The Reset operation is used as a system (software) reset that puts the device in normal operating mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST). The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

Execute the CE# pin low → sends the Reset-Enable command (66h), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99h), and drives CE# high.

The Software Reset during an active Program or Erase operation aborts the operation, which can result in corrupting or losing the data of the targeted address range. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

Note: The Status and Function Registers remain unaffected.

Figure 8.27 SOFTWARE RESET ENABLE, SOFTWARE RESET OPERATIONS (RSTEN, 66h + RST, 99h)



8.29 SECURITY INFORMATION ROW (OTP AREA)

The security information row is comprised of an additional 4 x 256 bytes of programmable information. The security bits can be reprogrammed by the user. Any program security instruction issued while program cycle is in progress is rejected without having any effect on the cycle that is in progress.

Table 8.6 Information Row Address

Address Assignment	A[23:16]	A[15:8]	A[7:0]
IRL0(Information row lock0)	00h	00h	Byte address
IRL1	00h	10h	Byte address
IRL2	00h	20h	Byte address
IRL3	00h	30h	Byte address

Bit 7~4 of the Function Register is used to permanently lock the programmable memory array.
-When Function Register bit IRLx = “0”, the 256 bytes of the programmable memory array can be programmed.
-When Function Register bit IRLx = “1”, the 256 bytes of the programmable memory array function as read only.

8.30 INFORMATION ROW PROGRAM OPERATION (IRP, 62h)

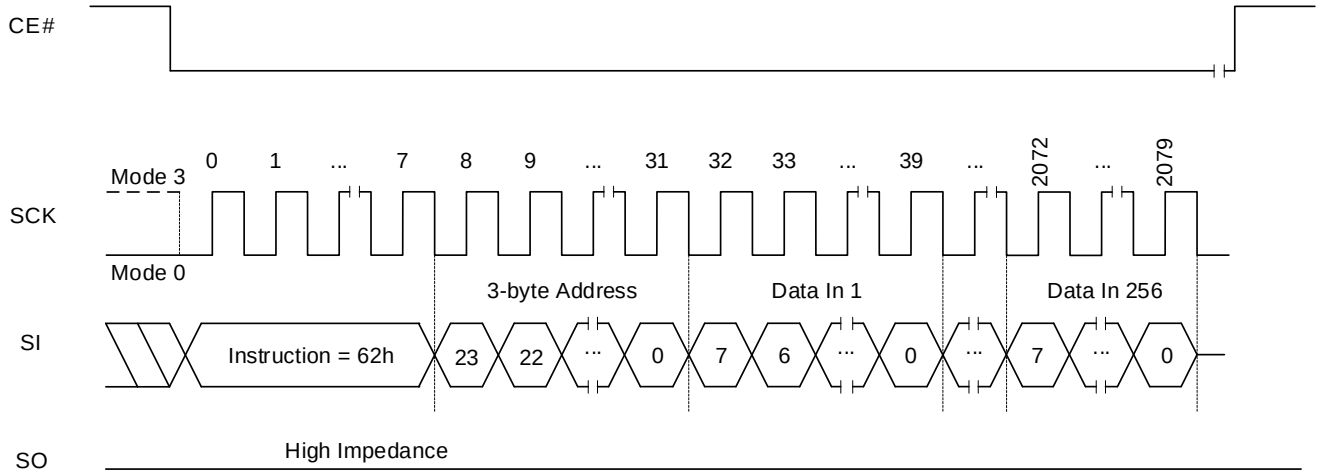
The Information Row Program (IRP) instruction allows up to 256 bytes data to be programmed into the memory in a single operation. Before the execution of IRP instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The IRP instruction code, three address bytes and program data (1 to 256 bytes) should be sequentially input via the SI line. Three address bytes has to be input as specified in the Table 8.6 Information Row Address. Program operation will start once the CE# goes high, otherwise the IRP instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page. The previously latched data are discarded and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: Information Row is only One Time Programmable (OTP). Once an information row is programmed, the data cannot be altered.

Figure 8.28 IRP COMMAND (Information Row Program) OPERATION



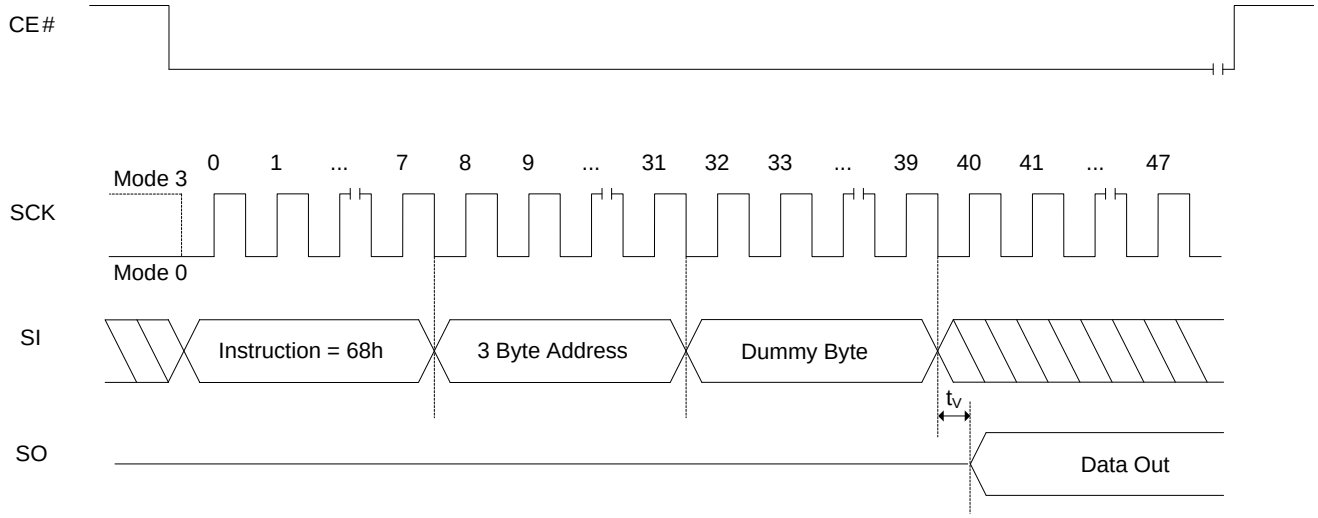
8.31 INFORMATION ROW READ OPERATION (IRRD, 68h)

The IRRD instruction is used to read memory data at up to a 104MHZ clock.

The IRRD instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single IRRD instruction. The IRRD instruction is terminated by driving CE# high (VIH). If a IRRD instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 8.29 IRRD COMMAND (Information Row Read) OPERATION



9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.5V to V_{CC} + 0.5V
All Output Voltage with Respect to Ground		-0.5V to V_{CC} + 0.5V
V_{CC}		-0.5V to +6.0V

Note:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

9.2 OPERATING RANGE

Part Number	IS25LQ025/512/010/020/040B
Operating Temperature (Extended Grade E)	-40°C to 105°C
Operating Temperature (V Grade: Hybrid Flow)	-40°C to 125°C
Operating Temperature (Automotive Grade A1)	-40°C to 85°C
Operating Temperature (Automotive Grade A2)	-40°C to 105°C
Operating Temperature (Automotive Grade A3)	-40°C to 125°C
V_{CC} Power Supply	2.3 V (VMIN) – 3.6 V (VMAX); 3.3 V (Typ)

9.3 DC CHARACTERISTICS

(Under operating range)

Symbol	Parameter	Condition		Min	Typ(2)	Max	Units
I_{CC1}	V_{CC} Active Read Current	V_{CC} = VMAX at 33MHz, SO = Open			10	15	mA
I_{CC2}	V_{CC} Program/Erase Current	V_{CC} = VMAX at 33MHz, SO = Open			15	30	mA
I_{SB1}	V_{CC} Standby Current CMOS	V_{CC} = VMAX, CE# = V_{CC}			8	50	µA
I_{SB2}	Deep power down current	V_{CC} = VMAX, CE# = V_{CC}			1	5	µA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
V_{IL} (1)	Input Low Voltage			-0.5		$0.3V_{CC}$	V
V_{IH} (1)	Input High Voltage			$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	VMIN < V_{CC} < VMAX	I_{OL} = 100 µA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Notes:

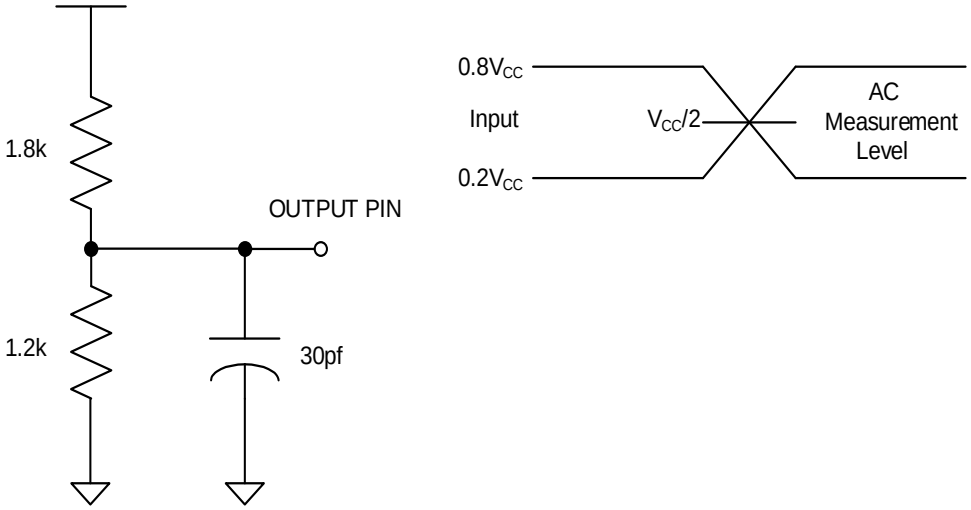
1. **Maximum DC voltage on input or I/O pins is Vcc + 0.5V. During voltage transitions, input or I/O pins may overshoot Vcc by + 2.0 V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0 V for a period of time not to exceed 20ns.**

2. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ), TA=25°C**

9.4 AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Load Capacitance		30	pF
TR,TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
VREFI	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		V

Figure9.1 Output test load & AC measurement I/O Waveform



9.5 AC CHARACTERISTICS

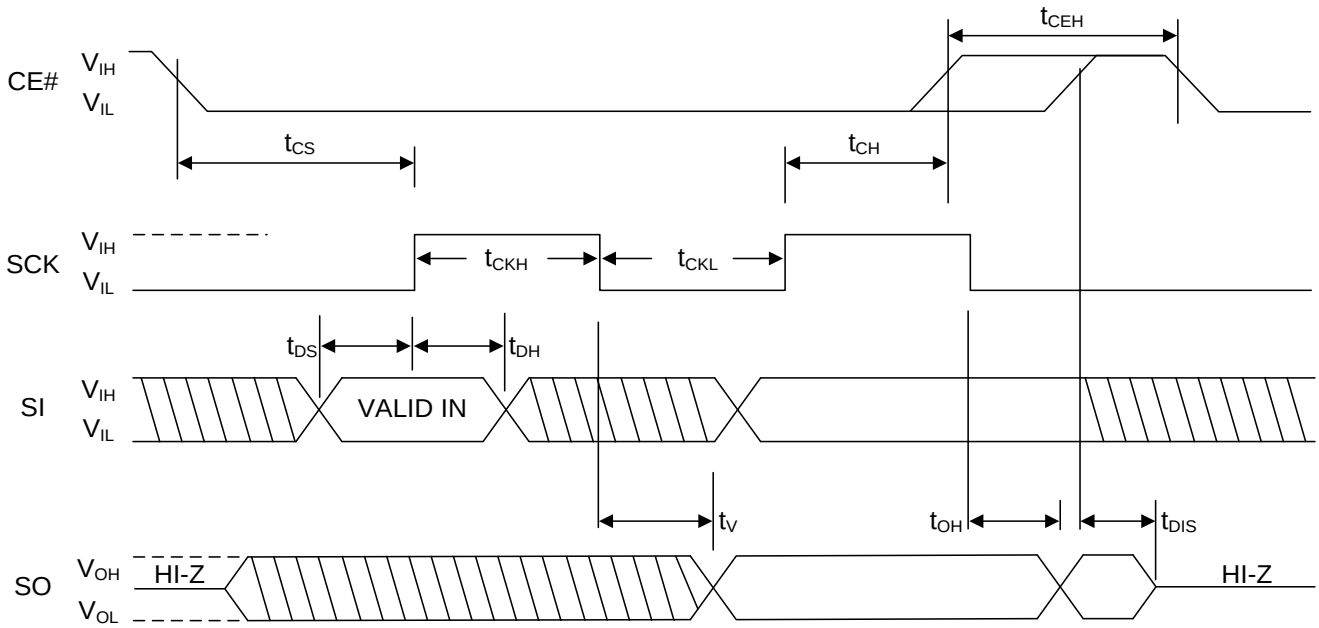
(Under operating range, refer to section 9.4 for AC measurement conditions)

Symbol	Parameter		Min	Typ	Max	Units
f_{CT}	Clock Frequency for fast read mode		0		104	MHz
f_C	Clock Frequency for read mode		0		33	MHz
t_{RI}	Input Rise Time				8	ns
t_{FI}	Input Fall Time				8	ns
t_{CKH}	SCK High Time		4			ns
t_{CKL}	SCK Low Time		4			ns
t_{CEH}	CE# High Time		7			ns
t_{CS}	CE# Setup Time		10			ns
t_{CH}	CE# Hold Time		5			ns
t_{DS}	Data In Setup Time		2			ns
t_{DH}	Data in Hold Time		2			ns
t_{HS}	Hold Setup Time		15			ns
t_{HD}	Hold Time		15			ns
t_V	Output Valid				8	ns
t_{OH}	Output Hold Time Normal Mode		2			ns
t_{DIS}	Output Disable Time				8	ns
t_{HD}	Output Hold Time		2			ns
t_{HLCH}	HOLD Active Setup Time relative to SCK		5			ns
t_{CHHH}	HOLD Active Hold Time relative to SCK		5			ns
t_{HHCH}	HOLD Not Active Setup Time relative to SCK		5			ns
t_{CHHL}	HOLD Not Active Hold Time relative to SCK		5			ns
t_{LZ}	HOLD to Output Low Z				12	ns
t_{HZ}	HOLD to Output High Z				12	ns
t_{EC}	Sector Erase Time (4Kbyte)			70	300	ms
	Block Erase Time (32Kbyte)			130	500	ms
	Block Erase time (64Kbyte)(1)			200	1000	ms
	Chip Erase Time	256Kb		0.10	0.5	s
		512Kb		0.25	1	
		1Mb		0.4	1.5	
		2Mb		0.75	2	
		4Mb		1.5	3	
t_{PP}	Page Program Time	Extended and Hybrid (E and V)		0.5	1	ms
		Automotive grades (A1, A2, A3)		0.5	2	
t_{VCE}	Vcc(min) to CE# Low		1			ms
t_{res1}	Release deep power down				3	µs
t_{DP}	Deep power down				3	µs
t_W	Write Status Register time			2	10	ms
t_{SUS}	Suspend to read ready				100	µs
t_{SRST}	Software Reset cover time				100	µs

Note1: 64Kbyte Block Erase time is not applicable to IS25LQ025B and IS25LQ512B.

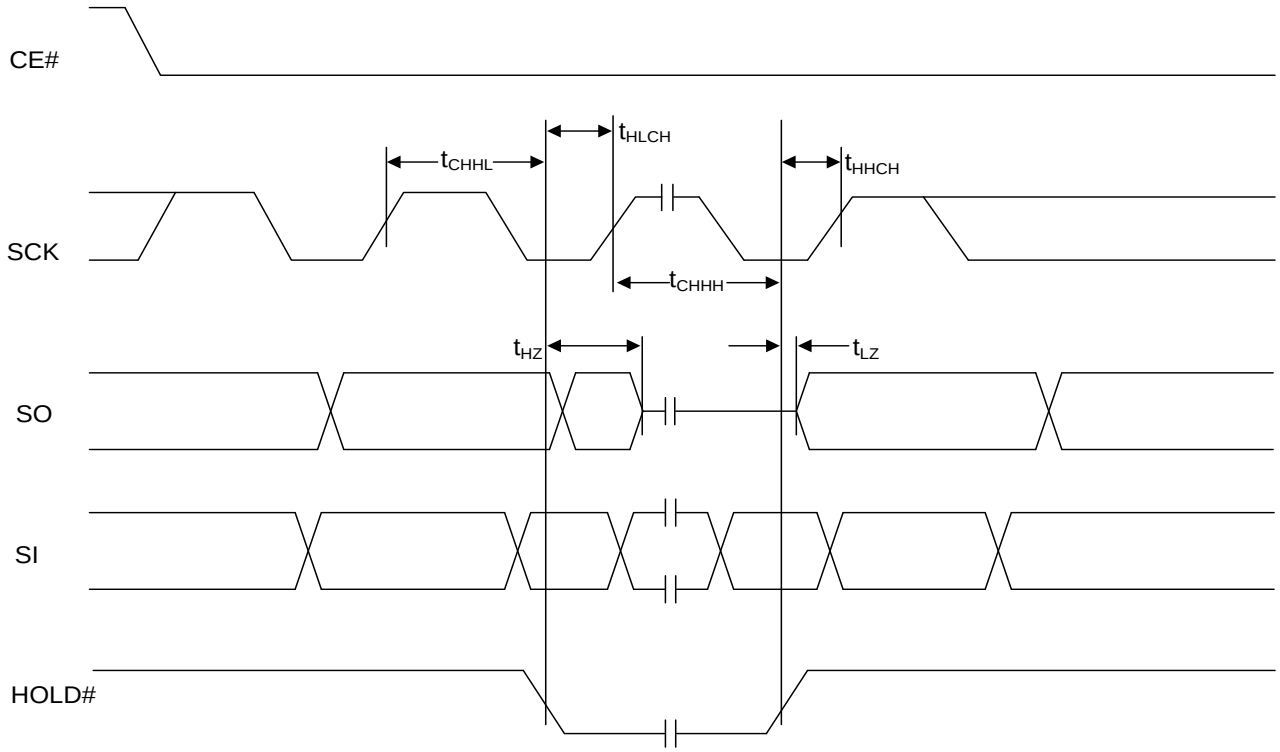
9.6 SERIAL INPUT/OUTPUT TIMING

Figure 9.2 SERIAL INPUT/OUTPUT TIMING (1)



Note1: For SPI Mode 0 (0,0)

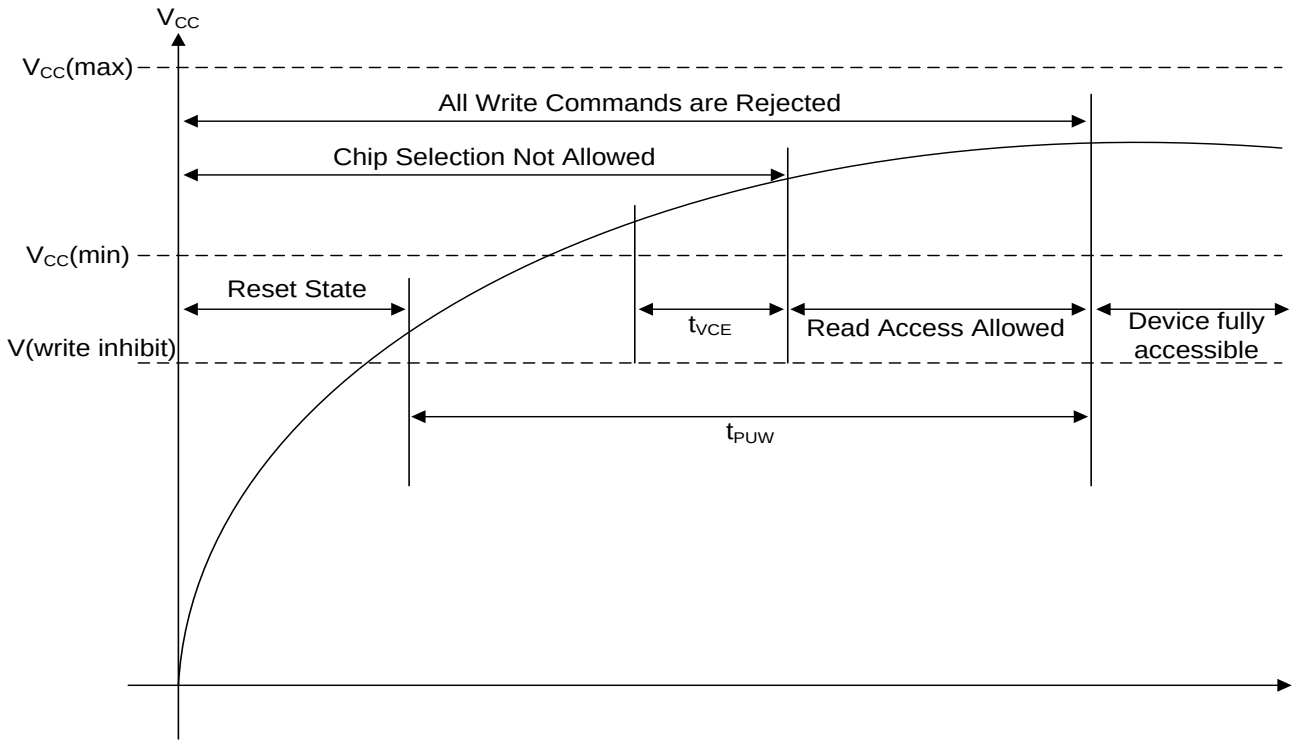
Figure 9.3 HOLD TIMING



9.7 POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level. (Adding a simple pull-up resistor on CE# is recommended.)

Power up timing



Symbol	Parameter	Min.	Max	Unit
tVCE(1)	Vcc(min) to CE# Low	1		ms
tPUW(1)	Power-up time delay to write instruction	1	10	ms
V_{WI}(1)	Write Inhibit Voltage		1.9	V

Note1: These parameters are characterized and are not 100% tested.

9.8 PROGRAM/ERASE PERFORMANCE

Parameter		Typ	Max	Unit	Remarks
Sector Erase Time (4KB)		70	300	ms	From writing erase command to erase completion
Block Erase Time (32KB)		130	500	ms	
Block Erase Time (64KB)		200	1000	ms	
Chip Erase Time	256Kb	0.10	0.5	s	
	512Kb	0.25	1		
	1Mb	0.4	1.5		
	2Mb	0.75	2		
	4Mb	1.5	3		
Page Programming Time	Extended and Hybrid (E and V)	0.5	1	ms	From writing program command to program completion
	Automotive grades (A1, A2, A3)	0.5	2		
Byte Program		8	25	µs	

Note: These parameters are characterized and are not 100% tested.

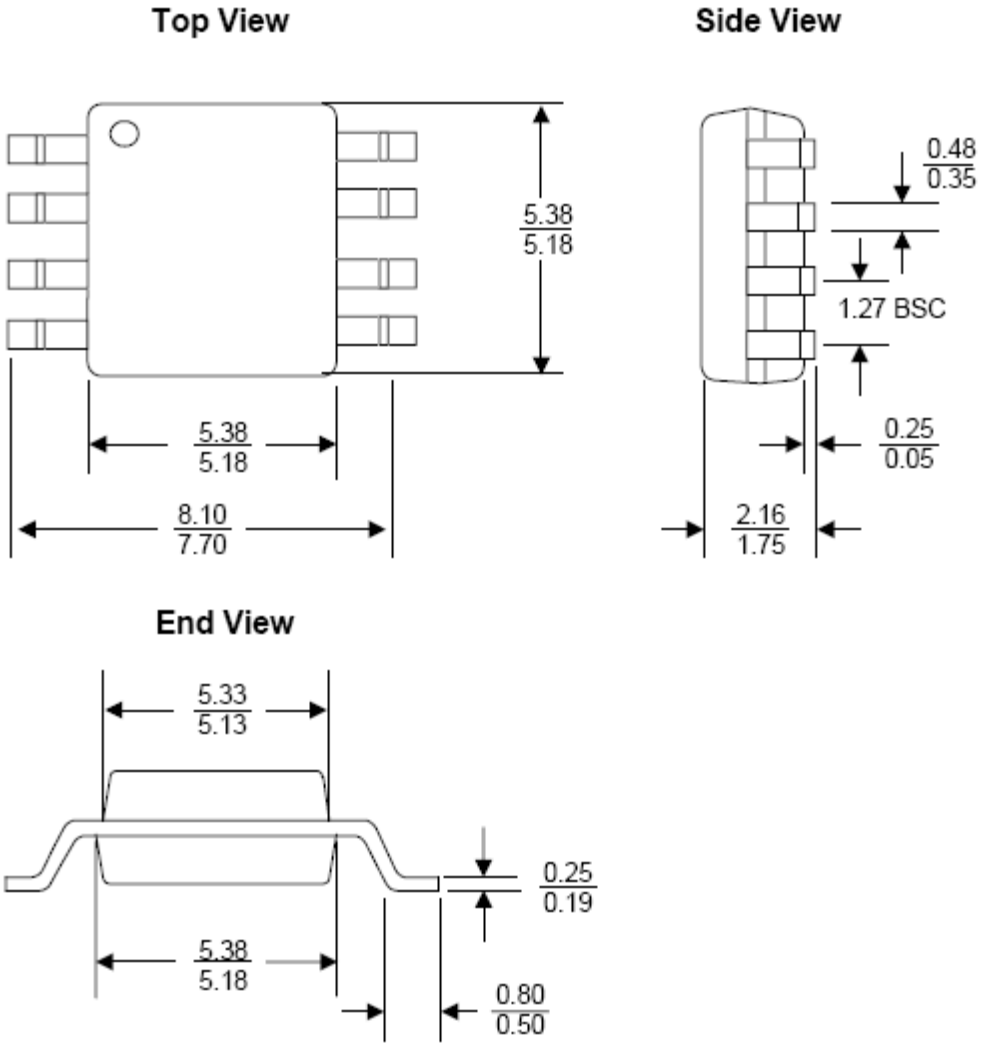
9.9 RELIABILITY CHARACTERISTICS

Parameter	Min	Unit	Test Method
Endurance	100,000	Cycles	JEDEC Standard A117
Data Retention	20	Years	JEDEC Standard A103
ESD – Human Body Model	2,000	Volts	JEDEC Standard A114
ESD – Machine Model	200	Volts	JEDEC Standard A115
Latch-Up	100 + ICC1	mA	JEDEC Standard 78

Note: These parameters are characterized and are not 100% tested.

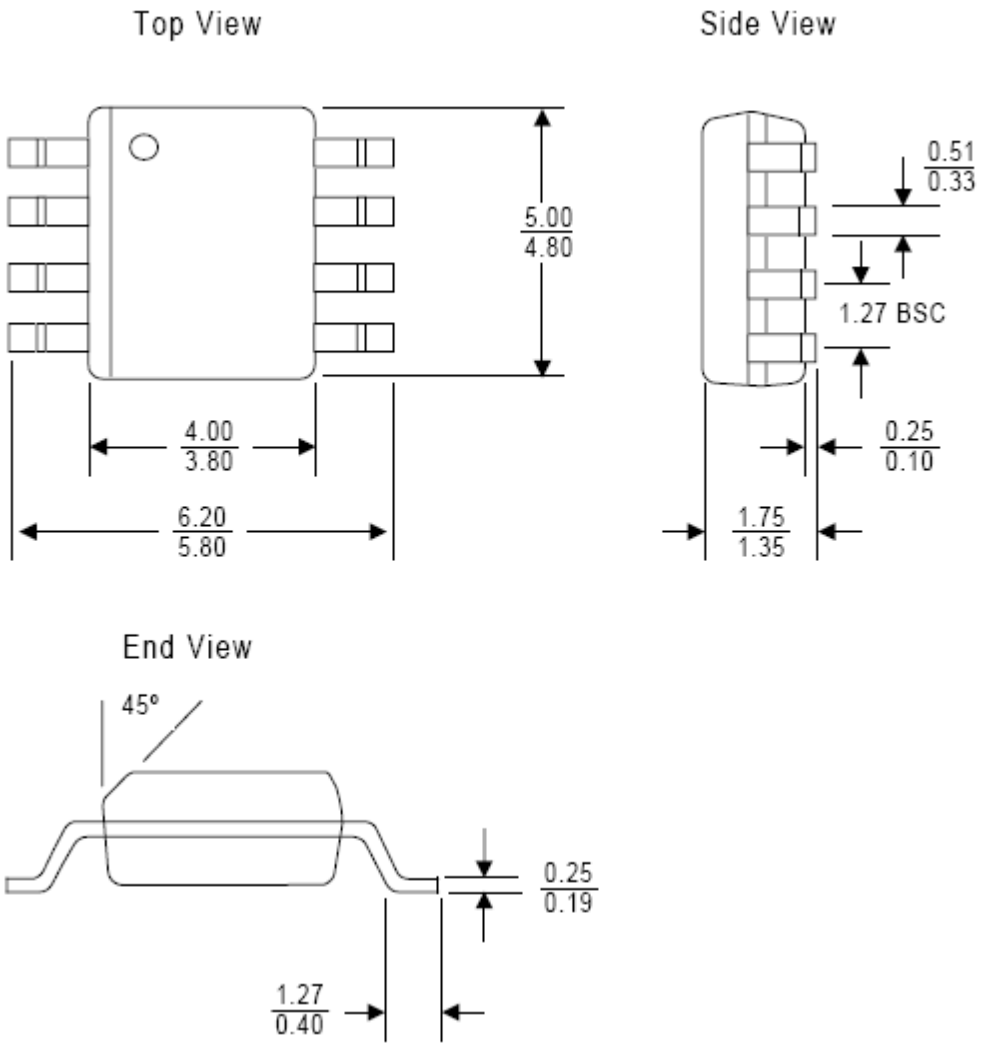
10. PACKAGE TYPE INFORMATION

10.1 8-PIN JEDEC 208MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (JB)



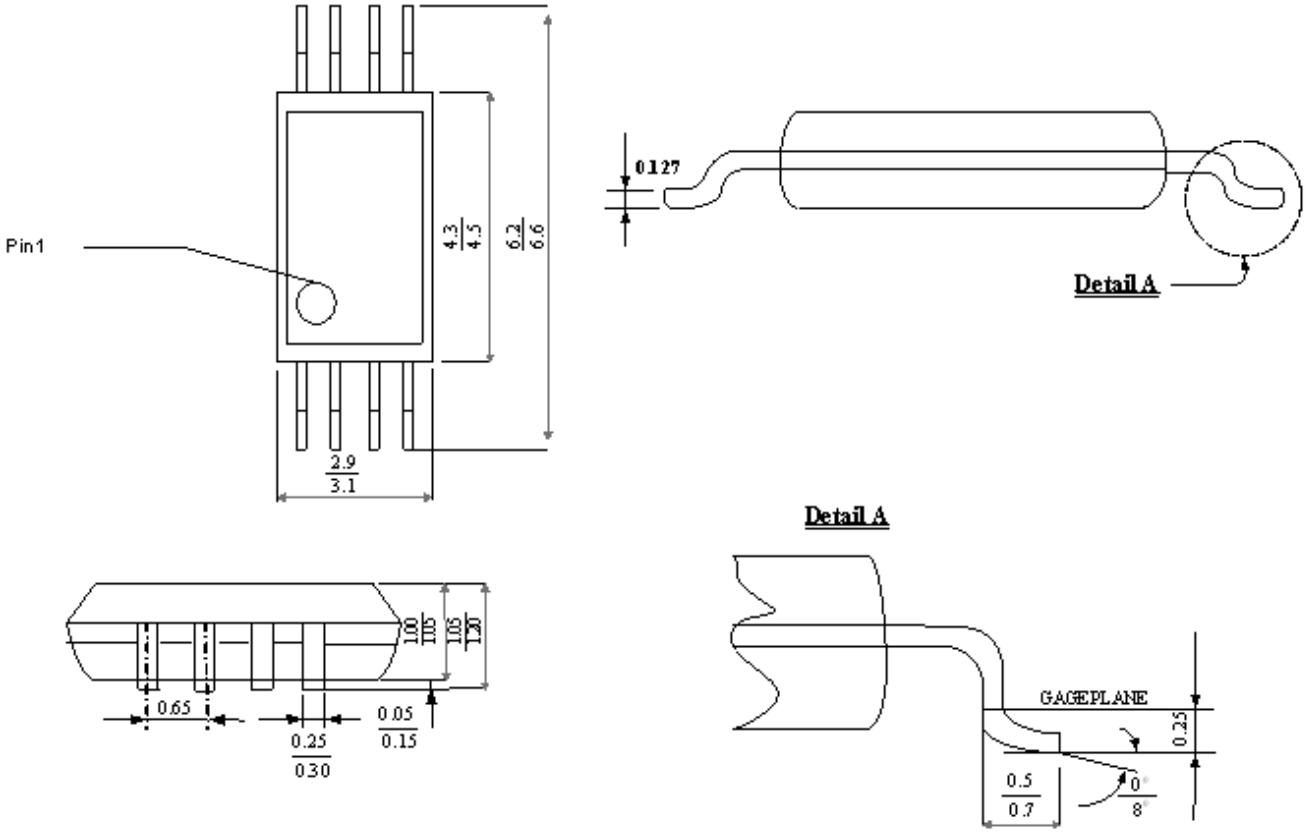
Note: All dimensions are in millimeters.

10.2 8-PIN JEDEC 150MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (JN)



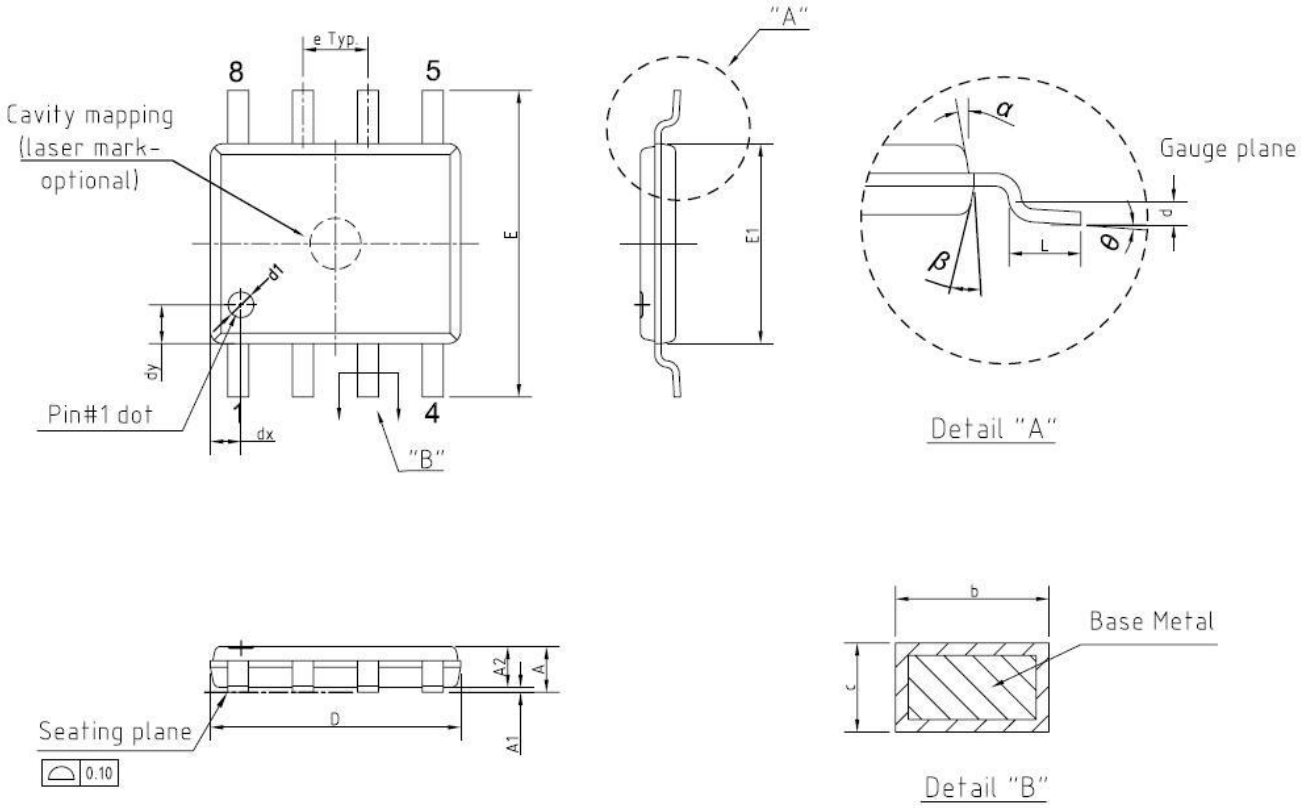
Note: All dimensions are in millimeters.

10.3 8-PIN 150MIL TSSOP PACKAGE (JD)



Note: All dimensions are in millimeters.

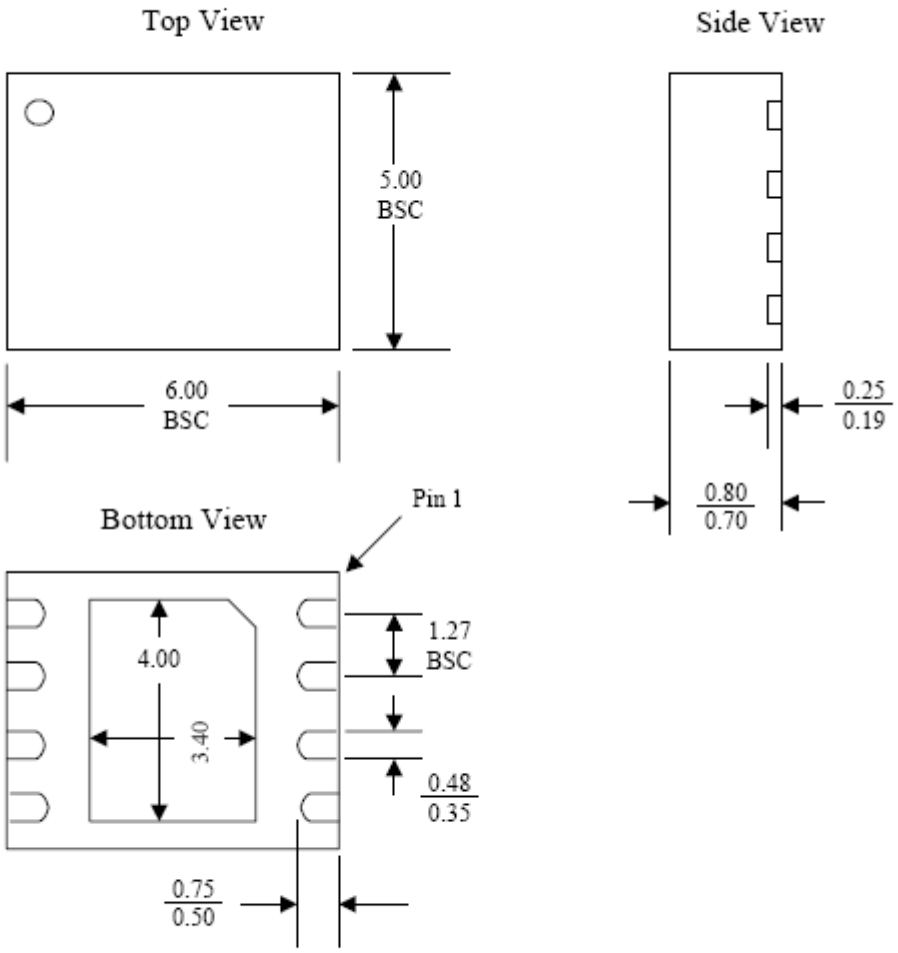
10.4 8-PIN 150MIL VVSOP PACKAGE (JV)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.88	---	---	34.6
A1	0.05	---	0.14	2.0	---	5.5
A2	0.63	---	0.74	24.8	---	29.1
b	0.33	0.41	0.51	13.0	16.1	20.1
c	0.13	---	0.18	5.1	---	7.1
D	4.80	4.90	5.00	189.0	192.9	196.9
d	---	0.25	---	---	10.0	---
d1	---	0.50typ	---	---	19.7typ	---
dx	---	0.60typ	---	---	23.6typ	---
dy	---	0.76typ	---	---	29.9typ	---
E	5.80	6.00	6.20	228.3	236.2	244.1
E1	3.80	3.90	4.00	149.6	153.5	157.5
e	---	1.27	---	---	50.0	---
L	0.41	0.71	1.27	16.1	28.0	50.0
α	---	10°	---	---	10°	---
β	---	10°	---	---	10°	---
θ	0°	---	10°	0°	---	10°

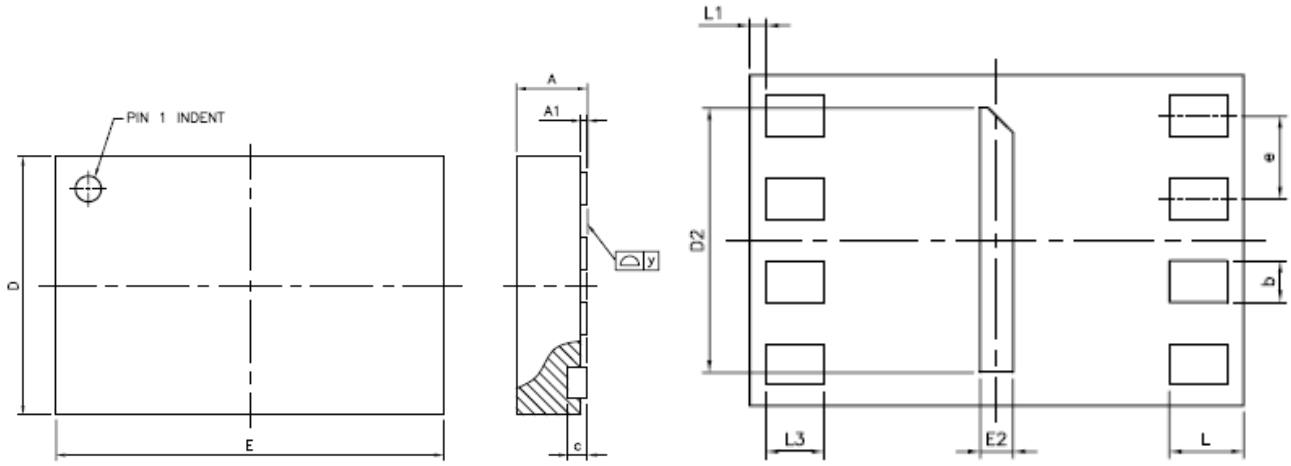
NOTES:
1. MOLD BODY DIMENSION DOES NOT INCLUDE END FLASH.
2. THE MOLDED END FLASH IS MAX. 0.15 mm.
3. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.

10.5 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 6X5MM (JK)



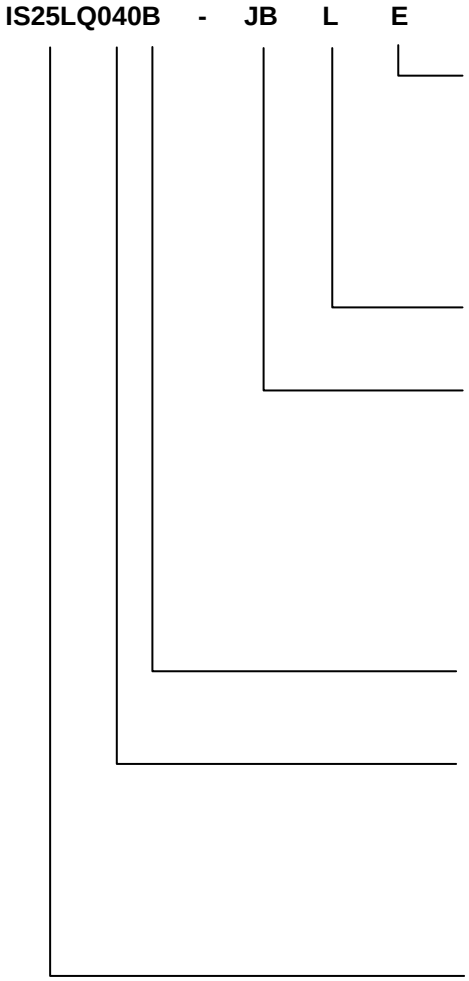
Note: All dimensions are in millimeters.

10.6 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (USON) PACKAGE 2X3MM (JU)



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	——	0.15 REF.	——
D	1.90	2.00	2.10
D2	1.55	1.60	1.65
E	2.90	3.00	3.10
E2	0.15	0.20	0.25
e	——	0.50	——
L	0.40	0.45	0.50
L1	——	0.10	——
L3	0.30	0.35	0.40
y	0.00	——	0.075

11. ORDERING INFORMATION



TEMPERATURE RANGE
E = Extended (-40°C to +105°C)
V = Hybrid Flow (-40°C to +125°C)
A1 = Automotive Grade (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)
A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE TYPE
JB = 8-pin SOIC 208mm
JN = 8-pin SOIC 150mm
JD = 8-pin TSSOP 150mil
JV = 8-pin VVSOP 150mil
JK = 8-contact WSON (6x5mm)
JU = 8-contact USON (2x3mm)
JW = KGD (Call Factory)

DIE REVISION
B = Revision B

DENSITY
040 = 4 Mbit
020 = 2 Mbit
010 = 1 Mbit
512 = 512 Kbit
025 = 256 Kbit

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
25LQ = FLASH, 2.3V ~ 3.6V, Quad SPI

Density	Frequency (MHz)	Order Part Number[1]		Package
4Mb	104	IS25LQ040B-JBLE	IS25LQ040B-JBLV	8-pin SOIC 208mil
		IS25LQ040B-JNLE	IS25LQ040B-JNLV	8-pin SOIC 150mil
		IS25LQ040B-JVLE	IS25LQ040B-JVLV	8-pin VVSOP 150mil
		IS25LQ040B-JKLE	IS25LQ040B-JKLV	8-contact WSON (6x5mm)
		IS25LQ040B-JULE	IS25LQ040B-JULV	8-contact USON (2x3mm)
		AEC-Q100 Grade	IS25LQ040B-JBLA*	8-pin SOIC 208mil
			IS25LQ040B-JNLA*	8-pin SOIC 150mil
			IS25LQ040B-JVLA*	8-pin VVSOP 150mil
			IS25LQ040B-JKLA*	8-contact WSON (6x5mm)
			IS25LQ040B-JULA*	8-contact USON (2x3mm)
		IS25LQ040B-JWLE		KGD (Call Factory)
2Mb		IS25LQ020B-JBLE	IS25LQ020B-JBLV	8-pin SOIC 208mil
		IS25LQ020B-JNLE	IS25LQ020B-JNLV	8-pin SOIC 150mil
		IS25LQ020B-JDLE	IS25LQ020B-JDLV	8-pin TSSOP 150mil
		IS25LQ020B-JVLE	IS25LQ020B-JVLV	8-pin VVSOP 150mil
		IS25LQ020B-JKLE	IS25LQ020B-JKLV	8-contact WSON (6x5mm)
		IS25LQ020B-JULE	IS25LQ020B-JULV	8-contact USON (2x3mm)
		AEC-Q100 Grade	IS25LQ020B-JBLA*	8-pin SOIC 208mil
			IS25LQ020B-JNLA*	8-pin SOIC 150mil
			IS25LQ020B-JDLA*	8-pin TSSOP 150mil
			IS25LQ020B-JVLA*	8-pin VVSOP 150mil
			IS25LQ020B-JKLA*	8-contact WSON (6x5mm)
			IS25LQ020B-JULA*	8-contact USON (2x3mm)
		IS25LQ020B-JWLE		KGD (Call Factory)
1Mb		IS25LQ010B-JBLE	IS25LQ010B-JBLV	8-pin SOIC 208mil
		IS25LQ010B-JNLE	IS25LQ010B-JNLV	8-pin SOIC 150mil
		IS25LQ010B-JDLE	IS25LQ010B-JDLV	8-pin TSSOP 150mil
		IS25LQ010B-JVLE	IS25LQ010B-JVLV	8-pin VVSOP 150mil
		IS25LQ010B-JKLE	IS25LQ010B-JKLV	8-contact WSON (6x5mm)
		IS25LQ010B-JULE	IS25LQ010B-JULV	8-contact USON (2x3mm)
		AEC-Q100 Grade	IS25LQ010B-JBLA*	8-pin SOIC 208mil
			IS25LQ010B-JNLA*	8-pin SOIC 150mil
			IS25LQ010B-JDLA*	8-pin TSSOP 150mil
			IS25LQ010B-JVLA*	8-pin VVSOP 150mil
			IS25LQ010B-JKLA*	8-contact WSON (6x5mm)
			IS25LQ010B-JULA*	8-contact USON (2x3mm)
		IS25LQ010B-JWLE		KGD (Call Factory)

Density	Frequency (MHz)	Order Part Number[1]		Package
512K	104	IS25LQ512B-JBLE	IS25LQ512B-JBLV	8-pin SOIC 208mil
		IS25LQ512B-JNLE	IS25LQ512B-JNLV	8-pin SOIC 150mil
		IS25LQ512B-JDLE	IS25LQ512B-JDLV	8-pin TSSOP 150mil
		IS25LQ512B-JVLE	IS25LQ512B-JVLV	8-pin VVSOP 150mil
		IS25LQ512B-JKLE	IS25LQ512B-JKLV	8-contact WSON (6x5mm)
		IS25LQ512B-JULE	IS25LQ512B-JULV	8-contact USON (2x3mm)
		AEC-Q100 Grade	IS25LQ512B-JBLA*	8-pin SOIC 208mil
			IS25LQ512B-JNLA*	8-pin SOIC 150mil
			IS25LQ512B-JDLA*	8-pin TSSOP 150mil
			IS25LQ512B-JVLA*	8-pin VVSOP 150mil
			IS25LQ512B-JKLA*	8-contact WSON (6x5mm)
			IS25LQ512B-JULA*	8-contact USON (2x3mm)
		IS25LQ512B-JWLE		KGD (Call Factory)
256K		IS25LQ025B-JBLE	IS25LQ025B-JBLV	8-pin SOIC 208mil
		IS25LQ025B-JNLE	IS25LQ025B-JNLV	8-pin SOIC 150mil
		IS25LQ025B-JDLE	IS25LQ025B-JDLV	8-pin TSSOP 150mil
		IS25LQ025B-JVLE	IS25LQ025B-JVLV	8-pin VVSOP 150mil
		IS25LQ025B-JKLE	IS25LQ025B-JKLV	8-contact WSON (6x5mm)
		IS25LQ025B-JULE	IS25LQ025B-JULV	8-contact USON (2x3mm)
		AEC-Q100 Grade	IS25LQ025B-JBLA*	8-pin SOIC 208mil
			IS25LQ025B-JNLA*	8-pin SOIC 150mil
			IS25LQ025B-JDLA*	8-pin TSSOP 150mil
			IS25LQ025B-JVLA*	8-pin VVSOP 150mil
			IS25LQ025B-JKLA*	8-contact WSON (6x5mm)
			IS25LQ025B-JULA*	8-contact USON (2x3mm)
		IS25LQ025B-JWLE		KGD (Call Factory)

Notes:

1. **Contact Factory for other Packaging options.**
2. **For Temp Grade, E: Extended grade, V: Hybrid Flow (Non-AEC-Q100 devices)**
   Auto Grades: A1, A2, A3 are AEC-Q100 devices with PPAP.

E = Extended Grade	-40°C to 105°C
V = Hybrid Flow	-40°C to 125°C
A1= Auto Grade 1	-40°C to 85°C
A2 = Auto Grade 2	-40°C to 105°C
A3 = Auto Grade 3	-40°C to 125°C