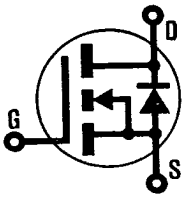
INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRFD020
IRFD022

N-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



4-PIN DIP

50 Volt, 0.10 Ohm, 1-Watt HEXDIP

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HEXDIP 4-pin, Dual-In-Line Package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features represent the state-of-the-art in power device packaging

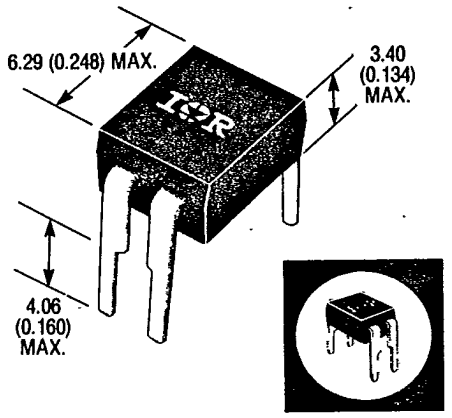
FEATURES:

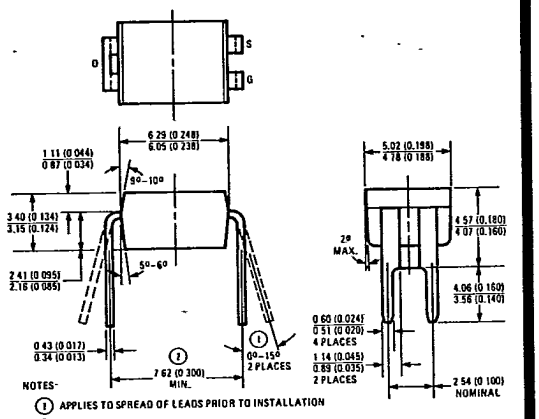
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD020	50V	0.10Ω	2.4A
IRFD022	50V	0.12Ω	2.2A

CASE STYLE AND DIMENSIONS





Case Style HD-1 (Similar to JEDEC Outline MO-001)
Dimensions in Millimeters and (Inches)

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IRFD020, IRFD022 Devices

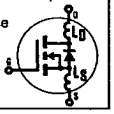
Absolute Maximum Ratings

Parameter		IRFD020	IRFD022	Units
V_{DS}	Drain - Source Voltage ①	50	50	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	50	50	V
I_D @ T_C = 25°C	Continuous Drain Current	2.4	2.2	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.4	A
I_{DM}	Pulsed Drain Current ②	19	18	A
V_{GS}	Gate - Source Voltage	±20		V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0		W
	Linear Derating Factor	0.0080		W/K⑥
I_{LM}	Inductive Current, Clamped	(See Fig. 14) L = 100μH 19	18	A
I_L	Unclamped Inductive Current (Avalanche Current) ③	(See Fig. 15) 2.2		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD020	50	—	—	V	V_{GS} = 0V, I_D = 250 μA
		IRFD022					
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ④	IRFD020	2.4	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
		IRFD022	2.2	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ④	IRFD020	—	0.080	0.10	Ω	V_{GS} = 10V, I_D = 1.4A
		IRFD022	—	0.11	0.12	Ω	
g_{fs}	Forward Transconductance ④	ALL	4.9	7.3	—	S(℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 7.5A
C_{iss}	Input Capacitance	ALL	—	400	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	—	260	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	—	44	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.7	13	ns	V_{DD} = 25V, I_D ≈ 15A, R_G = 18Ω, R_D = 1.7Ω
t_r	Rise Time	ALL	—	55	83	ns	See Fig. 16
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	16	24	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	—	26	39	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	16	24	nC	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	4.7	7.1	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	4.7	7.1	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W⑤	Typical socket mount

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD020	—	—	2.4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD022	—	—	2.2	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD020	—	—	19	A	
		IRFD022	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	1.4	V	T_C = 25°C, I_S = 2.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	57	130	310	ns	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	0.17	0.34	0.85	μC	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C
② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
③ @ V_{dd}= 25V, T_J = 25°C, L = 100 μH, R_G = 25Ω
④ Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%
⑤ K/W = °C/W, W/K = W/°C

4-PIN DIP

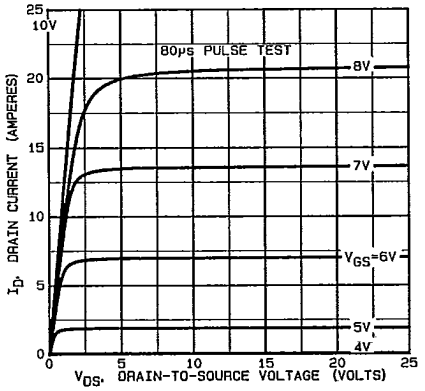


Fig. 1 — Typical Output Characteristics

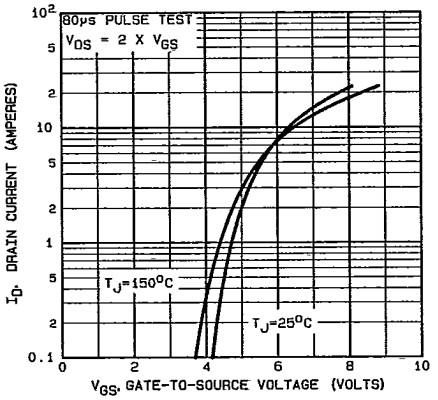


Fig. 2 — Typical Transfer Characteristics

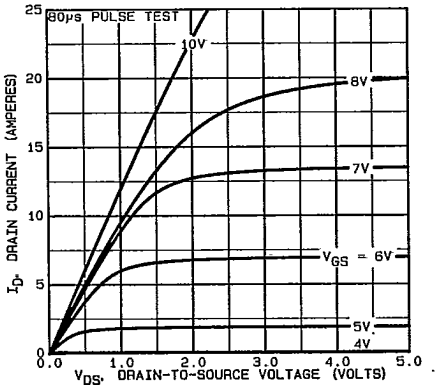


Fig. 3 — Typical Saturation Characteristics

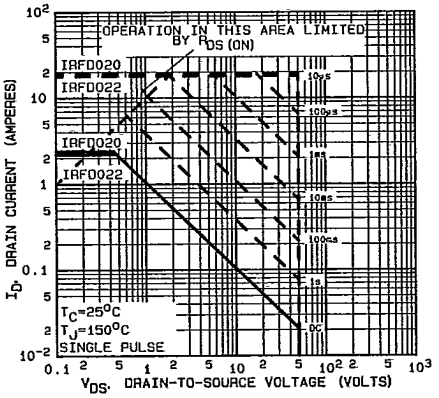


Fig. 4 — Maximum Safe Operating Area

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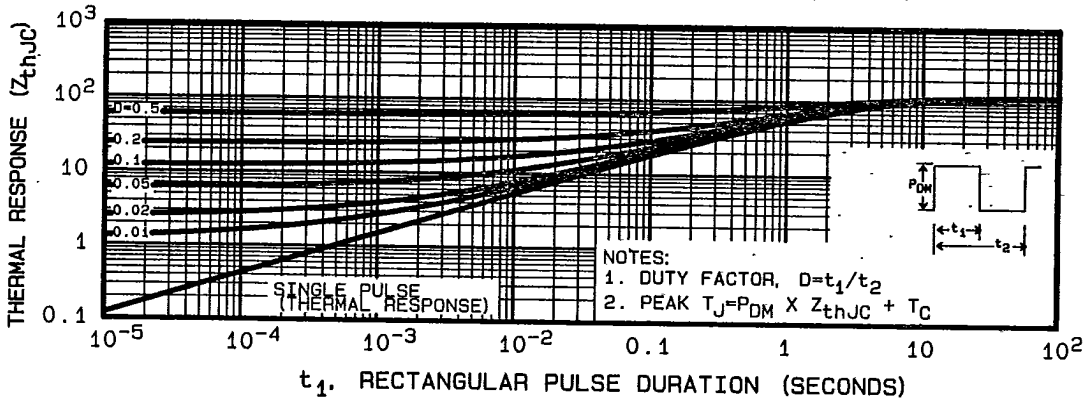


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

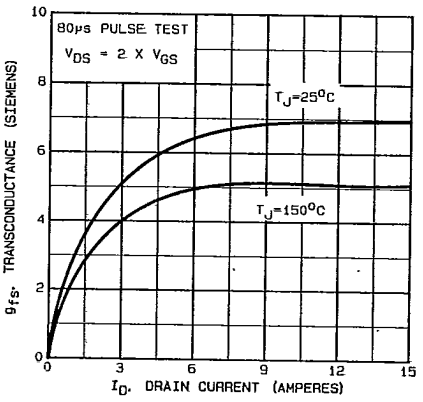


Fig. 6 — Typical Transconductance Vs. Drain Current

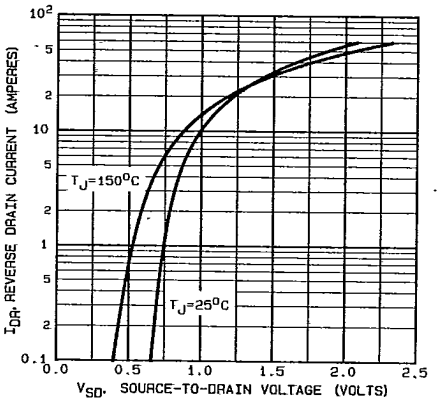


Fig. 7 — Typical Source-Drain Diode Forward Voltage

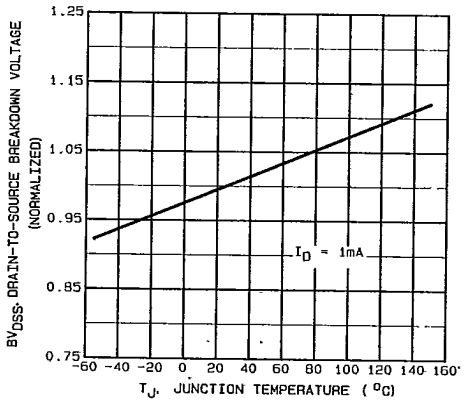


Fig. 8 — Breakdown Voltage Vs. Temperature

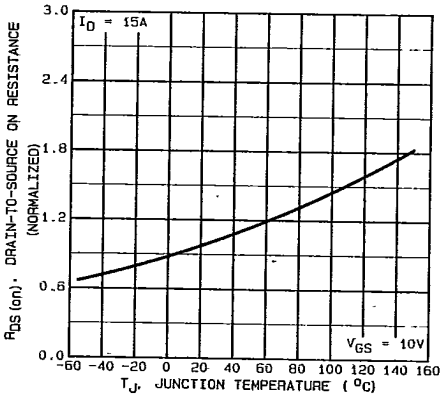


Fig. 9 — Normalized On-Resistance Vs. Temperature

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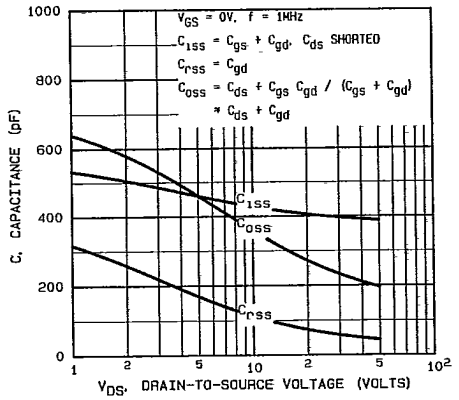


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

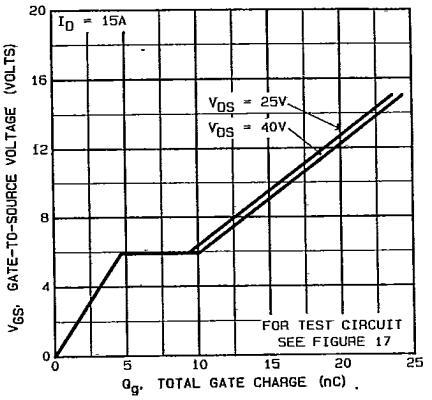


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

4-PIN DIP

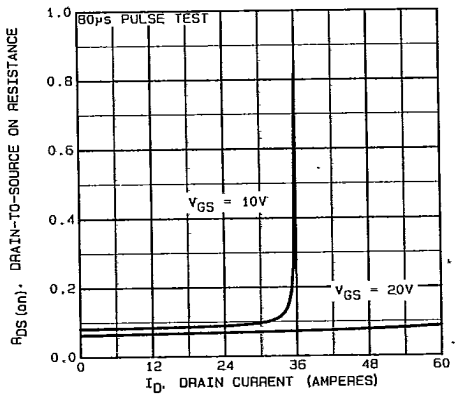


Fig. 12 — Typical On-Resistance Vs. Drain Current

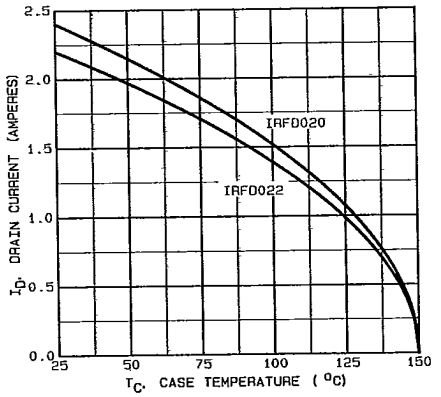


Fig. 13 — Maximum Drain Current Vs. Case Temperature

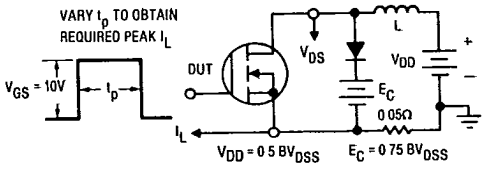


Fig. 14a — Clamped Inductive Test Circuit

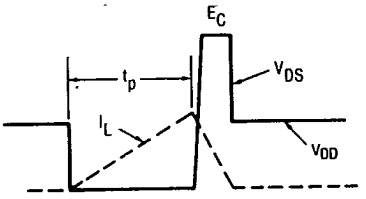


Fig. 14b — Clamped Inductive Waveforms

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IRFD020, IRFD022 Devices

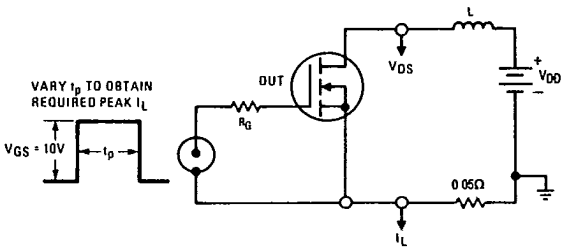


Fig. 15a — Unclamped Inductive Test Circuit

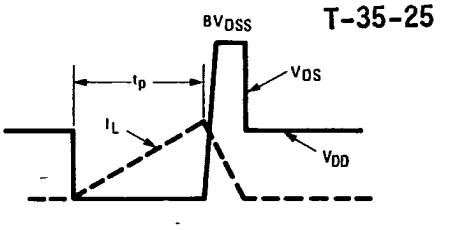


Fig. 15b — Unclamped Inductive Load Test Waveforms

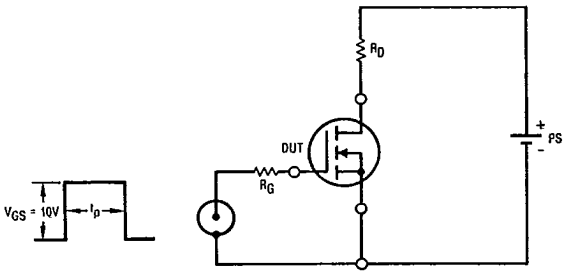


Fig. 16 — Switching Time Test Circuit

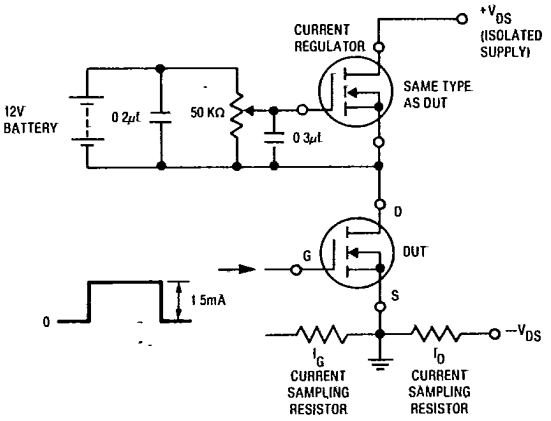


Fig. 17 — Gate Charge Test Circuit

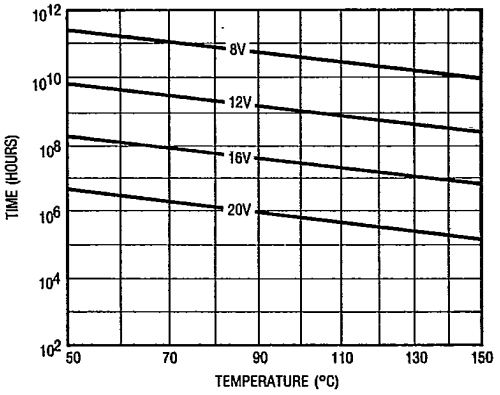


*Fig. 18 — Typical Time to Accumulated 1% Gate Failure

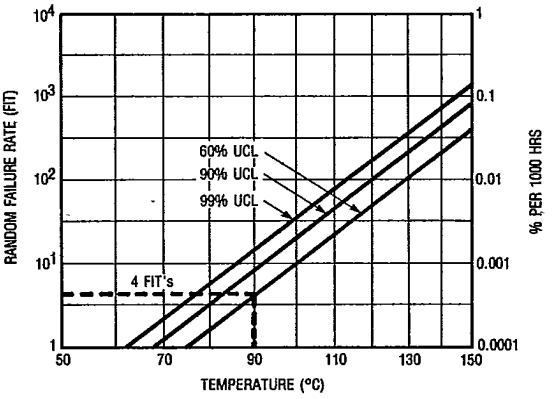


*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.

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