KERSEMI ELECTRONIC CO.,LTD.

IRF840A

SMPS MOSFET

TO-220AB



Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

Benefits
- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN1001)

V_{DSS}	Rds(on) max	I_D
500V	0.85Ω	8.0A

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	5.1	
I_{DM}	Pulsed Drain Current ①	32	
P_D @T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies:
- Two Transistor Forward
- Haft Bridge
- Full Bridge

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.58	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.85	Ω	V_{GS} = 10V, I_D = 4.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 500V, V_{GS} = 0V
		——	——	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.7	——	——	S	V_{DS} = 50V, I_D = 4.8A
Q_g	Total Gate Charge	——	——	38	nC	I_D = 8.0A
Q_{gs}	Gate-to-Source Charge	——	——	9.0		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	18		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	11	——	ns	V_{DD} = 250V
t_r	Rise Time	——	23	——		I_D = 8.0A
$t_{d(off)}$	Turn-Off Delay Time	——	26	——		R_G = 9.1Ω
t_f	Fall Time	——	19	——		R_D = 31Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	——	1018	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	155	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	8.0	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	1490	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	42	——		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	56	——		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	510	mJ
I_{AR}	Avalanche Current①	——	8.0	A
E_{AR}	Repetitive Avalanche Energy①	——	13	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient		62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	32		
V_{SD}	Diode Forward Voltage	——	——	2.0	V	T_J = 25°C, I_S = 8.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	422	633	ns	T_J = 25°C, I_F = 8.0A
Q_{rr}	Reverse RecoveryCharge	——	2.0	3.0	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

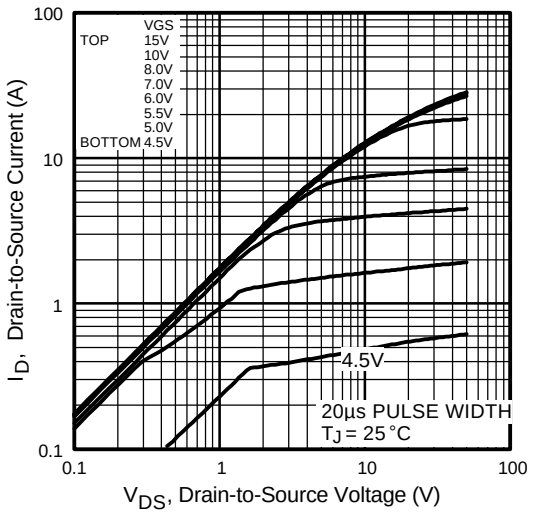


Fig 1. Typical Output Characteristics

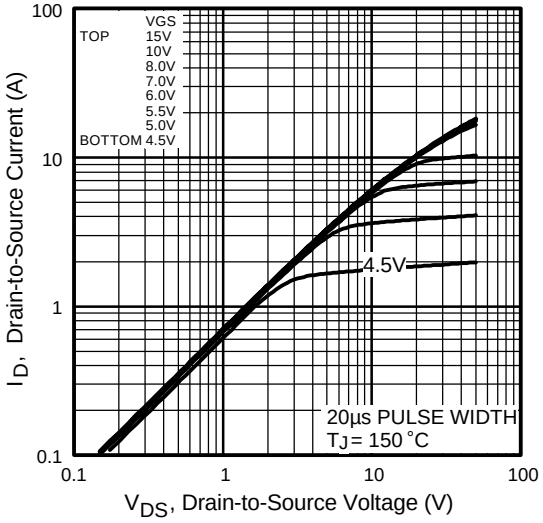


Fig 2. Typical Output Characteristics

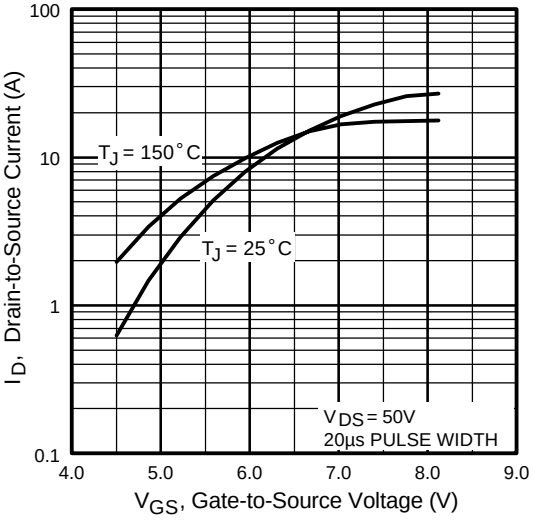


Fig 3. Typical Transfer Characteristics

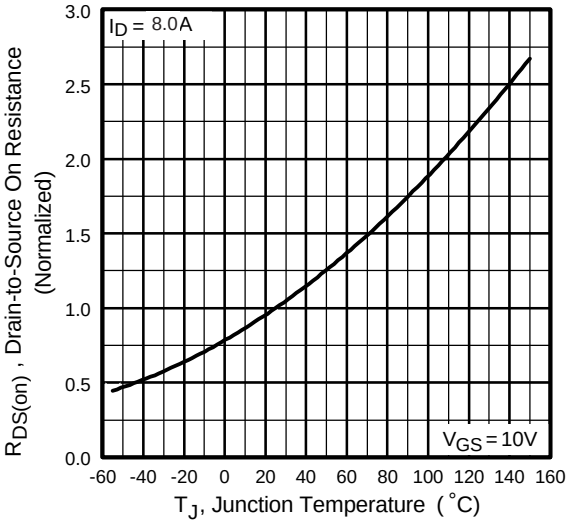


Fig 4. Normalized On-Resistance Vs. Temperature

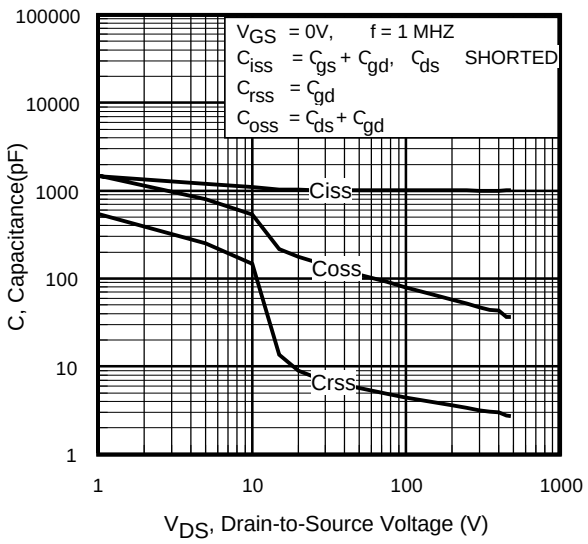


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

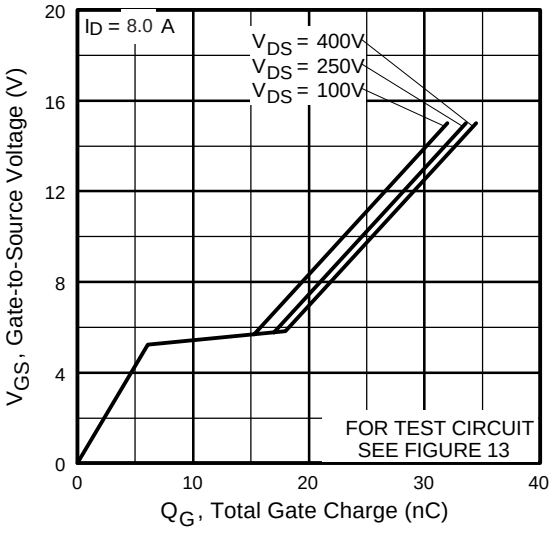


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

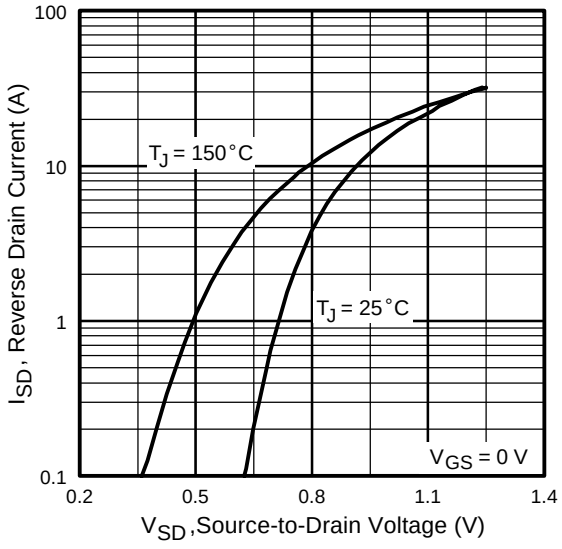


Fig 7. Typical Source-Drain Diode Forward Voltage

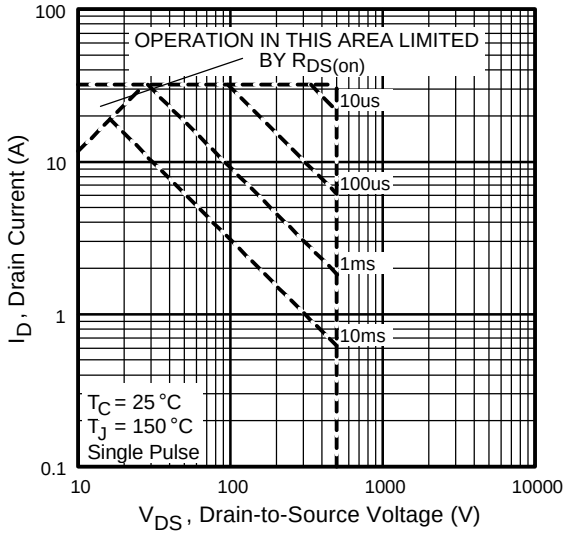


Fig 8. Maximum Safe Operating Area

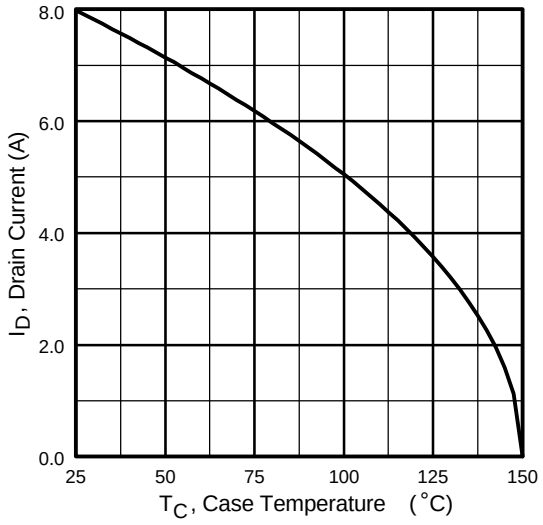


Fig 9. Maximum Drain Current Vs. Case Temperature

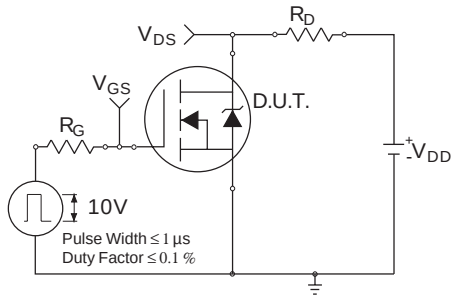


Fig 10a. Switching Time Test Circuit

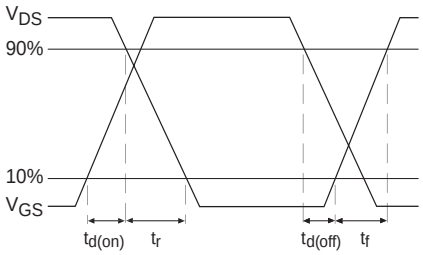


Fig 10b. Switching Time Waveforms

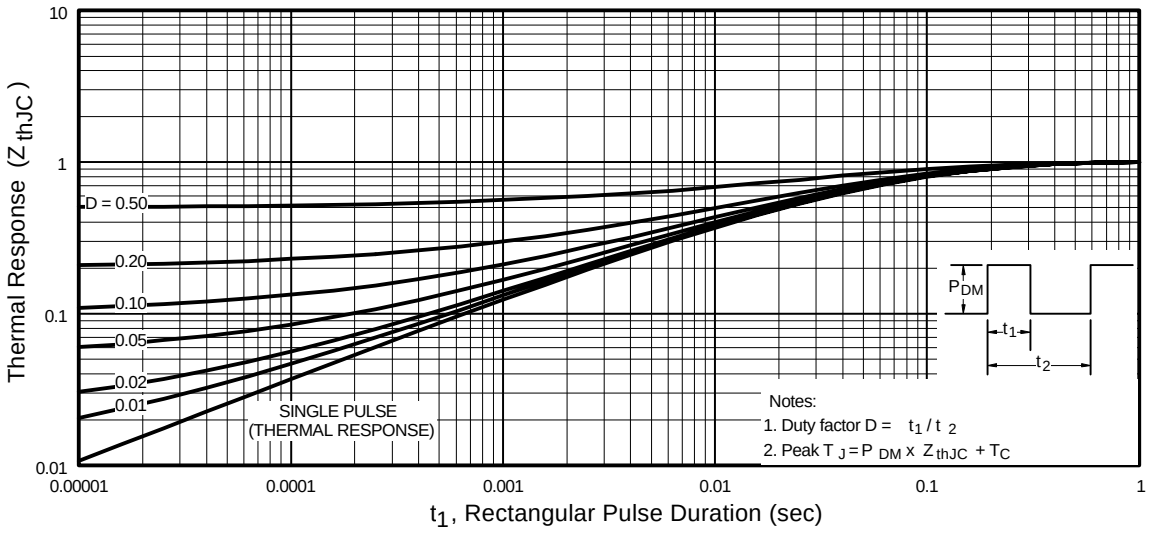


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

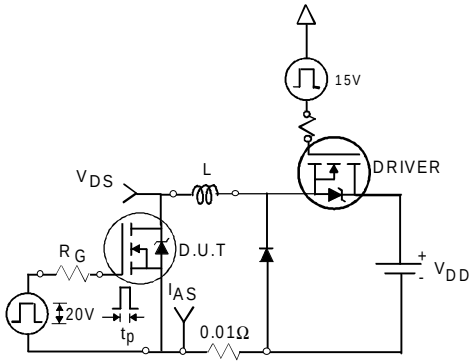


Fig 12a. Unclamped Inductive Test Circuit

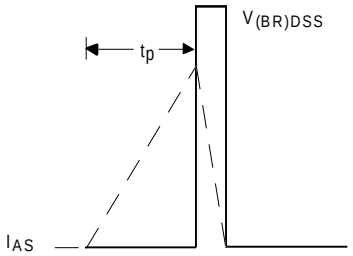


Fig 12b. Unclamped Inductive Waveforms

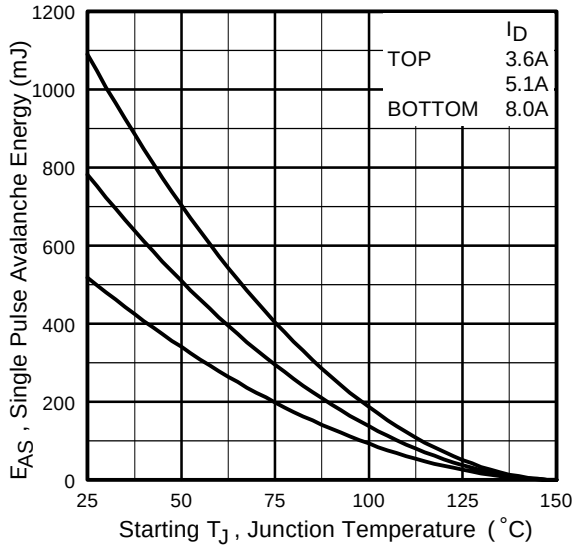


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

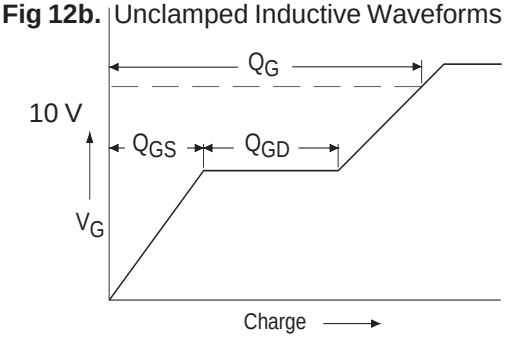


Fig 13a. Basic Gate Charge Waveform

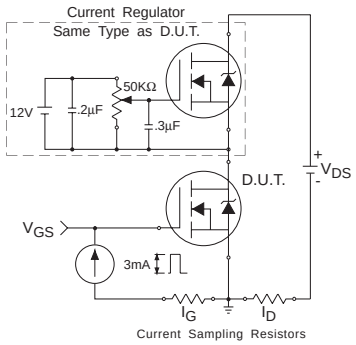


Fig 13b. Gate Charge Test Circuit

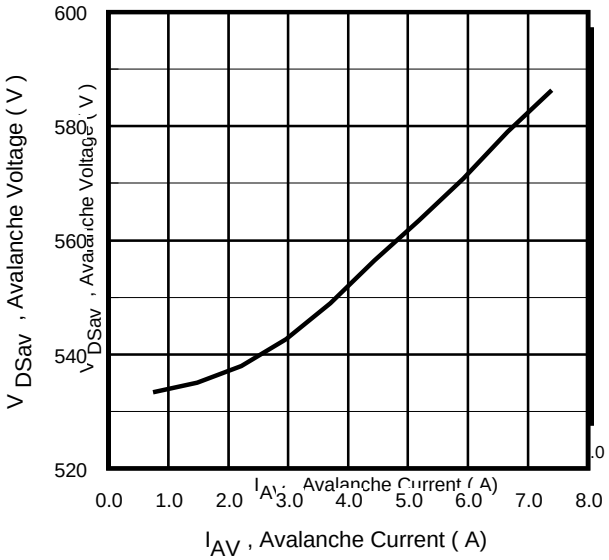
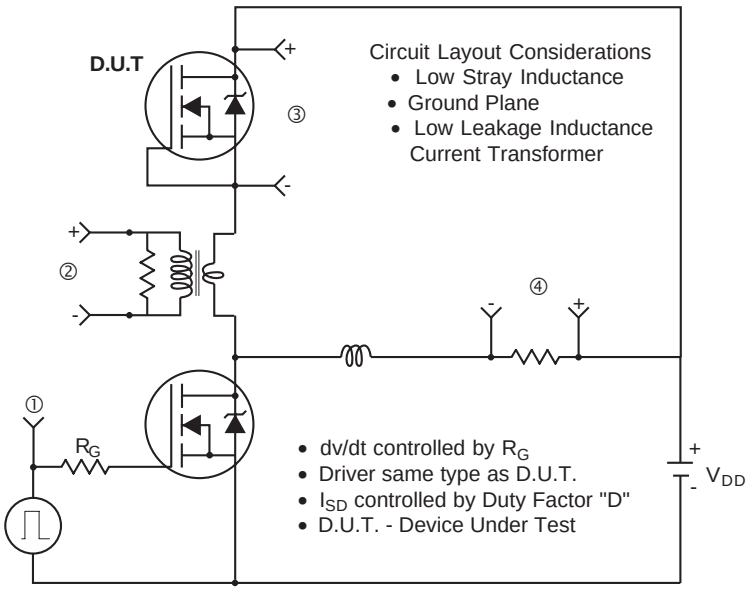
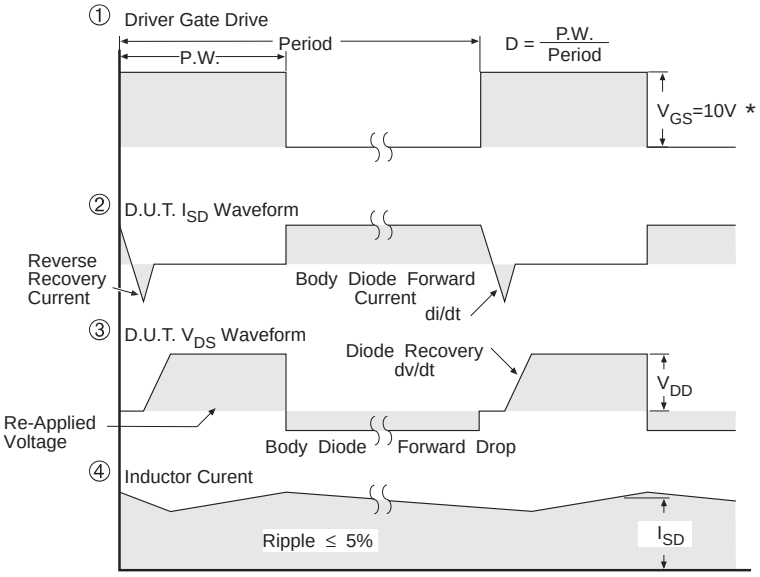


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit





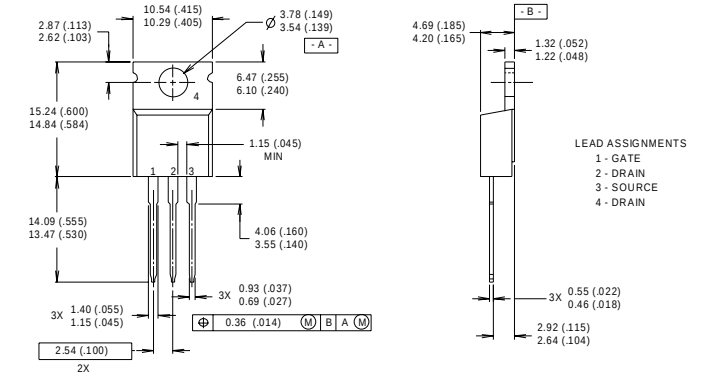
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



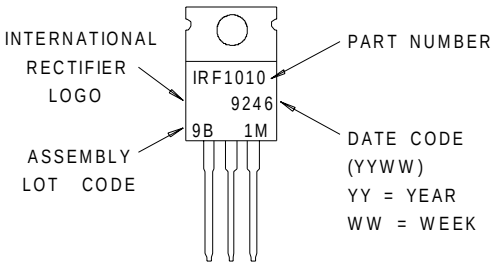
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 16 mH
R_G = 25Ω, I_{AS} = 8.0A. (See Figure 12)

③ I_{SD} ≤ 8.0A, di/dt ≤ 100A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}