Data Sheet July 1999 File Number 1579.4

3.3A, 400V, 1.800 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17404.

Ordering Information

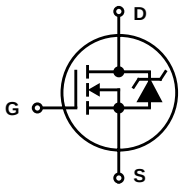
PART NUMBER	PACKAGE	BRAND
IRF720	TO-220AB	IRF720

NOTE: When ordering, use the entire part number.

Features

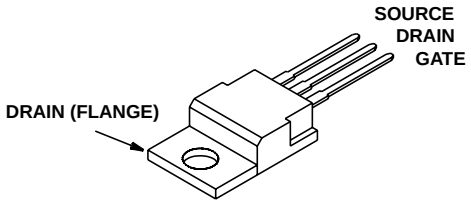
- 3.3A, 400V
- $r_{DS(ON)} = 1.800\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
http://www.intersil.com or 407-727-9207 | Copyright © Intersil Corporation 1999

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

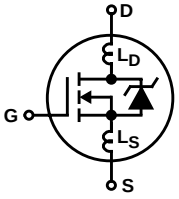
		IRF720	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	400	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	400	V
Continuous Drain Current	I_D	3.3	A
$T_C = 100^oC$	I_D	2.1	A
Pulsed Drain Current (Note 3)	I_{DM}	13	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	50	W
Linear Derating Factor		0.4	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	190	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

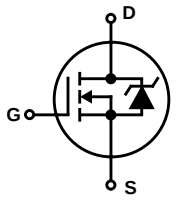
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V, (Figure 10)		400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$		-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V (Figure 7)		3.3	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1.8A, V_{GS} = 10V, (Figures 8, 9)		-	1.5	1.8	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 10V$, I_D = 2.0A, (Figure 12)		1.7	2.7	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, $I_D \approx$ 3.3A, R_{GS} = 18Ω, V_{GS} = 10V, R_L = 59Ω MOSFET Switching Times are Essentially Independent of Operating Temperature		-	10	15	ns
Rise Time	t_r			-	14	21	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	30	45	ns
Fall Time	t_f			-	13	20	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{G(REF)}$ = 1.5mA, (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	12	20	nC
Gate to Source Charge	Q_{gs}			-	2.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	6.0	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 10)		-	360	-	pF
Output Capacitance	C_{OSS}			-	55	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	20	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	2.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 	-	-	3.3	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	13	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 3.3A$, $V_{GS} = 0V$, (Figure 13)	-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 3.3A$, $dI_{SD}/dt = 100A/\mu s$	120	-	600	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 3.3A$, $dI_{SD}/dt = 100A/\mu s$	0.64	-	3.0	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, L = 31µH, $R_{GS} = 25\Omega$, peak $I_{AS} = 3.3A$.

Typical Performance Curves Unless Otherwise Specified

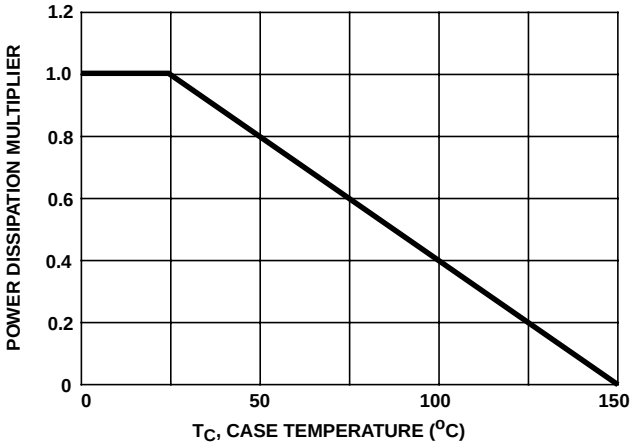


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

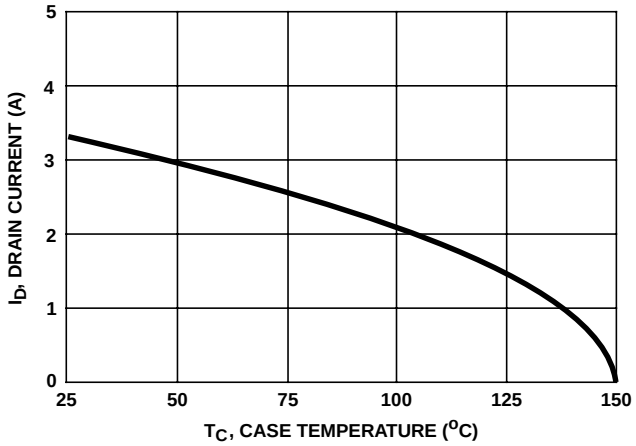


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

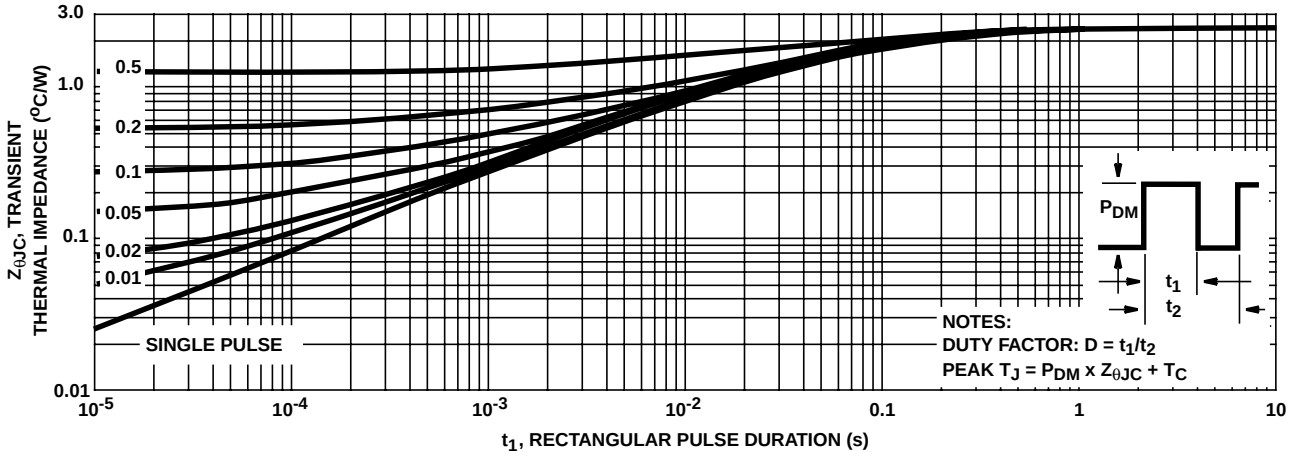


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

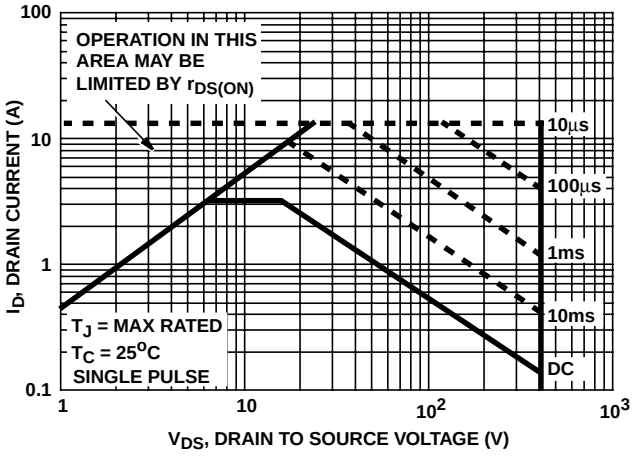


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

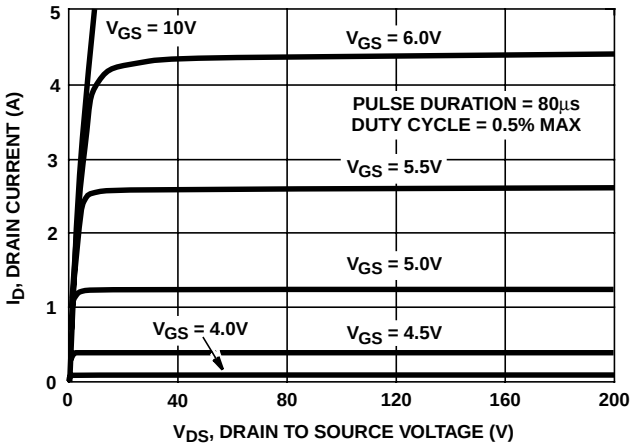


FIGURE 5. OUTPUT CHARACTERISTICS

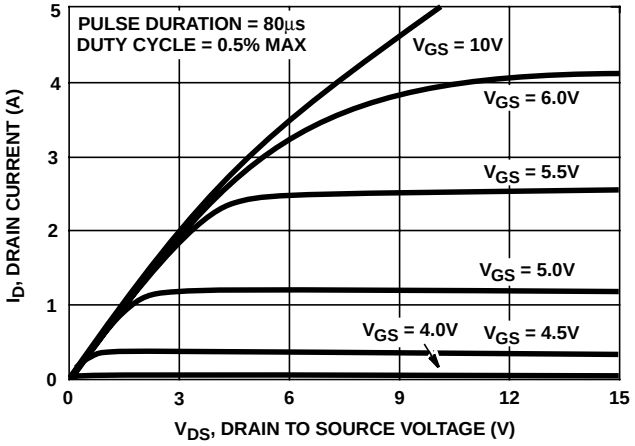


FIGURE 6. SATURATION CHARACTERISTICS

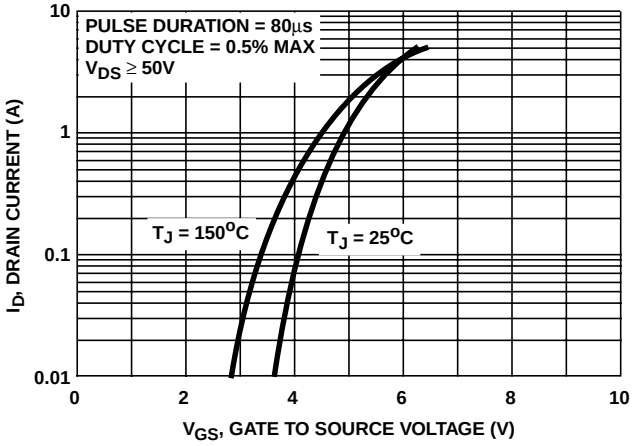


FIGURE 7. TRANSFER CHARACTERISTICS

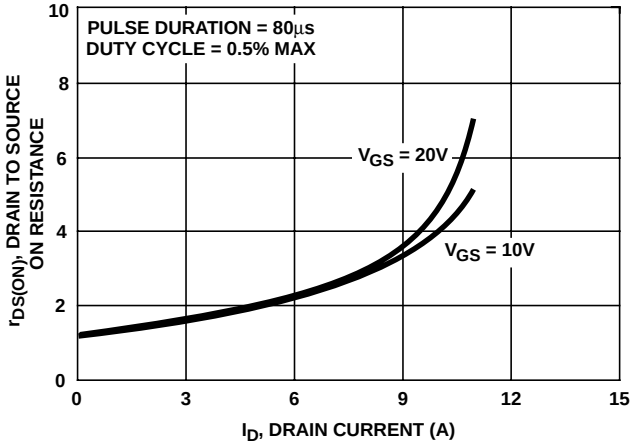


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

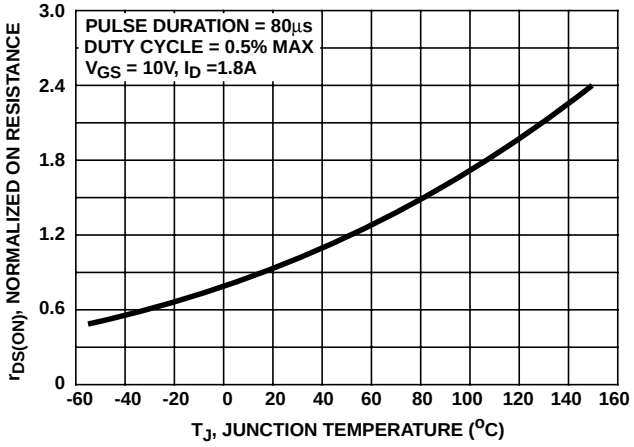


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

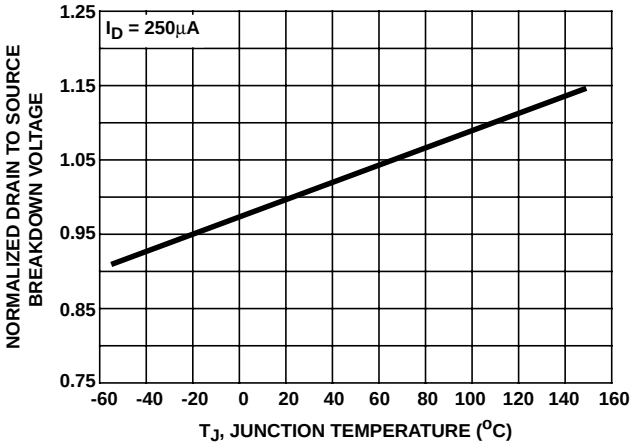


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

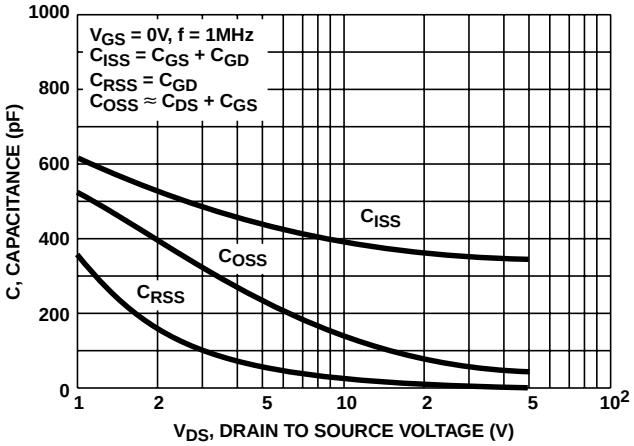


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

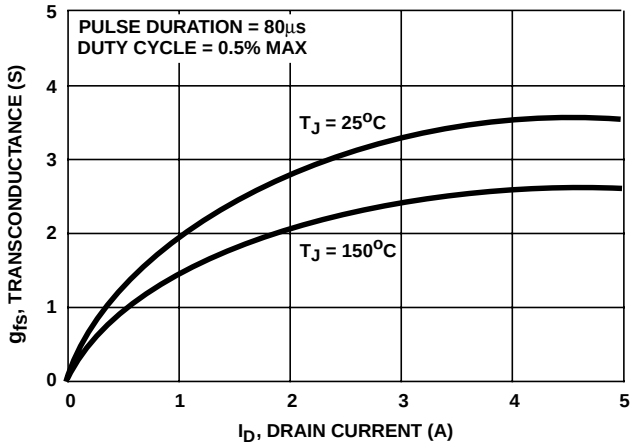


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

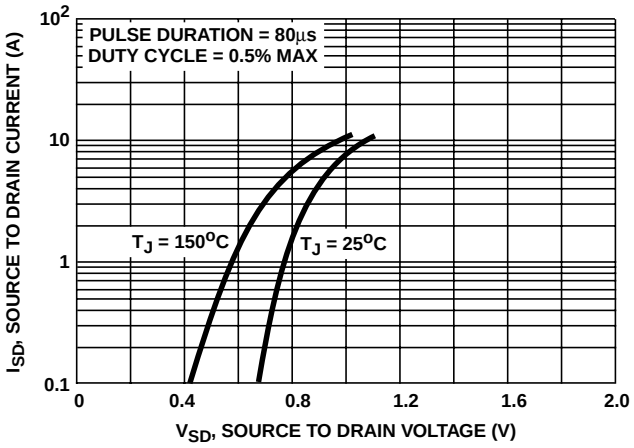


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

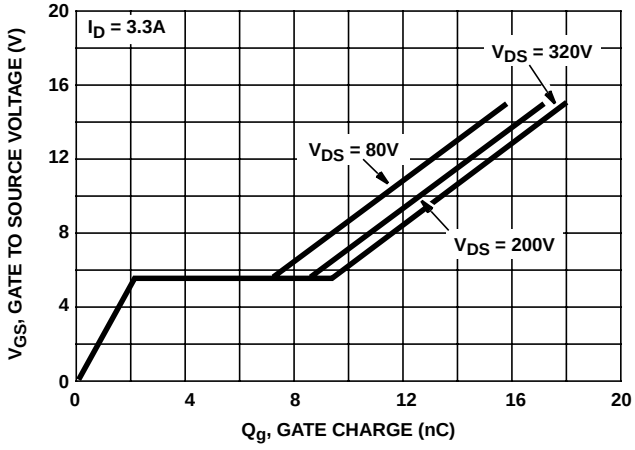


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

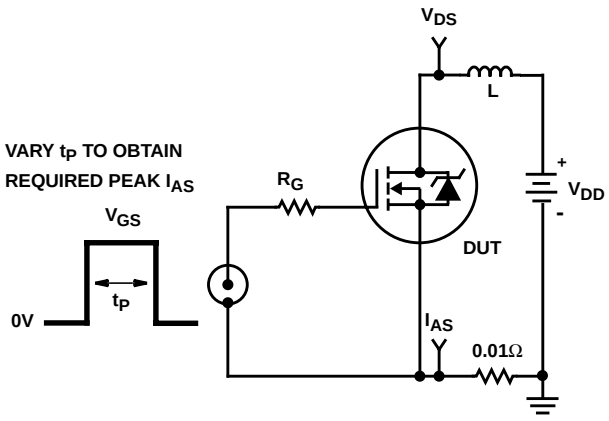


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

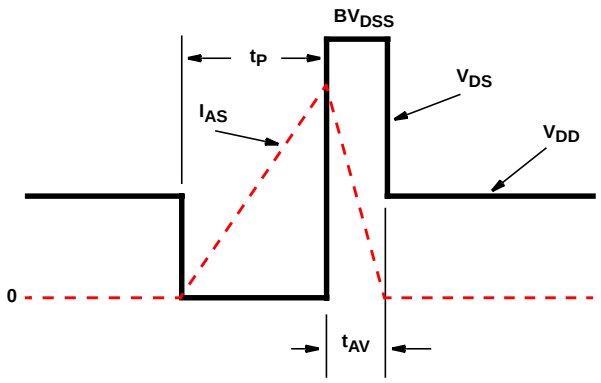


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

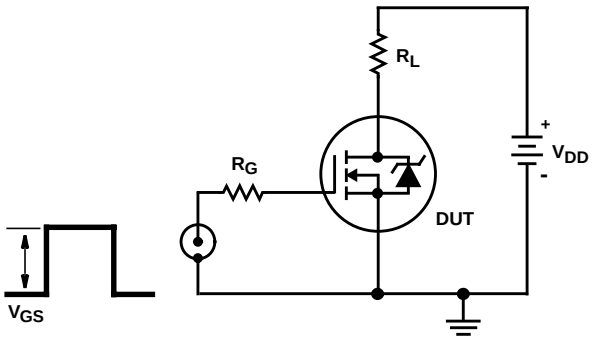


FIGURE 17. SWITCHING TIME TEST CIRCUIT

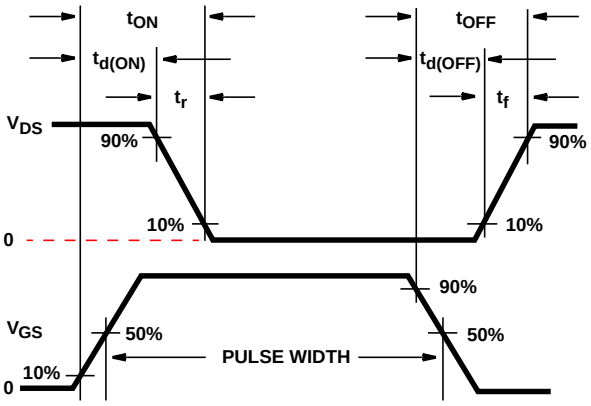


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

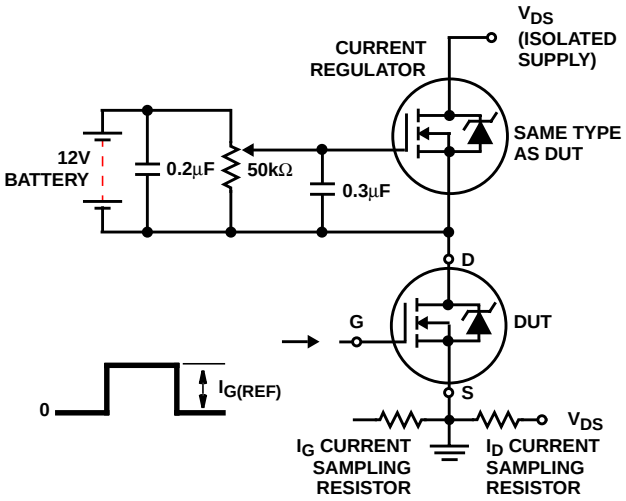


FIGURE 19. GATE CHARGE TEST CIRCUIT

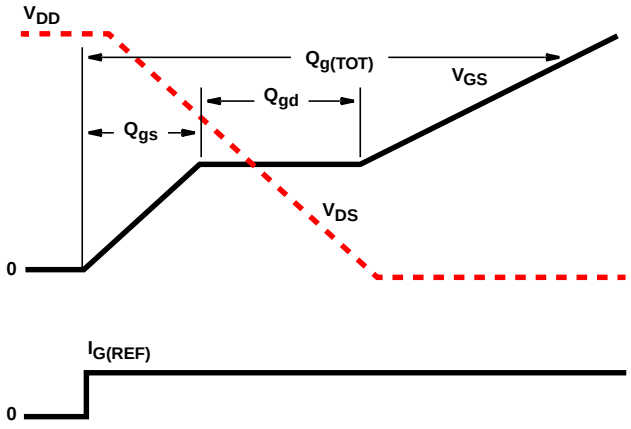


FIGURE 20. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029