International
IOR Rectifier

PD - 94291B

IRF3808

AUTOMOTIVE MOSFET

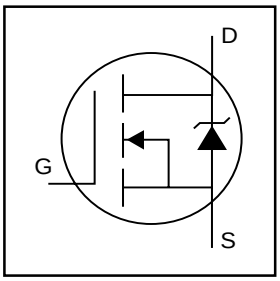
HEXFET® Power MOSFET

Typical Applications

- Integrated Starter Alternator
- 42 Volts Automotive Electrical Systems

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



V_{DSS} = 75V

$R_{DS(on)}$ = 0.007Ω

I_D = 140A⑥

Description

Designed specifically for Automotive applications, this Advanced Planar Stripe HEXFET ® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, low RθJC, fast switching speed and improved repetitive avalanche rating. This combination makes the design an extremely efficient and reliable choice for use in higher power Automotive electronic systems and a wide variety of other applications.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	140⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	97⑥	
I_{DM}	Pulsed Drain Current ①	550	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	430	mJ
I_{AR}	Avalanche Current①	82	A
E_{AR}	Repetitive Avalanche Energy⑦	See Fig.12a, 12b, 15, 16	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

HEXFET(R) is a registered trademark of International Rectifier.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.086	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.9	7.0	mΩ	V_{GS} = 10V, I_D = 82A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	100	—	—	S	V_{DS} = 25V, I_D = 82A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 75V, V_{GS} = 0V
		—	—	250		V_{DS} = 60V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	150	220	nC	I_D = 82A
Q_{gs}	Gate-to-Source Charge	—	31	47		V_{DS} = 60V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	50	76		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	V_{DD} = 38V
t_r	Rise Time	—	140	—		I_D = 82A
$t_{d(off)}$	Turn-Off Delay Time	—	68	—		R_G = 2.5Ω
t_f	Fall Time	—	120	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5310	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	890	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	6010	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	570	—		V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1140	—		V_{GS} = 0V, V_{DS} = 0V to 60V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	140⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	550		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 82A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	93	140	ns	T_J = 25°C, I_F = 82A
Q_{rr}	Reverse RecoveryCharge	—	340	510	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.130mH R_G = 25Ω, I_{AS} = 82A. (See Figure 12).

③ I_{SD} ≤ 82A, di/dt ≤ 310A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

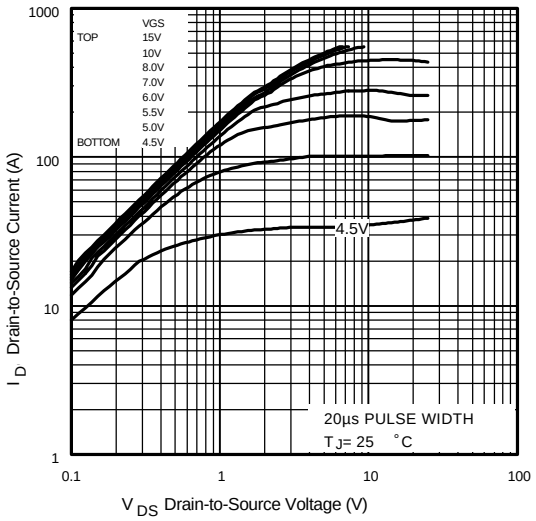


Fig 1. Typical Output Characteristics

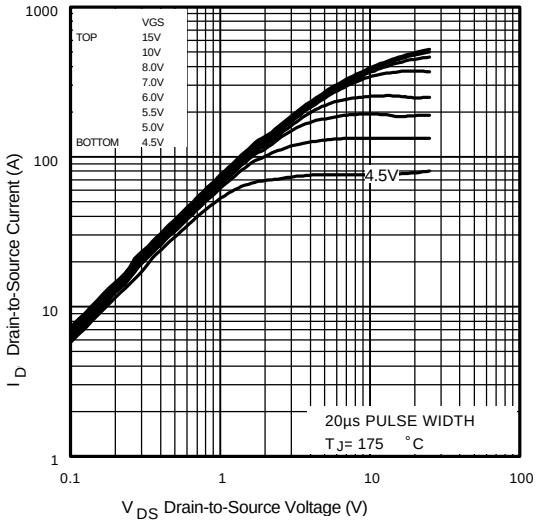


Fig 2. Typical Output Characteristics

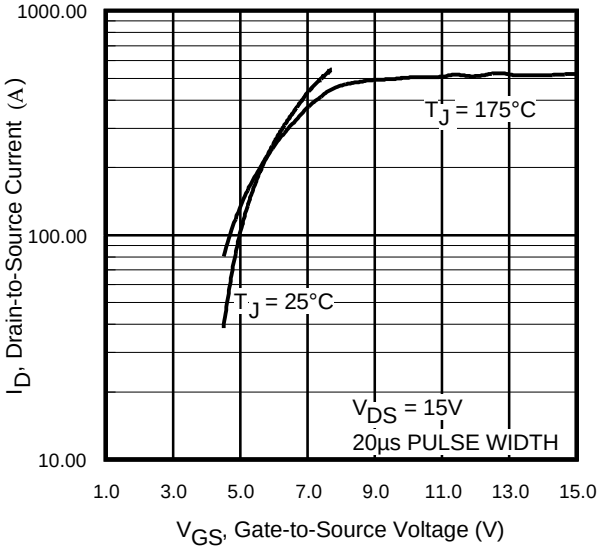


Fig 3. Typical Transfer Characteristics

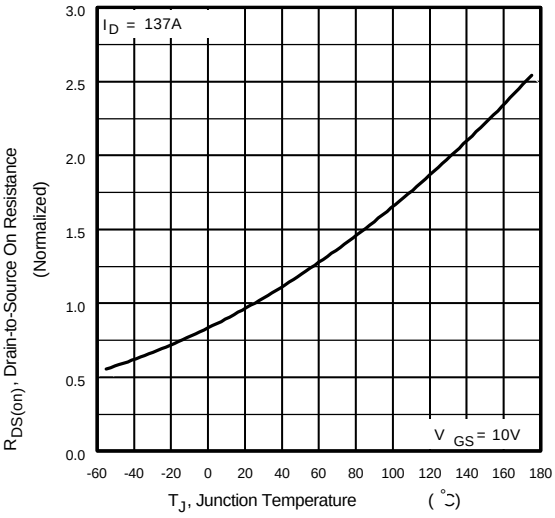


Fig 4. Normalized On-Resistance Vs. Temperature

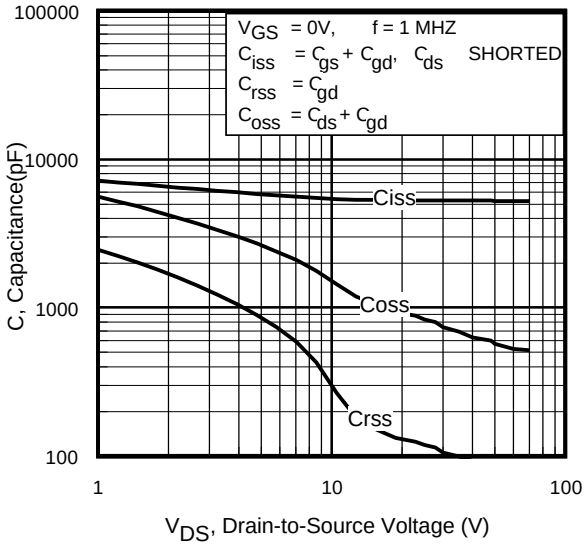


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

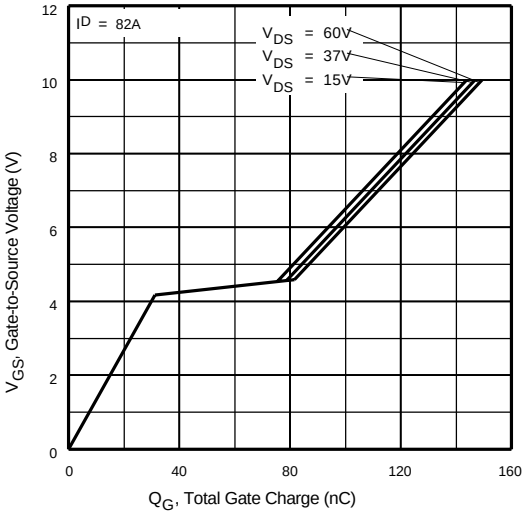


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

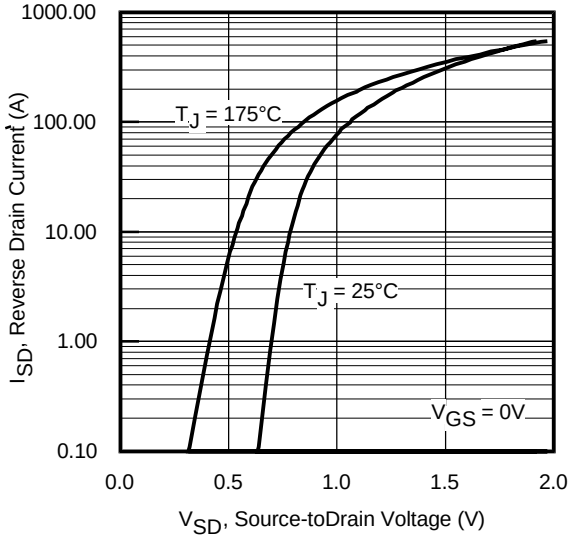


Fig 7. Typical Source-Drain Diode Forward Voltage

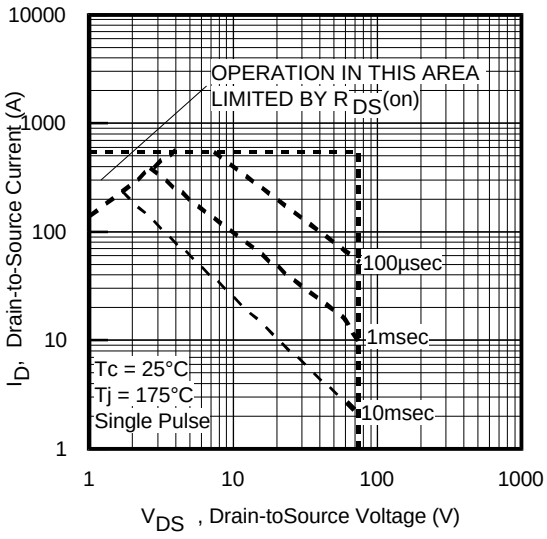


Fig 8. Maximum Safe Operating Area

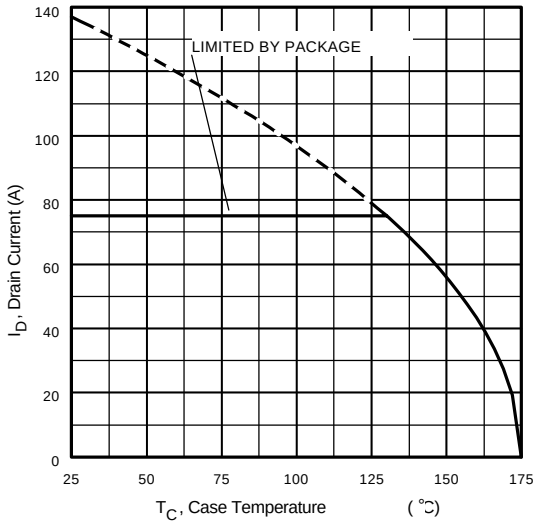


Fig 9. Maximum Drain Current Vs. Case Temperature

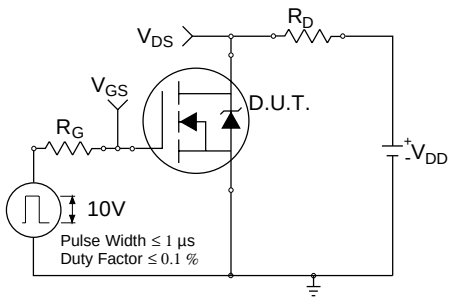


Fig 10a. Switching Time Test Circuit

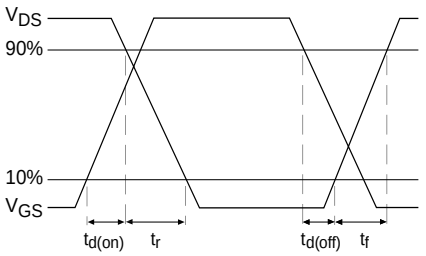


Fig 10b. Switching Time Waveforms

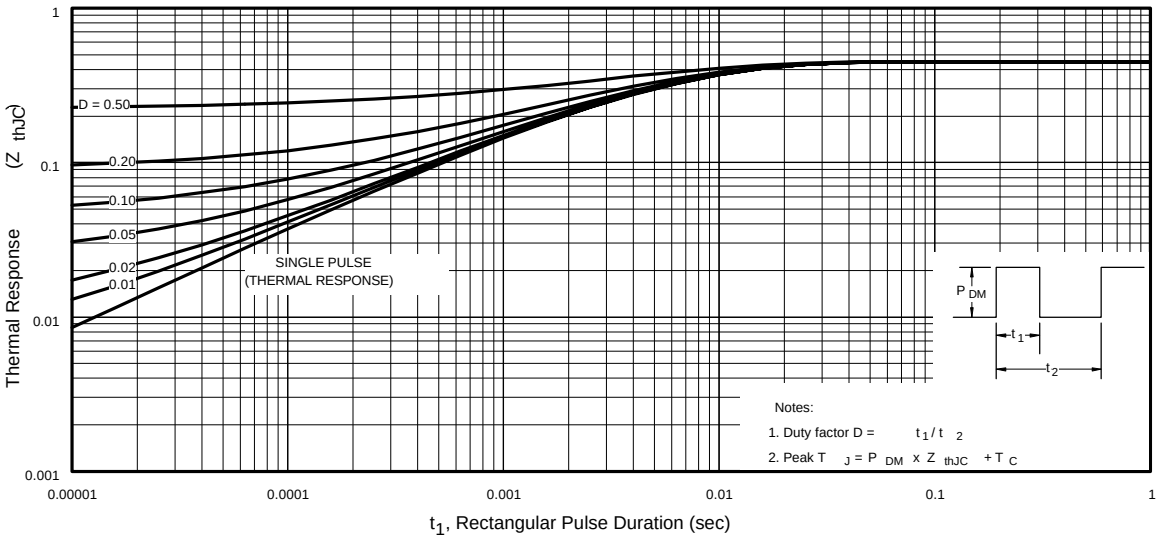


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

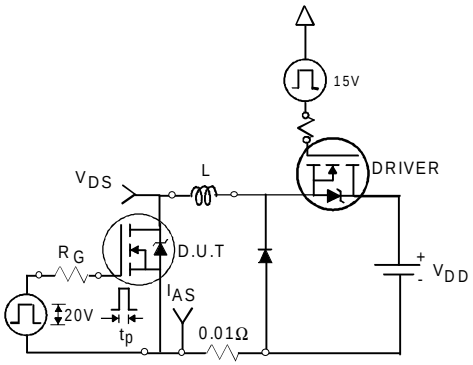


Fig 12a. Unclamped Inductive Test Circuit

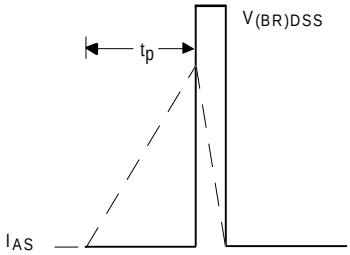


Fig 12b. Unclamped Inductive Waveforms

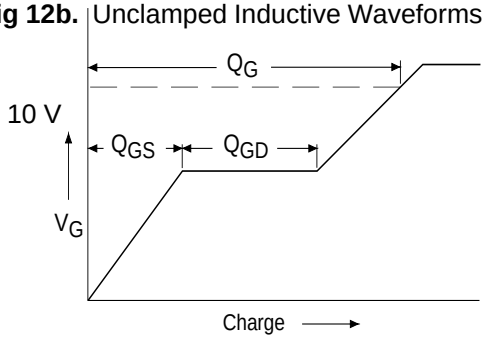


Fig 13a. Basic Gate Charge Waveform

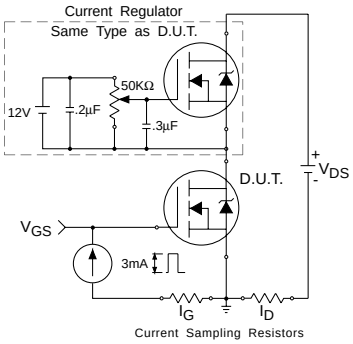


Fig 13b. Gate Charge Test Circuit

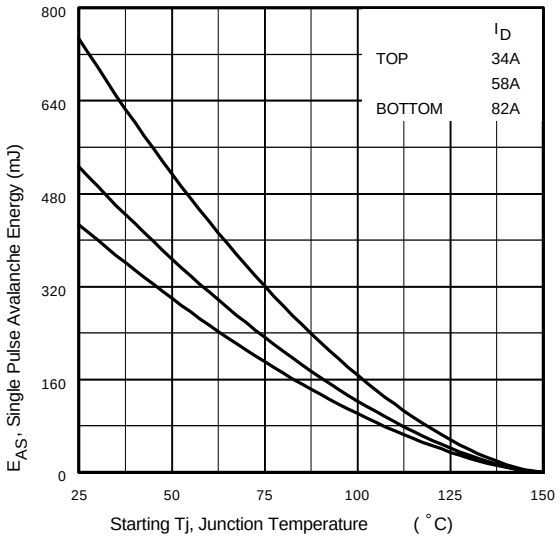


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

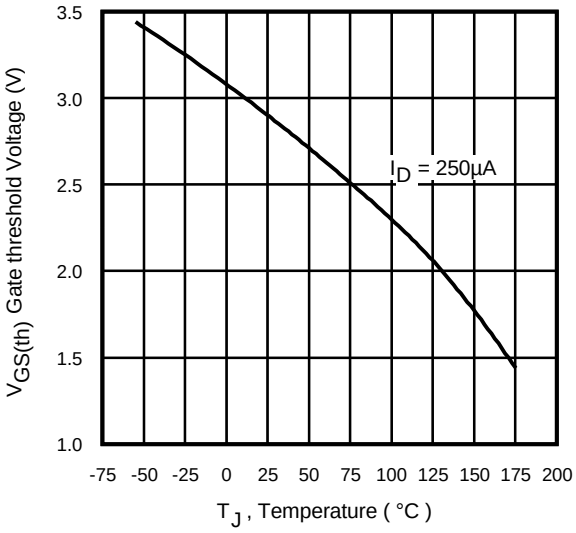


Fig 14. Threshold Voltage Vs. Temperature

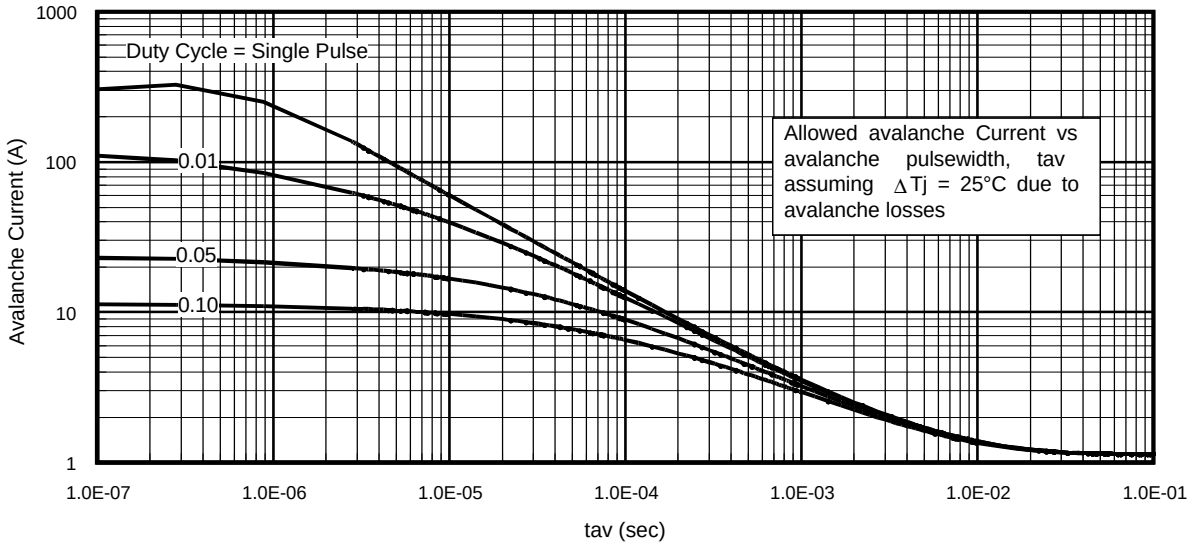


Fig 15. Typical Avalanche Current Vs.Pulsewidth

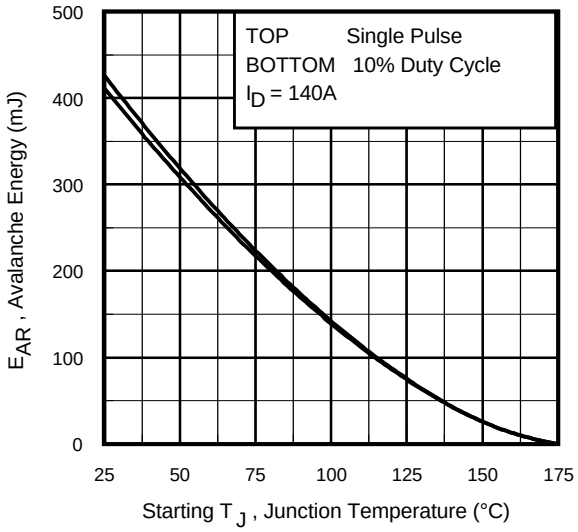


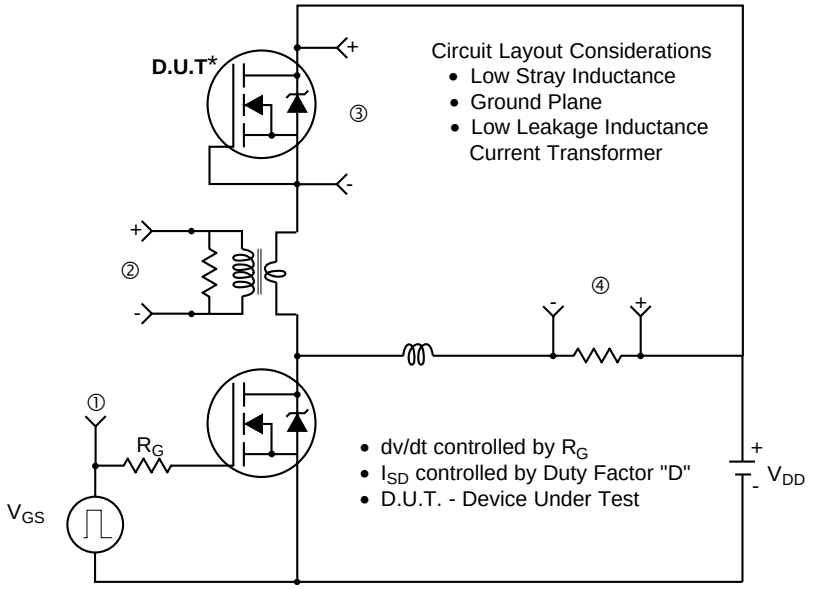
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

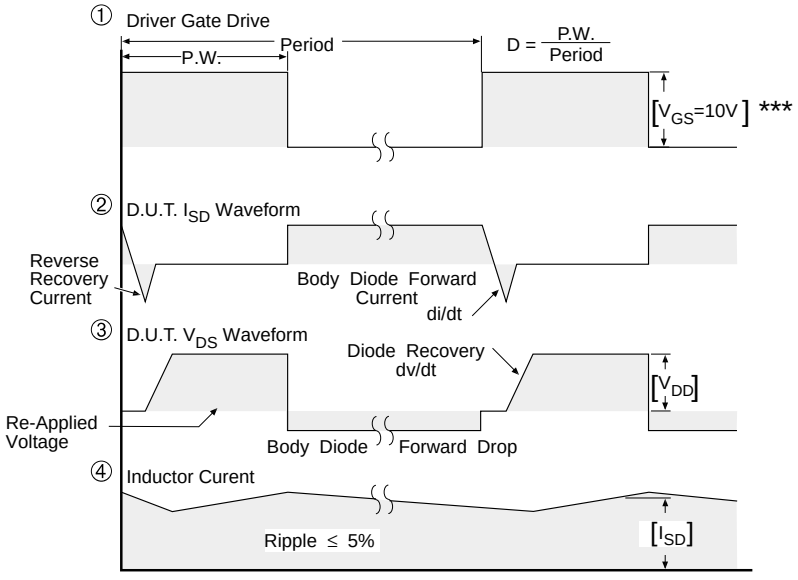
1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

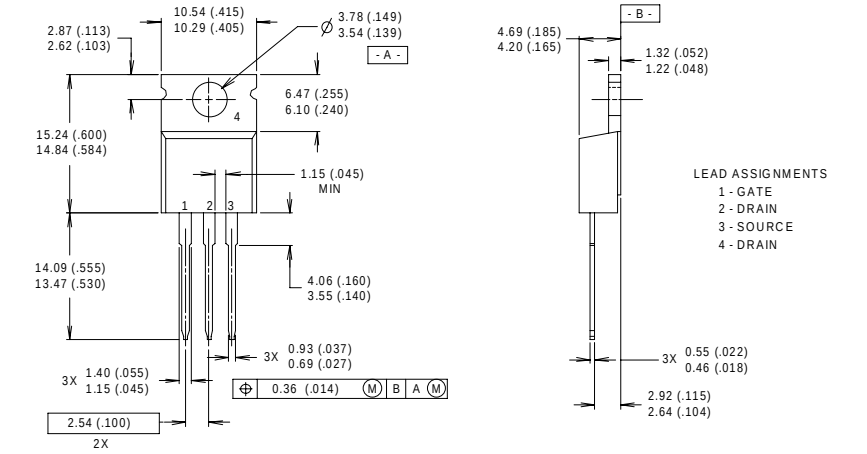


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

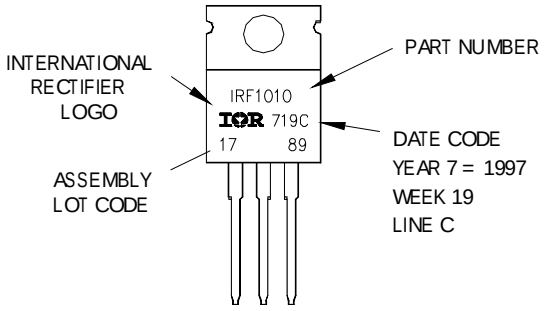


NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive (Q101) market.
Qualification Standards can be found on IR's Web site.

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