USER GUIDE FOR IR3640 EVALUATION BOARD

DESCRIPTION

The IR3640 is a PWM controller for use in high performance synchronous Buck DC/DC applications. This is designed to drive a pair of external NFETs using a programmable switching frequency up to 1.5MHz in voltage mode. It is housed in a in 20 Lead 3x4 MLPQ package.

Key features offered by the IR3640 include programmable soft-start ramp, Power Good, thermal protection, over voltage and over current protection, programmable switching frequency, tracking input, enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3640 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3640 is available in the IR3640 data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{cc}= +5V (5.5V Max)
- V_{out} = +1.8V @ 0- 25A
- F_s = 600kHz
- L = 0.33uH
- C_{in}= 4x10uF (ceramic 1210) + 2x330uF (electrolytic)
- C_{out}= 10x47uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 25A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3640 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT+	V_{out} (+1.8V)
VOUT-	Ground of Vout
Sync	Synchronous input
PGood	Power Good Signal

LAYOUT

The PCB is a 6-layer board. All of layers are 2 Oz. copper. The IR3640 and other components are mounted on the top and bottom side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3640. The feedback resistors are connected to the output voltage at the point of regulation and are located close to IR3640. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

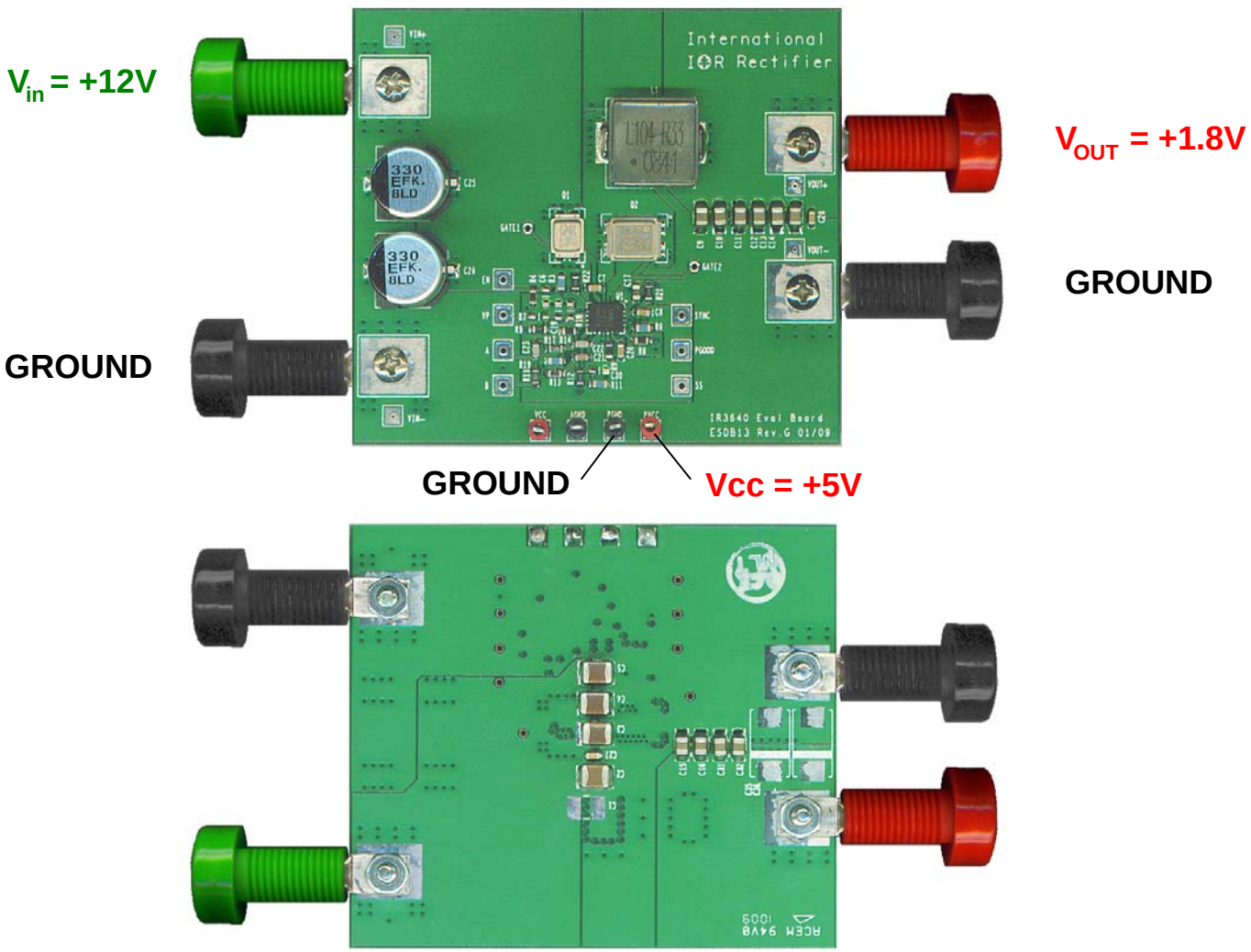


Fig. 1: Connection diagram of IR3640 evaluation board (top and bottom)

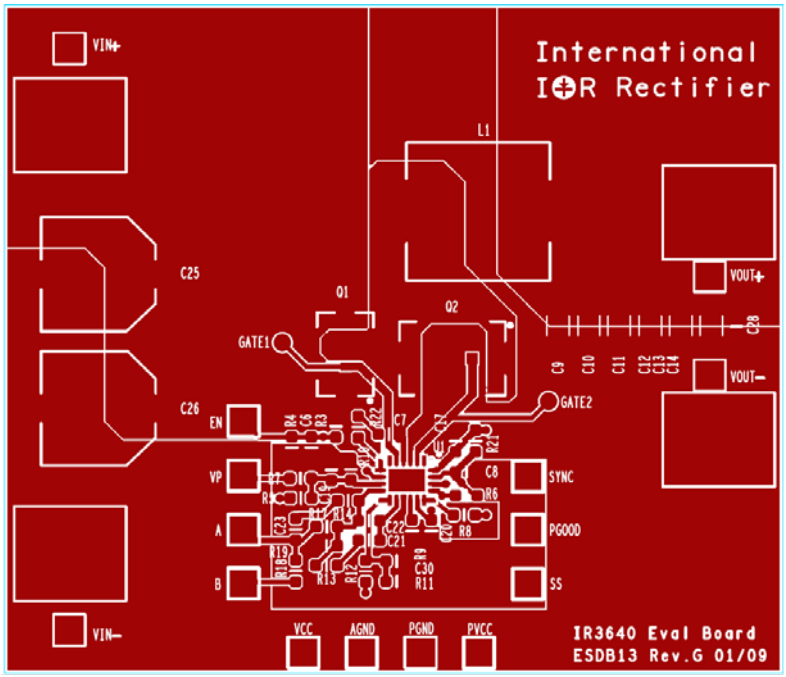


Fig. 2: Board layout, top layer

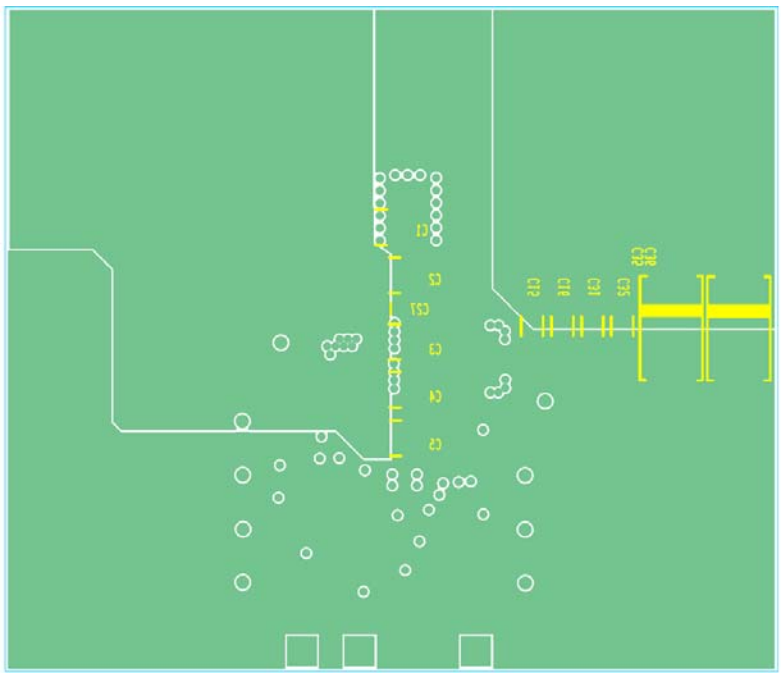
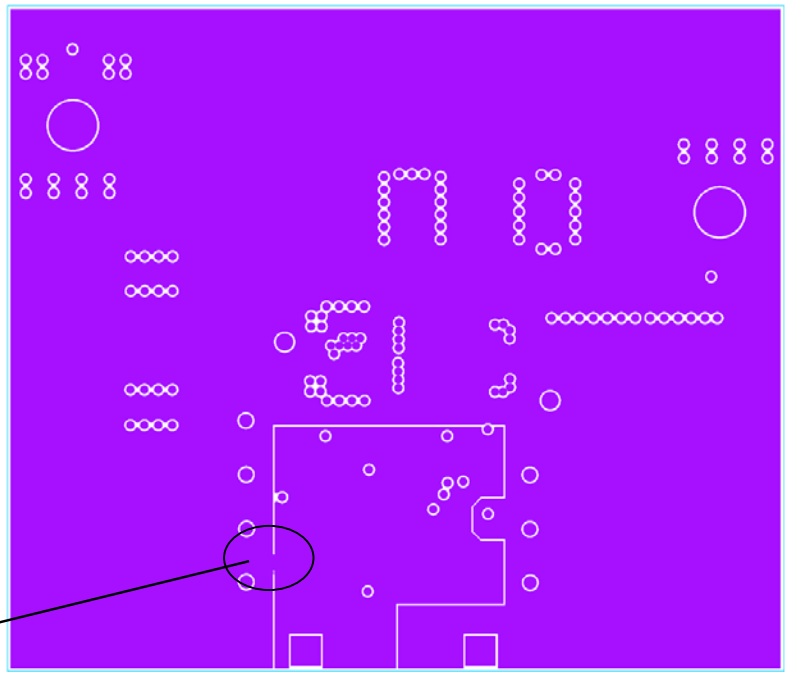


Fig. 3: Board layout, bottom layer



Single point connection between AGND and PGND.

Fig. 4: Board layout, mid-layer I

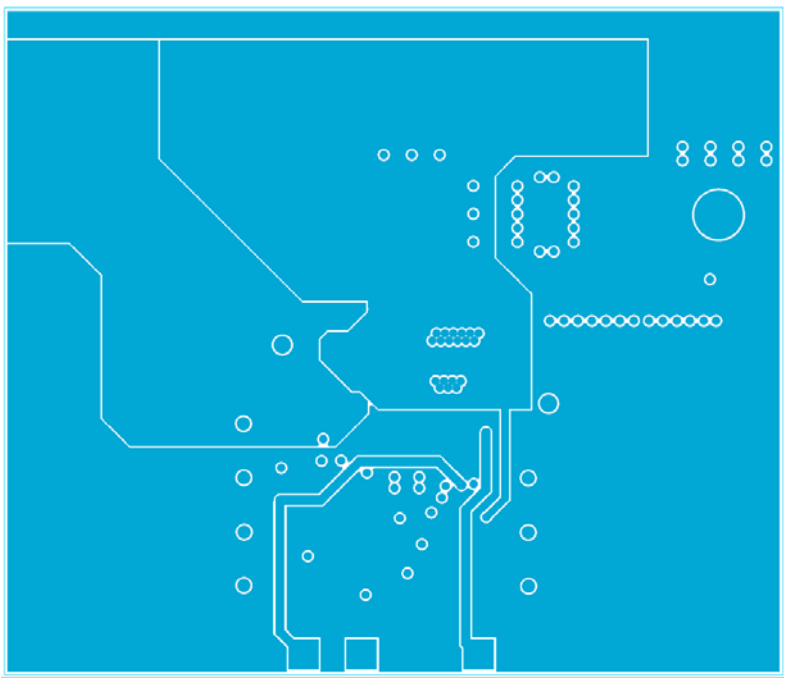


Fig. 5: Board layout, mid-layer II

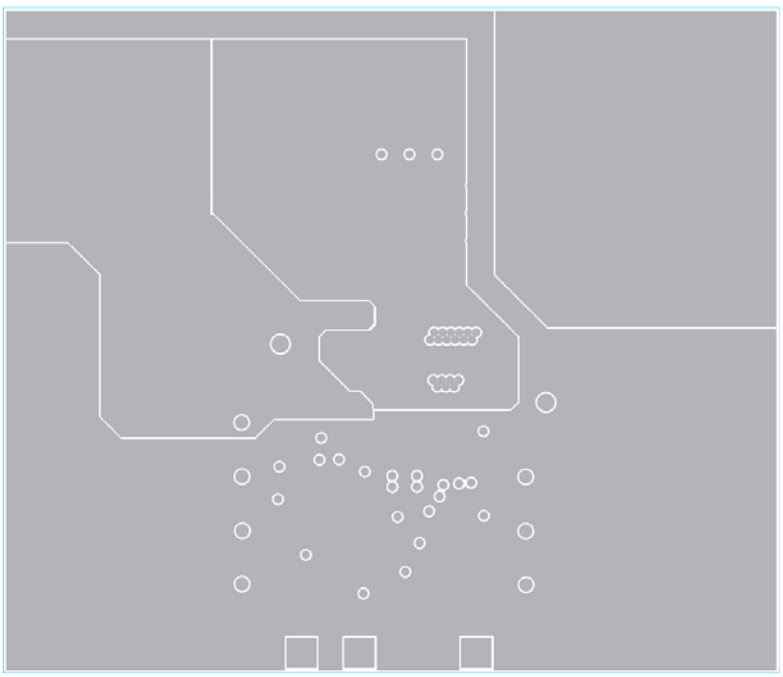


Fig. 6: Board layout, mid-layer III

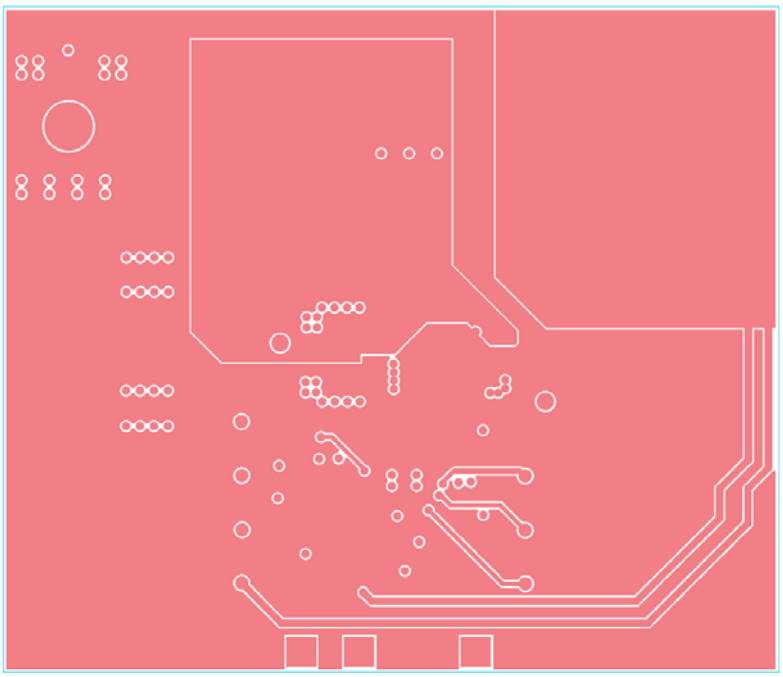


Fig. 7: Board layout, mid-layer IV

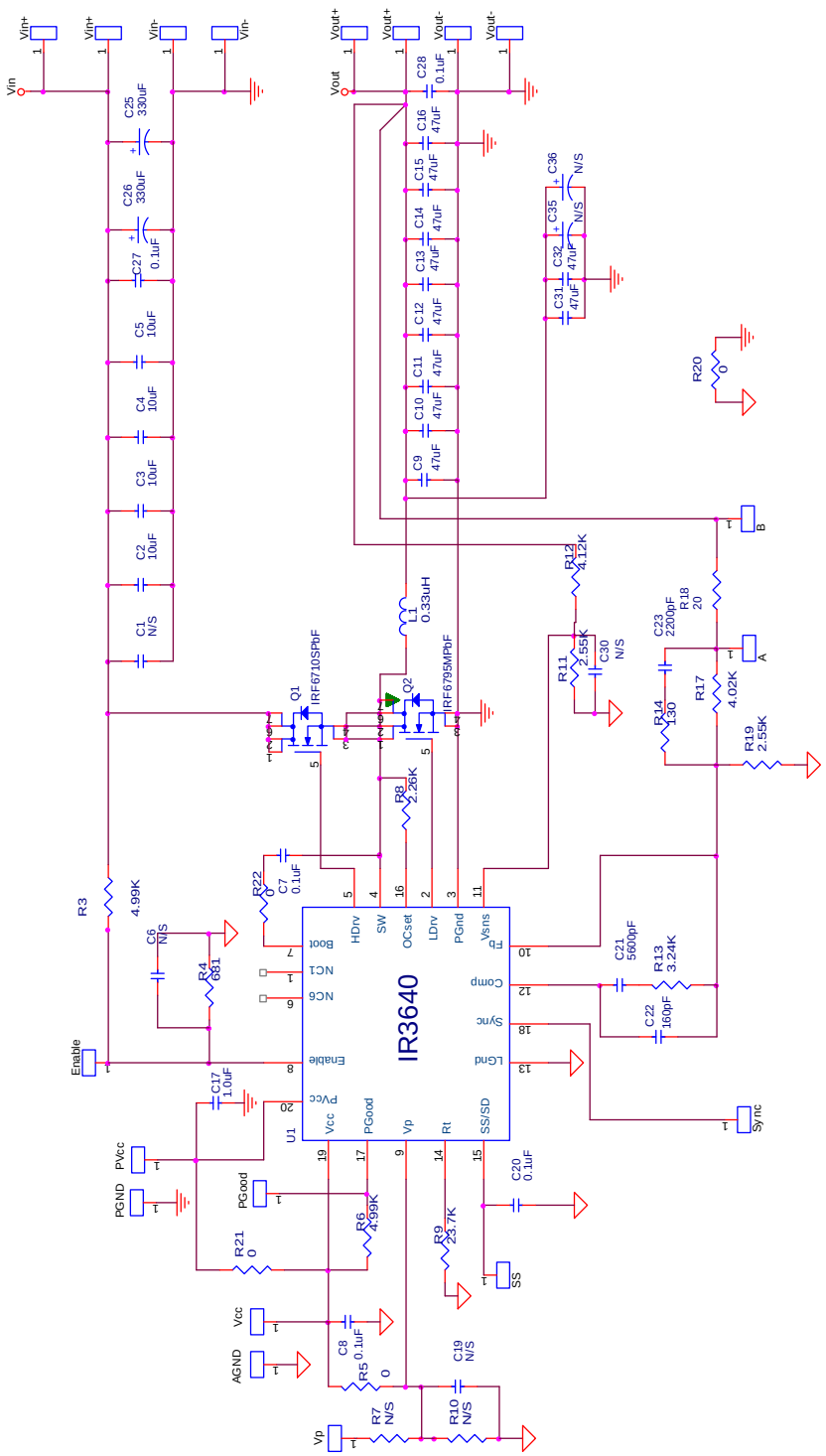


Fig.8: Schematic of the IR3640 evaluation board

Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
1	10	VOUT-,VOUT+,VIN-,VIN+,	0.075" SQ_SMT	SMT 0.075" Test Point		
		Sync,PVcc,PGood,PGND,B,A	_TestPoint			
2	4	C2,C3,C4,C5	10uF	Ceramic,25V,1210,X5R,10%	Taiyo-Yuden	TMK325BJ106MN-T
3	5	C7,C8,C20,C27,C28	0.1uF	Ceramic,50V,0603,X7R,10%	Panasonic	ECJ-1VB1H104K
4	10	C9,C10,C11,C12,C13,	47uF	Ceramic,4V,0805,X5R,10%	Murata Electronics	GRM21BR60G476ME15L
		C14,C15,C16,C31,C32				
5	1	C17	1.0uF	Ceramic,25V,0603,X5R,10%	Murata Electronics	GRM188R61E105KA12D
6	1	C21	5.6nF	Ceramic,25V,0603,C0G,5%	Panasonic-ECG	C1608C0G1E562J
7	1	C22	160pF	Ceramic,50V,0603,C0G,5%	Murata Electronics	GRM1885C1H161JA01D
8	1	C23	2200pF	Ceramic,50V,0603,C0G,5%	TDK Corporation	C1608C0G1H222J
9	2	C25,C26	330uF	SMD Elecrolytic, 25V,F-size,20%	Panasonic	EEE-FK1E331P
10	1	L1	0.33uH	SMT-Inductor,1.5mOhms,10x11mm,20%	Delta	MPL104-R33IR
11	1	Q1	IRF6710S2TRPbF	IRF6710 SQ 25V	International Rectifier	IRF6710S2TRPbF
12	1	Q2	IRF6795MPbF	IRF6795 MX 25V	International Rectifier	IRF6795MPbF
13	3	R5,R21,R22	0	Thick-film,0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
14	2	R3,R6	4.99K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX4991
15	1	R4	681	Thick-film,0603,1/10 W,1%	Vishey/Dale	CRCW0603681RFKEA
16	1	R8	2.26K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX2261
17	1	R9	23.7K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX2372
18	2	R11,R19	2.55K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX2551
19	1	R12	4.12K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX4121
20	1	R13	3.24K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX3241
21	1	R14	130	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX1300
22	1	R17	4.02K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX4021
23	1	R18	20	Thick-film,0603,1/10 W,1%	Vishey/Dale	CRCW060320R0FKEA
24	4	TP11,TP12,TP13,TP14	Label TP	0.250" x 0.300" test pad area		
25	1	U1	IR3640	IR3640,Controller,MLPQ,3x4mm	International Rectifier	IR3640

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0- 25A, Room Temperature, No Air Flow

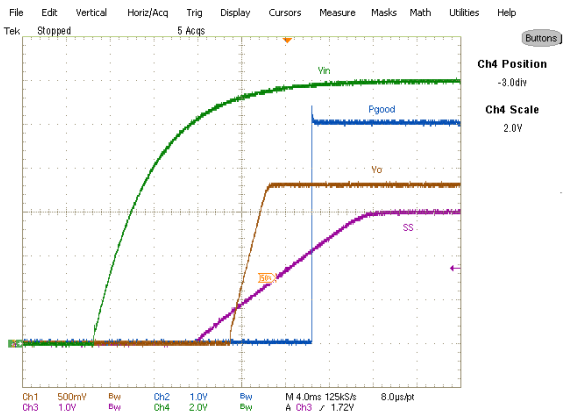


Fig. 9: Start up at 0A Load (Note 1)
Ch_1:V_o, Ch_2:PGood Ch_3:V_{SS} Ch_4: V_{in}

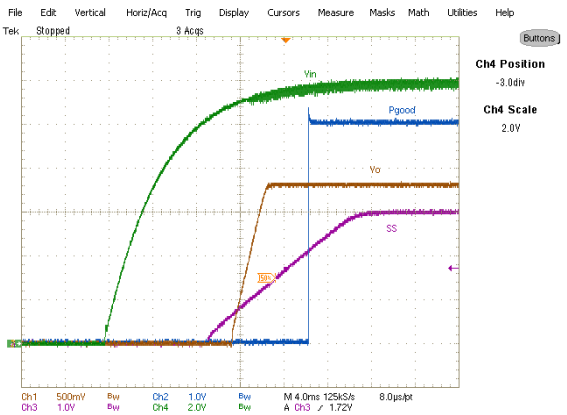


Fig. 10: Start up at 25A Load (Note 1)
Ch_1:V_o, Ch_2:PGood Ch_3:V_{SS} Ch_4: V_{in}

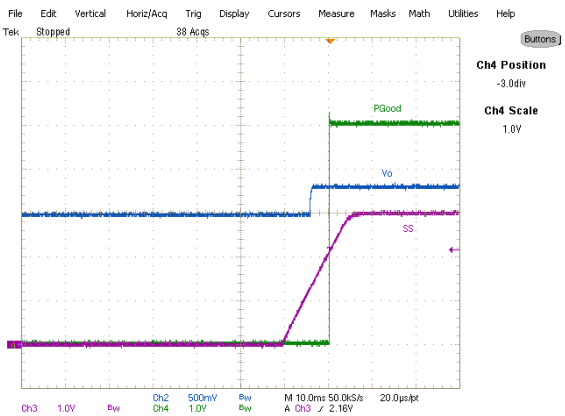


Fig. 11: Start up with 1.5V Prebias,
0A Load, Ch_2:V_{out} Ch_3:V_{SS} Ch_4: PGood

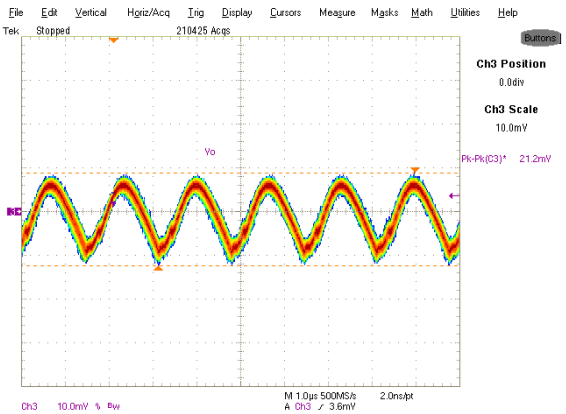


Fig. 12: Output Voltage Ripple, 25A load
Ch_3: V_{out}

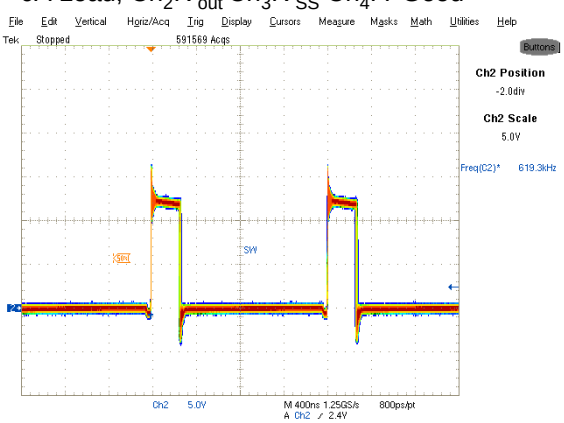


Fig. 13: Inductor node at 25A load
Ch_2:SW

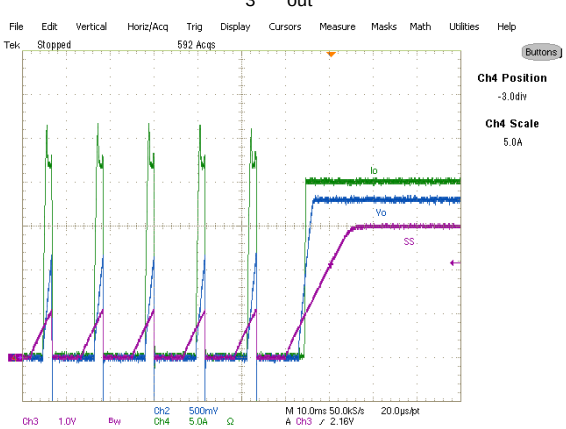


Fig. 14: Short (Hiccup) Recovery
Ch_2:V_{out}, Ch_3:V_{SS} , Ch_4:Io

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Room Temperature, No Air Flow

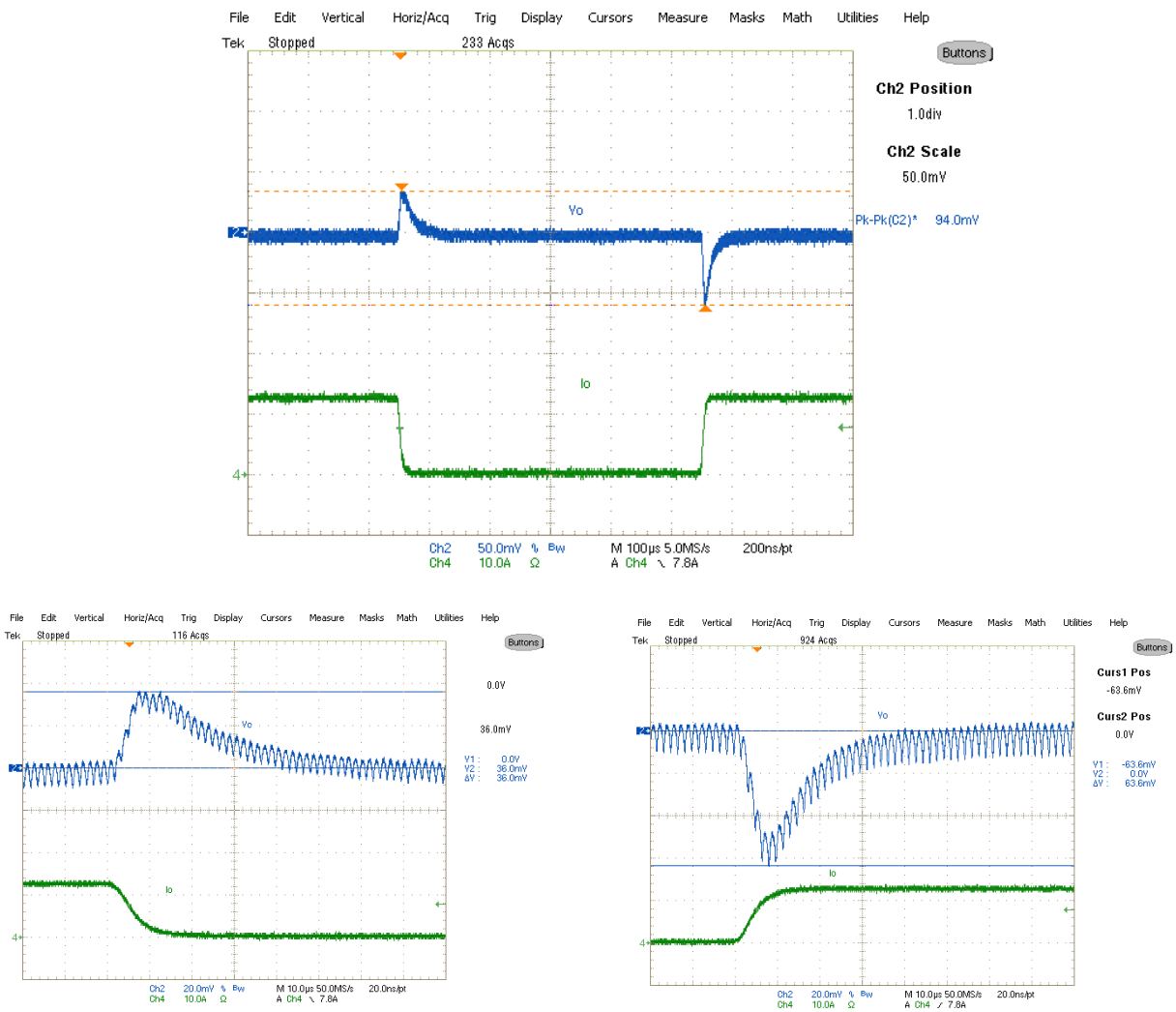


Fig. 15: Transient Response
0A-12.5A load Ch_2:V_{out}, Ch_4:I_o

Note1: Enable is tied to Vin via a resistor divider and triggered when Vin is exceeding above 10V.

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0-25A, Room Temperature, No Air Flow

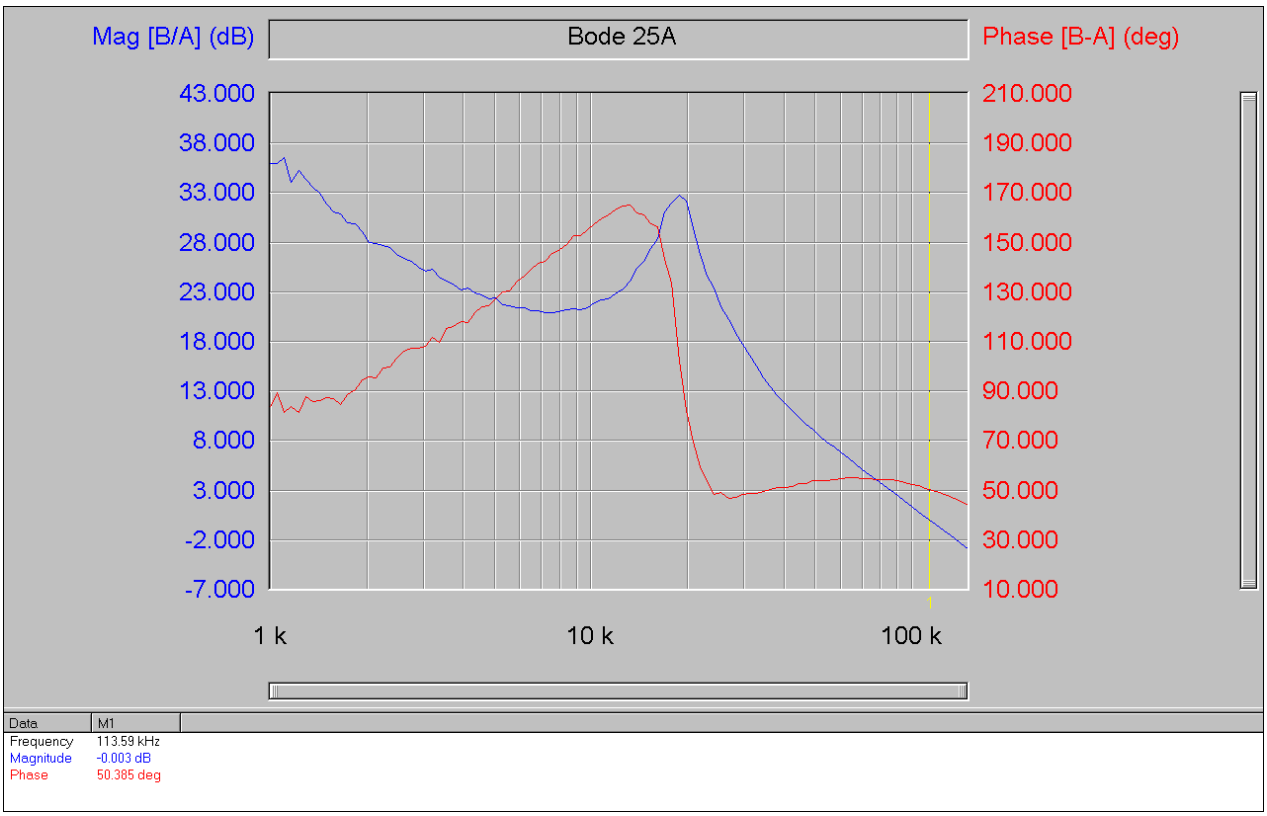
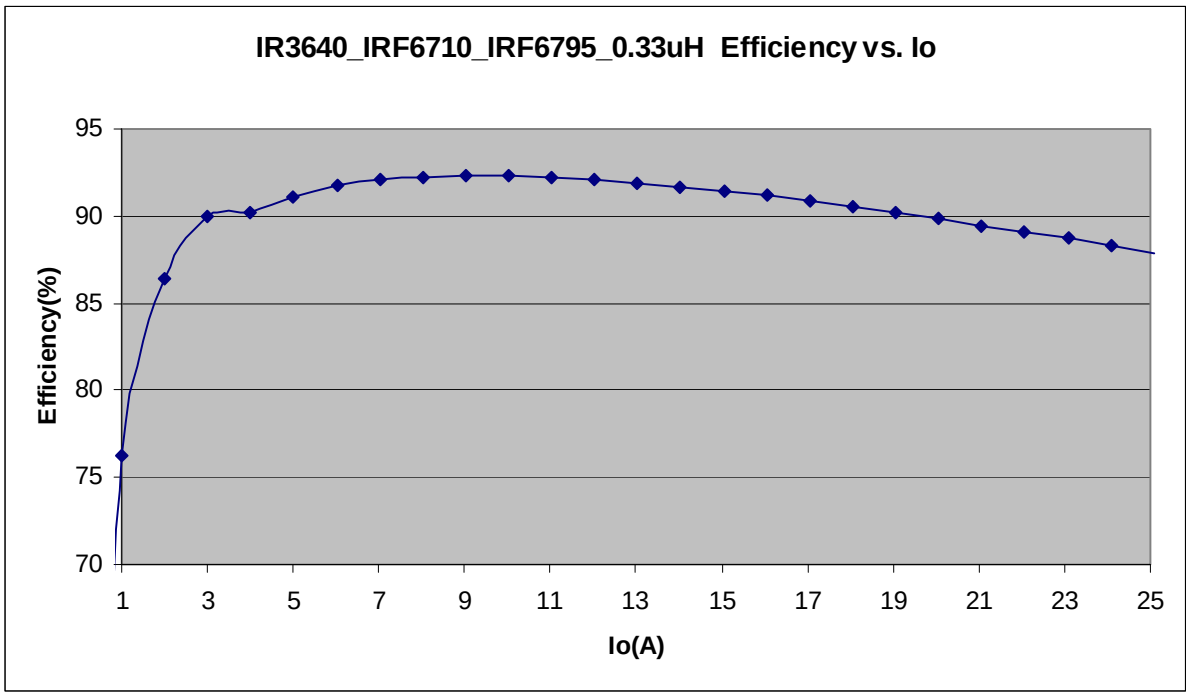


Fig.16: Bode Plot at 25A load shows a bandwidth of 113.6kHz and phase margin of 50.4 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=1.8V, Io=0-25A, Room Temperature, No Air Flow



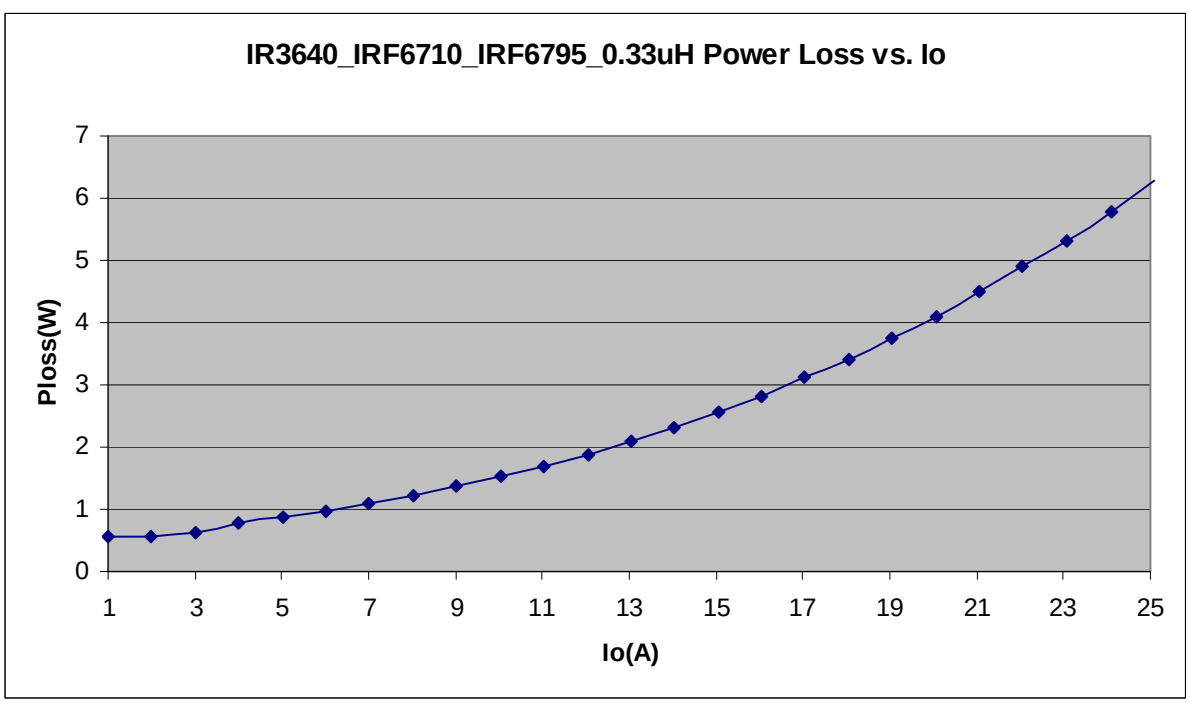


Fig.17: Efficiency and power loss vs. load current

THERMAL IMAGES
Vin=12V, Vo=1.8V, Io=25A, Room Temperature, No Air Flow

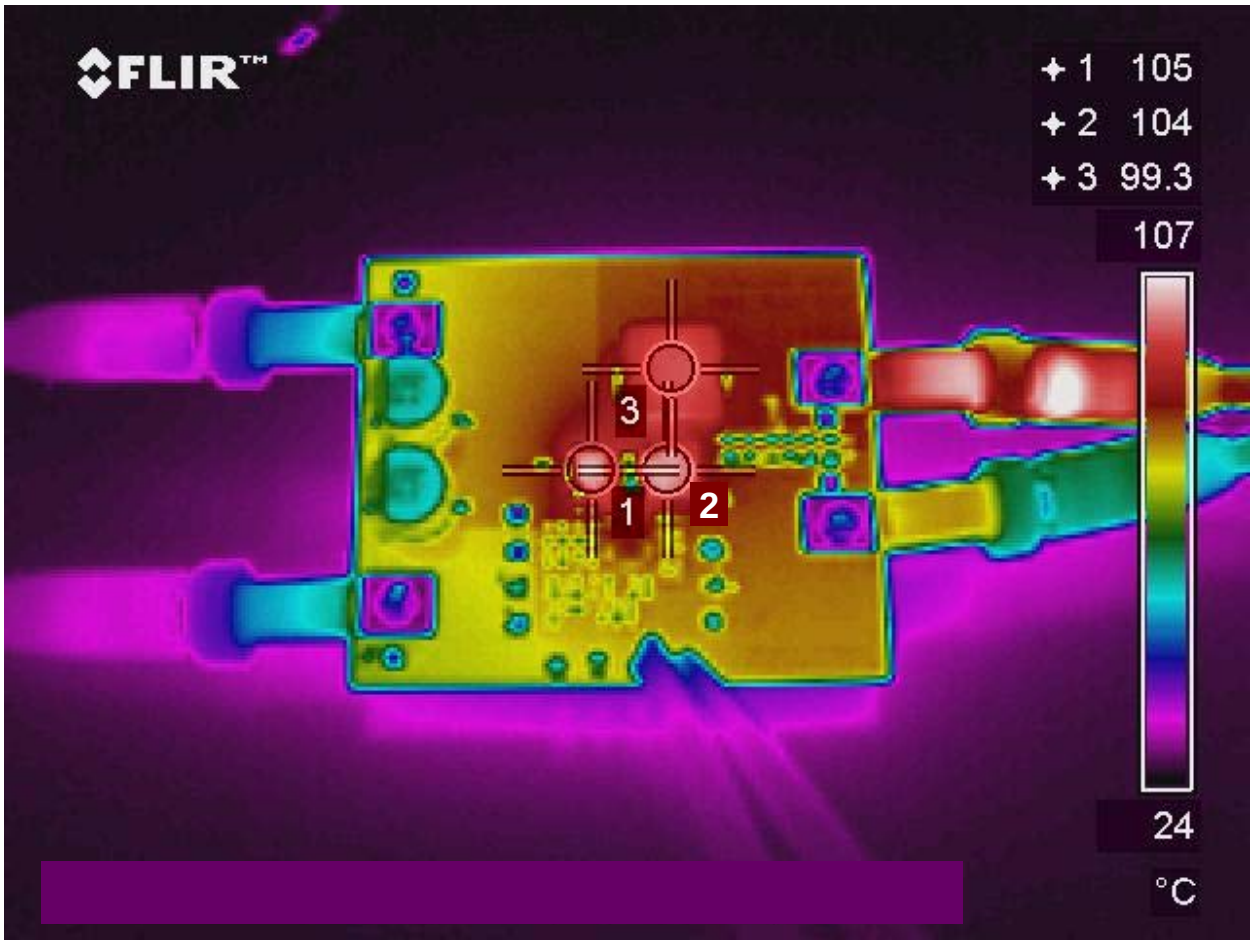


Fig.18: Thermal Image at 25A load
Test Point 1: Ctrl FET IRF6710, Test Point 2: Sync FET IRF6795
Test Point 3: Inductor

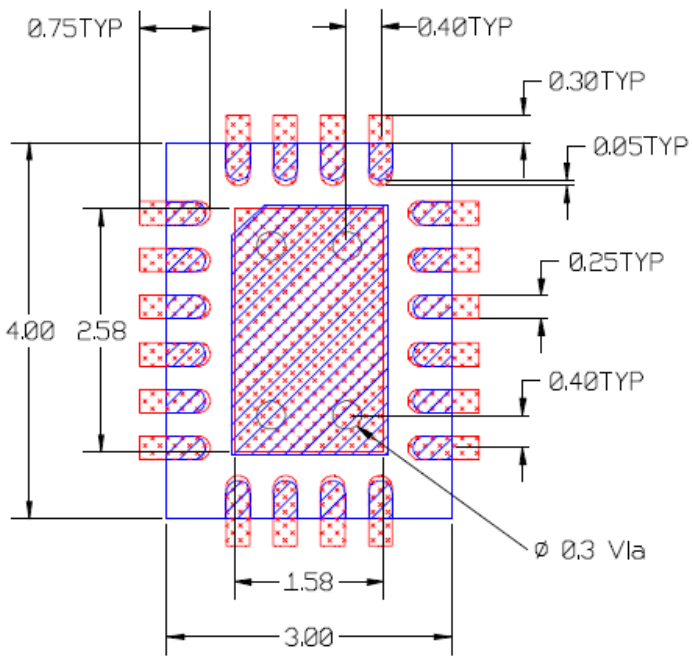
PCB Metal and Components Placement

Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ⩾ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension +0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.

Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ⩾ 0.17mm for 2 oz. Copper (⩾ 0.1mm for 1 oz. Copper and ⩾ 0.23mm for 3 oz. Copper).

Four 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



All Dimensions In mm

PCB Copper

Component

Solder Resist

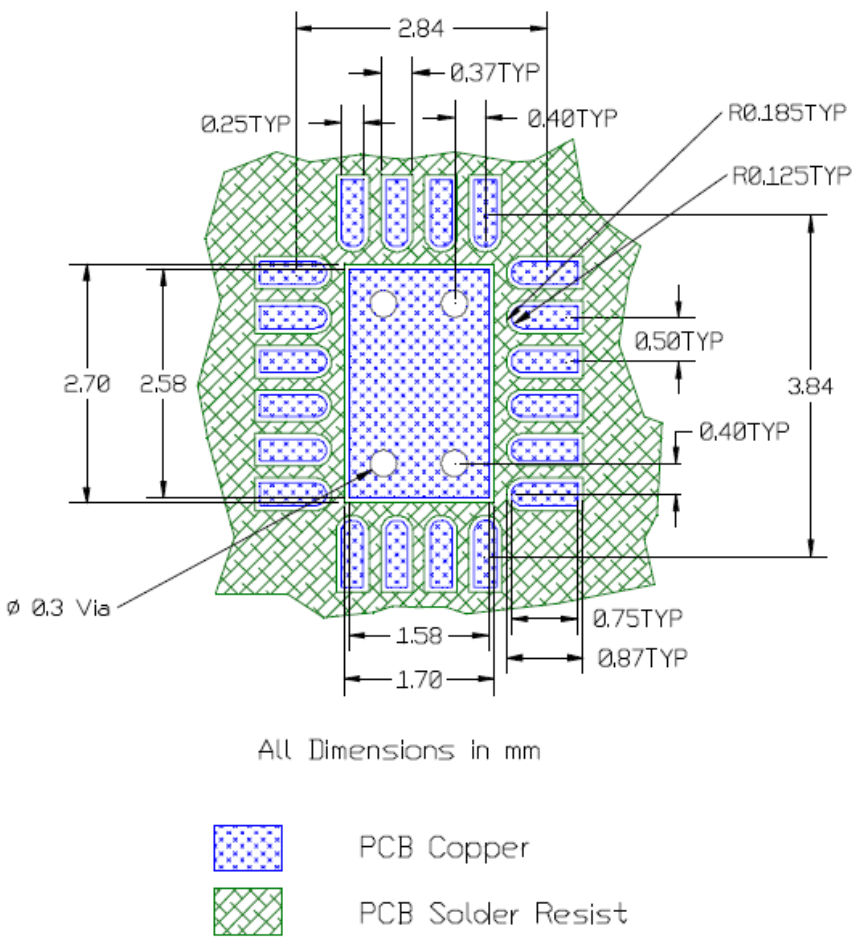
The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.

The minimum solder resist width is 0.13mm. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of $\geqslant$ 0.17mm remains.

The land pad should be Non Solder Mask Defined (NSMD), with a minimum pullback of the solder resist off the copper of 0.06mm to accommodate solder resist mis-alignment.

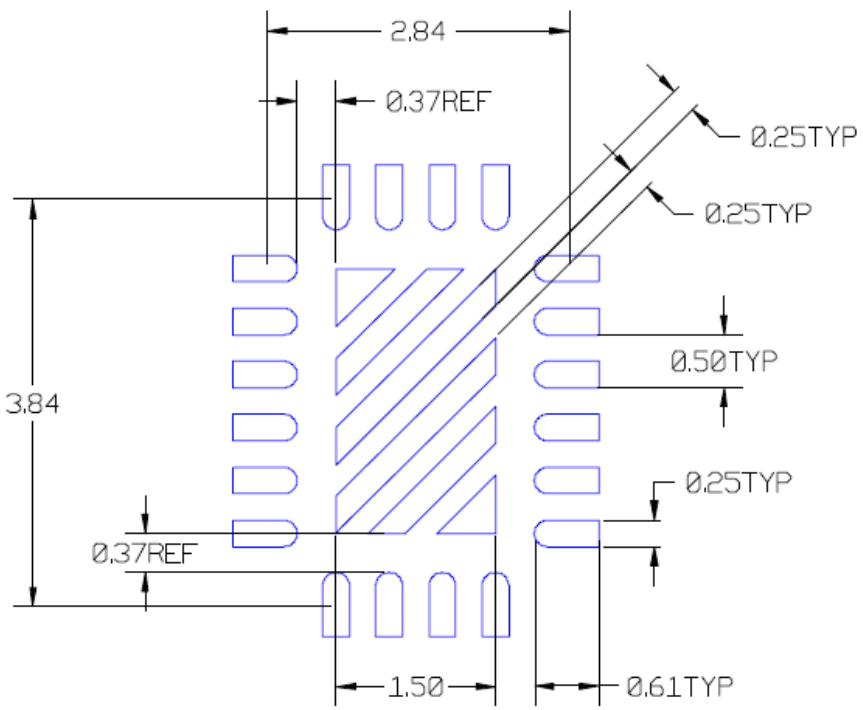
Ensure that the solder resist in-between the lead lands and the pad land is $\geqslant$ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

Each via in the land pad should be tented or plugged from bottom boardside with solder resist.



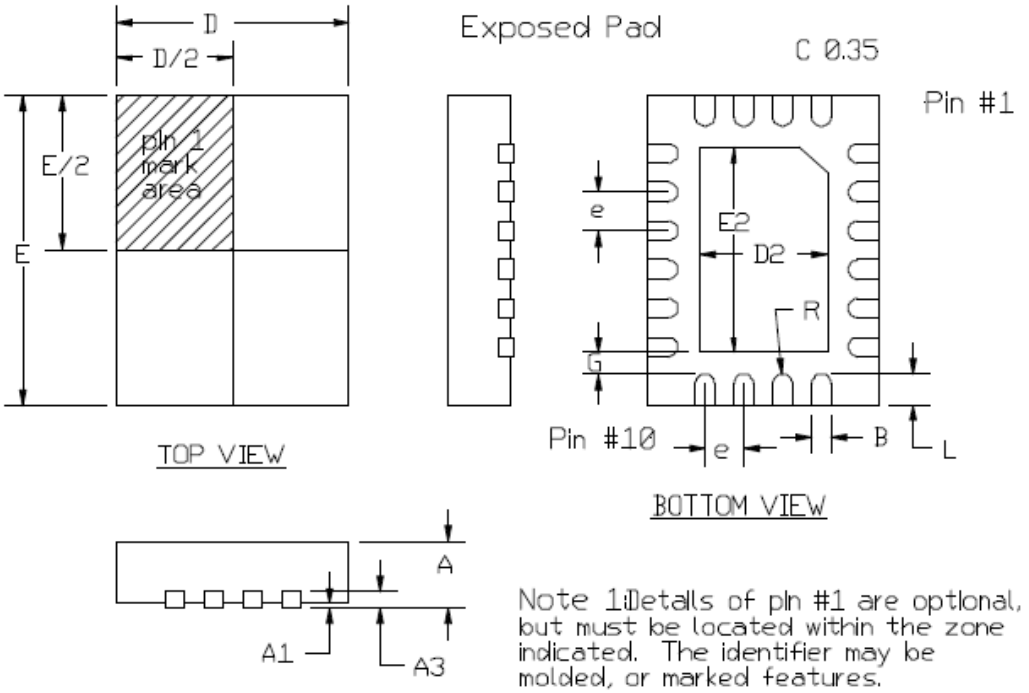
Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mmpitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture

All Dimensions in mm



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

20L 3x4 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
e	0.5 REF		
G	0.275 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

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