SupIRBuck™

8A HIGHLY INTEGRATED
WIDE-INPUT VOLTAGE, SYNCHRONOUS BUCK REGULATOR

Features

- Input Voltage Range: 3V to 26V
- Output Voltage Range: 0.5V to 12V
- Continuous 8A Load Capability
- Constant On-Time control
- Excellent Efficiency at very low output current levels
- Compensation Loop not required
- Programmable switching frequency, soft start, and over current protection
- Power Good Output
- Precision Voltage Reference (0.5V, +/-1%)
- Pre-bias Start Up
- Under/Over Voltage Fault Protection
- Ultra small, low profile 5 x 6mm QFN Package

Applications

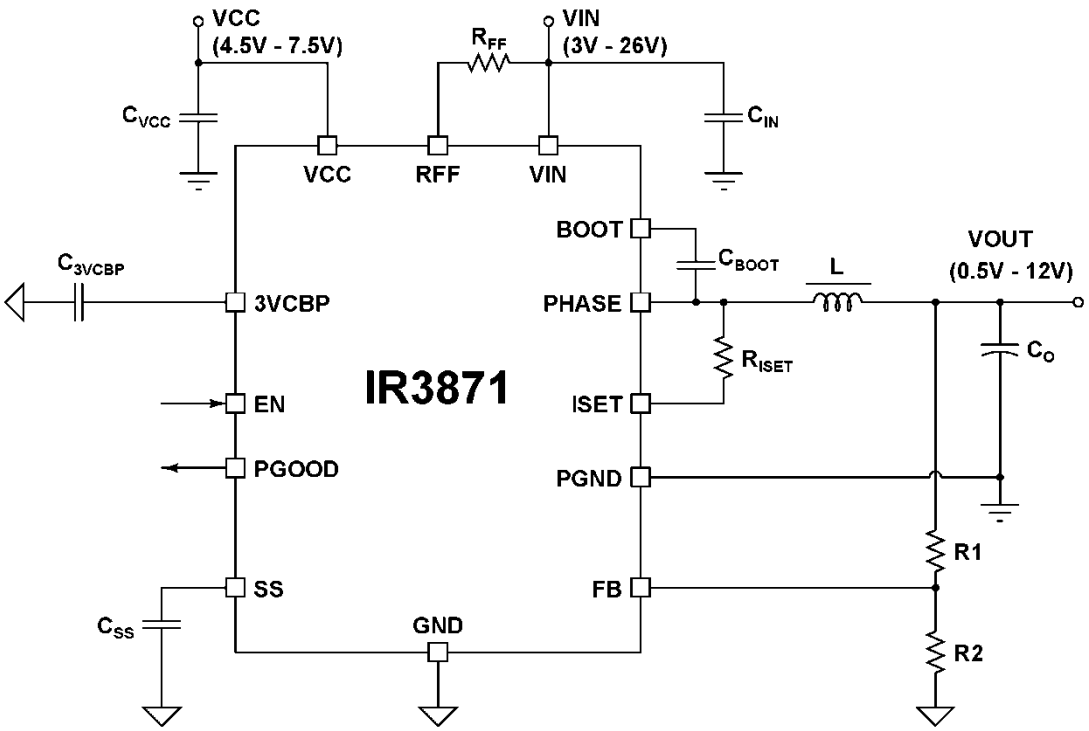
- Notebook and desktop computers
- Game consoles
- Consumer electronics – STB, LCD, TV, printers
- General purpose POL DC-DC converters

Description

The IR3871 ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC voltage regulator. The onboard constant on time hysteretic controller and MOSFETs make IR3871 a space-efficient solution that delivers up to 8A of precisely controlled output voltage in 60° C ambient temperature applications without airflow.

Programmable switching frequency, soft start, and over current protection allows for a very flexible solution suitable for many different applications and an ideal choice for battery powered applications.

Additional features include pre-bias startup, very precise 0.5V reference, over/under voltage shut down, power good output, and enable input with voltage monitoring capability.



ABSOLUTE MAXIMUM RATINGS

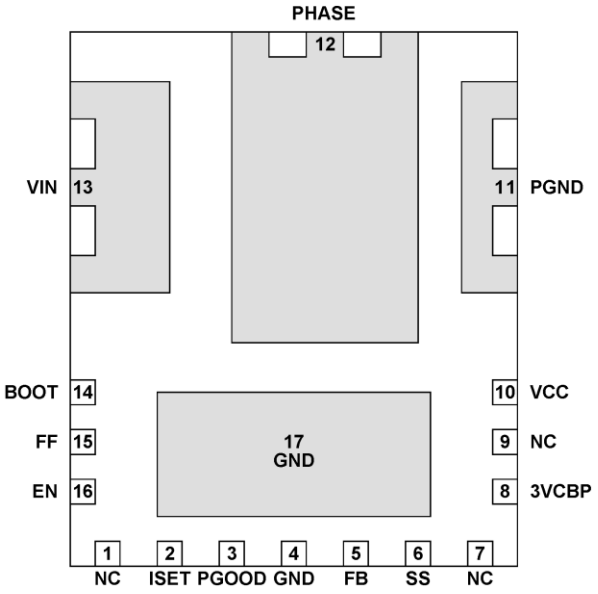
(Voltages referenced to GND unless otherwise specified)

- VIN. FF …….……. -0.3V to 30V
- VCC, PGood, EN ……...……..…… -0.3V to 8.0V
- Boot ……..……..…..…. -0.3V to 40V
- PHASE ……..... -0.3V to 30V(DC), -5V(100ns)
- Boot to PHASE …..……..….. -0.3V to 8V
- ISET ……..…..…… -0.3V to 30V
- PGND to GND ……...……..…….. -0.3V to +0.3V
- All other pins ……...…….…….. -0.3V to 3.9V
- Storage Temperature Range ..... -65°C To 150°C
- Junction Temperature Range ..... -40°C To 150°C
- ESD Classification …….…… JEDEC Class 1C
- Moisture sensitivity level ……..……..…. JEDEC Level 2 @ 260°C (Note 2)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PACKAGE INFORMATION

5mm x 6mm POWER QFN



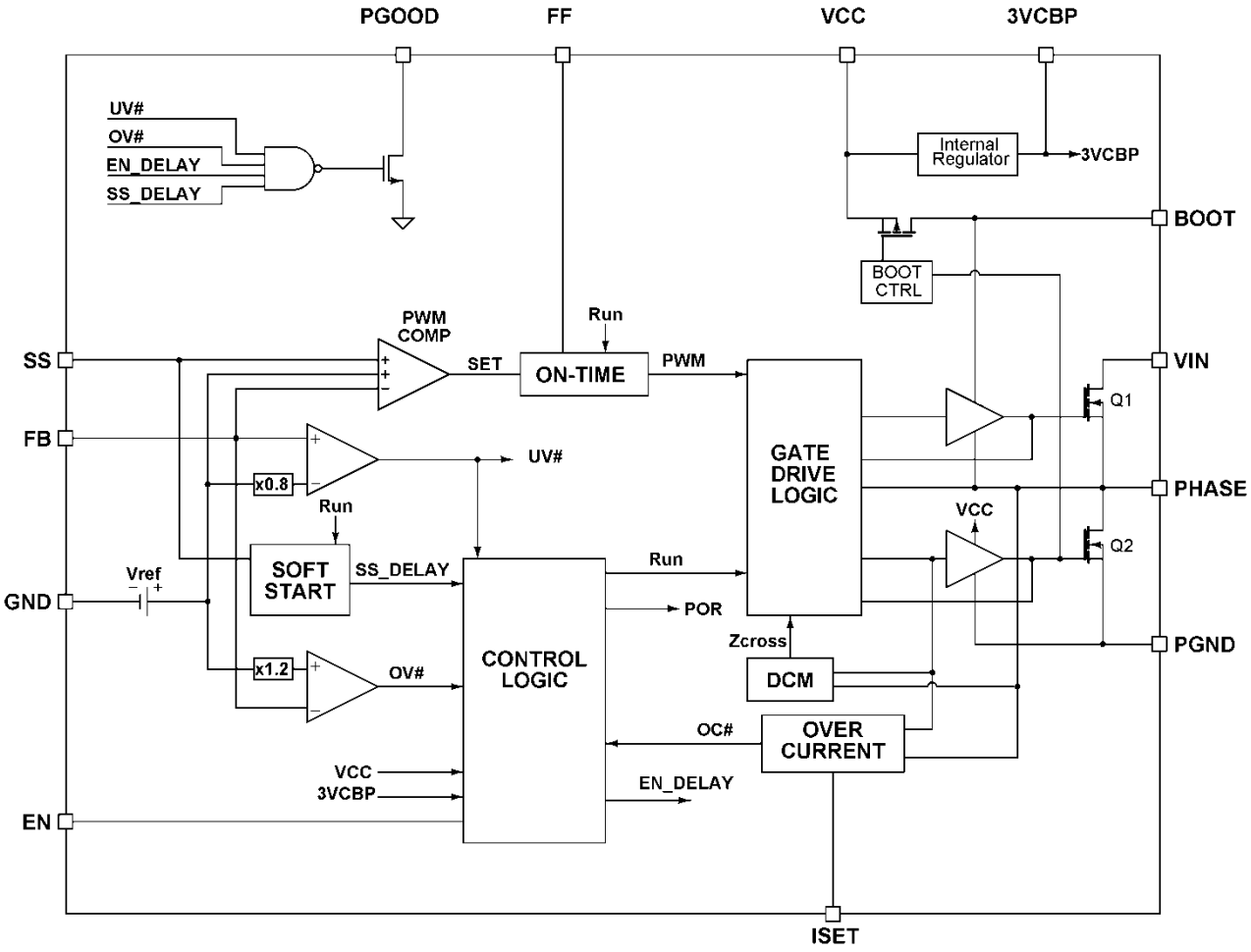
$$\theta_{JA} = 35^{o}C/W$$

$$\theta_{J\text{-}PCB} = 2^{o}C/W$$

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3871MTRPbF	17	4000
M	IR3871MTR1PbF	17	750

Simplified Block Diagram



Pin Description

NAME	NUMBER	I/O LEVEL	DESCRIPTION
NC	1	-----	No connection.
ISET	2		Connecting resistor to PHASE pin sets over current trip point.
PGOOD	3	5V	Power good open drain output – pull up with a resistor to 3.3V.
GND	4,17	Reference	Bias return and signal reference.
FB	5	3.3V	Inverting input to PWM comparator, OVP / PGood sense.
SS	6	3.3V	Soft start/shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to GND to set the startup time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
NC	7	-----	No connection.
3VCBP	8	3.3V	LDO output. A minimum of 1.0 µF ceramic capacitor is required from 3VCBP to GND.
NC	9	-----	No connection.
VCC	10	5V	Gate drive supply. A minimum of 1.0µF ceramic capacitor must be connected from this pin to the power return (PGND).
PGND	11	Reference	Power return.
PHASE	12	VIN	Phase node (or switching node) of MOSFET half bridge.
VIN	13	VIN	Input voltage for the system.
BOOT	14	VIN +VCC	Bootstrapped gate drive supply – connect a capacitor to PHASE.
FF	15	VIN	Input voltage feed forward – sets on-time with a resistor to VIN.
EN	16	5V	Enable pin to turn on and off the device. Use two external resistors to set the turn on threshold (see *Electrical Specifications*) for input voltage monitoring.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Unit
VIN	Input Voltage	3	26*	V
VCC	Supply Voltage	4.5	7.5	
V_{OUT}	Output Voltage	0.5	12	
I_{OUT}	Output Current	0	8	A
Fs	Switching Frequency	N/A	1000	kHz
T_J	Junction Temperature	0	125	°C

***** PHASE pin must not exceed 30V.

Electrical Specifications

Unless otherwise specified, these specification apply over VIN = 12V, VCC = 5V, 0°C ≤ T_J ≤ 125°C.

PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLIES						
VCC Turn-on Threshold			3.9	4.2	4.5	V
VCC Turn-off Threshold			3.6	3.9	4.2	V
VCC Threshold Hysteresis				150		mV
VCC Operating Current		R_{FF} = 200K, EN = HIGH, Fs = 300kHz		7.1		mA
VCC Shutdown Current		EN = LOW		35	50	µA
FF Shutdown Current		EN = LOW		2		µA
VIN Shutdown Current		EN = LOW		1		µA
INTERNAL LDO OUTPUT						
LDO Output Voltage Range		C_{3VCBP} = 1µF	3.1	3.3	3.5	V
Output Current					8	mA
CONTROL LOOP						
Reference Accuracy, V_{REF}		V_{REF}	0.495	0.5	0.505	V
On-Time Accuracy		R_{FF} = 180K, T_J = 65°C	280	300	320	ns
Min Off Time	1			400		ns
Soft-Start Current		EN = HIGH	8	10	12	µA
Zero Current Threshold	1	Measure at V_{PHASE}	-5	-2.4	0	mV
FAULT PROTECTION						
ISET Pin Output Current			18	20	22	µA
Under Voltage Threshold		Falling V_{FB} & Monitor PGOOD	0.37	0.4	0.43	V
Under Voltage Hysteresis	1	Rising V_{FB}		10		mV
Over Voltage Threshold		Rising V_{FB} & Monitor PGOOD	0.58	0.62	0.66	V
Over Voltage Hysteresis	1	Falling V_{FB}		10		mV
PGOOD Delay Threshold (V_{SS})				1		V

Electrical Specifications (continued)

Unless otherwise specified, these specification apply over VIN = 12V, VCC = 5V, $0^oC \le T_J \le 125^oC$.

PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
GATE DRIVE						
Dead Time	1	Monitor body diode conduction on PHASE pin	5		30	ns
BOOTSTRAP PFET						
Forward Voltage		I(BOOT) = 10mA	100	200	300	mV
UPPER MOSFET						
Static Drain-to-Source On-Resistance		VCC = 5V, I_D = 7A, $T_J = 25^oC$	14.5	20.8	25.5	mΩ
LOWER MOSFET						
Static Drain-to-Source On-Resistance		VCC = 5V, I_D = 9A, $T_J = 25^oC$	8	10	12.5	mΩ
LOGIC INPUT AND OUTPUT						
EN High Logic Level			2	-	-	V
EN Low Logic Level			-	-	0.6	V
EN Input Current		EN = 3.3V		11		µA
PGOOD Pull Down Resistance				25	50	Ω

Note 1: Guaranteed by design, not tested in production

Note 2: Upgrade to industrial/MSL2 level applies from date codes 1227 (marking explained on application note AN1132 page 2). Products with prior date code of 1227 are qualified with MSL3 for Consumer Market.

TYPICAL OPERATING DATA

Tested with demoboard shown in Figure 7, VIN = 12V, VCC = 5V, Vout = 1.05V, Fs = 300kHz, TA = 25ºC, no airflow, unless otherwise specified

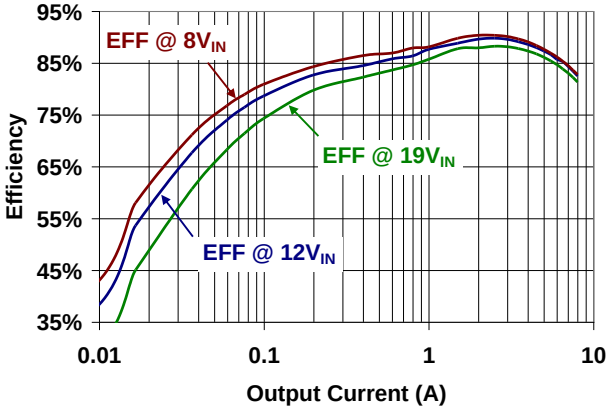


Figure 1. Efficiency vs. Output Current for V_{OUT} = 1.05V

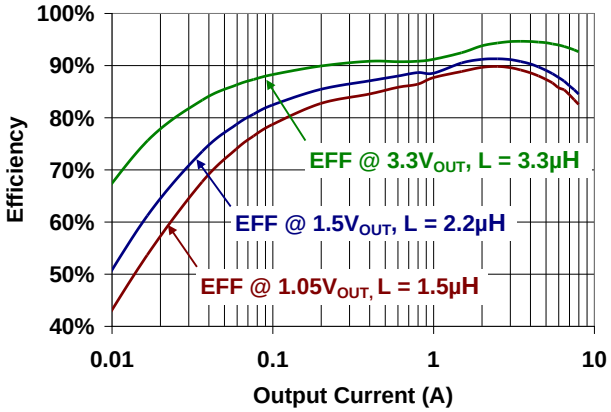


Figure 2. Efficiency vs. Output Current for VIN = 12V

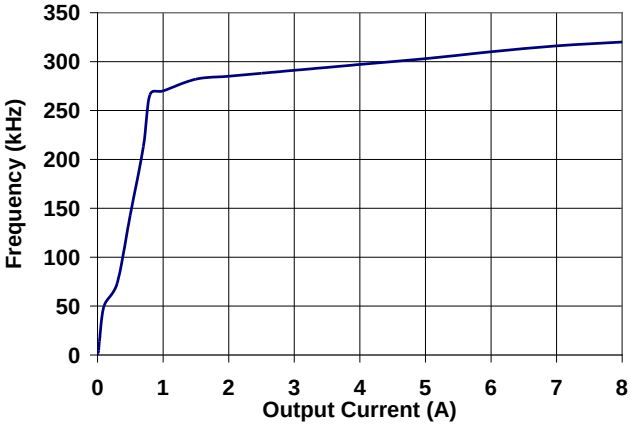


Figure 3. Switching Frequency vs. Output Current

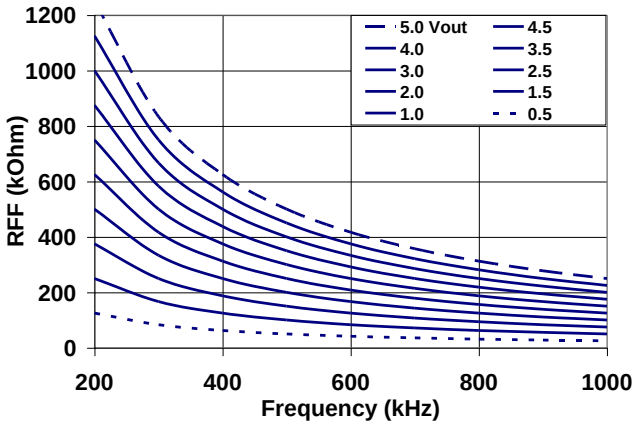


Figure 4. Frequency vs. R_{FF}

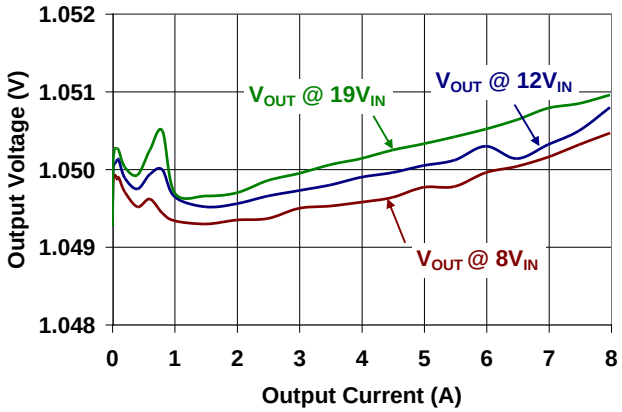


Figure 5. Output Voltage Regulation vs. Output Current

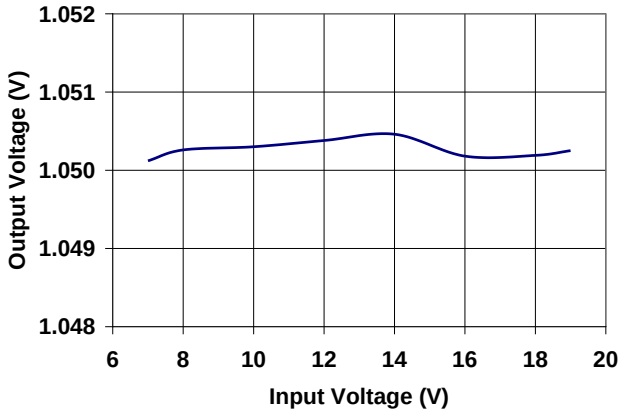


Figure 6. Output Voltage Regulation vs. Input Voltage at I_{OUT} = 8A

TYPICAL APPLICATION CIRCUIT

Demoboard Schematic: VOUT = 1.05V, Fs = 300kHz

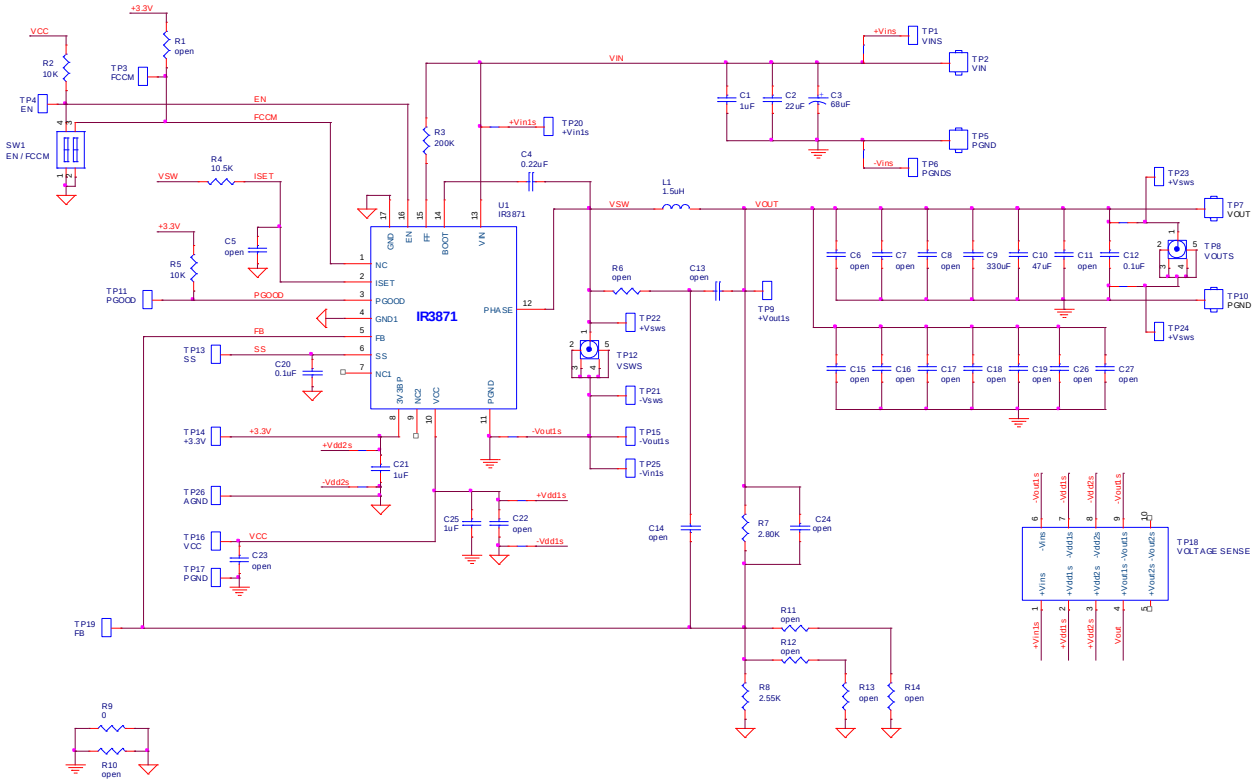


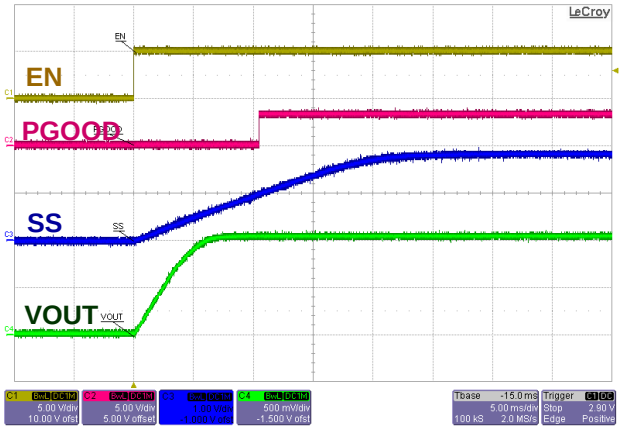
Figure 7. Typical Application Circuit for V_{OUT} = 1.05V, Fs = 300kHz

Demoboard Bill of Materials

Quantity	Reference	Value	Description	Manufacturer	Part-Number
1	C4	0.22uF	CAP,CER,0.22uF,50V,10%,X7R,0603	Murata Electronics	GRM188R71H224KA64D
3	C1, C21, C25	1uF	CAP,CER,1.0uF,25V,X7R,0603	Murata Electronics	GRM188R71E105KA12D
1	C2	22uF	CAP,22uF,25V,CERAMIC,X5R,1210	Panasonic	ECJ-4YB1E226M
1	C3	68uF	CAP,68uF,25V,ELECT,FK,SMD	Panasonic	EEV-FK1E680P
1	C9	330uF	POSCAP, 330uF, 2.5V, SMD	Sanyo	2R5TPE330M9
1	C10	47uF	CAP,CER,47uF,6.3V,X5R,0805	TDK	C2012X5R0J476M
2	C12, C20	0.1uF	CAP,CER,0.1uF,50V,10%,X7R,0603	TDK	C1608X7R1H104K
1	L1	1.5uH	INDUCTOR, 1.5uH, 11A, 6.7mOhm,SMD	CYNTEC	PCMB065T-1R5MS
2	R2, R5	10K	RES,10.0K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW060310K0FKEA
1	R9	0	RES,0.0,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06030000Z0EAHP
1	R3	200K	RES,200K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW0603200KFKEA
1	R4	10.5K	RES,10.5K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW060310K5FKEA
1	R7	2.8K	RES,2.8K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06032K80FKEA
1	R8	2.55K	RES,2.55K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06032K55FKEA
1	SW1	SPST	SWITCH, DIP, SPST, SMT	C&K Components	SD02H0SK
1	U1	IR3871	5mm x 6mm QFN	IR	IR3871MPBF

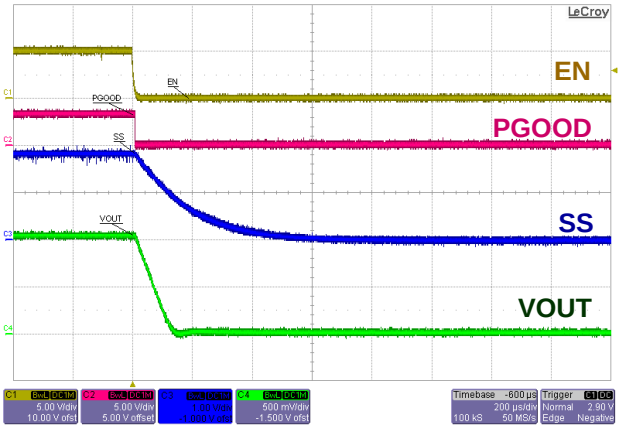
TYPICAL OPERATING DATA

Tested with demoboard shown in Figure 7, VIN = 12V, VCC = 5V, Vout = 1.05V, Fs = 300kHz, T_A = 25ºC, no airflow, unless otherwise specified



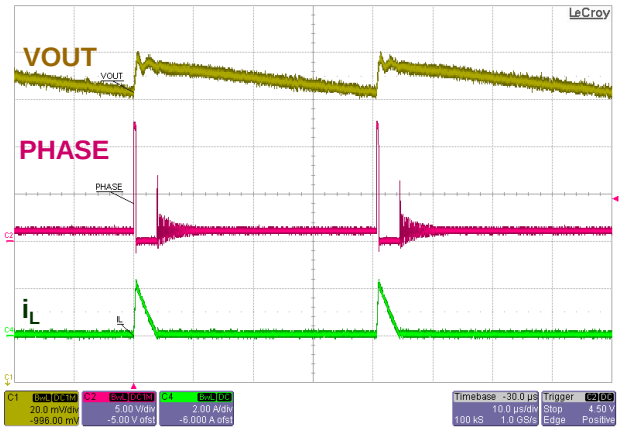
5V/div 5V/div 1V/div 500mV/div 5ms/div

Figure 8: Startup



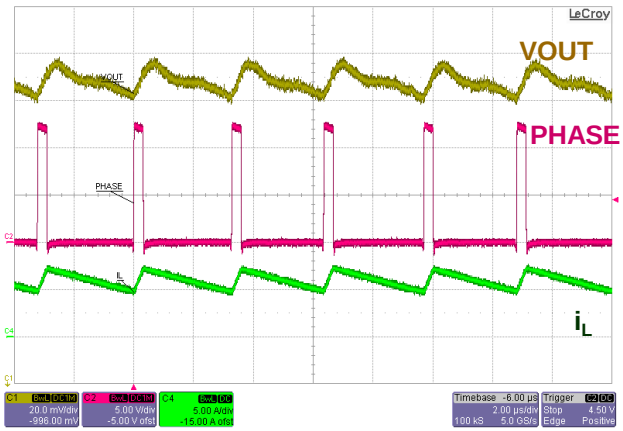
5V/div 5V/div 1V/div 500mV/div 200µs/div

Figure 9: Shutdown



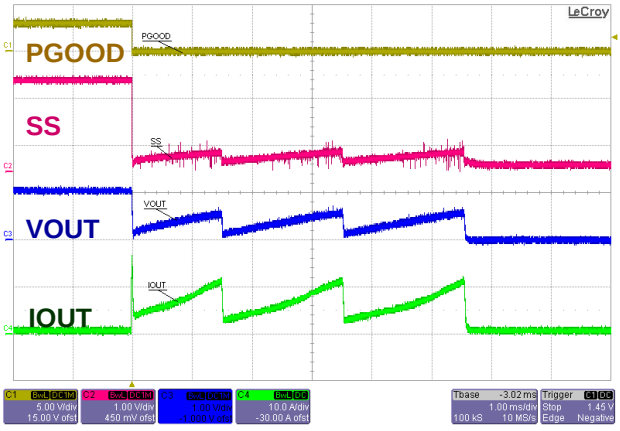
20mV/div 5V/div 2A/div 10µs/div

Figure 10: DCM (I_{OUT} = 0.1A)



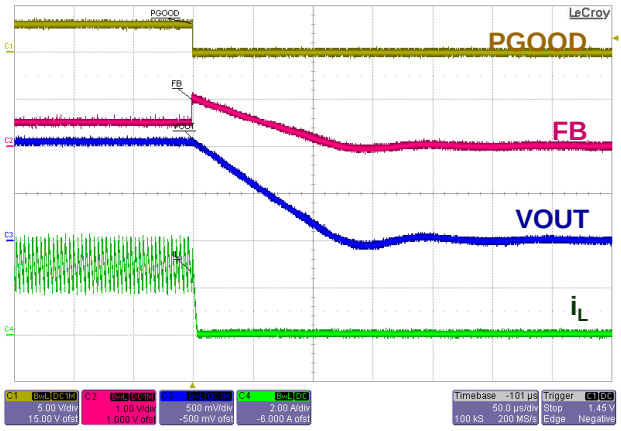
20mV/div 5V/div 5A/div 2µs/div

Figure 11: CCM (I_{OUT} = 6A)



5V/div 1V/div 1V/div 10A/div 1ms/div

Figure 12: Over Current Protection (tested by shorting VOUT to PGND)



5V/div 1V/div 500mV/div 2A/div 50µs/div

Figure 13: Over Voltage Protection (tested by shorting FB to V_{OUT})

TYPICAL OPERATING DATA

Tested with demoboard shown in Figure 7, VIN = 12V, VCC = 5V, Vout = 1.05V, Fs = 300kHz, T_A = 25ºC, no airflow, unless otherwise specified

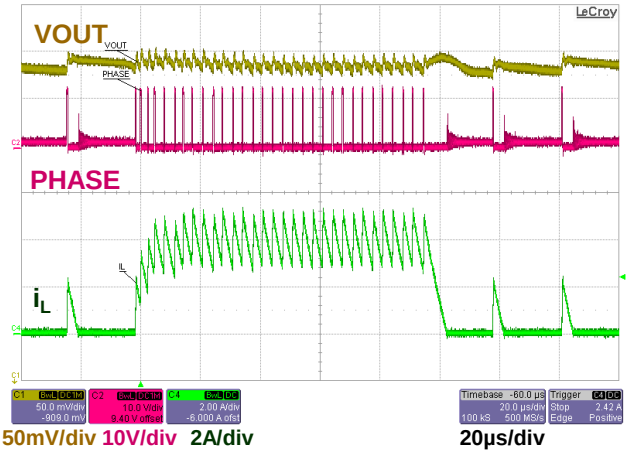


Figure 14: Load Transient 0-4A

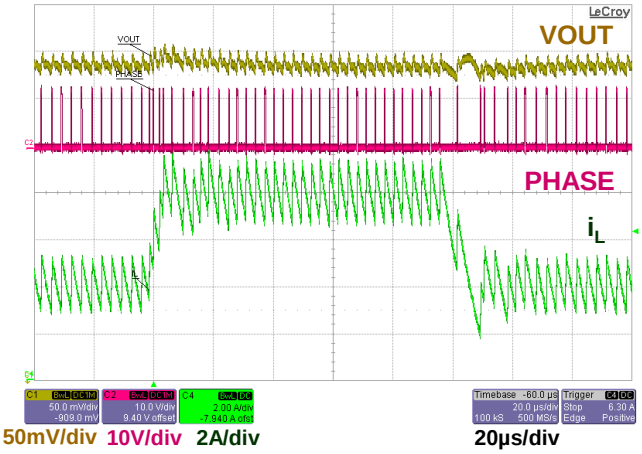


Figure 15: Load Transient 4-8A

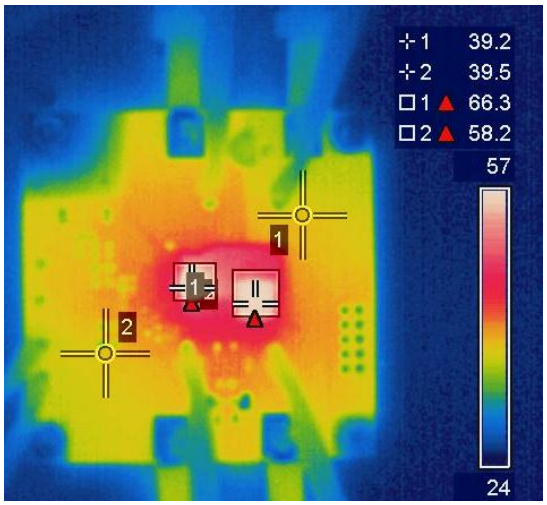


Figure 16: Thermal Image at VIN = 12V, I_{OUT} = 8A (IR3871: 66ºC, Inductor: 58ºC, PCB: 40ºC)

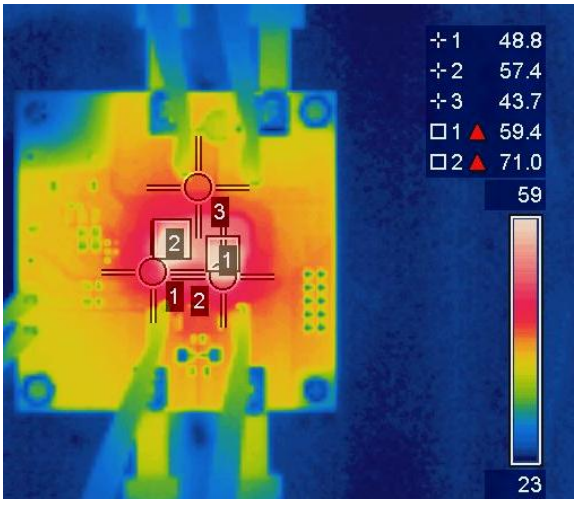


Figure 17: Thermal Image at VIN = 19V, I_{OUT} = 8A (IR3871: 71ºC, Inductor: 59ºC, PCB: 44ºC)

CIRCUIT DESCRIPTION

PWM COMPARATOR

The PWM comparator initiates a SET signal (PWM pulse) when the FB pin falls below the reference (Vref) or the soft start (SS) voltage.

ON-TIME GENERATOR

The PWM on-time duration is programmed with an external resistor (R_{FF}) from the input supply (VIN) to the FF pin. The simplified calculation for R_{FF} is shown in equation 1. The FF pin is held to an internal reference after EN goes HIGH. A copy of the current in R_{FF} charges a timing capacitor, which sets the on-time duration, as shown in equation 2.

$$R_{FF} = \frac{V_{OUT}}{1V \cdot 20\,pF \cdot F_{SW}} \quad (1)$$

$$T_{ON} = \frac{R_{FF} \cdot 1V \cdot 20\,pF}{V_{IN}} \quad (2)$$

CONTROL LOGIC

The control logic monitors input power sources, sequences the converter through the soft-start and protective modes, and initiates an internal RUN signal when all conditions are met.

VCC and 3VCBP pins are continuously monitored, and the IR3871 will be disabled if the voltage of either pin drops below the falling thresholds. EN_DELAY will become HIGH when VCC and 3VCBP are in the normal operating range and the EN pin = HIGH.

SOFT START

With EN = HIGH, an internal 10µA current source charges the external capacitor (C_{SS}) on the SS pin to set the output voltage slew rate during the soft start interval. The soft start time (t_{SS}) can be calculated from equation 3.

$$t_{SS} = \frac{C_{SS} \cdot 0.5V}{10\mu A} \quad (3)$$

The feedback voltage tracks the SS pin until SS reaches the 0.5V reference voltage (Vref), then feedback is regulated to Vref. C_{SS} will continue to be charged, and when SS pin reaches V_{SS} (see *Electrical Specification*), SS_DELAY goes HIGH. With EN_DELAY = LOW, the capacitor voltage and SS pin is held to the FB pin voltage. A normal startup sequence is shown in Figure 18.

PGOOD

The PGOOD pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. The PGOOD logic monitors EN_DELAY, SS_DELAY, and under/over voltage fault signals. PGOOD is released only when EN_DELAY and SS_DELAY = HIGH and output voltage is within the OV and UV thresholds.

PRE-BIAS STARTUP

IR3871 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

With constant on-time control, the output voltage is compared with the soft start voltage (SS) or Vref, depending on which one is lower, and will not start switching unless the output voltage drops below the reference. This scheme prevents discharge of a pre-biased output voltage.

SHUTDOWN

The IR3871 will shutdown if VCC is below its UVLO limit. The IR3871 can be shutdown by pulling the EN pin below its lower threshold. Alternatively, the output can be shutdown by pulling the soft start pin below 0.3V.

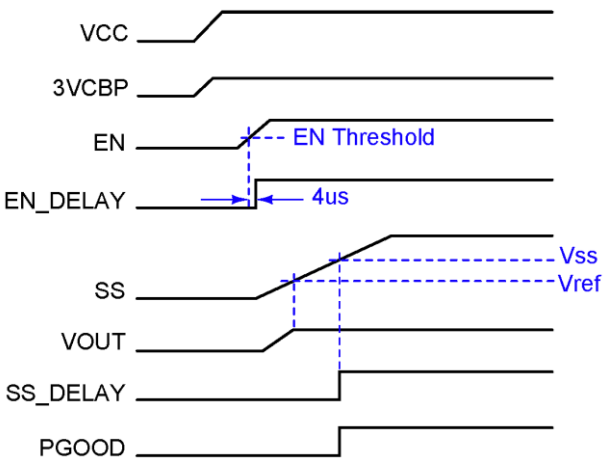


Figure 18. Normal Startup

CIRCUIT DESCRIPTION

UNDER/OVER VOLTAGE MONITOR

The IR3871 monitors the voltage at the FB node through a 350ns filter. If the FB voltage is below the under voltage threshold, UV# is set to LOW holding PGOOD to be LOW. If the FB voltage is above the over voltage threshold, OV# is set to LOW, the shutdown signal (SD) is set to HIGH, MOSFET gates are turned off, and PGOOD signal is pulled low. Toggling VCC or EN will allow the next start up. Figure 19 shows PGOOD status change when UV/OV is detected. The over voltage and under voltage thresholds can be found in the *Electrical Specification* section.

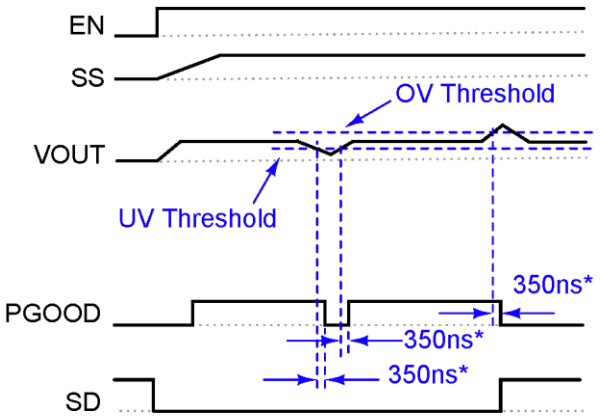


Figure 19(a). Under/Over Voltage Monitor

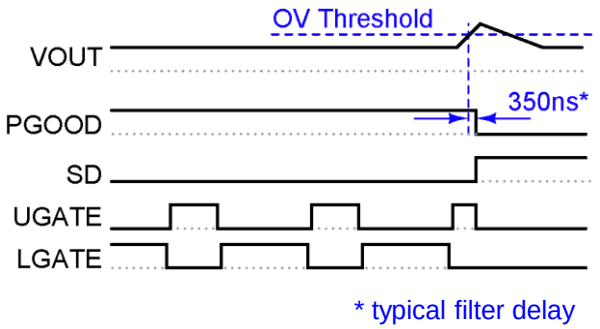


Figure 19(b). Over Voltage Protection

OVER CURRENT MONITOR

The over-current circuitry monitors the output current during each switching cycle. The voltage across the lower MOSFET, VPHASE, is monitored for over current and zero crossing. The OCP circuit evaluates VPHASE for an over current condition typically 270ns after the lower MOSFET is gated on. This delay functions to filter out switching noise. The minimum lower gate interval allows time to sample VPHASE.

The over current trip point is programmed with a resistor from the ISET pin to PHASE pin, as shown in equation 4, where Tj is the junction temperature of Q2 at operation conditions, and 0.4 is the temperature coefficient (~4000 ppm/°C) of Q2 R_{DSON}. When over current is detected, the output gates are tri-state and SS voltage is pulled to 0V. This initiates a new soft start cycle. If there is a total of four OC events, the IR3871 will disable switching, as shown in Figure 20. Toggling VCC or EN will allow the next start up.

$$R_{SET} = \frac{R_{DSON} \cdot I_{OC}}{20\ \mu A} \cdot \left(1 + \frac{T_j - 25}{100} \cdot 0.4\right) \quad (4)$$

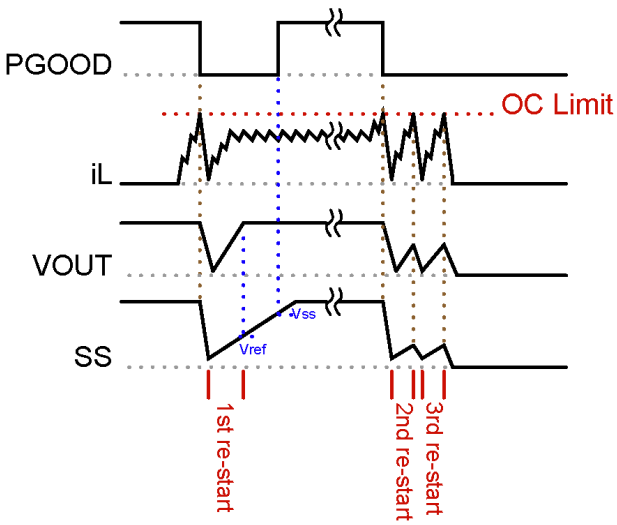


Figure 20. Over Current Protection

CIRCUIT DESCRIPTION

GATE DRIVE LOGIC

The gate drive logic features adaptive dead time, diode emulation, and a minimum lower gate interval.

An adaptive dead time prevents the simultaneous conduction of the upper and lower MOSFETs. The lower gate voltage (LGATE) must be below approximately 1V after PWM goes HIGH before the upper MOSFET can be gated on. Also, the upper gate voltage (UGATE), the difference voltage between UGATE and PHASE, must be below approximately 1V after PWM goes LOW before the lower MOSFET can be gated on.

The control MOSFET is gated on after the adaptive delay for PWM = HIGH and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW. The lower MOSFET is driven 'off' when the signal ZCROSS indicates that the inductor current has reversed as detected by the PHASE voltage crossing the zero current threshold. The synchronous MOSFET stays 'off' until the next PWM falling edge. When the lower peak of inductor current is above zero, a forced continuous current condition is selected. The control MOSFET is gated on after the adaptive delay for PWM = HIGH, and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW.

The synchronous MOSFET gate is driven on for a minimum duration. This minimum duration allows time to recharge the bootstrap capacitor and allows the current monitor to sample the PHASE voltage.

STABILITY CONSIDERATIONS

Constant-on-time control is a fast , ripple based control scheme. Unstable operation can occur if certain conditions are not met. The system instability is usually caused by:

- Switching noise coupled to FB input. This causes the PWM comparator to trigger prematurely after the 400ns minimum Q2 on-time. It will result in double or multiple pulses every switching cycle instead of the expected single pulse. Double pulsing can causes higher output voltage ripple, but in most application it will not affect operation. This can usually be prevented by careful layout of the ground plane and the FB sensing trace.
- Steady state ripple on FB pin being too small. The PWM comparator in IR3871 requires minimum 7mVp-p ripple voltage to operate stably. Not enough ripple will result in similar double pulsing issue described above. Solving this may require using output capacitors with higher ESR.
- ESR loop instability. The stability criteria of constant on-time is: ESR*Cout>Ton/2. If ESR is too small that this criteria is violated then sub-harmonic oscillation will occur. This is similar to the instability problem of peak-current-mode control with D>0.5. Increasing ESR is the most effective way to stabilize the system, but the price paid is the larger output voltage ripple.
- For applications with all ceramic output capacitors, the ESR is usually too small to meet the stability criteria. In these applications, external slope compensation is necessary to make the loop stable. The ramp injection circuit, composed of R6, C13, and C14, shown in Figure 7 is required. The inductor current ripple sensed by R6 and C13 is AC coupled to the FB pin through C14. C14 is usually chosen between 1 to 10nF, and C13 between 10 to 100nF. R6 should then be chosen such that L/DCR = C13*R6.

COMPONENT SELECTION

Selection of components for the converter is an iterative process which involves meeting the specifications and trade-offs between performance and cost. The following sections will guide one through the process.

INDUCTOR SELECTION

Inductor selection involves meeting the steady state output ripple requirement, minimizing the switching loss of upper MOSFETs, meeting transient response specifications and minimizing the output capacitance. The output voltage includes a DC voltage and a small AC ripple component due to the low pass filter which has incomplete attenuation of the switching harmonics. Neglecting the inductance in series with the output capacitor, the magnitude of the AC voltage ripple is determined by the total inductor ripple current flowing through the total equivalent series resistance (ESR) of the output capacitor bank.

$$\Delta I = \frac{T_{ON} \cdot (V_{IN} - V_{OUT})}{2 \cdot L} \quad (5)$$

One can use equation 5 to find the required inductance. ΔI is defined as shown in Figure 21. The main advantage of small inductance is increased inductor current slew rate during a load transient, which leads to a smaller output capacitance requirement as discussed in the *Output Capacitor Selection* section. The draw back of using smaller inductances is increased switching power loss in upper MOSFET, which reduces the system efficiency and increases the thermal dissipation.

INPUT CAPACITOR SELECTION

The main function of the input capacitor bank is to provide the input ripple current and fast slew rate current during the load current step up. The input capacitor bank must have adequate ripple current carrying capability to handle the total RMS current. Figure 21 shows a typical input current. Equation 6 shows the RMS input current. The RMS input current contains the DC load current and the inductor ripple current. As shown in equation 5, the inductor ripple current is unrelated to the load current. The maximum RMS input current occurs at the maximum output current. The maximum power dissipation in the input capacitor equals the square of the maximum RMS input current times the input capacitor's total ESR.

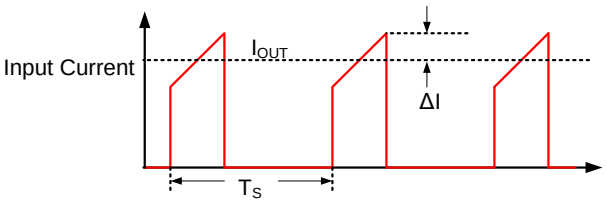


Figure 21. Typical Input Current Waveform.

$$I_{IN\_RMS} = \sqrt{\frac{1}{Ts} \cdot \int_0^{Ts} f^2(t) \cdot dt}$$

$$= I_{OUT} \cdot \sqrt{Ton \cdot Fs} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{I_{OUT}}\right)^2} \quad (6)$$

The voltage rating of the input capacitor needs to be greater than the maximum input voltage because of high frequency ringing at the phase node. The typical percentage is 25%.

COMPONENT SELECTION

OUTPUT CAPACITOR SELECTION

Selection of the output capacitor requires meeting voltage overshoot requirements during load removal, and meeting steady state output ripple voltage requirements. The output capacitor is the most expensive converter component and increases the overall system cost. The output capacitor decoupling in the converter typically includes the low frequency capacitor, such as Specialty Polymer Aluminum, and mid frequency ceramic capacitors.

The first purpose of output capacitors is to provide current when the load demand exceeds the inductor current, as shown in Figure 22. Equation 7 shows the charge requirement for a certain load. The advantage provided by the IR3871 at a load step is to reduce the delay compared to a fixed frequency control method (in microseconds or (1-D)*Ts). If the load increases right after the PWM signal goes low, the longest delay will be equal to the minimum lower gate on as shown in the *Electrical Specification* table. The IR3871 also reduces the inductor current slew time, the time it takes for the inductor current to reach equality with the output current, by increasing the switching frequency up to 2.5MHz. The result reduces the recovery time.

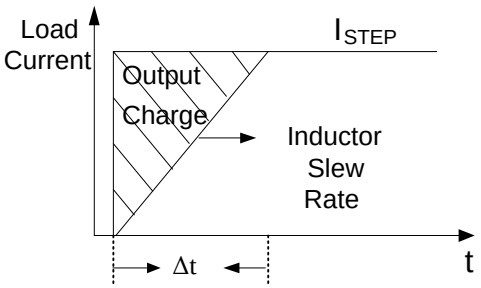


Figure 22. Charge Requirement during Load Step

$$Q = C \cdot V = 0.5 \cdot Istep \cdot \Delta t \quad (7a)$$

$$C_{OUT} = \frac{1}{V_{DROP}} \left[\frac{1}{2} \cdot \frac{L \cdot Istep^2}{(V_{IN} - V_{OUT})} \right] \quad (7b)$$

The output voltage drop, VDROP, initially depends on the characteristic of the output capacitor. VDROP is the sum of the equivalent series inductance (ESL) of the output capacitor times the rate of change of the output current and the ESR times the change of the output current. VESR is usually much greater than VESL. The IR3871 requires a total ESR such that the ripple voltage at the FB pin is greater than 7mV.

The second purpose of the output capacitor is to minimize the overshoot of the output voltage when the load decreases as shown in Figure 23. By using the law of energy before and after the load removal, equation 8 shows the output capacitance requirement for a load step.

$$C_{OUT} = \frac{L \cdot I_{STEP}^2}{V_{OS}^2 - V_{OUT}^2} \quad (8)$$

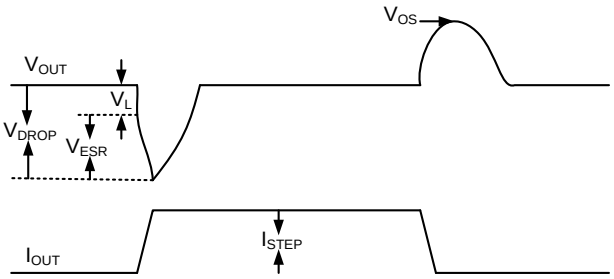


Figure 23. Typical Output Voltage Response Waveform.

BOOT CAPACITOR SELECTION

The boot capacitor starts the cycle fully charged to a voltage of VB(0). Cg equals 0.65nF in IR3871. Choose a sufficiently small ΔV such that VB(0)-ΔV exceeds the maximum gate threshold voltage to turn on the high side MOSFET.

$$C_{BOOT} = C_g \cdot \left(\frac{V_B(0)}{\Delta V} - 1 \right) \quad (9)$$

Choose a boot capacitor value larger than the calculated C_{BOOT} in equation 9. Equation 9 is based on charge balance at CCM operation. Usually the boot capacitor will be discharged to a much lower voltage when the circuit is operating in DCM mode at light load, due to much longer Q2 off time and the bias current drawn by the IC. Boot capacitance needs to be increased if insufficient turn-on of Q1 is observed at light load, typically larger than 0.1µF is needed. The voltage rating of this part needs to be larger than VB(0) plus the desired derating voltage. Its ESR and ESL needs to be low in order to allow it to deliver the large current and di/dt's which drive MOSFETs most efficiently. In support of these requirements a ceramic capacitor should be chosen.

DESIGN EXAMPLE

Design Criteria:

Input Voltage, VIN, = 6V to 21V
Output Voltage, VOUT = 1.25V
Switching Frequency, FS = 400KHz
Inductor Ripple Current, 2ΔI = 3A
Maximum Output Current, IOUT = 6A
Over Current Trip, IOC = 9A
Overshoot Allowance, VOS = VOUT + 50mV
Undershoot Allowance, VDROP = 50mV

Find R_{FF} :

$$R_{FF} = \frac{1.25V}{1V \cdot 20pF \cdot 400kHz} = 156\,k\Omega$$

Pick a standard value 158 kΩ, 1% resistor.

Find R_{SET} :

$$R_{SET} = \frac{1.4 \cdot 10m\Omega \cdot 9A}{20\mu A} = 6.3\,k\Omega$$

The R_{DSON} of the lower MOSFET could be expected to increase by a factor of 1.4 over temperature. Therefore, pick a 6.49kΩ, 1% standard resistor.

Find a resistive voltage divider for V_{OUT} = 1.25V:

$$V_{FB} = \frac{R_2}{R_2 + R_1} \cdot V_{OUT} = 0.5V$$

R_2 = 1.33kΩ, R_1 = 1.96 kΩ, both 1% standard resistors.

Choose the soft start capacitor:
Once the soft start time has chosen, such as 1000us to reach to the reference voltage, a 22nF for C_{SS} is used to meet 1000µs.

Choose an inductor to meet the design specification:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot 2\Delta I \cdot F_s}$$
$$= \frac{1.25V \cdot (21V - 1.25V)}{21V \cdot 3A \cdot 400kHz}$$
$$= 1.0\mu H$$

Choose an inductor with the lowest DCR and AC power loss as possible to increase the overall system efficiency. For instance, choose an FDU0650-R82M manufactured by TOKO. The inductance of this part is 820nH and has 4.2mΩ DCR. Ripple current needs to be recalculated using the chosen inductor.

$$\Delta I = \frac{1.25V \cdot (21V - 1.25V)}{2 \cdot 21V \cdot 0.82\mu H \cdot 400kHz} = 1.75A$$

Choose an input capacitor:

$$I_{IN\_RMS} = 6A \cdot \sqrt{\frac{1.25V}{21V}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{1.75A}{6A}\right)^2} = 1.5A$$

A Panasonic 10µF (ECJ3YB1E106M) accommodates 6 Arms of ripple current at 300KHz. Due to the chemistry of multilayer ceramic capacitors, the capacitance varies over temperature and operating voltage, both AC and DC. One 10µF capacitor is recommended. In a practical solution, one 1µF capacitor is required along with 10µF. The purpose of the 1µF capacitor is to suppress the switching noise and deliver high frequency current.

Choose an output capacitor:

To meet the undershoot specification, select a set of output capacitors which has an equivalent ESR of 10mΩ (50mV/5A). To meet the overshoot specification, equation 8 will be used to calculate the minimum output capacitance. As a result, 160µF will be needed for 5A load remover. Combine those two requirements, one can choose a set of output capacitors from manufactures such as SP-Cap (Specialty Polymer Capacitor) from Panasonic or POSCAP from Sanyo. A 150µF (EEFSL0D151R) from Panasonic is recommended. This capacitor has 9mΩ ESR which leaves margin for the voltage drop of the ESL during load step up. The typical ESL for this capacitor is around 2nH.

LAYOUT RECOMMENDATION

Bypass Capacitor:
One 1µF high quality ceramic capacitor should be placed as near VCC pin as possible. The other end of capacitor can be connected to a via or connected directly to GND plane. Use a GND plane instead of a thin trace to the GND pin because a thin trace have too much impedance.

Boot Circuit:
C_{BOOT} should be placed near the BOOT and PHASE pins to reduce the impedance when the upper MOSFET turns on.

Power Stage:
Figure 24 shows the current paths and their directions for the on and off periods. The on time path has low average DC current and high AC current. Therefore, it is recommended to place the input ceramic capacitor, upper, and lower MOSFET in a tight loop as shown in Figure 24.

The purpose of the tight loop from the input ceramic capacitor is to suppress the high frequency (10MHz range) switching noise and reduce Electromagnetic Interference (EMI). If this path has high inductance, the circuit will cause voltage spikes and ringing, and increase the switching loss. The off time path has low AC and high average DC current. Therefore, it should be laid out with a tight loop and wide trace at both ends of the inductor. Lowering the loop resistance reduces the power loss. The typical resistance value of 1-ounce copper thickness is 0.5mΩ per square inch.

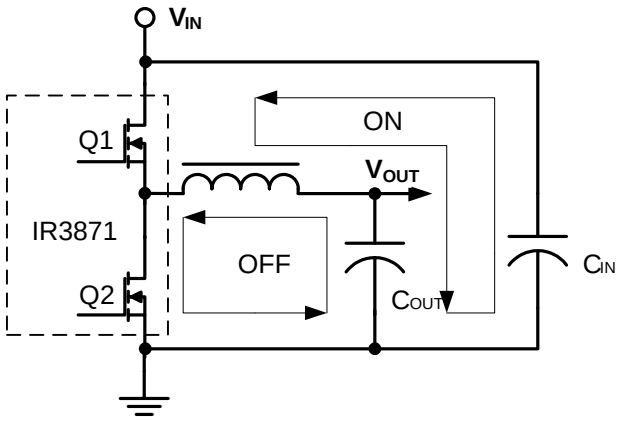


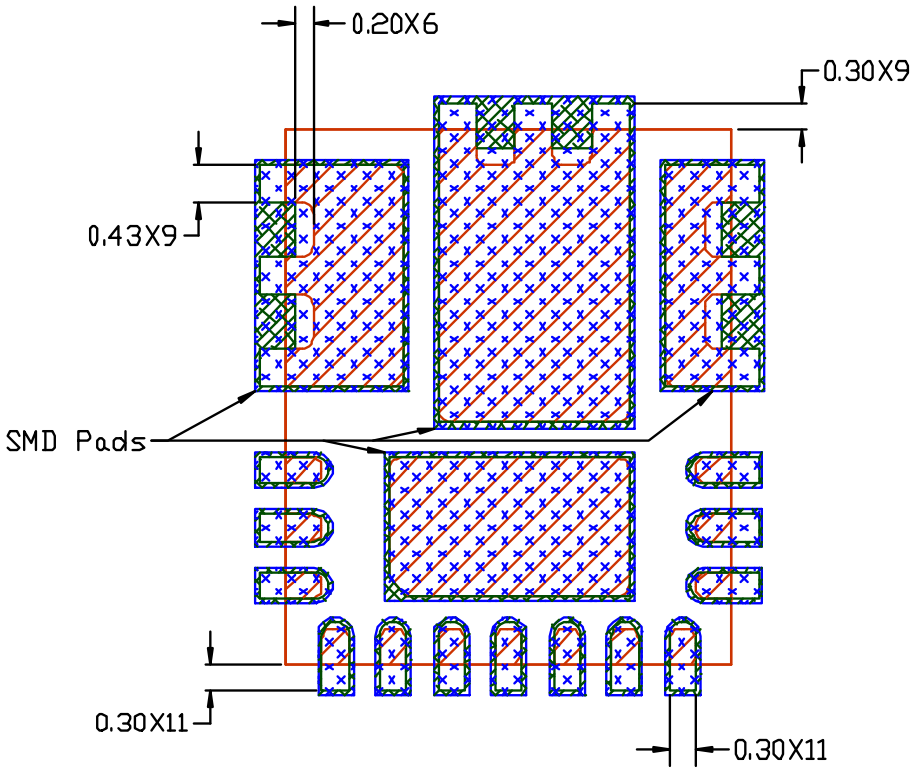
Figure 24. Current Path of Power Stage

PCB Metal and Components Placement

Lead lands (the 13 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large toe fillet that can be easily inspected.

Pad lands (the 4 big pads) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than; 0.17mm for 2 oz. Copper or no less than 0.1mm for 1 oz. Copper or no less than 0.23mm for 3 oz. Copper.



All Dimensions In mm

PCB Copper

PCB Solder Resist

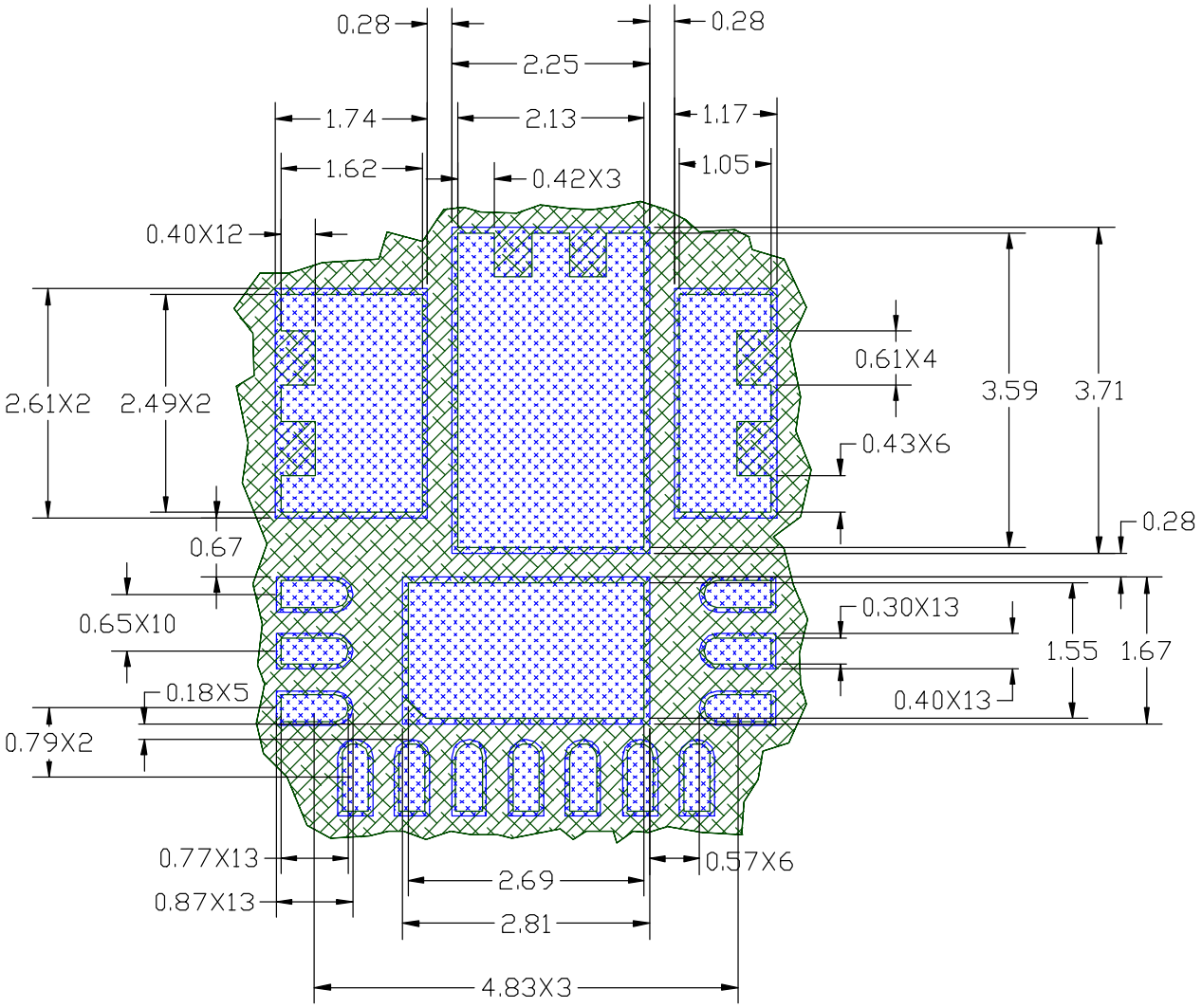
Component Pad

Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist misalignment.

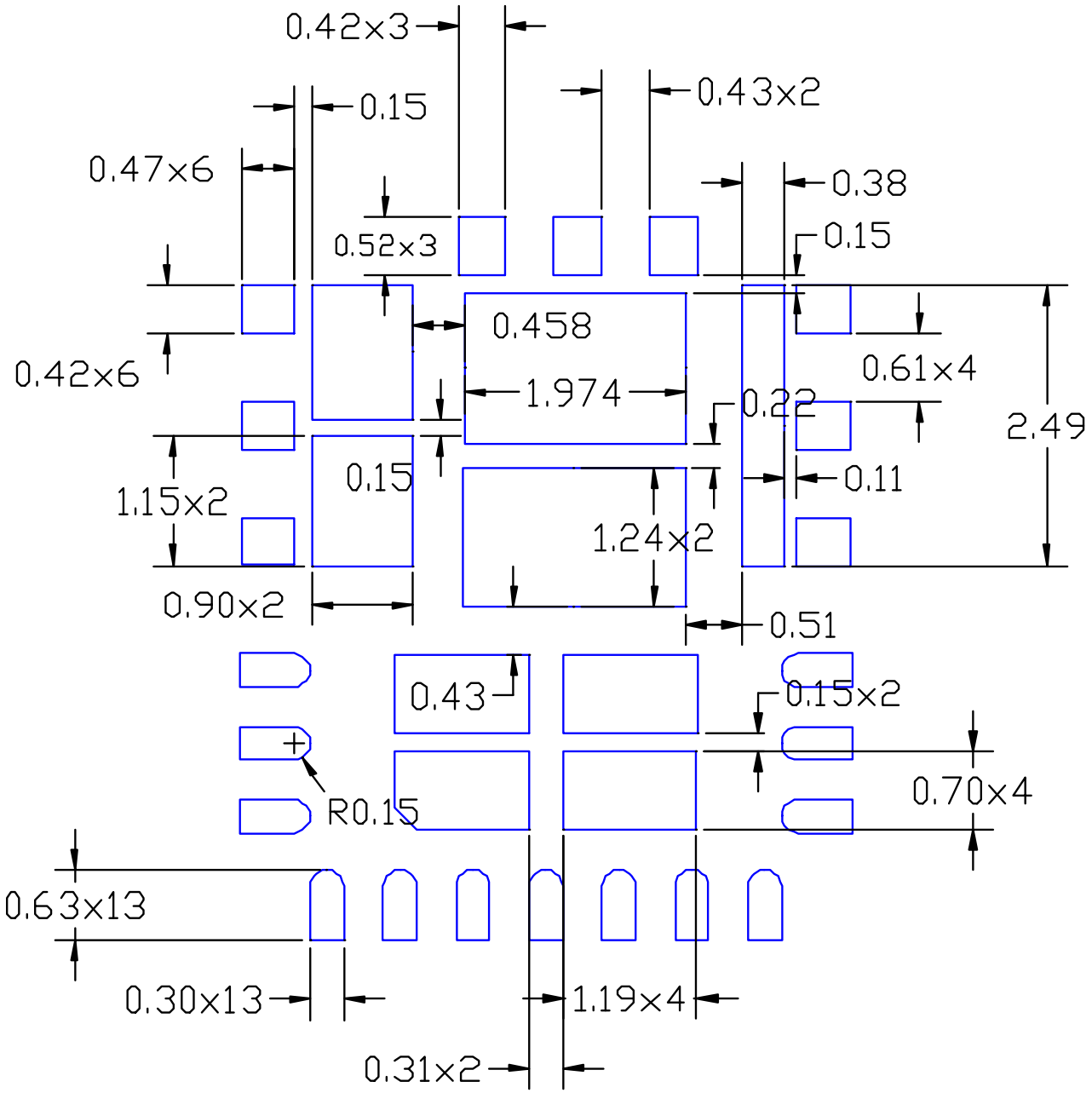
Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

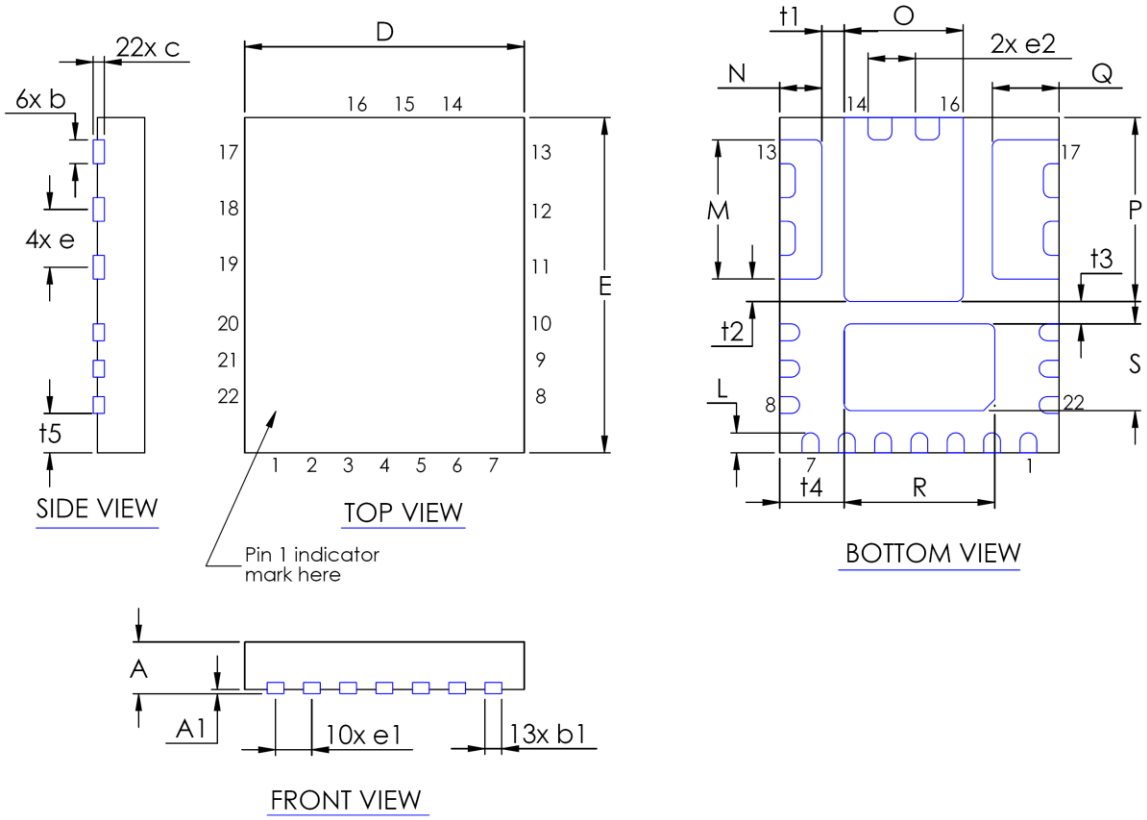


Stencil Design

The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will open.

The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back in order to decrease the risk of shorting the center land to the lead lands when the part is pushed into the solder paste.





DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.8	1	0.0315	0.0394	L	0.35	0.45	0.0138	0.0177
A1	0	0.05	0	0.002	M	2.441	2.541	0.0962	0.1001
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0314
b1	0.25	0.35	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.970 BASIC		Q	1.265	1.365	0.0498	0.05374
E	6.000 BASIC		2.364 BASIC		R	2.644	2.744	0.1042	0.1081
e	1.033 BASIC		0.0407 BASIC		S	1.5	1.6	0.0591	0.063
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0259 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	

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